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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



Protection Device

TVS (Transient Voltage Suppressor)

ESD113-B1 Series

Bi-directional, 3.6 V, 0.2 pF, 0201, 0402, RoHS and Halogen Free compliant

ESD113-B1-02ELS
ESD113-B1-02EL

Data Sheet

Revision 1.2, 2014-05-14
Final

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1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
 - IEC61000-4-2 (ESD): ± 20 kV (air / contact)
 - IEC61000-4-4 (EFT): ± 2.5 kV / ± 50 A (5/50 ns)
 - IEC61000-4-5 (surge): ± 3 A (8/20 μ s)
- Bi-directional, working voltage up to: $V_{RWM} = \pm 3.6$ V
- Ultra low capacitance $C_L = 0.20$ pF (typical) at $f = 1$ GHz
- Very low clamping voltage: $V_{CL} = 14$ V (typical) at $I_{TLP} = 16$ A
- Very low reverse current. $I_R < 1$ nA (typical)
- Very low dynamic resistance: $R_{DYN} = 0.45$ Ω (typical)
- Pb-free and halogen-free package (RoHS compliant)



1.2 Application Examples

- USB 3.0, Firewire, DVI, HDMI, S-ATA, DisplayPort, Thunderbolt
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

1.3 Product Description

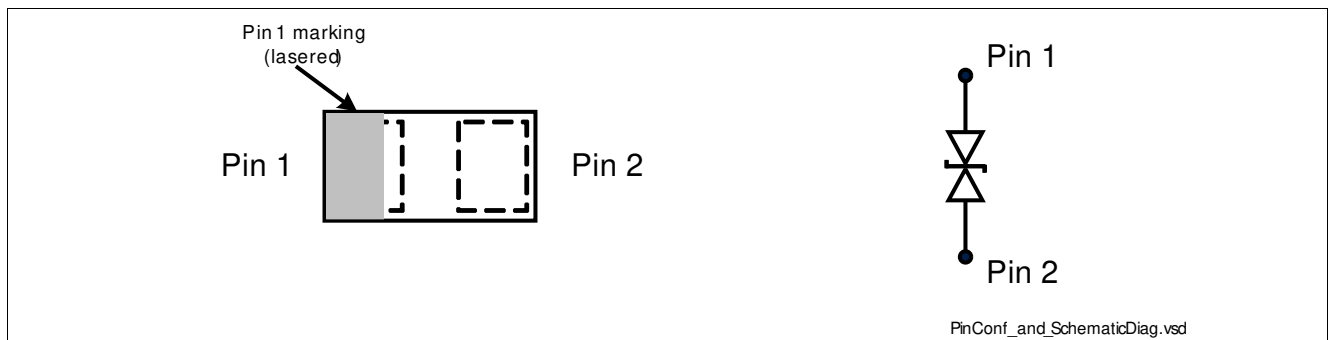


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

| Type | Package | Configuration | Marking code |
|-----------------|-----------|------------------------|--------------|
| ESD113-B1-02ELS | TSSLP-2-4 | 1 line, bi-directional | <u>2</u> |
| ESD113-B1-02EL | TSLP-2-20 | 1 line, bi-directional | CC |

2 Maximum Ratings

Table 2-1 Maximum Rating at $T_A = 25\text{ °C}$, unless otherwise specified¹⁾

| Parameter | Symbol | Values | Unit |
|-------------------------------------|-----------|------------|------|
| ESD air discharge ²⁾ | V_{ESD} | ± 20 | kV |
| ESD contact discharge ²⁾ | | ± 20 | |
| Peak pulse power | P_{PK} | 36 | W |
| Peak pulse current ³⁾ | I_{PP} | ± 3 | A |
| Operating temperature | T_{OP} | -55 to 125 | °C |
| Storage temperature | T_{stg} | -65 to 150 | °C |

- 1) Device is electrically symmetrical
- 2) V_{ESD} according to IEC61000-4-2
- 3) Non-repetitive current pulse 8/20 μ s exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component.

3 Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

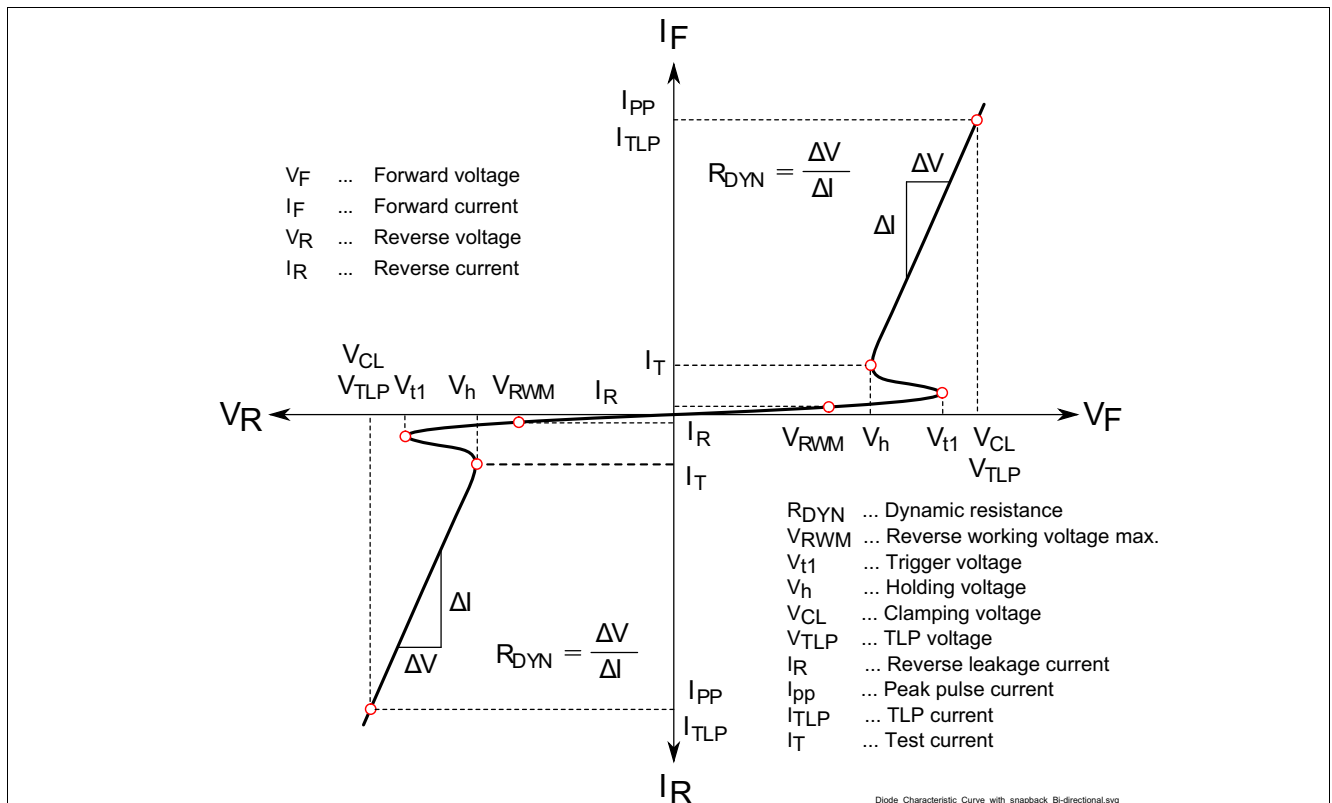


Figure 3-1 Definitions of electrical characteristics

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified
Table 3-1 DC Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------------|-----------|--------|------|------|------|-----------------------|
| | | Min. | Typ. | Max. | | |
| Reverse working voltage | V_{RWM} | -3.6 | – | 3.6 | V | |
| Trigger voltage | V_{t1} | 4 | – | – | | |
| Holding voltage | V_h | 4 | 4.6 | 5.5 | | $I_T = 10\text{ mA}$ |
| Reverse leakage current | I_R | – | <1 | 20 | nA | $V_R = 3.3\text{ V}$ |

1) Device is electrically symmetrical

Table 3-2 AC Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|-------------------|--------|--------|------|------|------|--------------------------------------|
| | | Min. | Typ. | Max. | | |
| Line capacitance | C_L | – | 0.2 | 0.35 | pF | $V_R = 0\text{ V}, f = 1\text{ MHz}$ |
| | | – | 0.2 | – | | $V_R = 0\text{ V}, f = 1\text{ GHz}$ |
| Series inductance | L_S | – | 0.2 | – | nH | ESD113-B1-02ELS |
| | | – | 0.4 | – | | ESD113-B1-02EL |

Table 3-3 ESD and Surge Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified ¹⁾

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|----------------------------------|-----------|--------|------|------|----------|--|
| | | Min. | Typ. | Max. | | |
| Clamping voltage ²⁾ | V_{CL} | – | 14 | – | V | $I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$ |
| | | – | 20 | – | | $I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$ |
| Clamping voltage ³⁾ | | – | 6 | – | | $I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ |
| | | – | 8 | – | | $I_{PP} = 3\text{ A}, t_p = 8/20\text{ }\mu\text{s}$ |
| Dynamic resistance ²⁾ | R_{DYN} | – | 0.45 | – | Ω | $t_p = 100\text{ ns}$ |

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$.

3) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A=25^\circ\text{C}$, unless otherwise specified

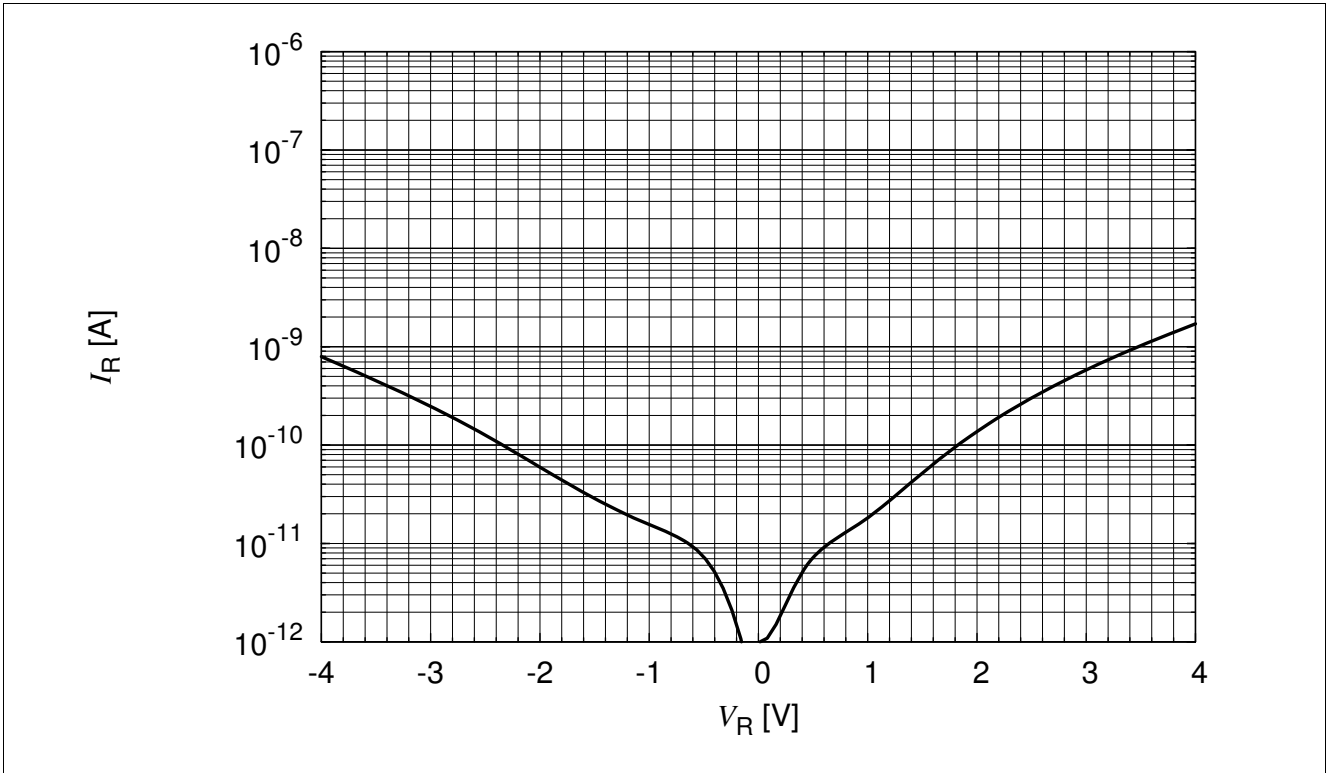


Figure 4-1 Reverse leakage current $I_R = f(V_R)$

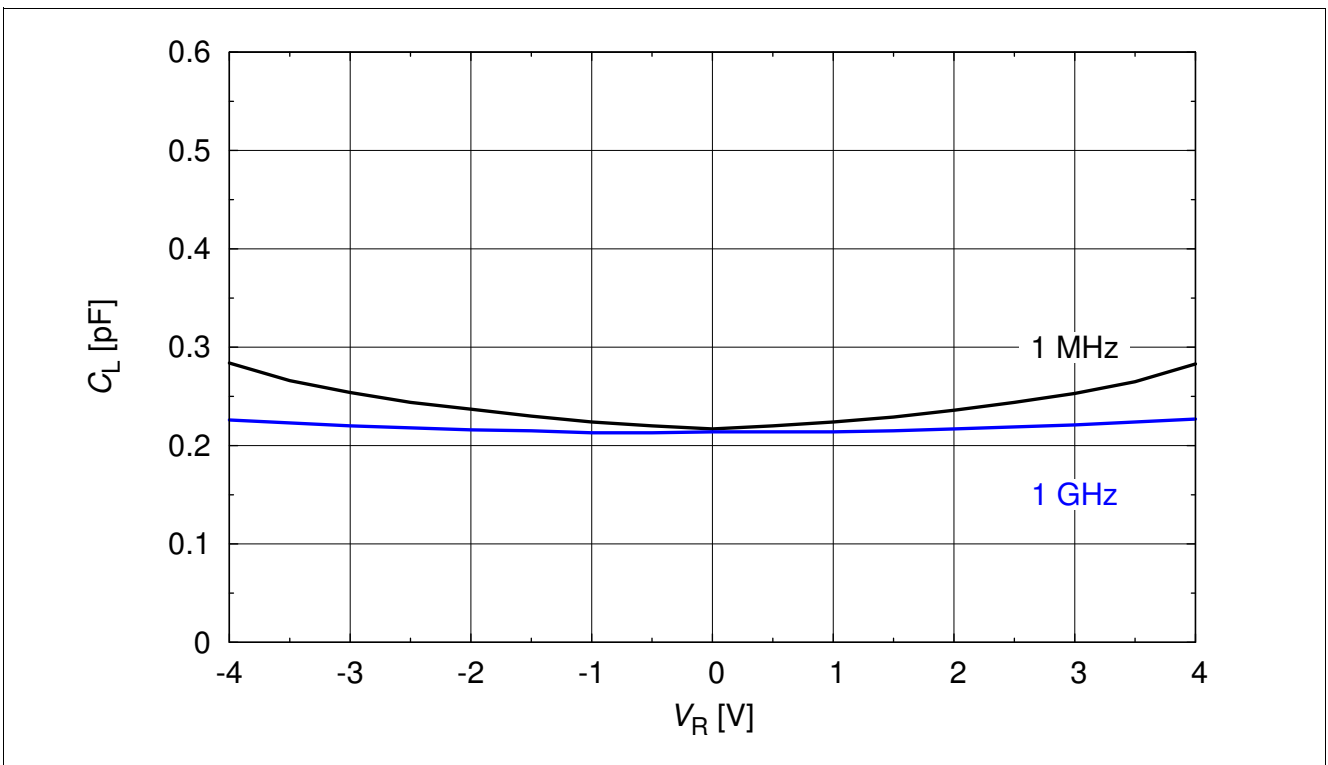


Figure 4-2 Line capacitance $C_L = f(V_R)$

Typical Characteristics Diagrams

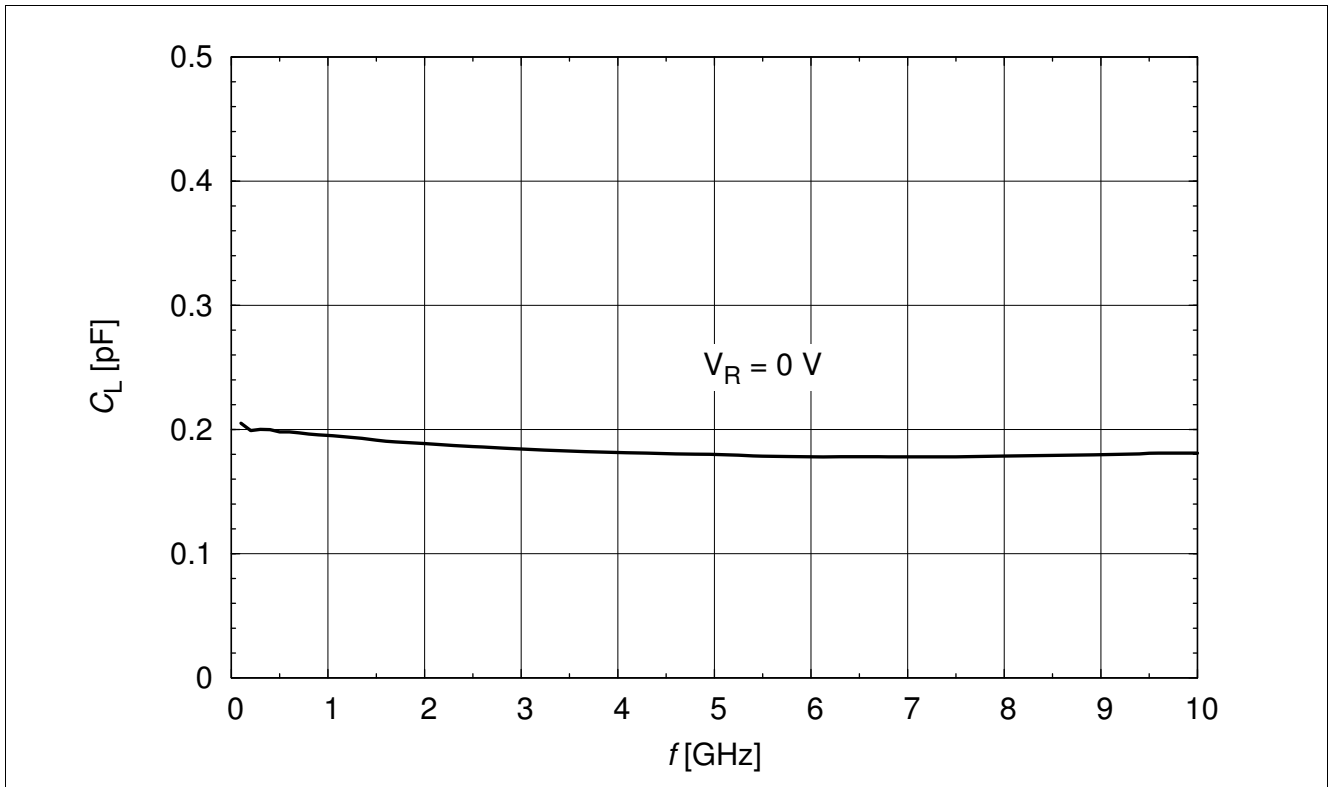


Figure 4-3 Line capacitance: $C_L = f(f)$, $V_R = 0$ V

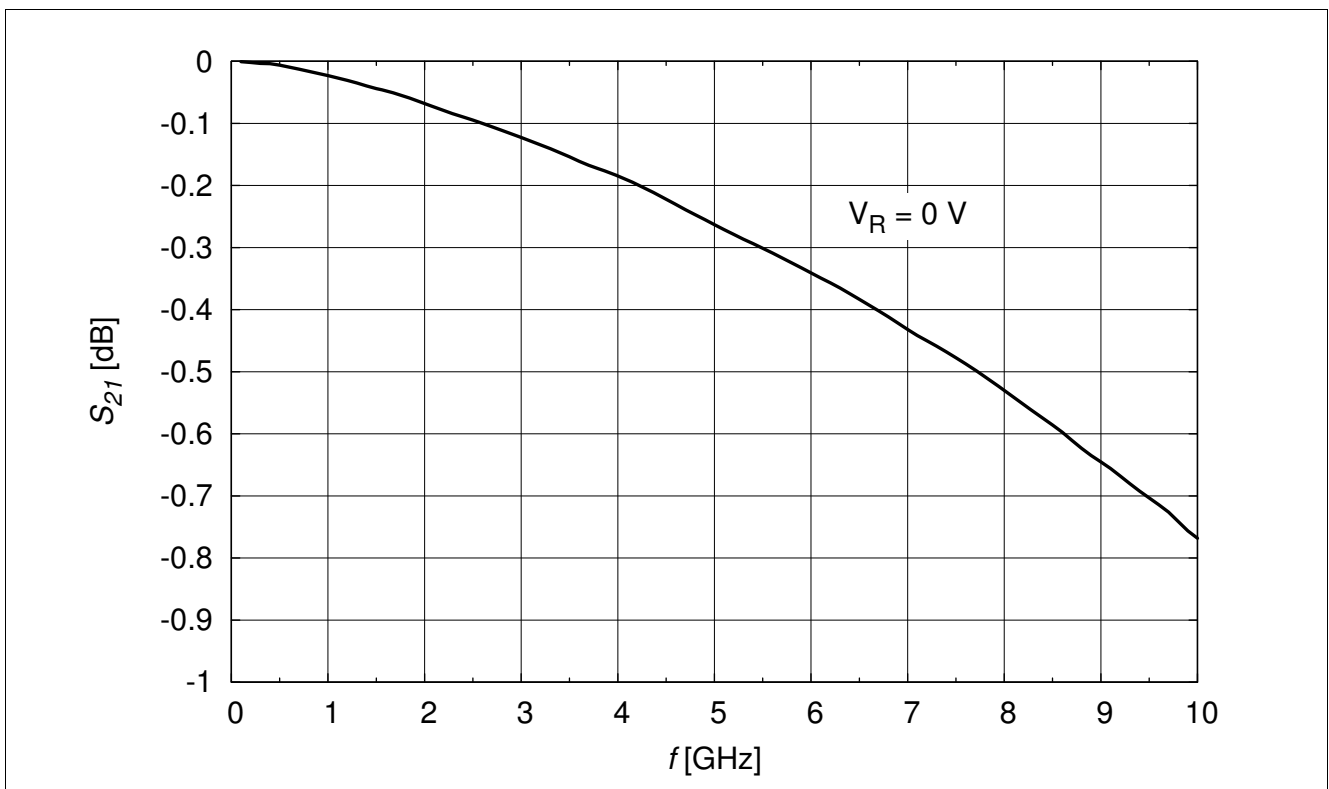


Figure 4-4 Insertion loss vs. frequency in a 50 Ω system

Typical Characteristics Diagrams

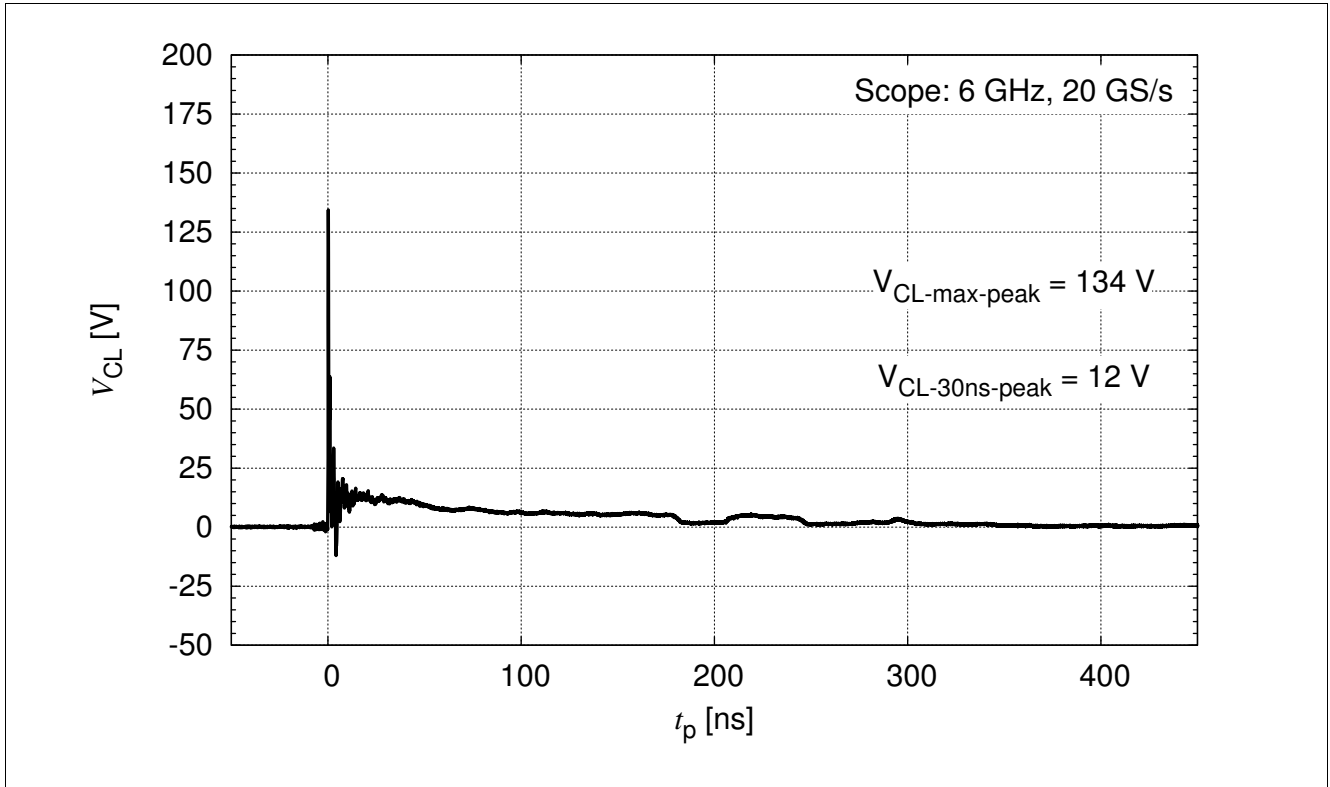


Figure 4-5 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positiv pulse from pin 1 to pin 2

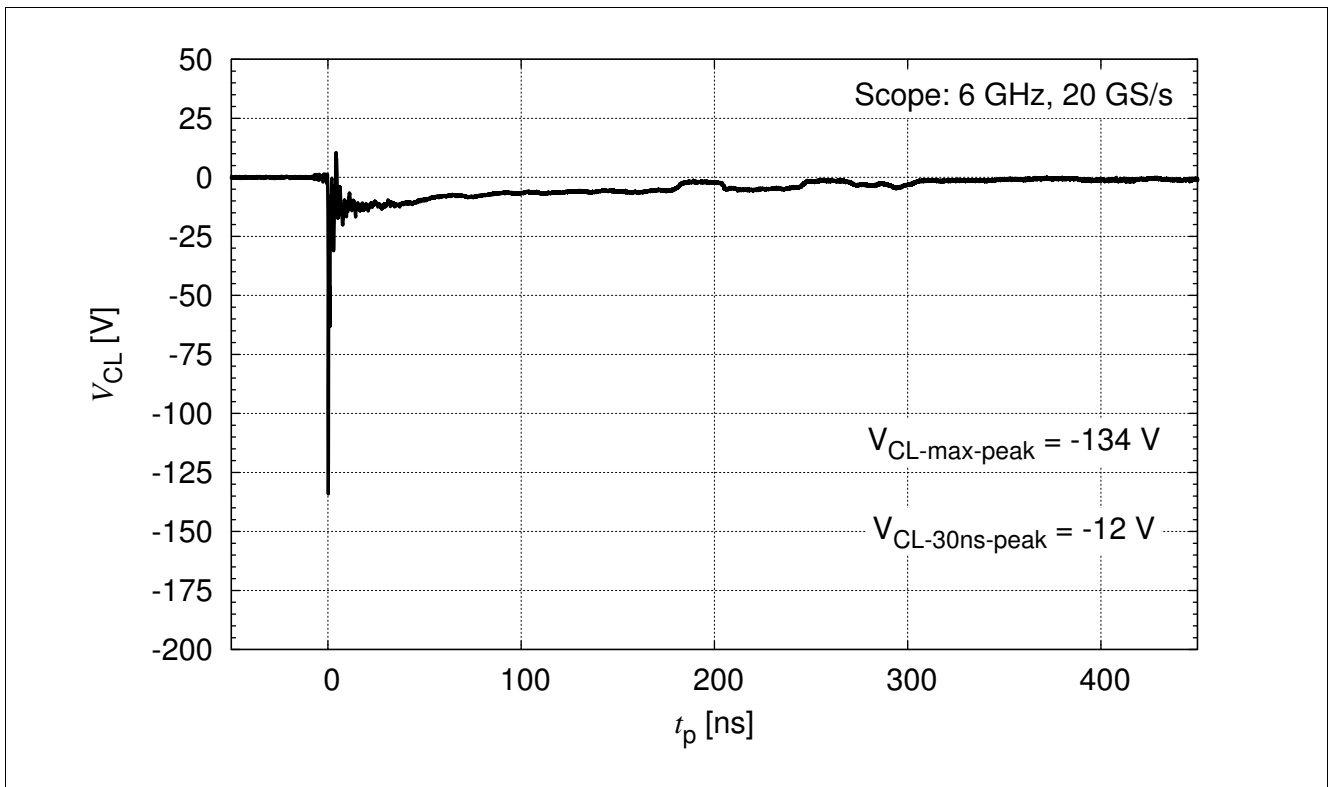


Figure 4-6 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negativ pulse from pin 1 to pin 2

Typical Characteristics Diagrams

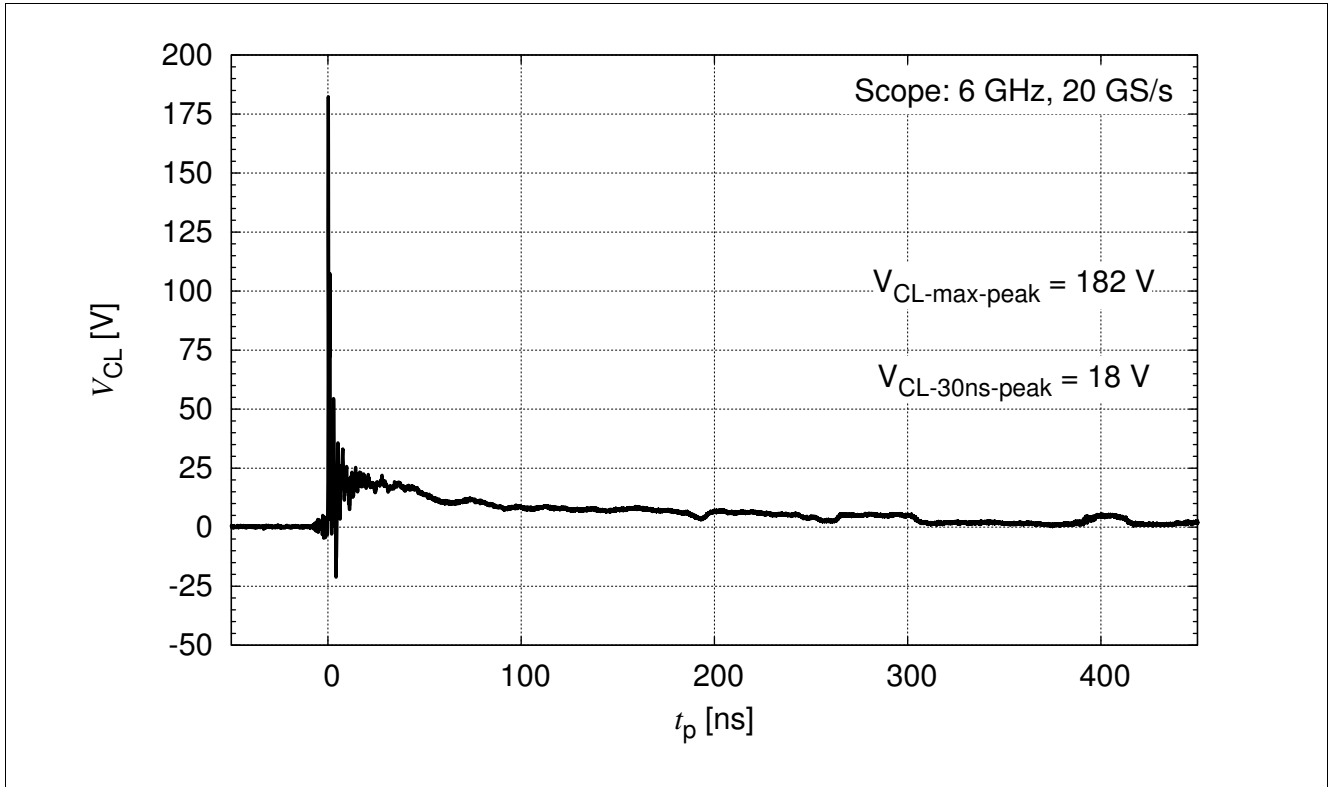


Figure 4-7 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positiv pulse from pin 1 to pin 2

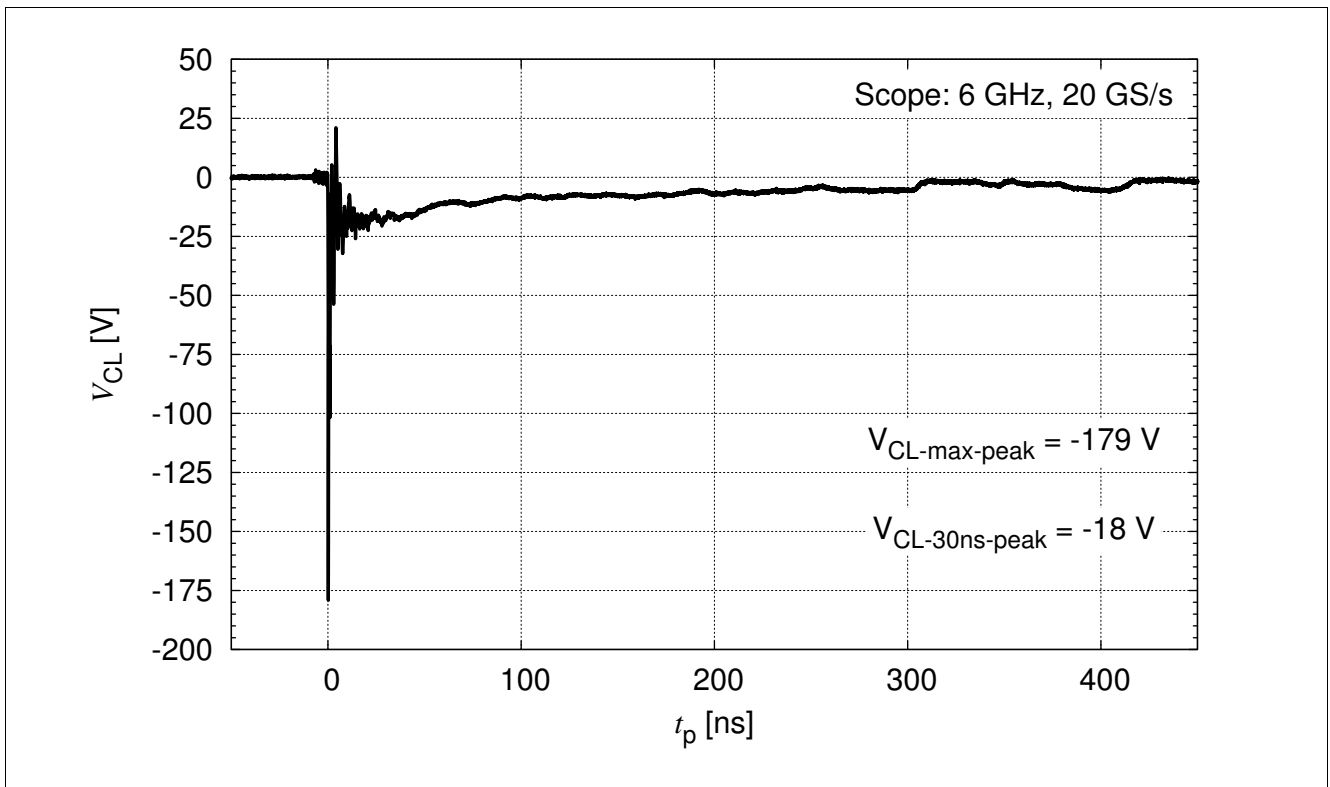


Figure 4-8 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negativ pulse from pin 1 to pin 2

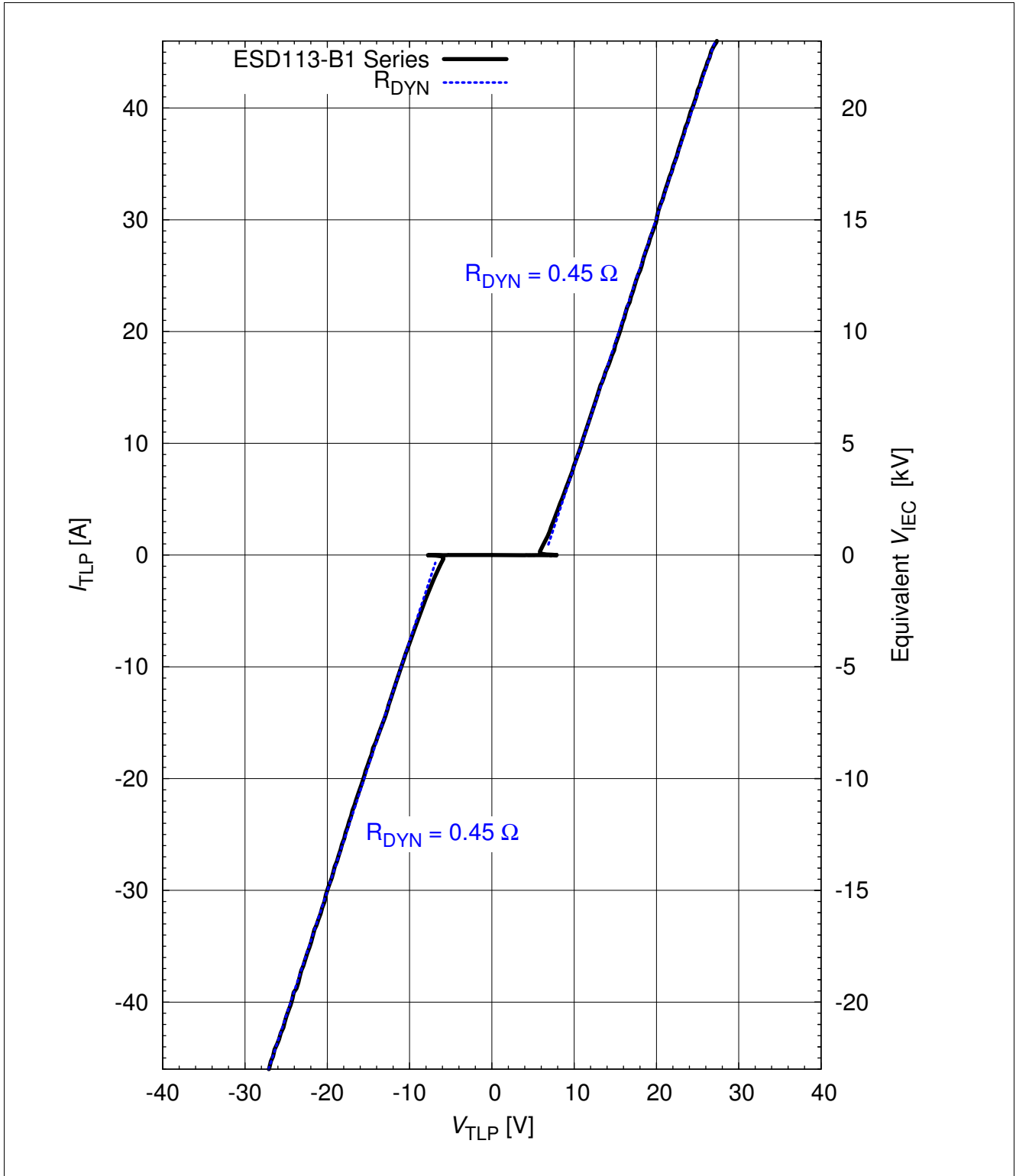


Figure 4-9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

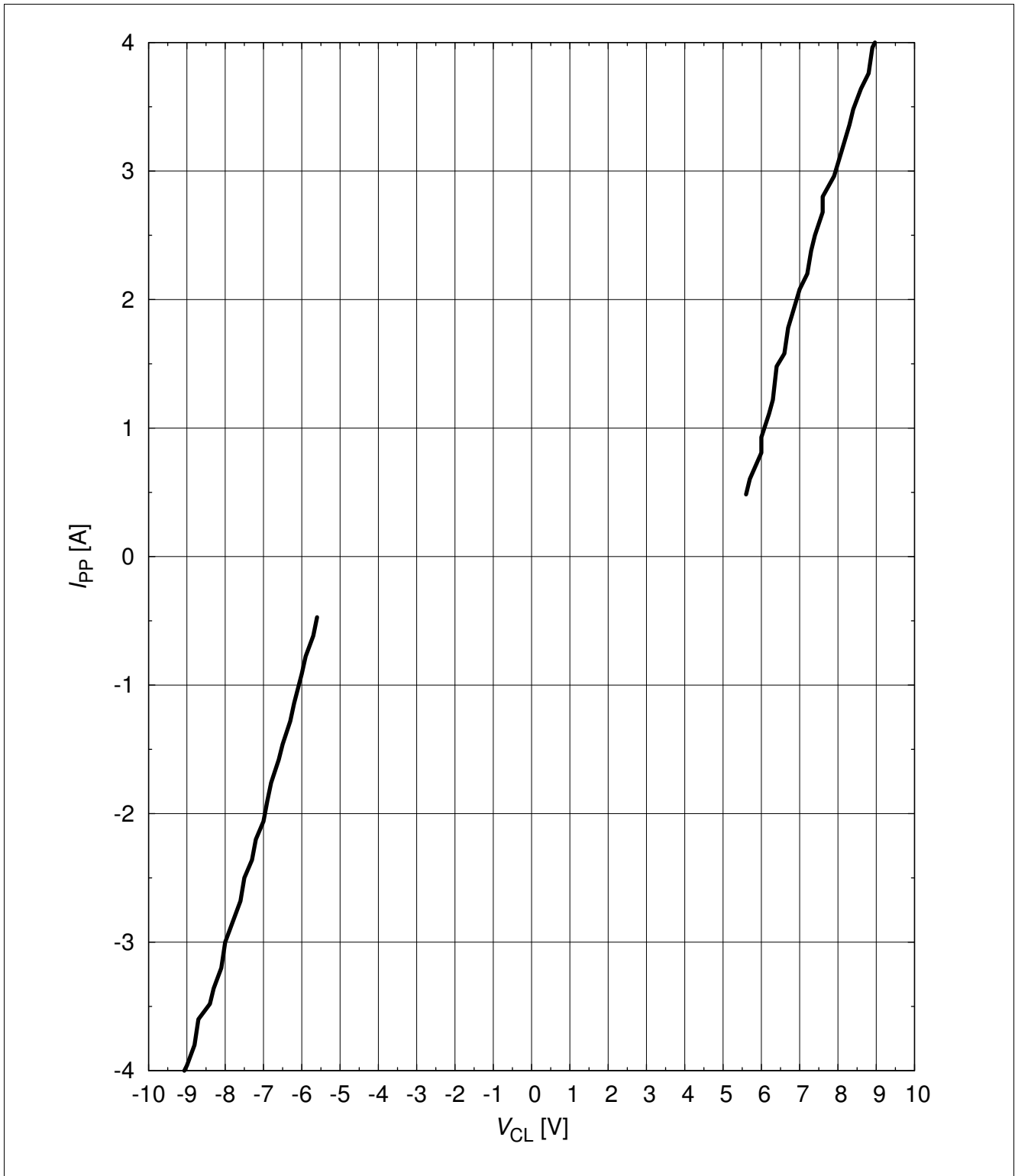


Figure 4-10 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$ [1], pin 1 to pin 2

5 Package Information

5.1 TSSLP-2-4

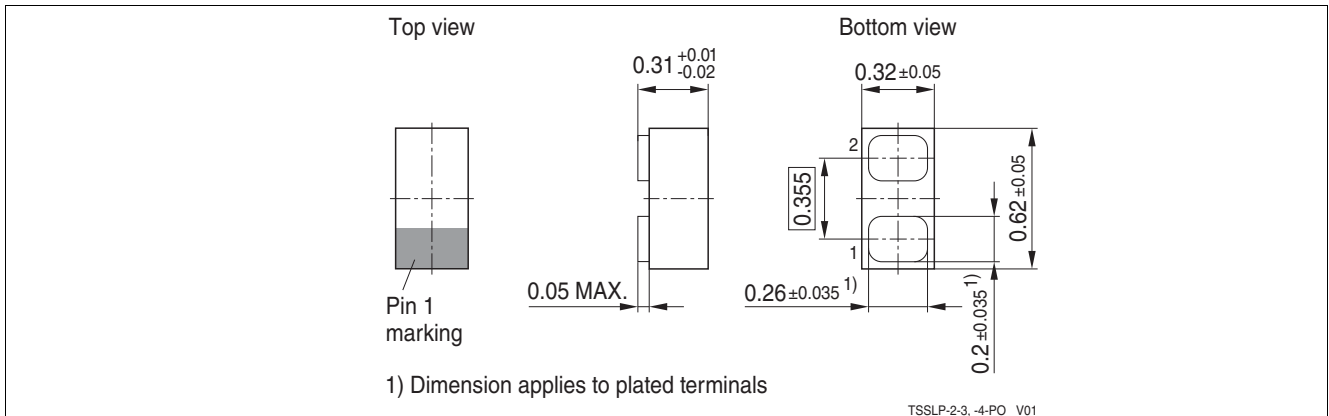


Figure 5-1 TSSLP-2-4 Package outline (dimension in mm)

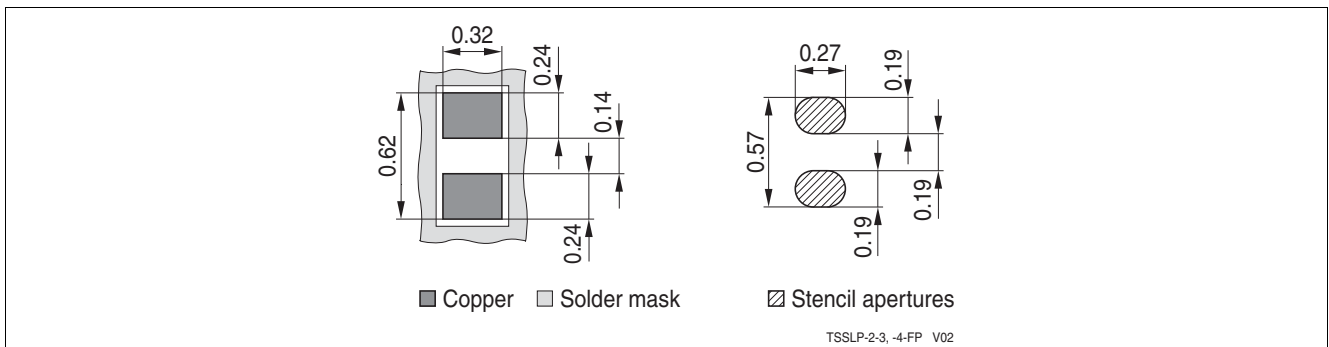


Figure 5-2 TSSLP-2-4 Footprint (dimension in mm)

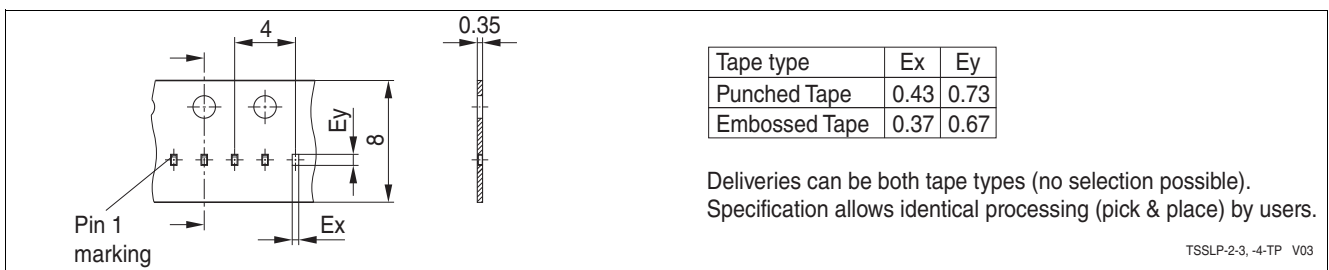


Figure 5-3 TSSLP-2-4 Packing (dimension in mm)

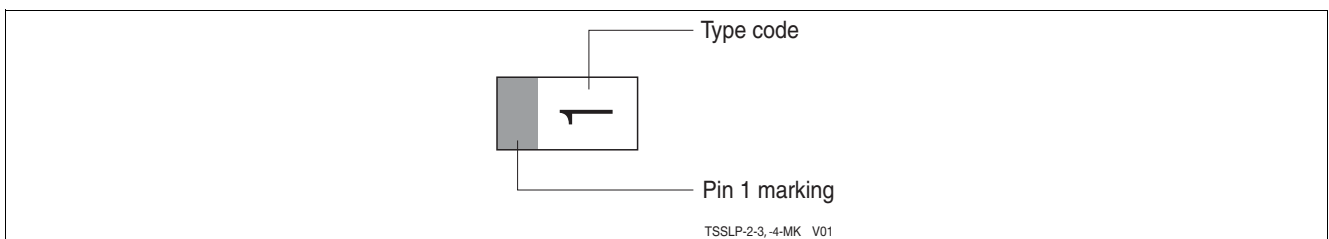


Figure 5-4 TSSLP-2-4 Marking example [Table 1-1 "Part Information" on Page 3](#)

5.2 TSLP-2-20

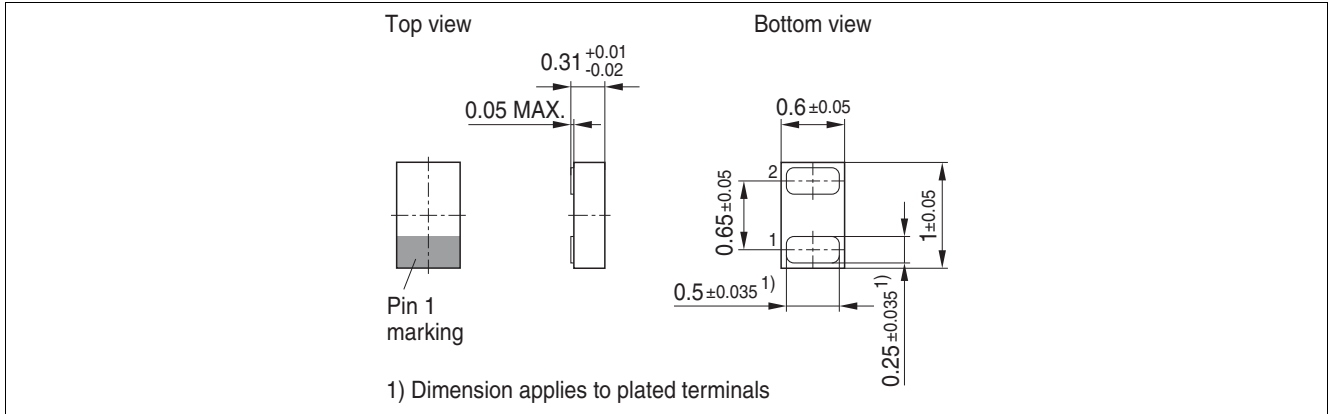


Figure 5-5 TSLP-2-20 Package outline (dimension in mm)

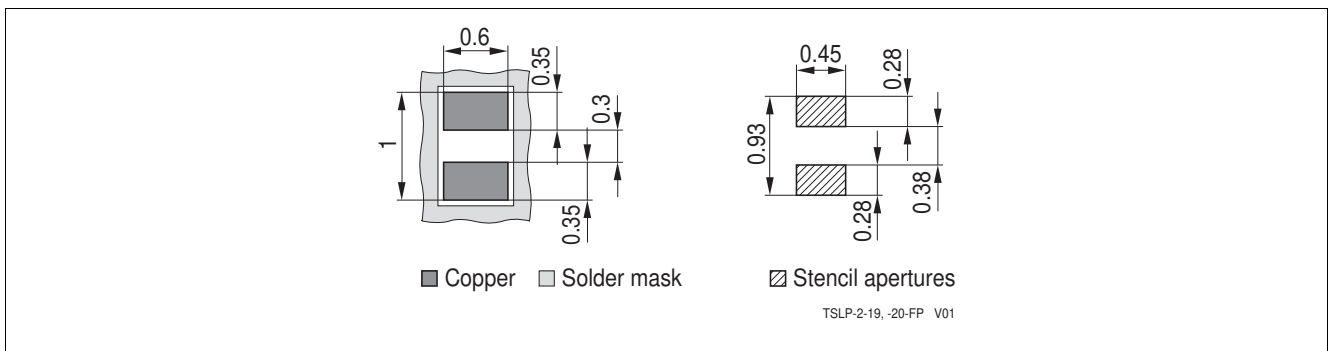


Figure 5-6 TSLP-2-20 Footprint (dimension in mm)

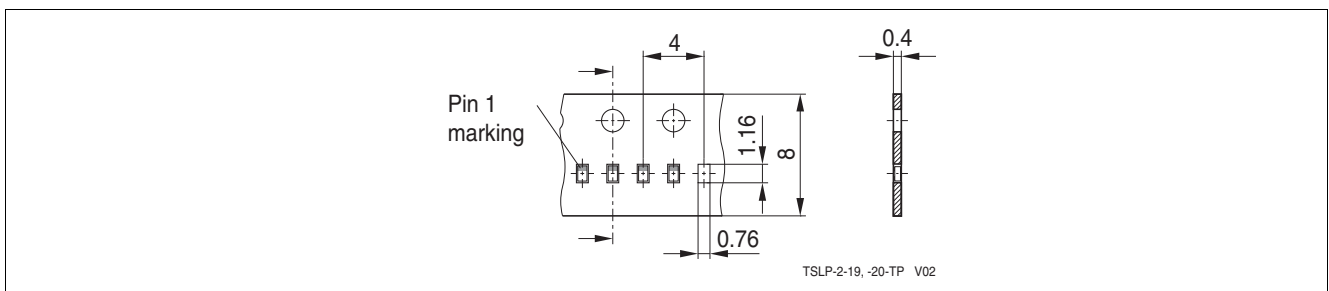


Figure 5-7 TSLP-2-20 Packing (dimension in mm)

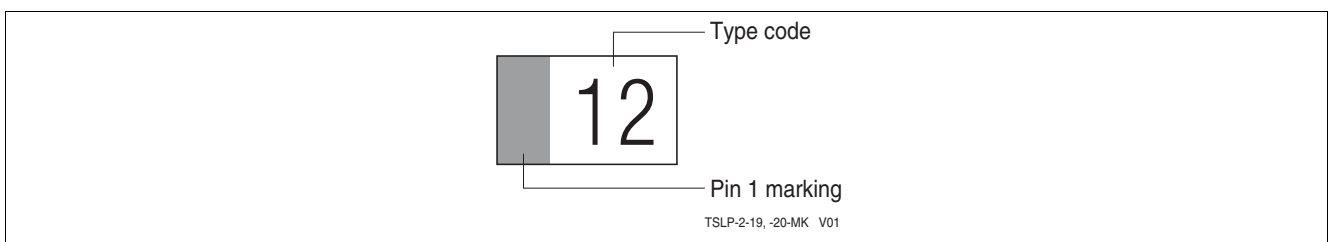


Figure 5-8 TSSLP-2-4 Marking example [Table 1-1 "Part Information" on Page 3](#)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

Revision History: Rev.1.1, 2013-02-06

| Page or Item | Subjects (major changes since previous revision) |
|---------------------------------|--|
| Revision 1.2, 2014-05-14 | |
| All | New type ESD113-B1-02EL inserted |
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