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Protection Device

TVS (Transient Voltage Suppressor)

ESD114-U1-02 Series

Uni-directional, 5.3 V, 0.4 pF, 0402, 0201, RoHS and Halogen Free compliant

ESD114-U1-02ELS
ESD114-U1-02EL

Data Sheet

Revision 1.0, 2014-10-30
Final

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1 Product Overview

1.1 Features

- ESD / Transient protection of high speed data lines exceeding
 - IEC61000-4-2 (ESD): **±20 kV (contact)**
 - IEC61000-4-4 (EFT): **±2 kV / ±40 A (5/50 ns)**
 - IEC61000-4-5 (surge): **±3 A (8/20 μs)**
- Maximum working voltage: $V_{RWM} = \pm 5.3 \text{ V}$
- Ultra low capacitance: $C_L = 0.4 \text{ pF (typical)}$
- Very low clamping voltage $V_{CL} = +20 / -15 \text{ V (typical) at } I_{TLP} = 16 \text{ A}$
- Low dynamic resistance $R_{DYN} = 0.5 \Omega \text{ (typical)}$
- Very small form factor down to $0.62 \times 0.32 \times 0.31 \text{ mm}^3$
- Pb-free (RoHS compliant) and halogen free package



1.2 Application Examples

- USB 2.0, Mobile HDMI Link, MDDI, MIPI, etc.
- HDMI, DisplayPort, DVI, Ethernet, Firewire, S-ATA

1.3 Product Description

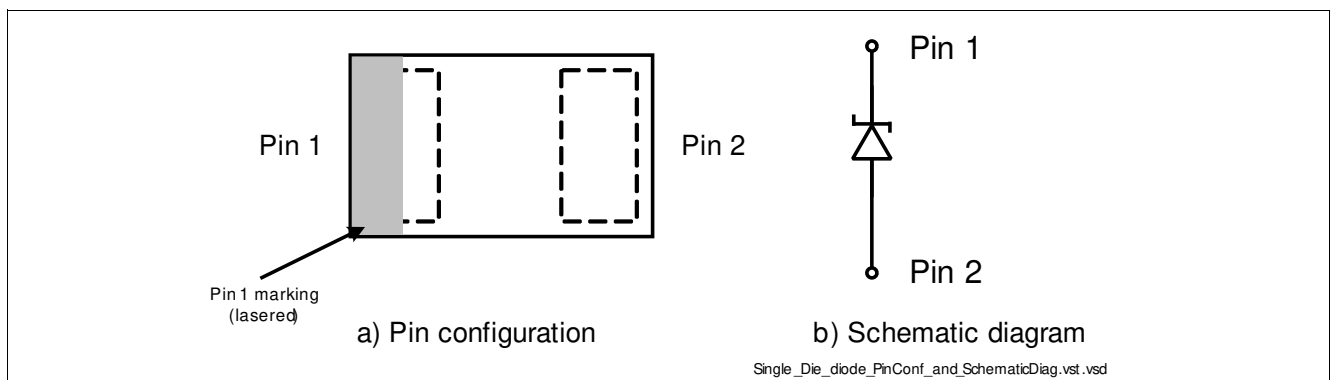


Figure 1 Pin Configuration and Schematic Diagram

Table 1 Ordering Information

Type	Package	Configuration	Marking code
ESD114-U1-02ELS	TSSLP-2-3	1 line, uni-directional	<u>K</u>
ESD114-U1-02EL	TSLP-2-19	1 line, uni-directional	K

2 Maximum Ratings

Table 2 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values	Unit
ESD contact discharge ¹⁾	V_{ESD}	± 20	kV
Peak pulse current ($t_p = 8/20\ \mu\text{s}$) ²⁾	I_{PP}	± 3	A
Operating temperature range	T_{OP}	-55 to 125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2

2) Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

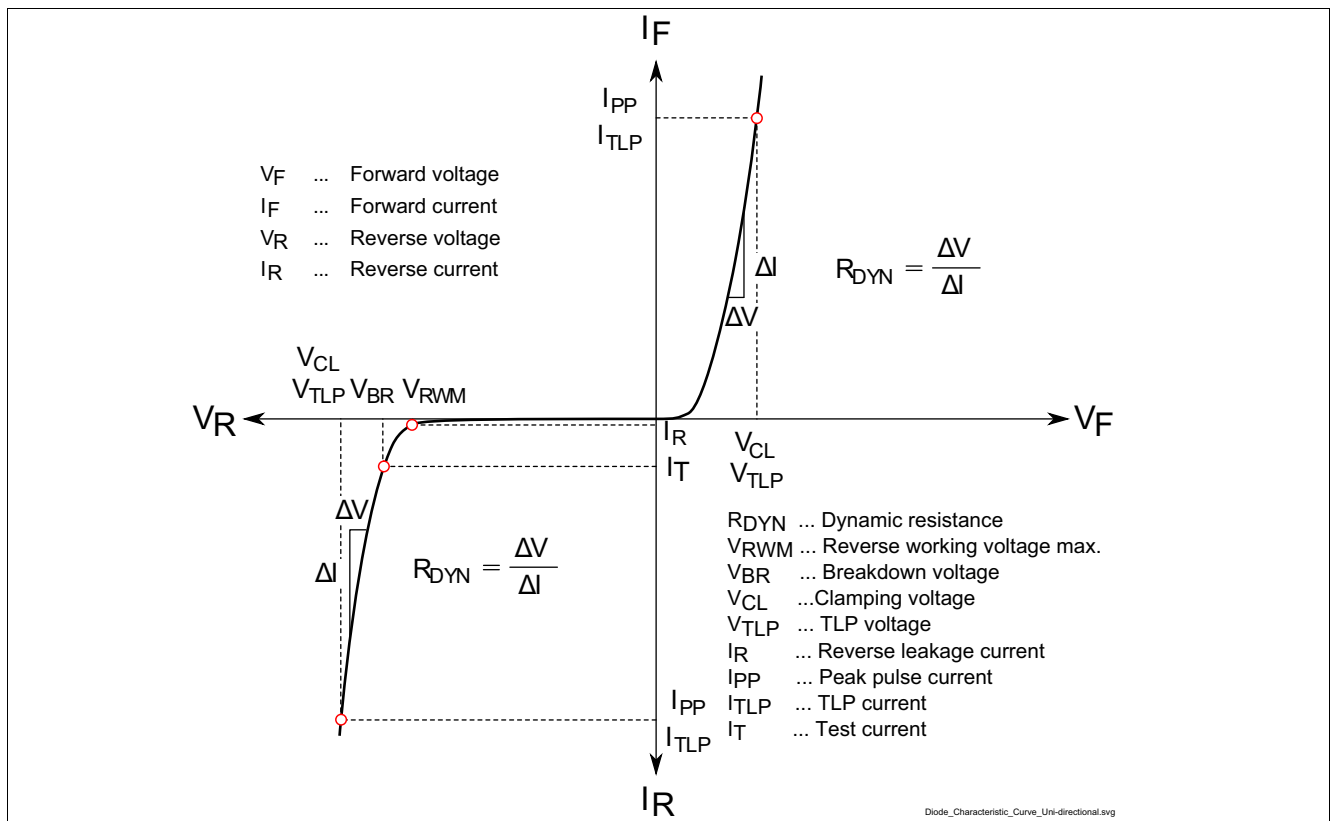


Figure 2 Definitions of Electrical Characteristics

Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified
Table 3 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	5.3	V	Pin 1 to Pin 2
Breakdown voltage	V_{BR}	6	–	–	V	$I_{BR} = 1\text{ mA}$, from Pin 1 to Pin 2
Reverse current	I_R	–	<10	100	nA	$V_R = 5.3\text{ V}$, from Pin 1 to Pin 2

Table 4 RF Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance ¹⁾	C_L	–	0.4	0.6	pF	$V_R = 0\text{ V}$, $f = 1\text{ MHz}$
Serie inductance	L_S	–	0.2	–	nH	ESD114-U1-02ELS
		–	0.4	–	nH	ESD114-U1-02EL

1) Total capacitance line to ground

Table 5 ESD Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage	V_{CL}	–	10	–	V	$I_{TLP} = 1\text{ A}$, from Pin 1 to Pin 2
		–	20	–		$I_{TLP} = 16\text{ A}$, from Pin 1 to Pin 2
		–	28	–		$I_{TLP} = 30\text{ A}$, from Pin 1 to Pin 2
		–	3	–		$I_{TLP} = 1\text{ A}$, from Pin 2 to Pin 1
		–	15	–		$I_{TLP} = 16\text{ A}$, from Pin 2 to Pin 1
		–	21	–		$I_{TLP} = 30\text{ A}$, from Pin 2 to Pin 1
Dynamic resistance ¹⁾	R_{DYN}	–	0.56	–	V	Pin 1 to Pin 2
		–	0.43	–	V	Pin 2 to Pin 1

1) Please refer to Application Note AN210[4]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 300\text{ ps}$, averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristics between $I_{PP1} = 10\text{ A}$ and $I_{PP2} = 40\text{ A}$.

4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25^\circ\text{C}$, unless otherwise specified

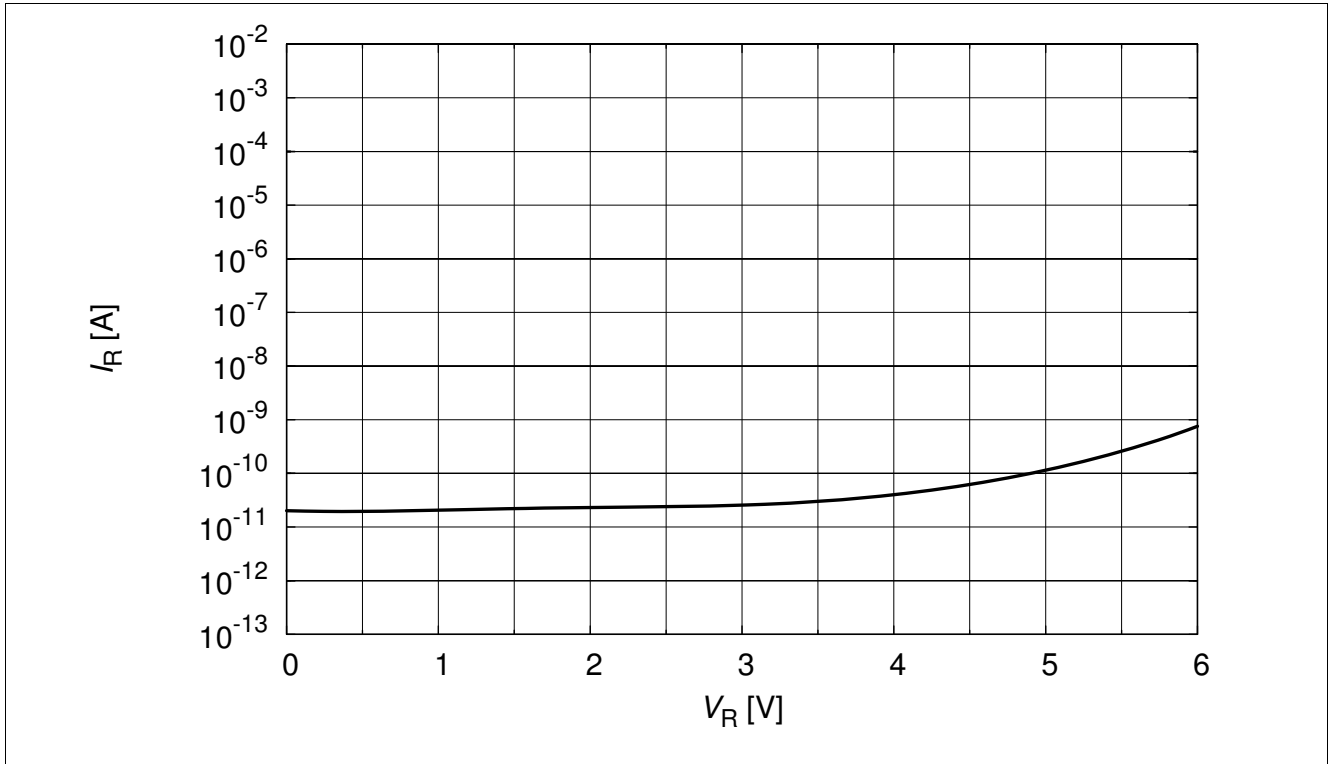


Figure 3 Reverse leakage current: $I_R = f(V_R)$

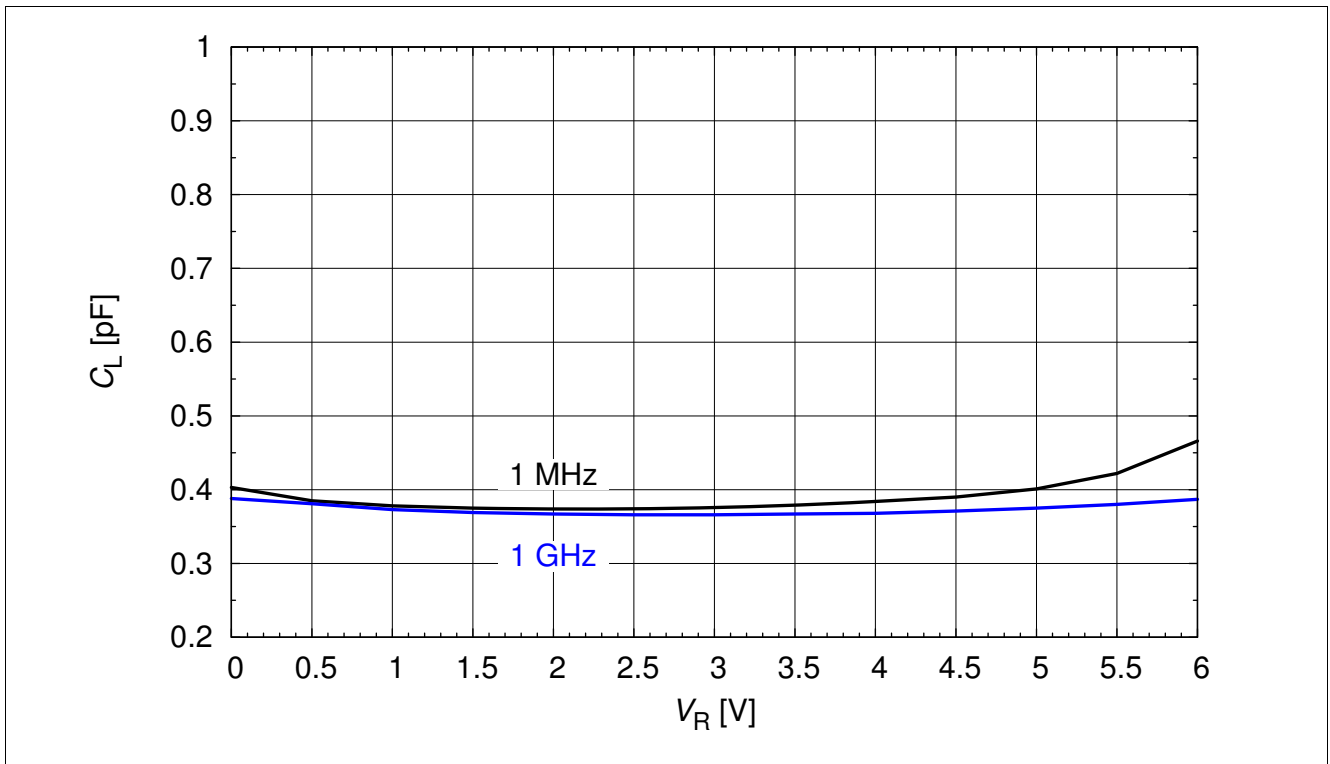


Figure 4 Line capacitance: $C_L = f(V_R)$

Typical Characteristics Diagrams

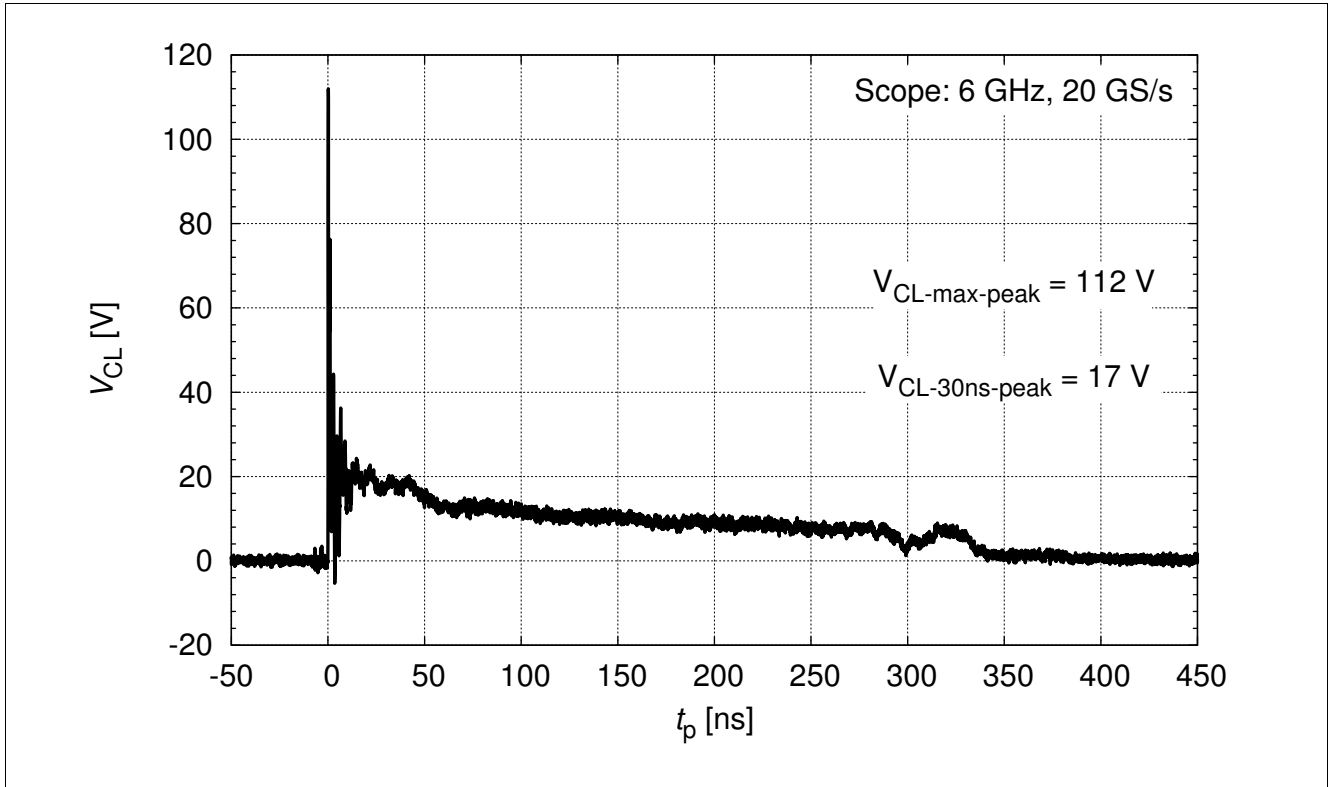


Figure 5 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

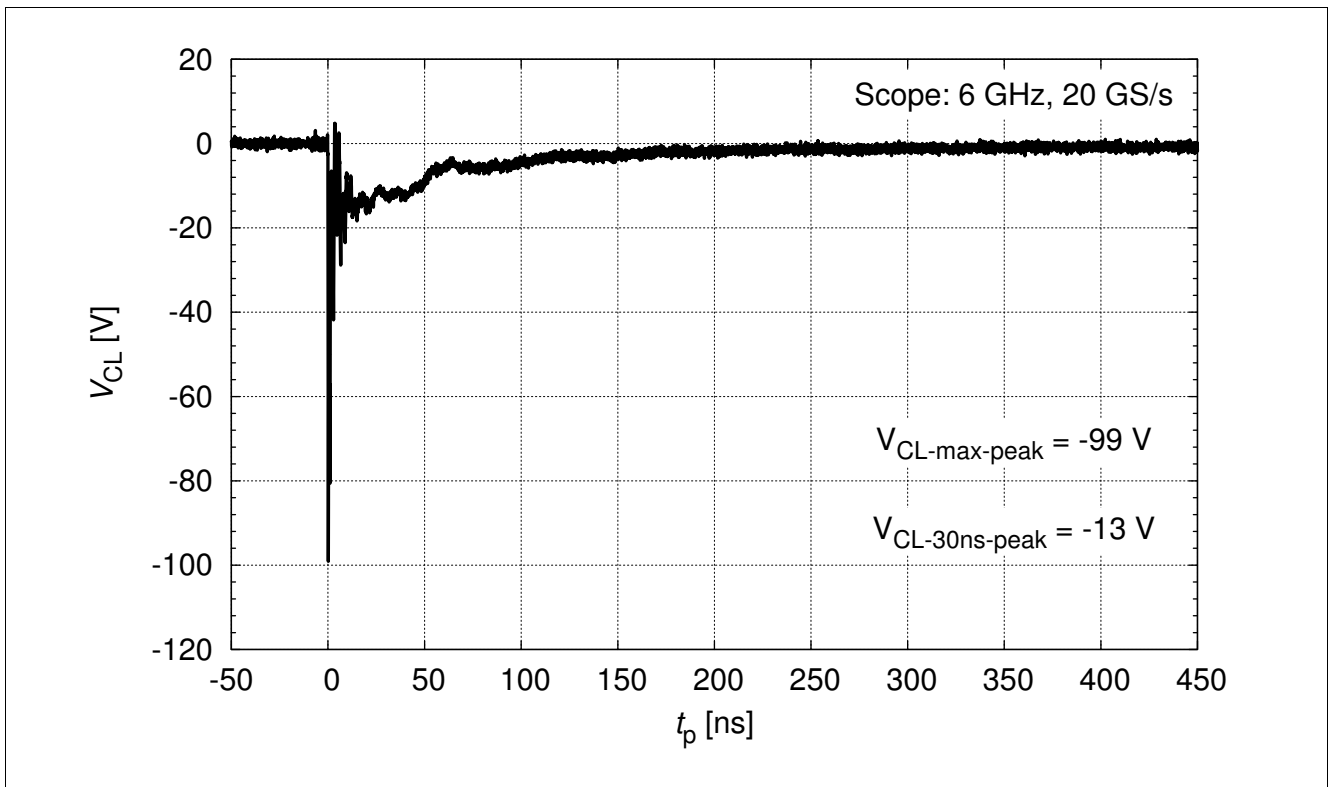


Figure 6 IEC61000-4-2 : $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

Typical Characteristics Diagrams

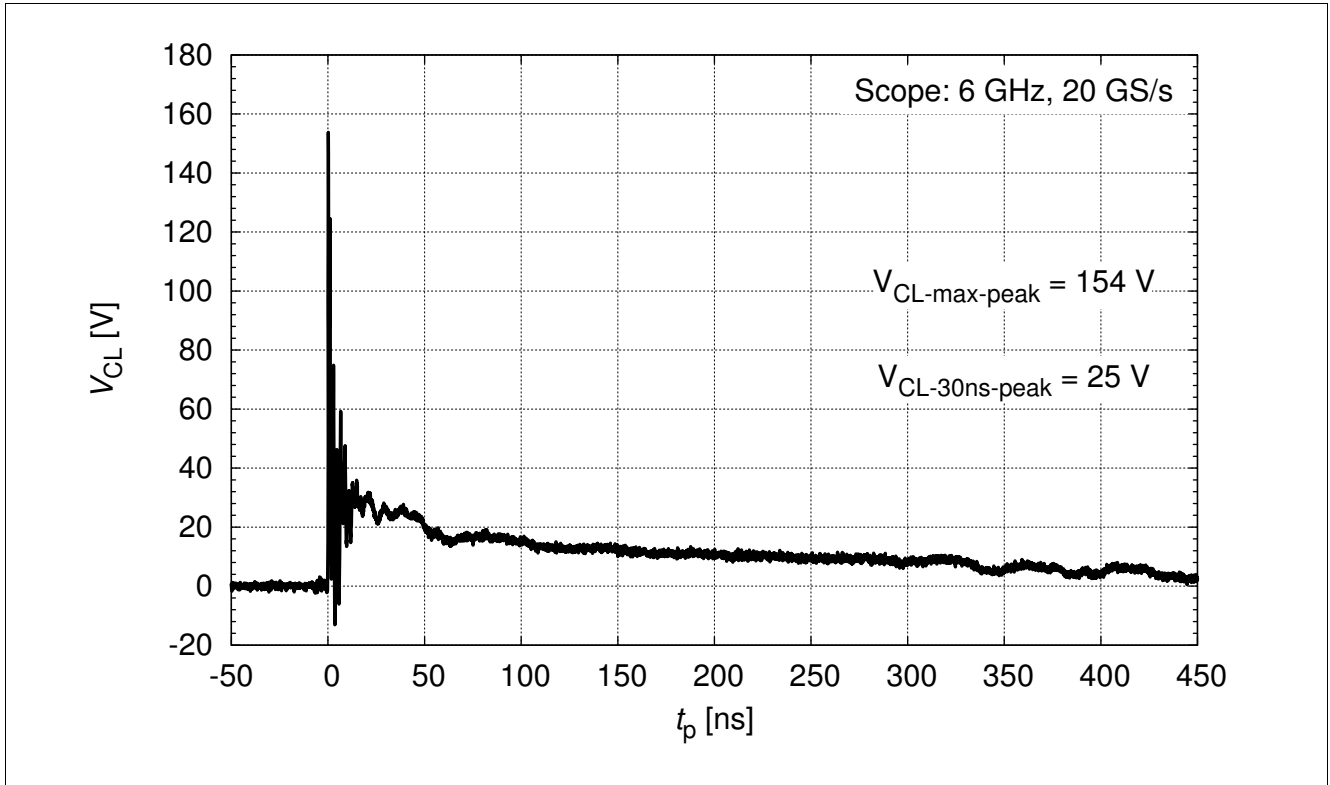


Figure 7 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

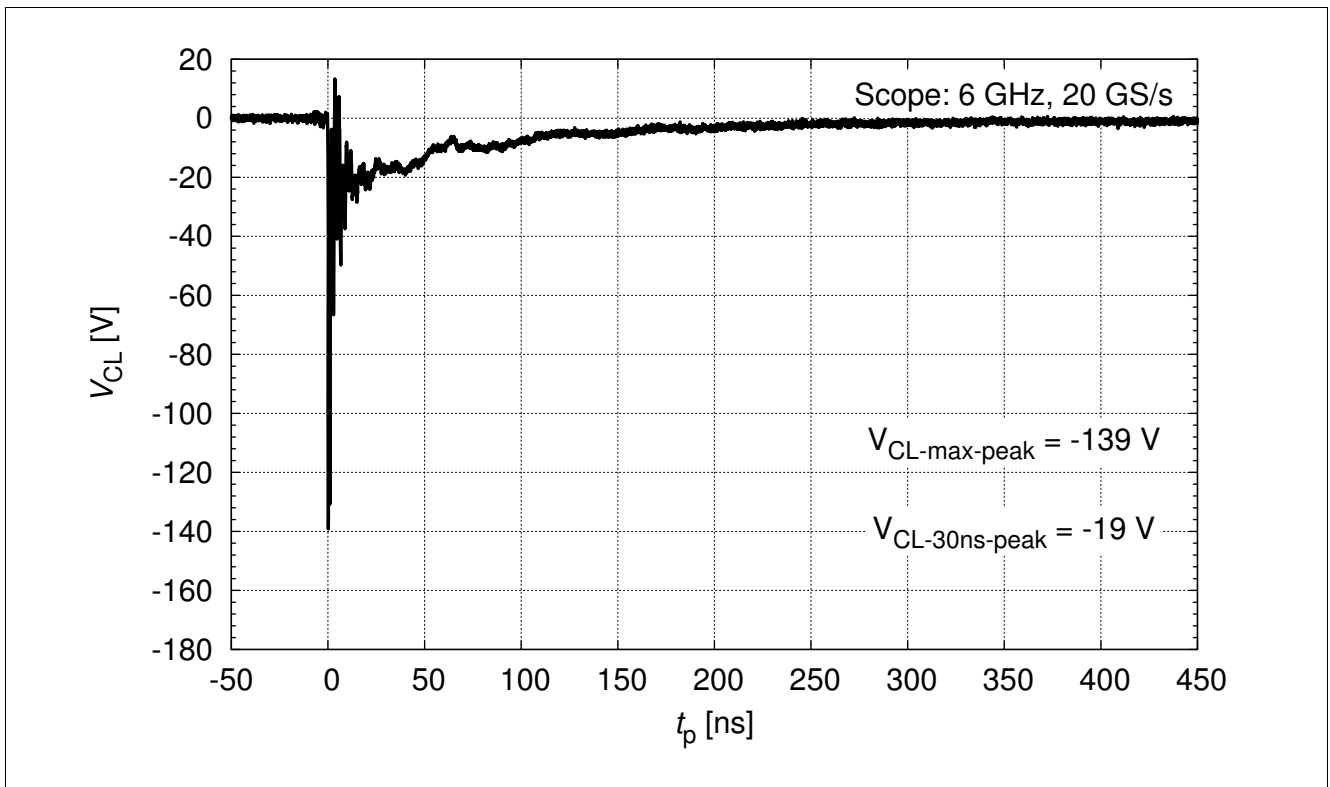


Figure 8 IEC61000-4-2 : $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

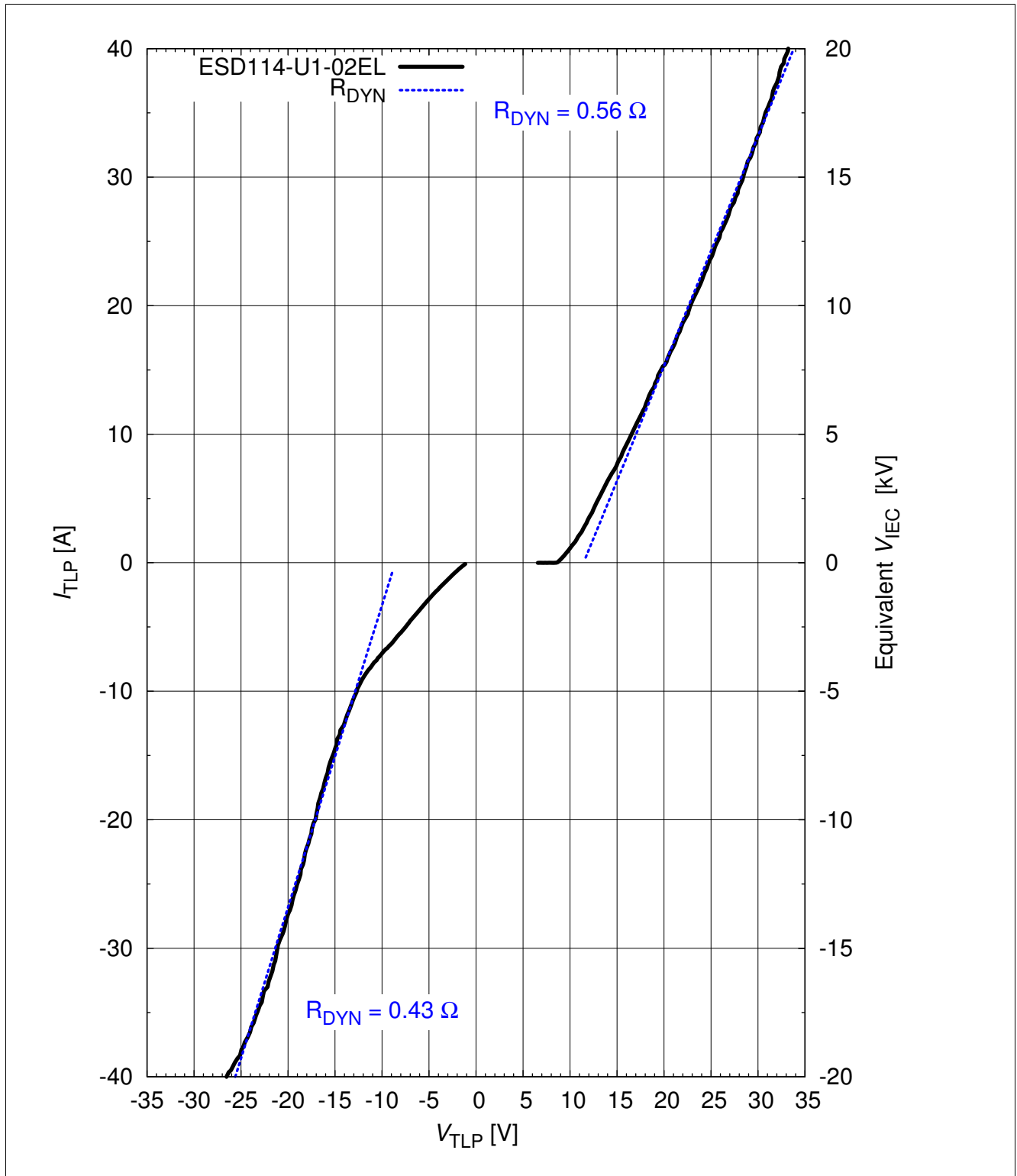


Figure 9 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1], pin 1 to pin 2

5 Package Information

5.1 TSSLP-2-3 (mm)[3]

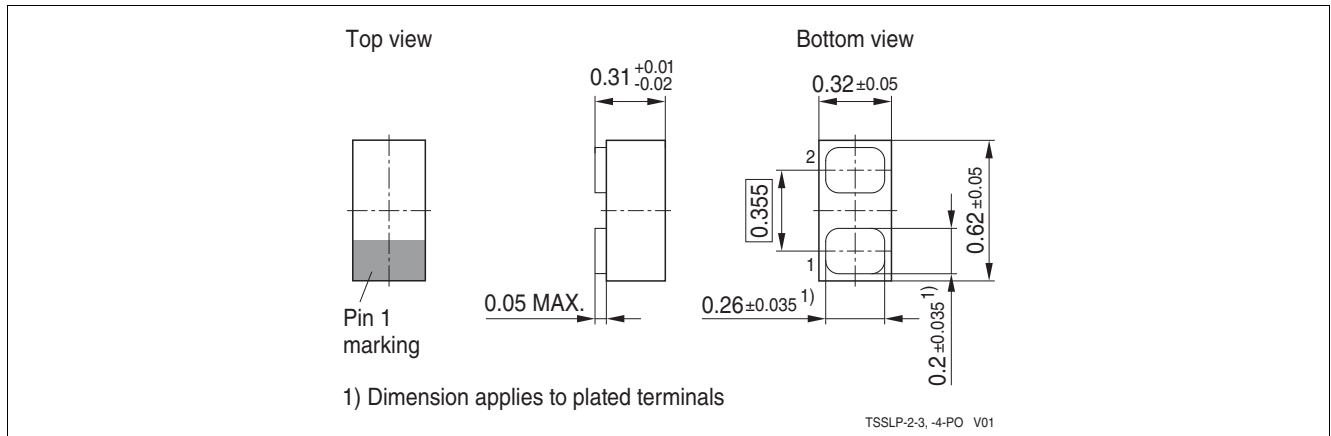


Figure 10 TSSLP-2-3: Package overview

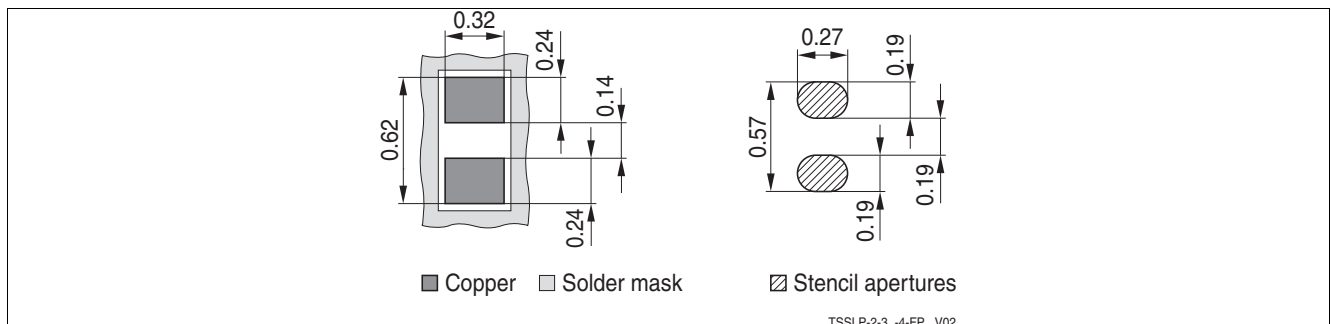


Figure 11 TSSLP-2-3 Footprint

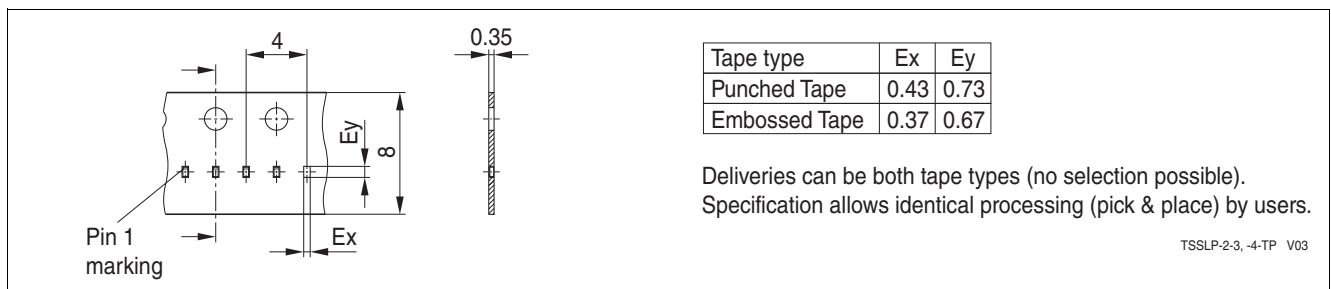


Figure 12 TSSLP-2-3: Packing

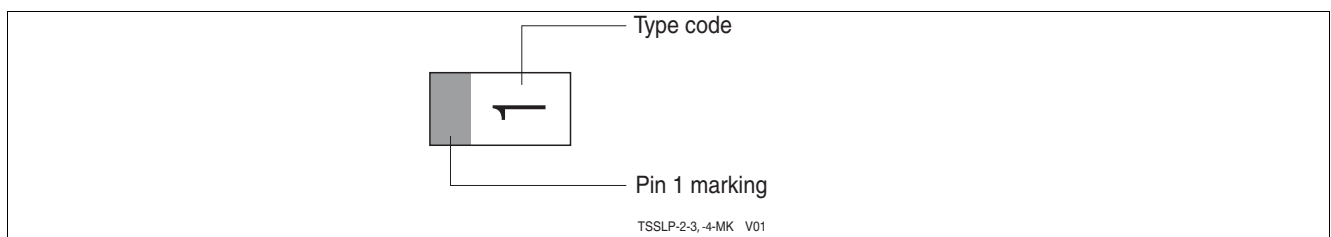


Figure 13 TSSLP-2-3: Marking (example)

5.2 TSLP-2-19 (mm)[3]

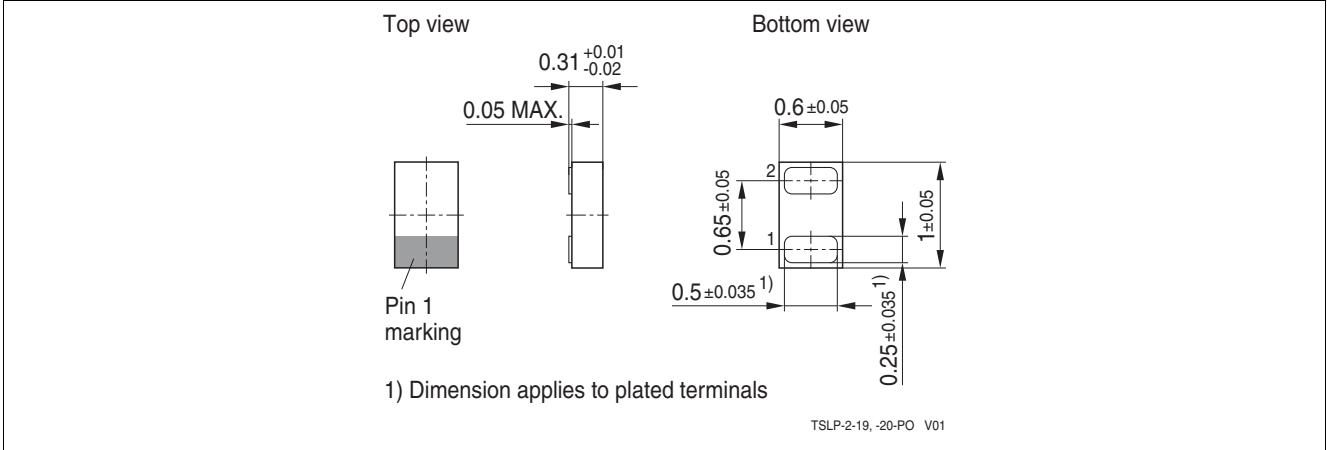


Figure 14 TSLP-2-19: Package Overview

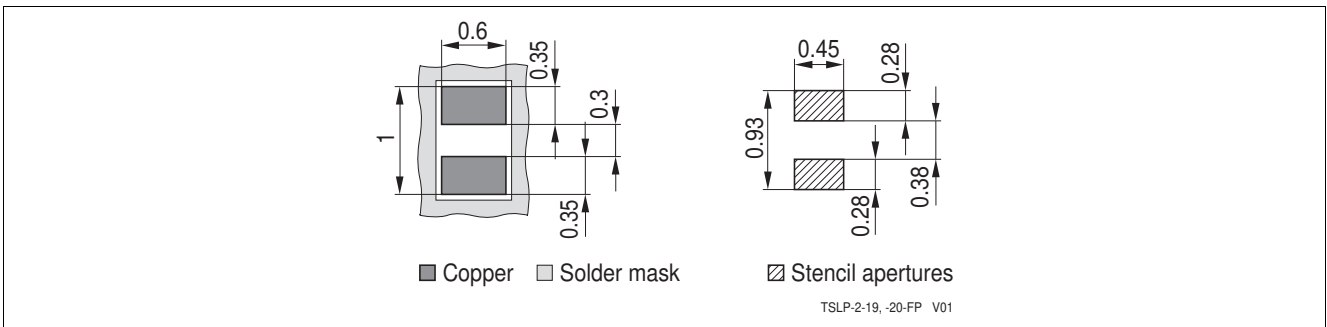


Figure 15 TSLP-2-19: Footprint

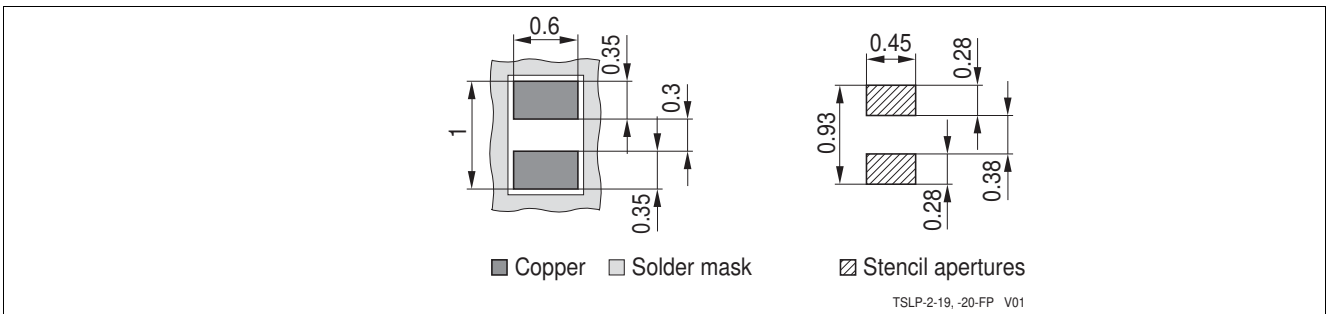


Figure 16 TSLP-2-19: Packing

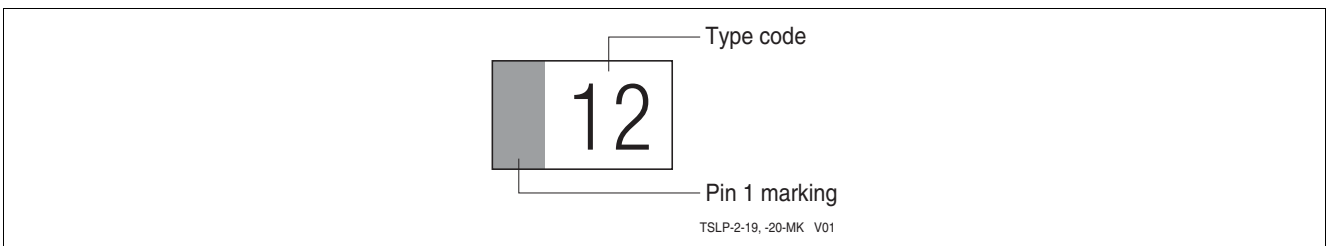


Figure 17 TSLP-2-19: Marking (example)

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection Design at System Level Using VF-TLP
- [2] Infineon AG - **Application Note AN140**: ESD Protection for Digital High-Speed Interfaces (HDMI, FireWire, ...) using ESD5V3U1U)
- [3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

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Page or Item	Subjects (major changes since previous revision)
Revision 1.0, 2014-10-30	
All	Status change to Final

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