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Protection Device

TVS (Transient Voltage Suppressor)

ESD128-B1-W0201

Bi-directional, 18 V (AC), 13 V (DC), 0.3 pF, 0201, RoHS and Halogen Free compliant

ESD128-B1-W0201

Data Sheet

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1 Product Overview

1.1 Features

- ESD / transient protection of high speed data lines according to:
 - IEC61000-4-2 (ESD): ± 15 kV (air/contact discharge)
 - IEC61000-4-4 (EFT): ± 2 kV / ± 40 A(5/50 ns)
 - IEC61000-4-5 (surge): ± 2 A (8/20 μ s)
- Bi-directional working voltage up to: $V_{RWM} = \pm 18$ V (AC), ± 13 V (DC)
- Line capacitance: $C_L = 0.3$ pF (typical) at $f = 1$ MHz
- Clamping voltage: $V_{CL} = 32$ V (typical) at $I_{TLP} = 16$ A with $R_{DYN} = 0.85$ Ω (typical)
- Very low reverse current. $I_R < 1$ nA (typical)
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 0201 and low profile (0.58 mm x 0.28 mm x 0.15 mm)
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package



Guidelines for optimized PCB design and assembly process available [\[2\]](#)



1.2 Application Examples

- ESD Protection of RF signal lines in Near Field Communication (NFC) applications [\[3\]](#)

1.3 Product Description

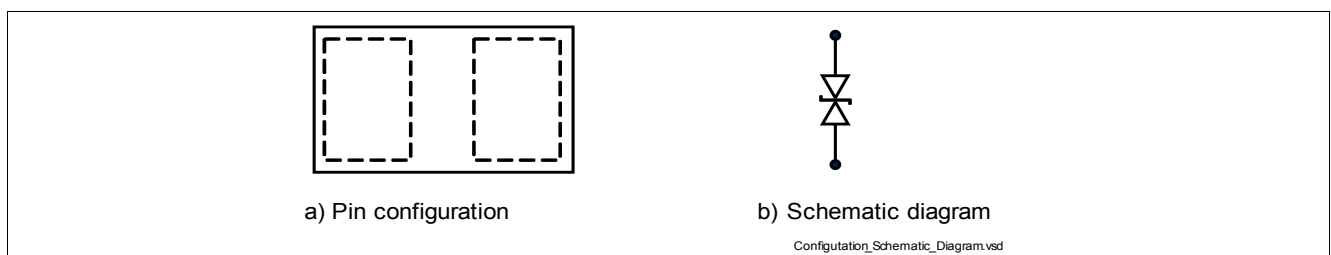


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD128-B1-W0201	WLL-2-1	1 line, bi-directional	K ¹⁾

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Maximum Ratings

Table 2-1 Maximum Ratings at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified¹⁾

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	$\pm 18^{2)}$ $\pm 13^{3)}$	V
ESD (air / contact) discharge ⁴⁾	V_{ESD}	± 15	kV
Peak pulse power ⁵⁾	P_{PK}	53	W
Peak pulse current ⁵⁾	I_{PP}	± 2	A
Operating temperature range	T_{OP}	-55 to 125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$

- 1) Device is electrically symmetrical
- 2) For RF peak voltage (NFC)
- 3) For DC voltage
- 4) V_{ESD} according to IEC61000-4-2
- 5) Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

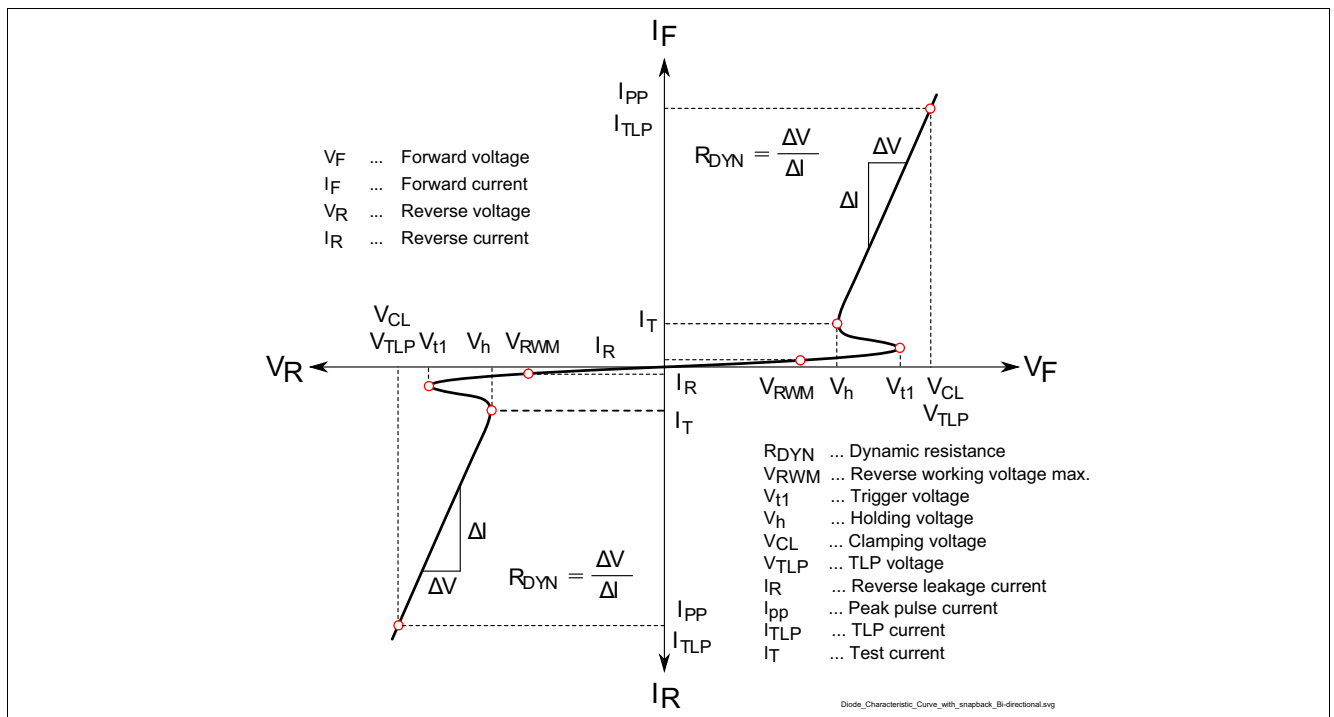


Figure 3-1 Definitions of electrical characteristics

Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified
Table 3-1 DC Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse current	I_R	–	<1	30	nA	$V_R = 18\text{ V}$
Trigger voltage	V_{t1}	20	22	–	V	
Holding voltage	V_h	13	17	21	V	$I_T = 40\text{ mA}$

1) Device is electrically symmetrical

Table 3-2 AC Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	0.15	0.3	0.5	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		–	0.3	–		$V_R = 0\text{ V}, f = 1\text{ GHz}$

Table 3-3 ESD and Surge Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage ²⁾	V_{CL}	–	32	–	V	$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$
Clamping voltage ³⁾		–	18.5	–		$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$
Dynamic resistance ²⁾	R_{DYN}	–	0.85	–	Ω	$t_p = 100\text{ ns}$

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1]. TLP parameter: $Z_0 = 50\text{ }\Omega$, $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$.

3) Stress pulse: 8/20 μs current waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

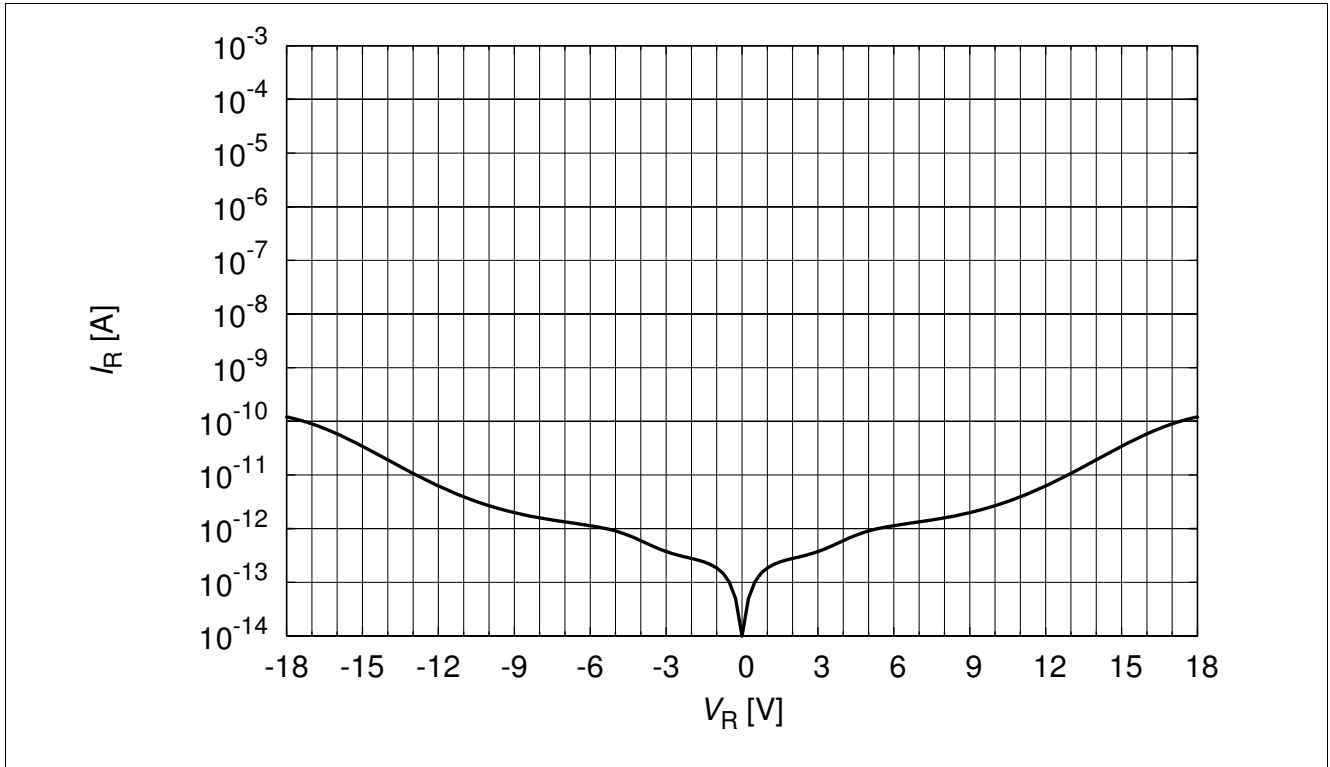


Figure 4-1 Reverse leakage current $I_R = f(V_R)$

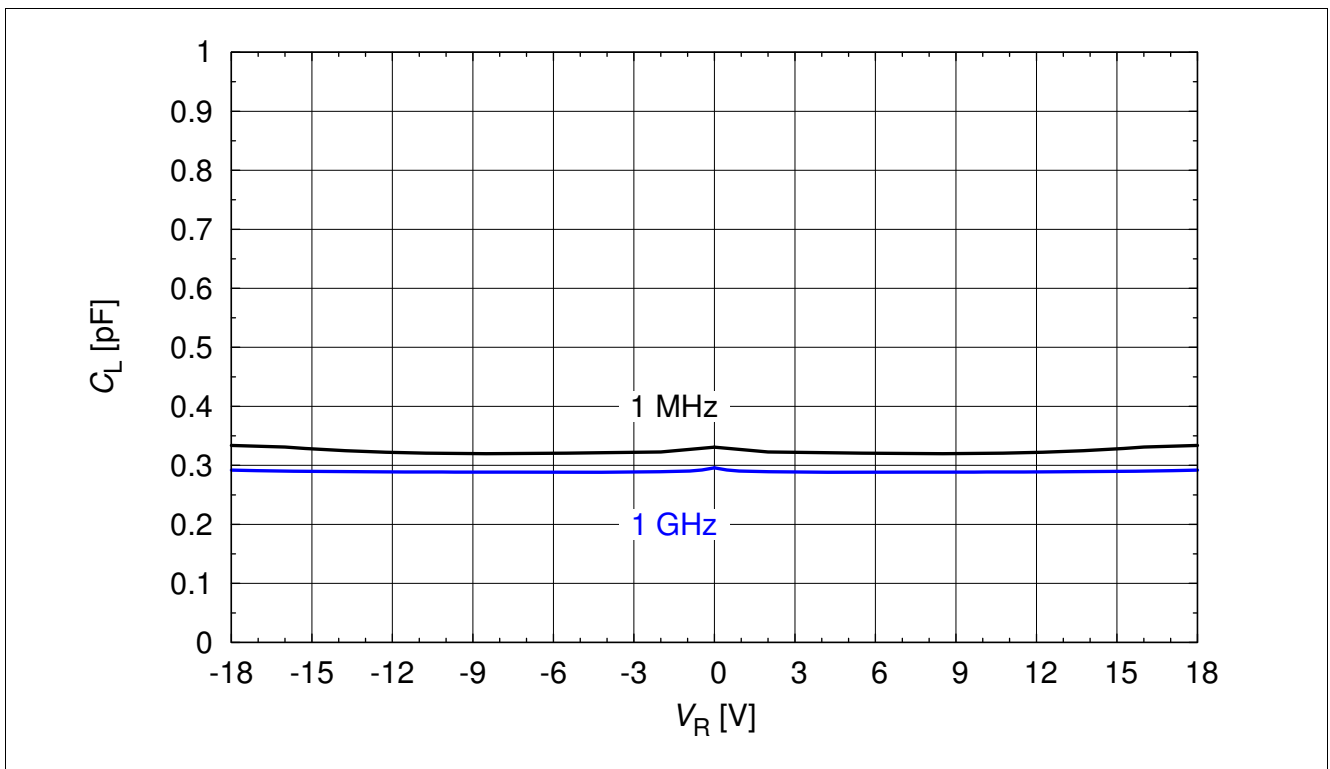


Figure 4-2 Line capacitance $C_L = f(V_R), f = 1\text{ MHz}$

Typical Characteristics Diagrams

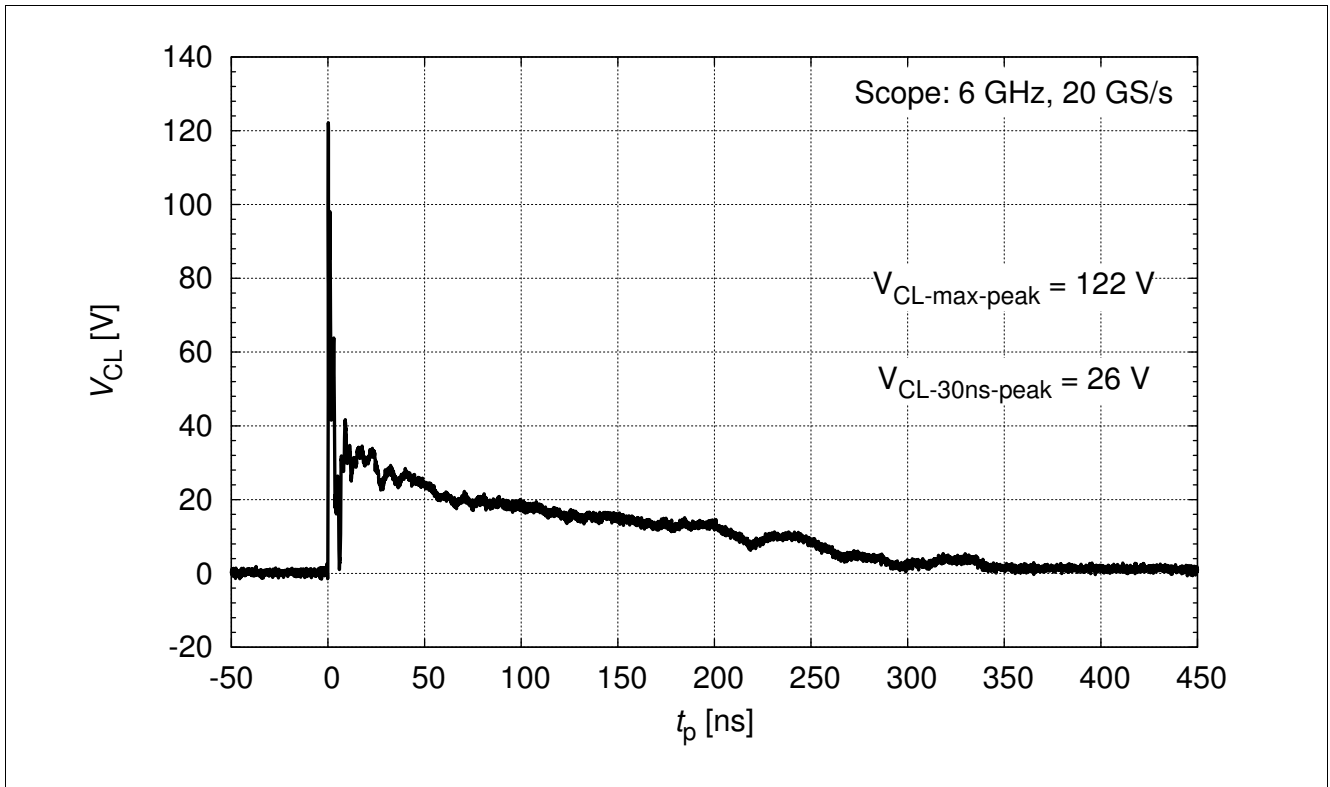


Figure 4-3 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse

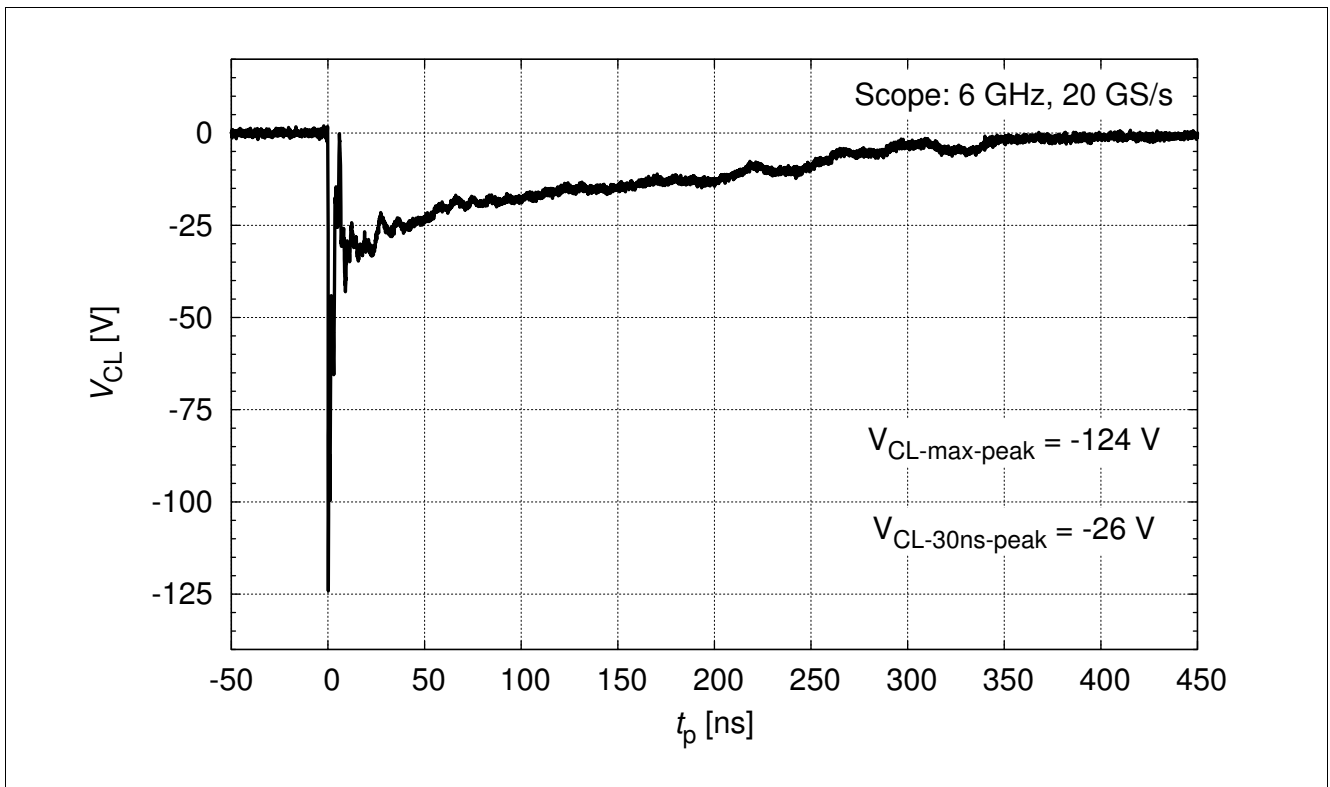


Figure 4-4 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse

Typical Characteristics Diagrams

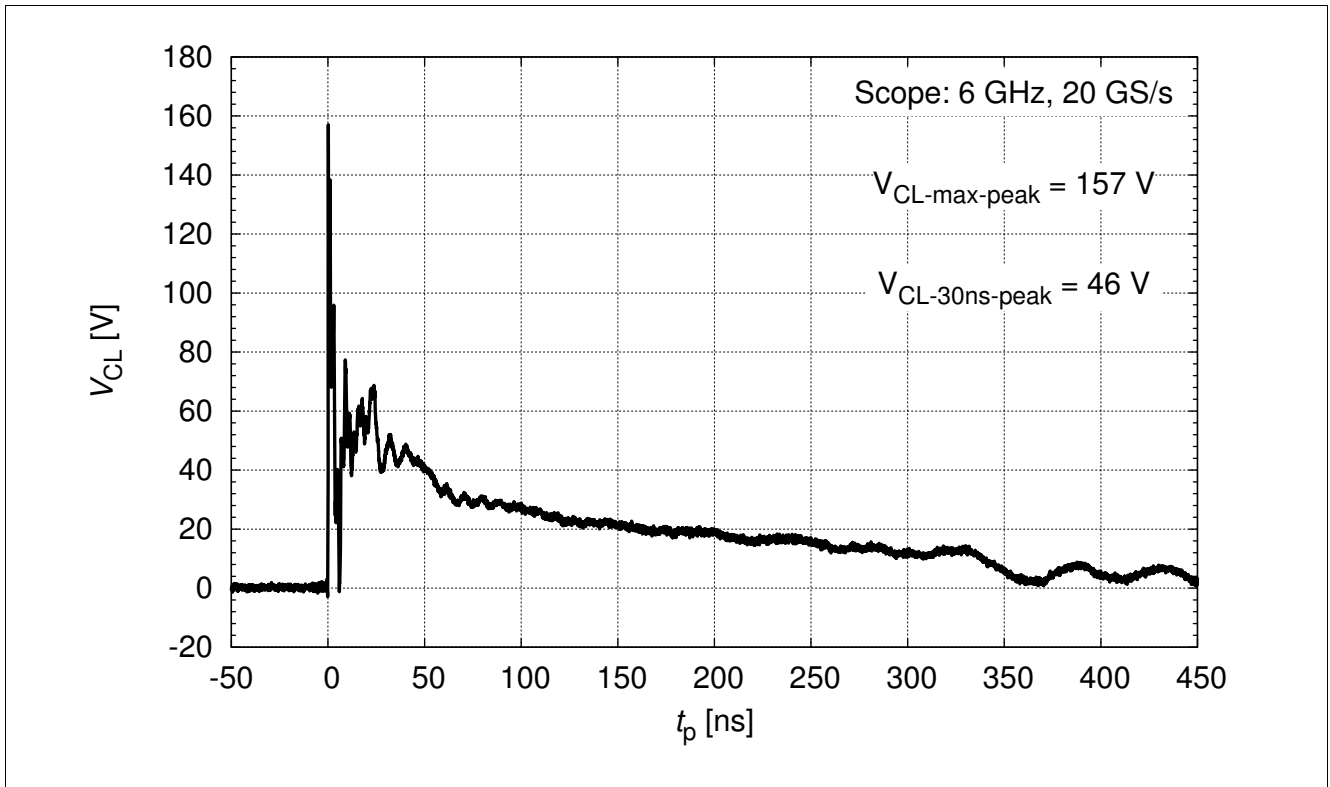


Figure 4-5 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positive pulse

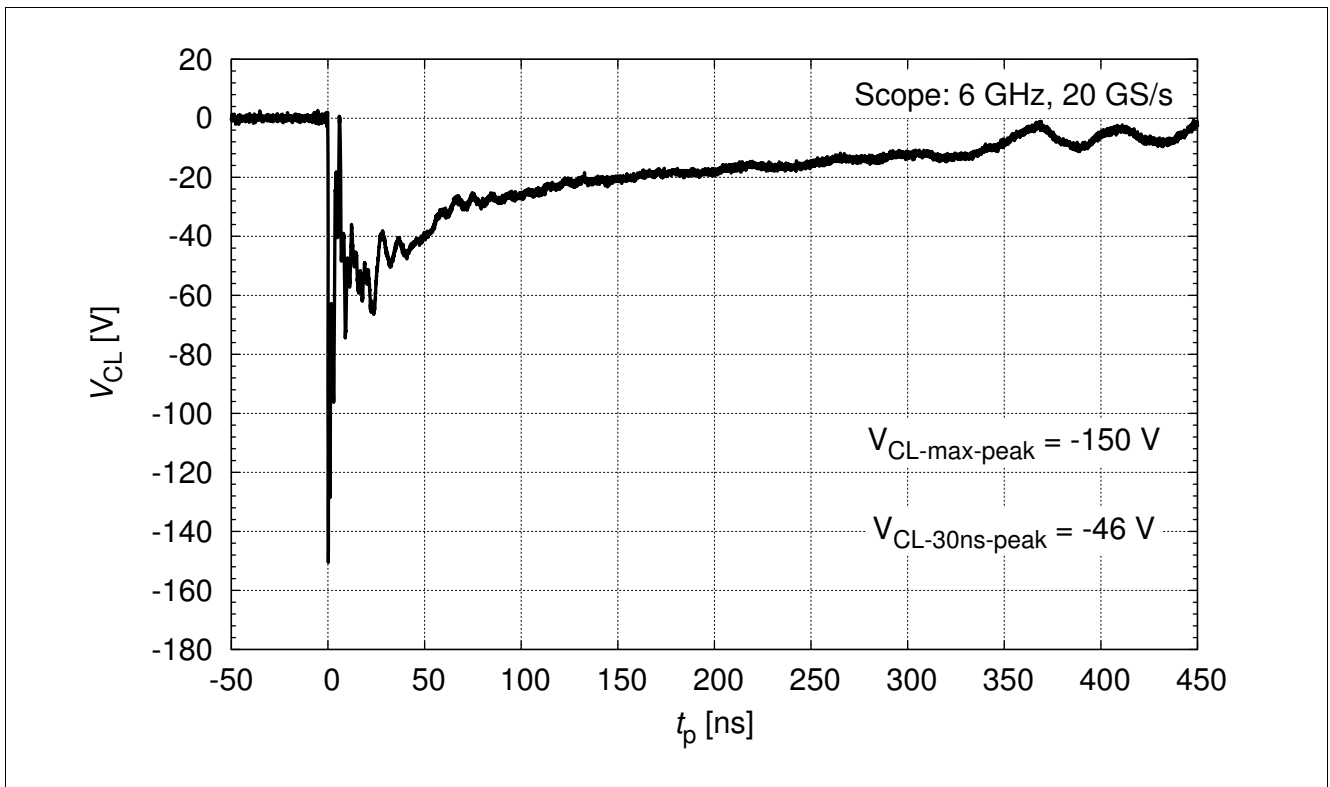


Figure 4-6 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negative pulse

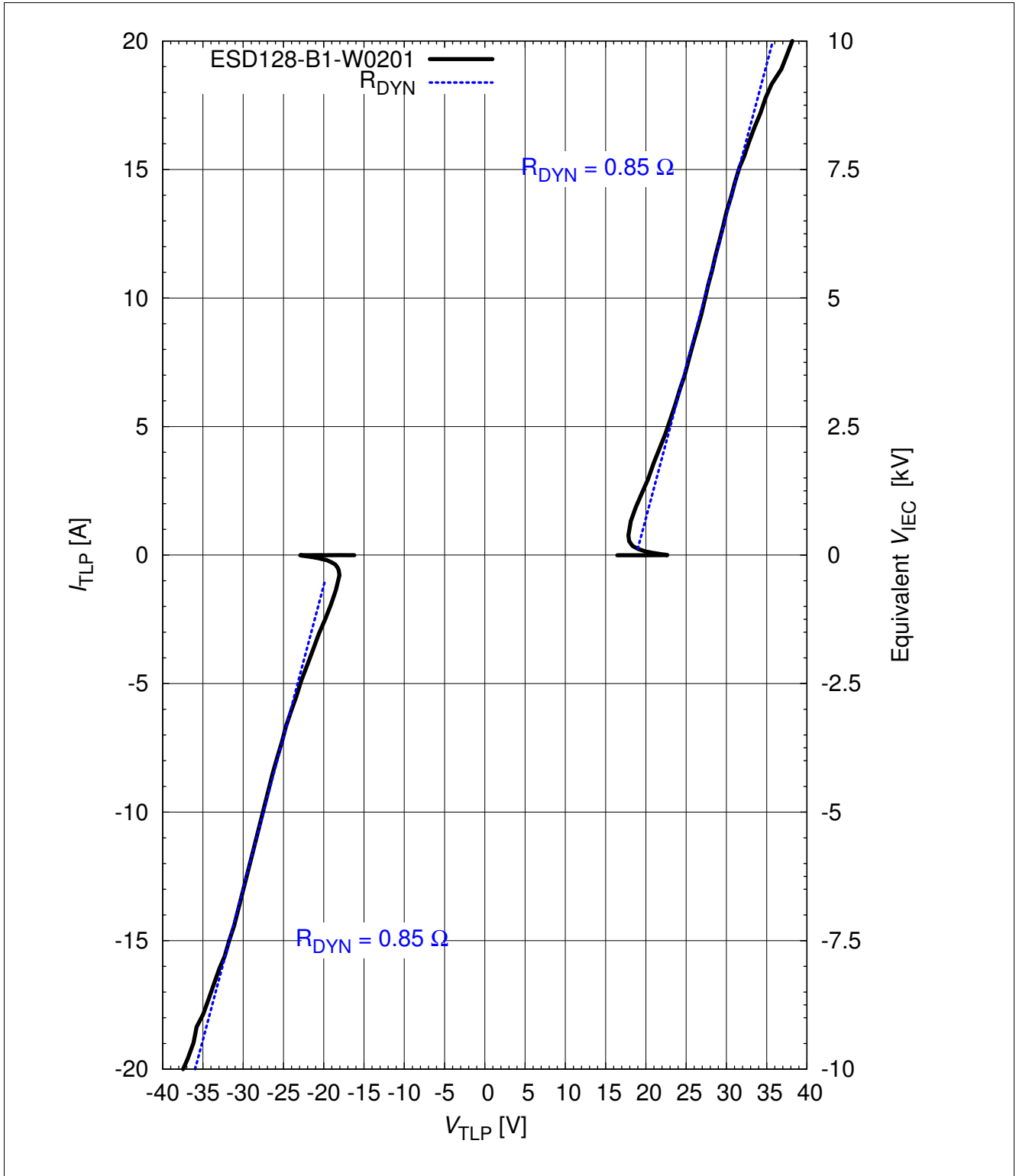


Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

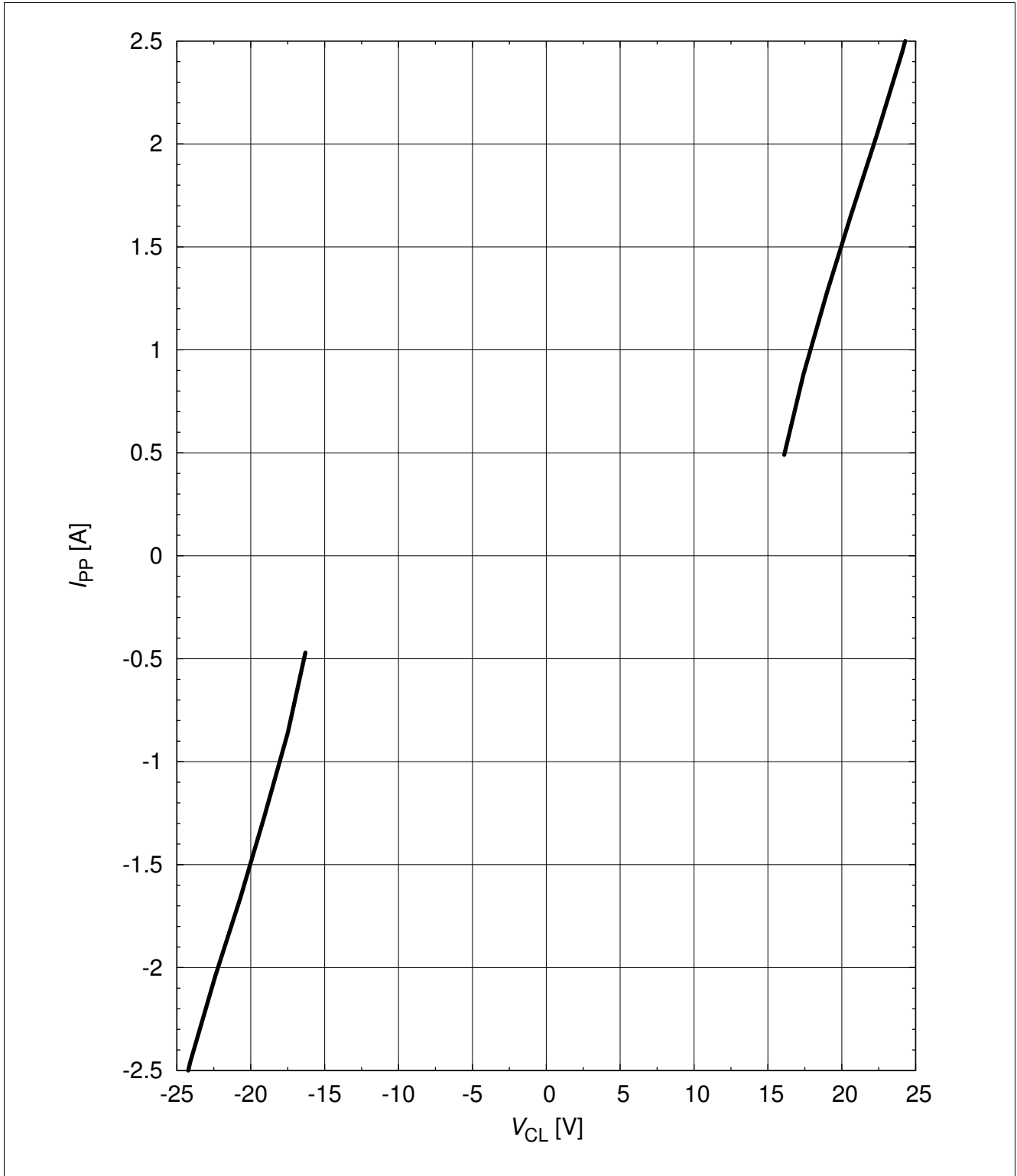


Figure 4-8 Clamping voltage(Surge): $I_{PP} = f(V_{CL})$ [1]

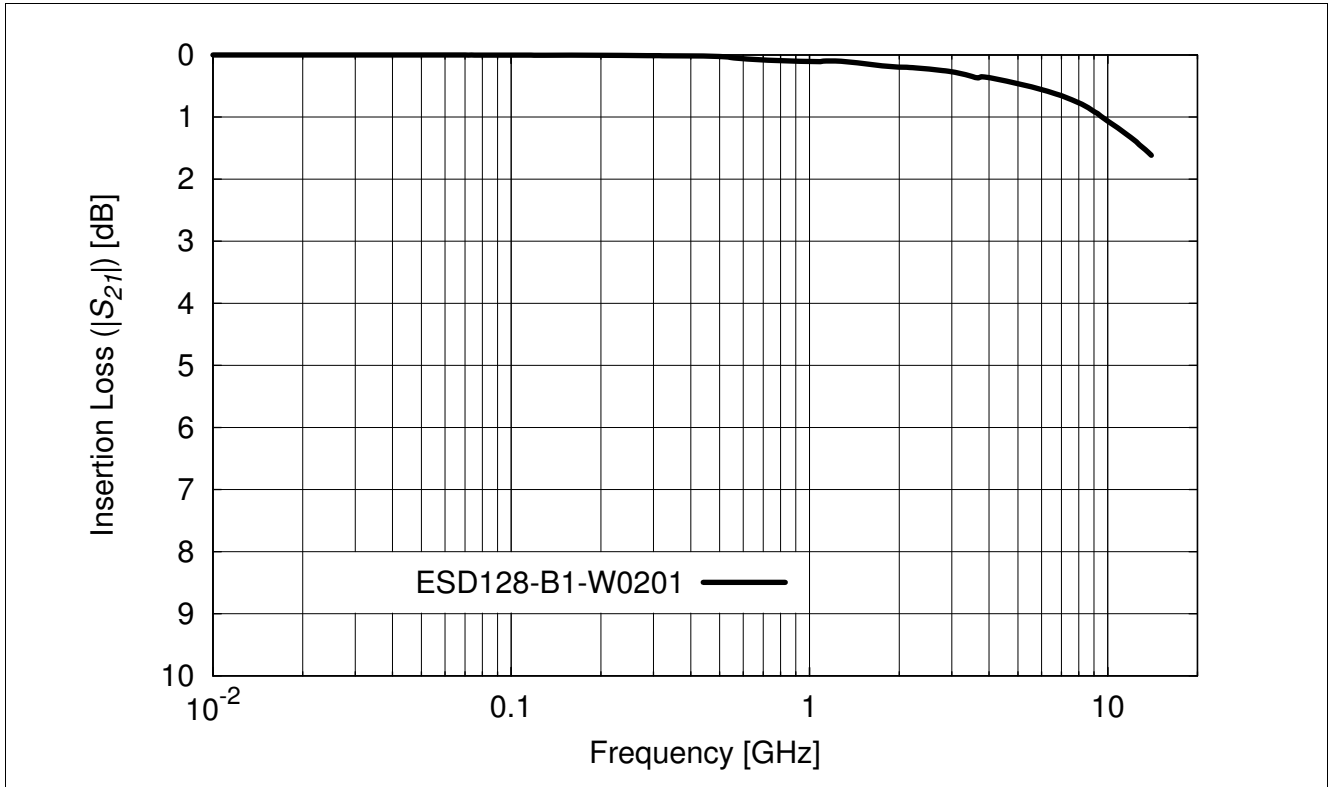


Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

5 Application Information

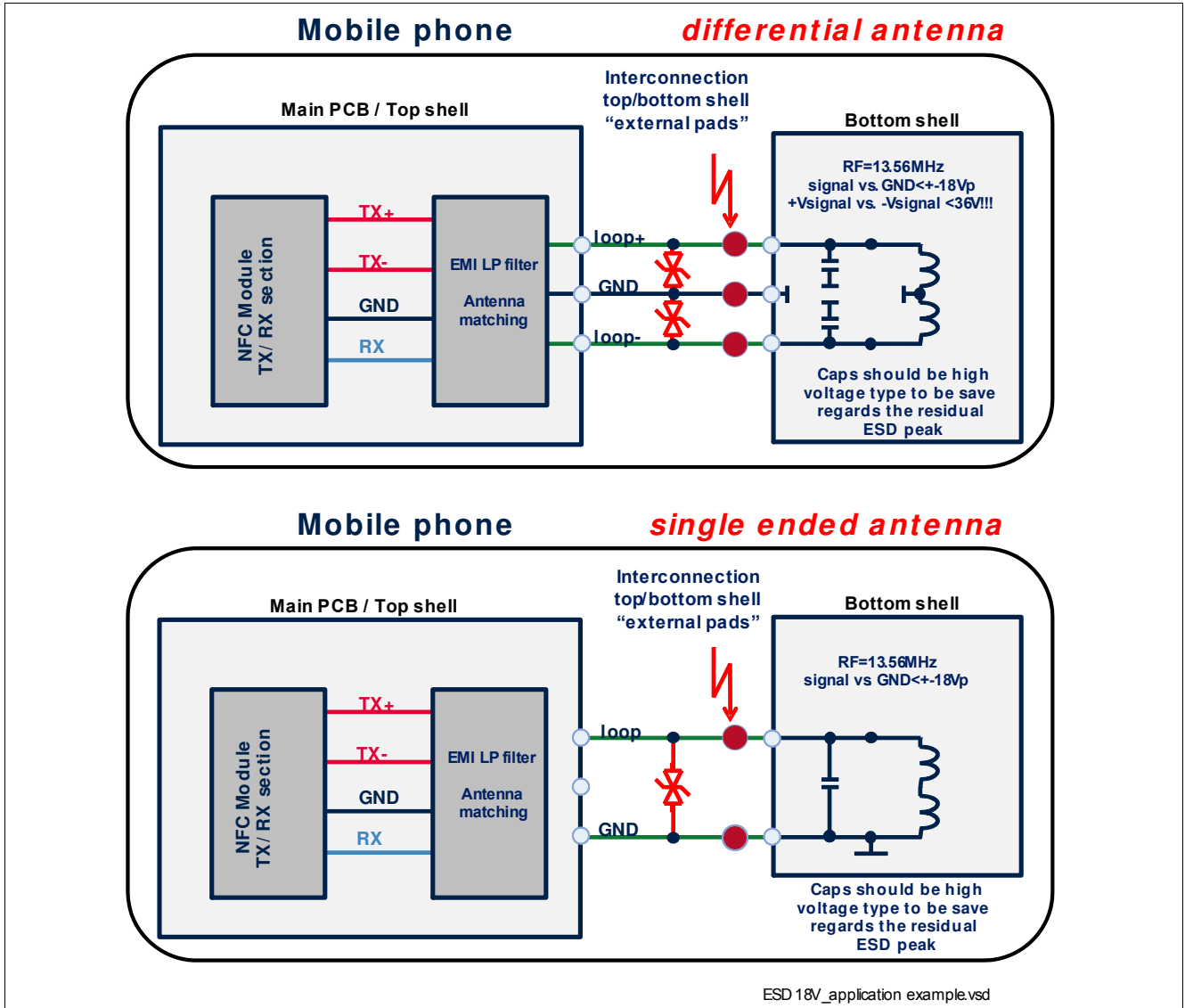


Figure 5-1 Bi-directional ESD / Transient protection for NFC Frontend [3]

6 Package Information

6.1 WLL-2-1

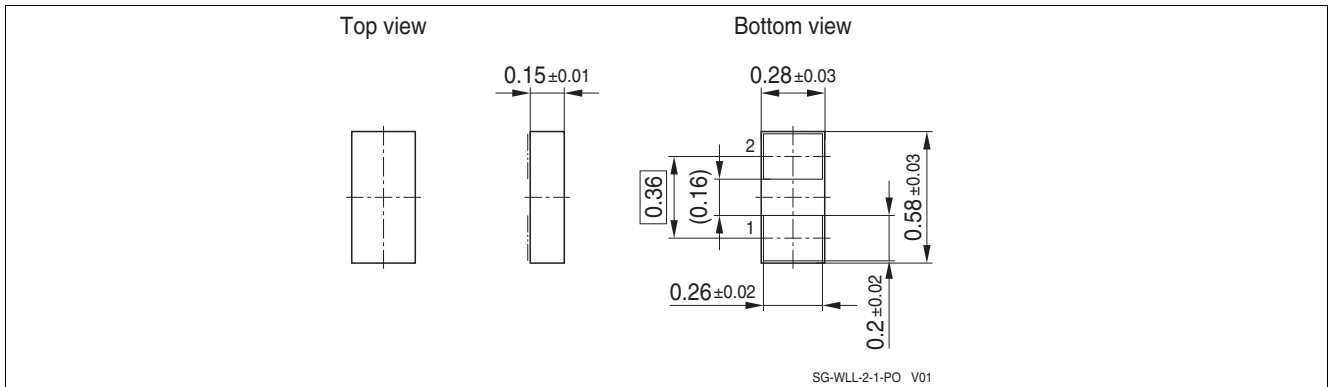


Figure 6-1 WLL-2-1 Package outline (dimension in mm)

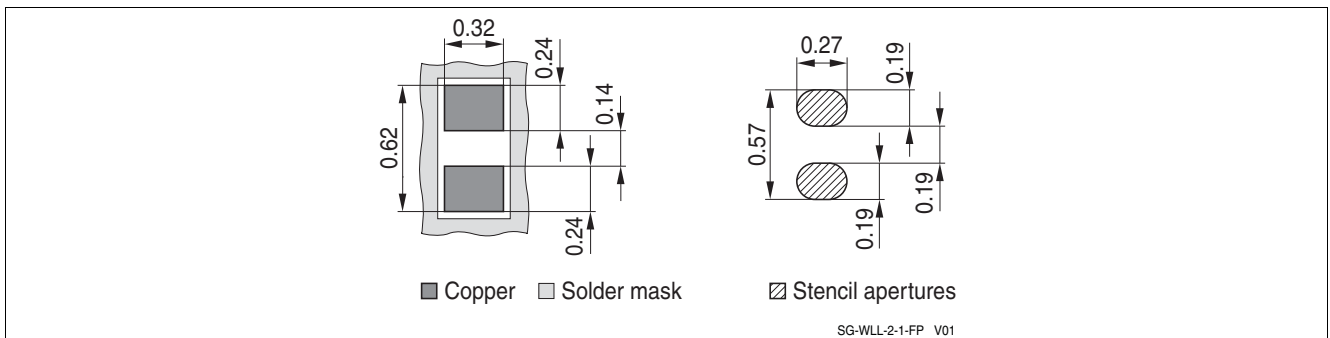


Figure 6-2 WLL-2-1 Footprint (see: Recommendation for Printed Circuit Board Assembly [2])

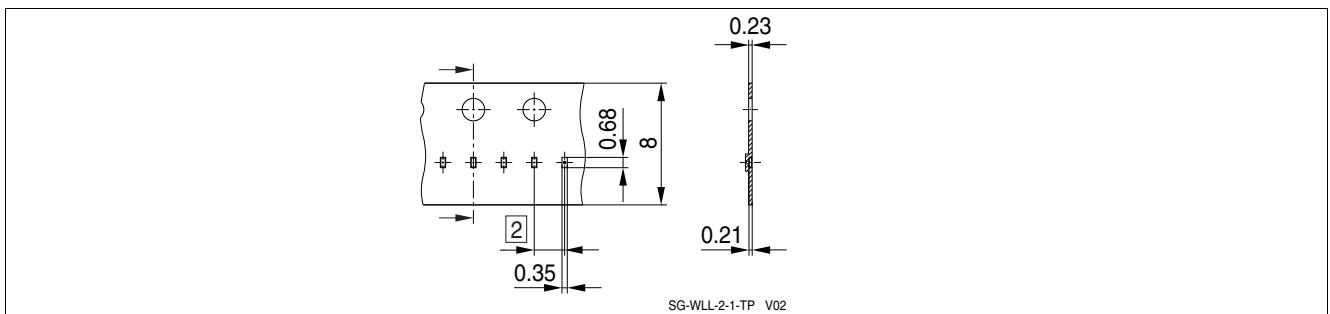


Figure 6-3 WLL-2-1 Packing (dimension in mm)

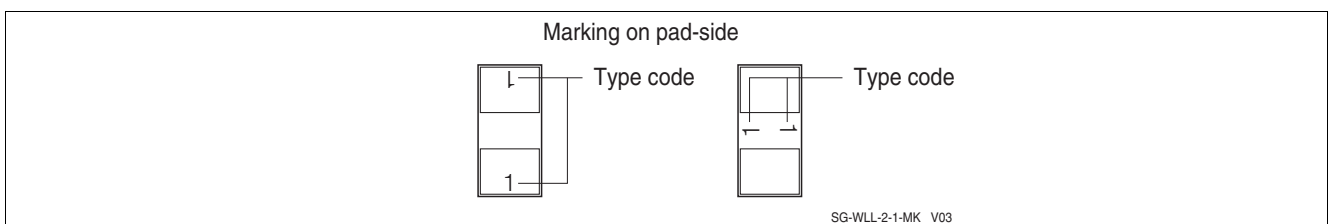


Figure 6-4 WLL-2-1 Marking example Table 1-1 "Part Information" on Page 3

References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
<http://www.infineon.com/dgdl/?fileId=db3a304344f7b4f9014503db540027c0>
- [3] Infineon AG - **Application Note AN244**: Tailored ESD Protection for the NFC Frontend

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Page or Item	Subjects (major changes since previous revision)
Revision 1.3, 2016-04-06	
All	New layout

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