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# Protection Device

TVS (Transient Voltage Suppressor)

## ESD202-B1-CSP01005

Bi-directional, 5.5 V, 6.5 pF, 01005, RoHS and Halogen Free compliant

ESD202-B1-CSP01005

## Data Sheet

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Final

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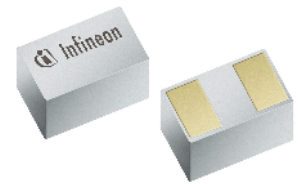
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# 1 Product Overview

## 1.1 Features

- ESD / transient protection of high speed data lines according to:
  - IEC61000-4-2 (ESD):  $\pm 17$  kV (air),  $\pm 15$  kV (contact discharge)
  - IEC61000-4-4 (EFT):  $\pm 2$  kV /  $\pm 40$  A(5/50 ns)
  - IEC61000-4-5 (surge):  $\pm 3$  A (8/20  $\mu$ s)
- Bi-directional working voltage up to:  $V_{RWM} = \pm 5.5$  V
- Line capacitance:  $C_L = 6.5$  pF (typical) at  $f = 1$  MHz
- Clamping voltage:  $V_{CL} = 13$  V (typical) at  $I_{TLP} = 16$  A with  $R_{DYN} = 0.2 \Omega$  (typical)
- Very low reverse current:  $I_R < 1$  nA (typical)
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 01005 and low profile (0.43 mm x 0.23 mm x 0.15 mm)
- Bi-directional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package



Guidelines for optimized PCB design and assembly process available [\[2\]](#)



## 1.2 Application Examples [\[3\]](#)

- ESD Protection of highly susceptible IC/ASICs in audio, headset, human digital interfaces
- Dedicated solution to boost space saving and high performance in miniaturized modern electronics

## 1.3 Product Description

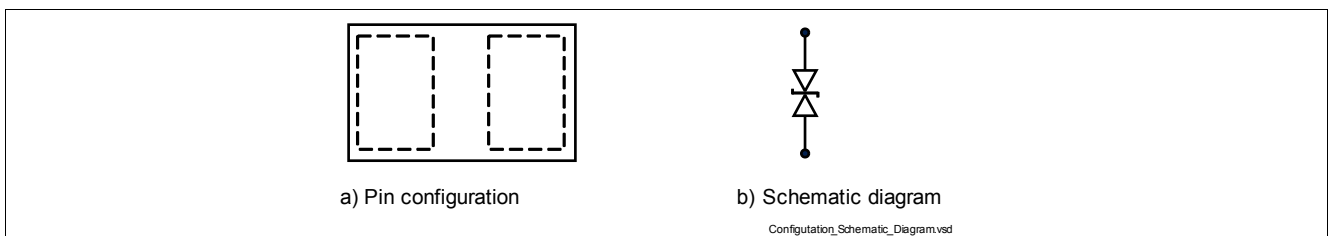


Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD202-B1-CSP01005	WLL-2-2	1 line, bi-directional	A <sup>1)</sup>

1) The device does not have any marking or date code on the device backside. The marking code is on pad side.

## 2 Maximum Ratings

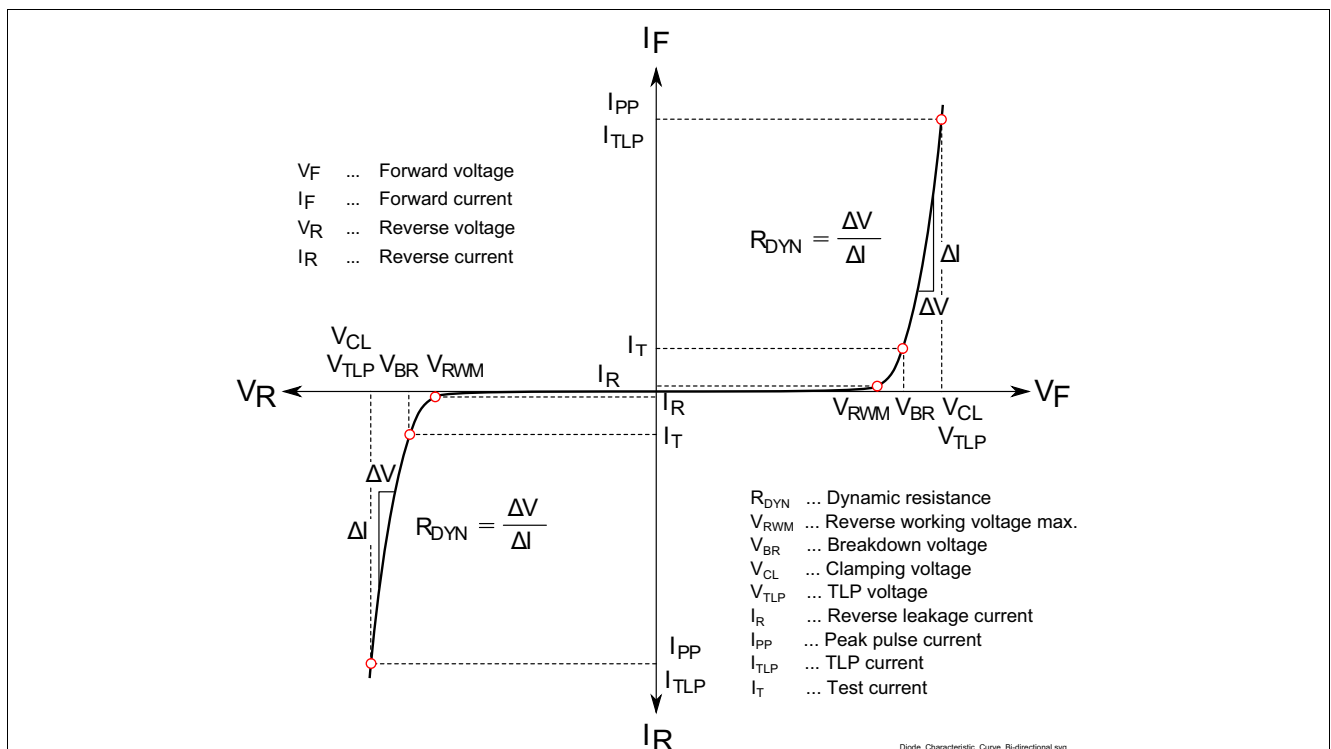
**Table 2-1 Maximum Ratings at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified <sup>1)</sup>**

Parameter	Symbol	Values	Unit
Reverse working voltage	$V_{RWM}$	$\pm 5.5$	V
ESD discharge <sup>2)</sup> contact air	$V_{ESD}$	$\pm 15$ $\pm 17$	kV
Peak pulse power <sup>3)</sup>	$P_{PK}$	36	W
Peak pulse current <sup>3)</sup>	$I_{PP}$	$\pm 3$	A
Operating temperature range	$T_{OP}$	-55 to 125	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$

- 1) Device is electrically symmetrical
- 2)  $V_{ESD}$  according to IEC61000-4-2 ( $R = 330\ \Omega$ ,  $C = 150\ \text{pF}$  discharge network)
- 3) Stress pulse: 8/20 $\mu\text{s}$  current waveform according to IEC61000-4-5

**Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.**

## 3 Electrical Characteristics



**Figure 3-1 Definitions of electrical characteristics**

## Electrical Characteristics

**Table 3-1 DC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified <sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Breakdown voltage	$V_{BR}$	6	-	10	V	$I_{BR} = 1\text{ mA}$
Reverse current	$I_R$	-	<1	100	nA	$V_R = 5.5\text{ V}$

1) Device is electrically symmetrical

**Table 3-2 AC Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	$C_L$	-	6.5	-	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		-	6.5	-		$V_R = 0\text{ V}, f = 1\text{ GHz}$

**Table 3-3 ESD and Surge Characteristics at  $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage <sup>2)</sup>	$V_{CL}$	-	13	-	V	$I_{TLP} = 16\text{ A}, t_p = 100\text{ ns}$
		-	17	-		$I_{TLP} = 30\text{ A}, t_p = 100\text{ ns}$
Clamping voltage <sup>3)</sup>		-	9.5	-		$I_{PP} = 1\text{ A}, t_p = 8/20\text{ }\mu\text{s}$
		-	12	-		$I_{PP} = 3\text{ A}, t_p = 8/20\text{ }\mu\text{s}$
Dynamic resistance <sup>2)</sup>	$R_{DYN}$	-	0.2	-	$\Omega$	$t_p = 100\text{ ns}$

1) Device is electrically symmetrical

 2) Please refer to Application Note AN210[1]. TLP parameter:  $Z_0 = 50\text{ }\Omega$ ,  $t_p = 100\text{ ns}$ ,  $t_r = 0.6\text{ ns}$ .

 3) Stress pulse: 8/20 $\mu\text{s}$  current waveform according to IEC61000-4-5

## 4 Typical Characteristics Diagrams

Typical characteristics diagrams at  $T_A = 25^\circ\text{C}$ , unless otherwise specified

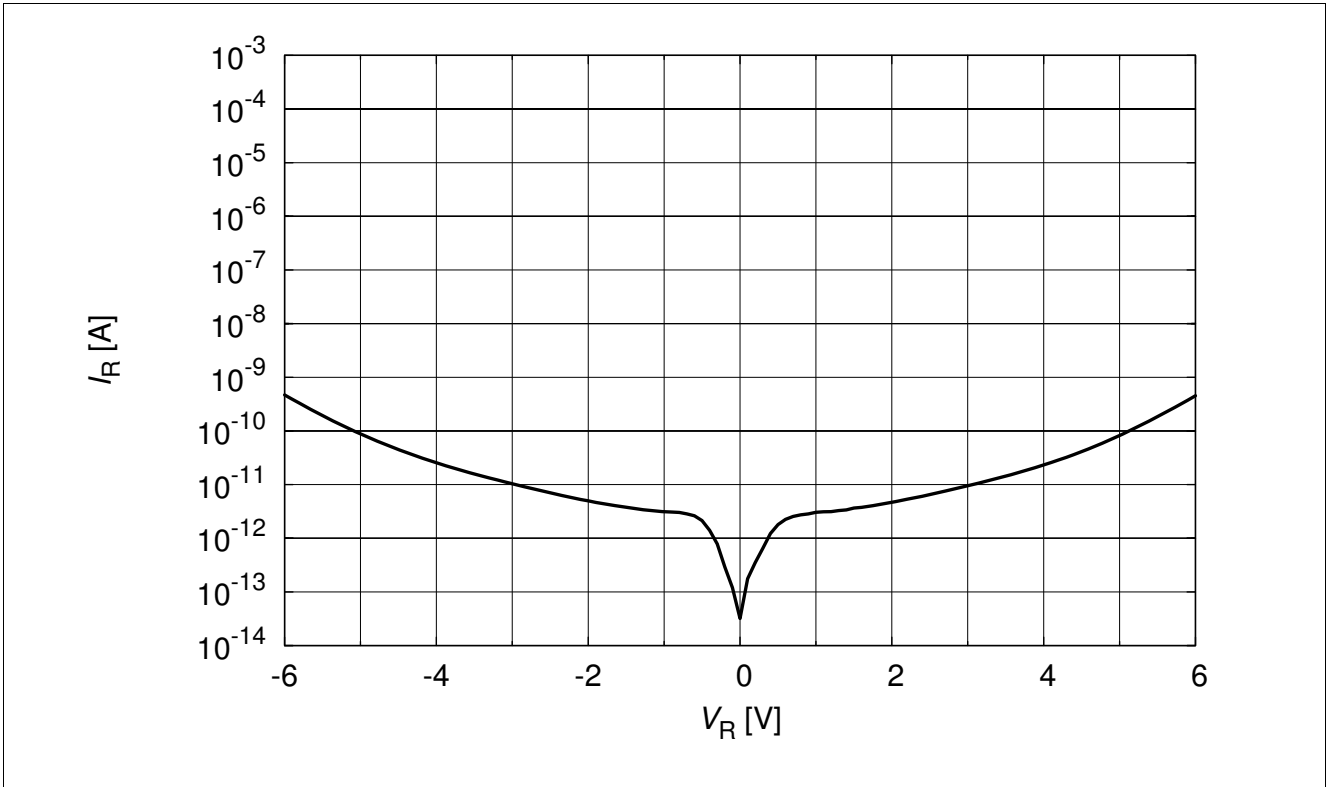


Figure 4-1 Reverse leakage current:  $I_R = f(V_R)$

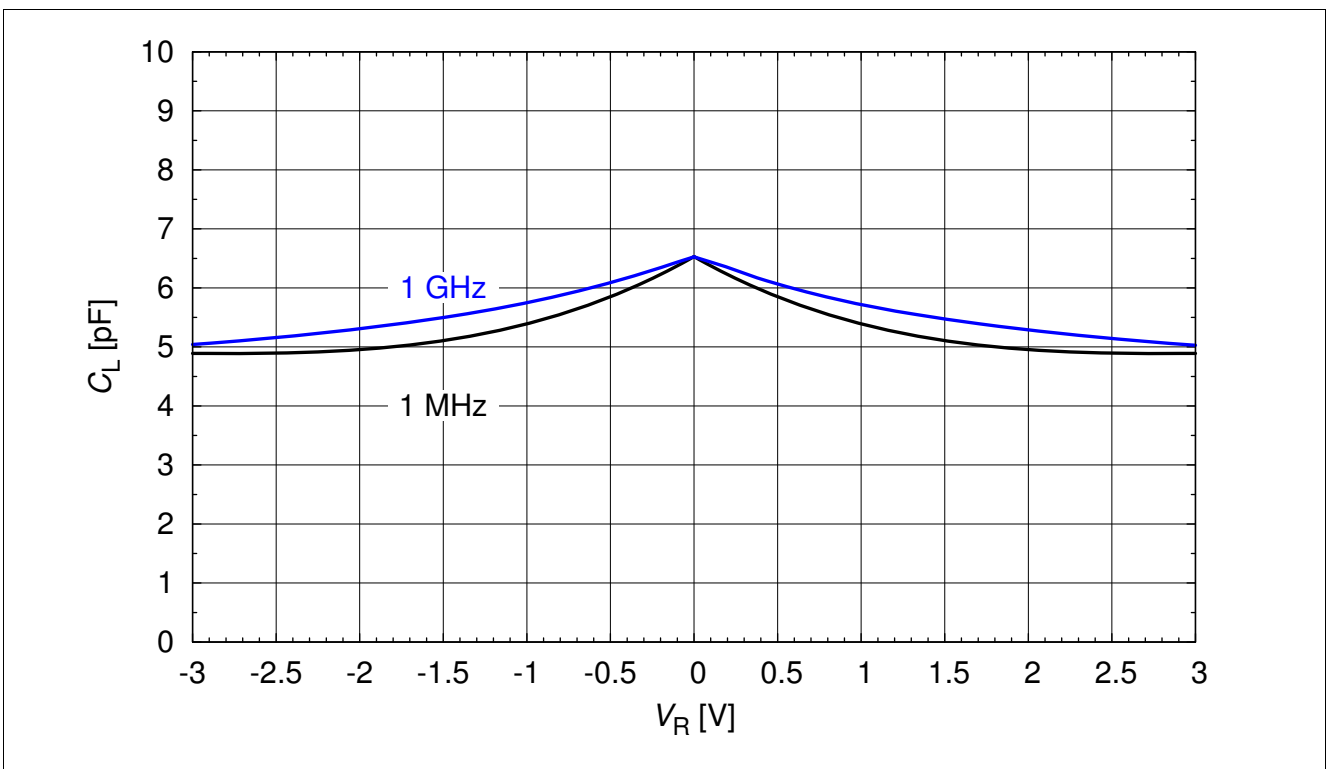


Figure 4-2 Line capacitance:  $C_L = f(V_R), f = 1 \text{ MHz}$

Typical Characteristics Diagrams

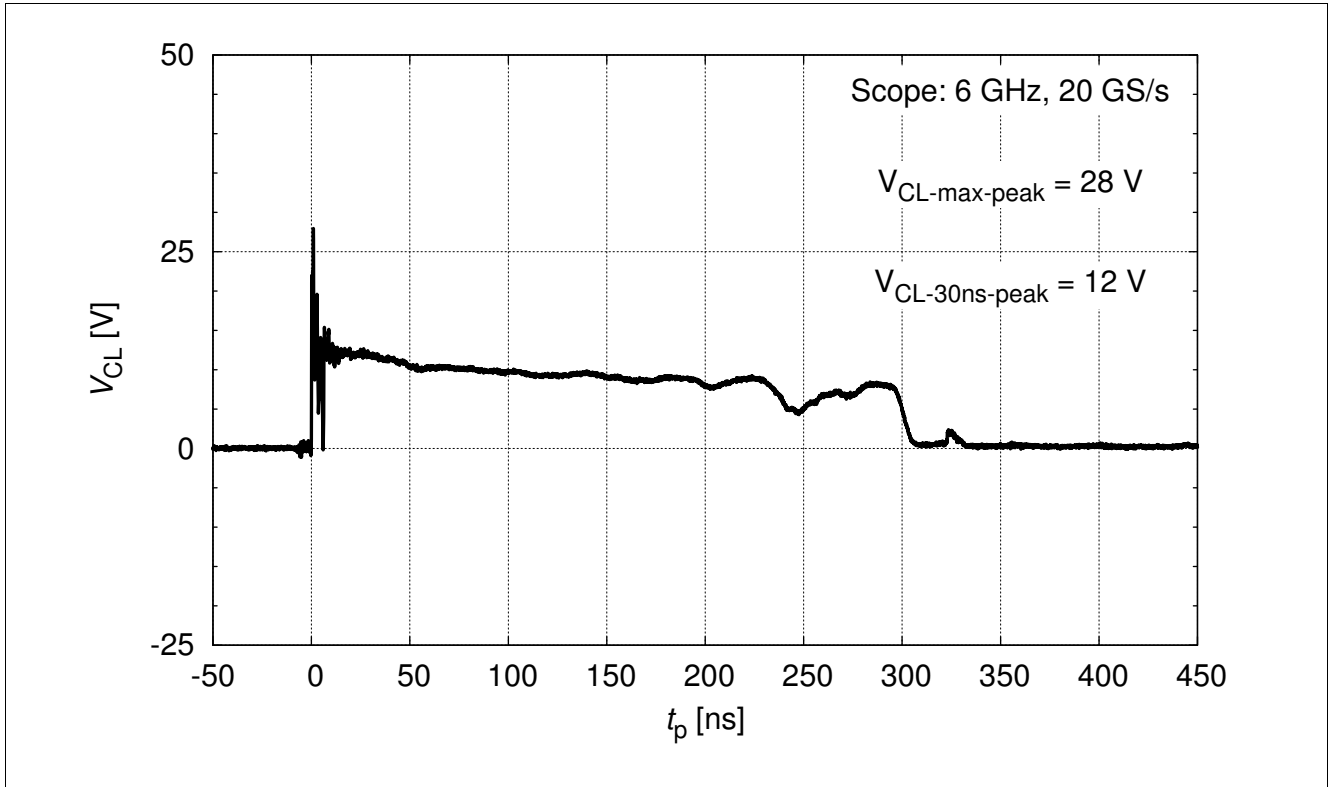


Figure 4-3 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV positive pulse

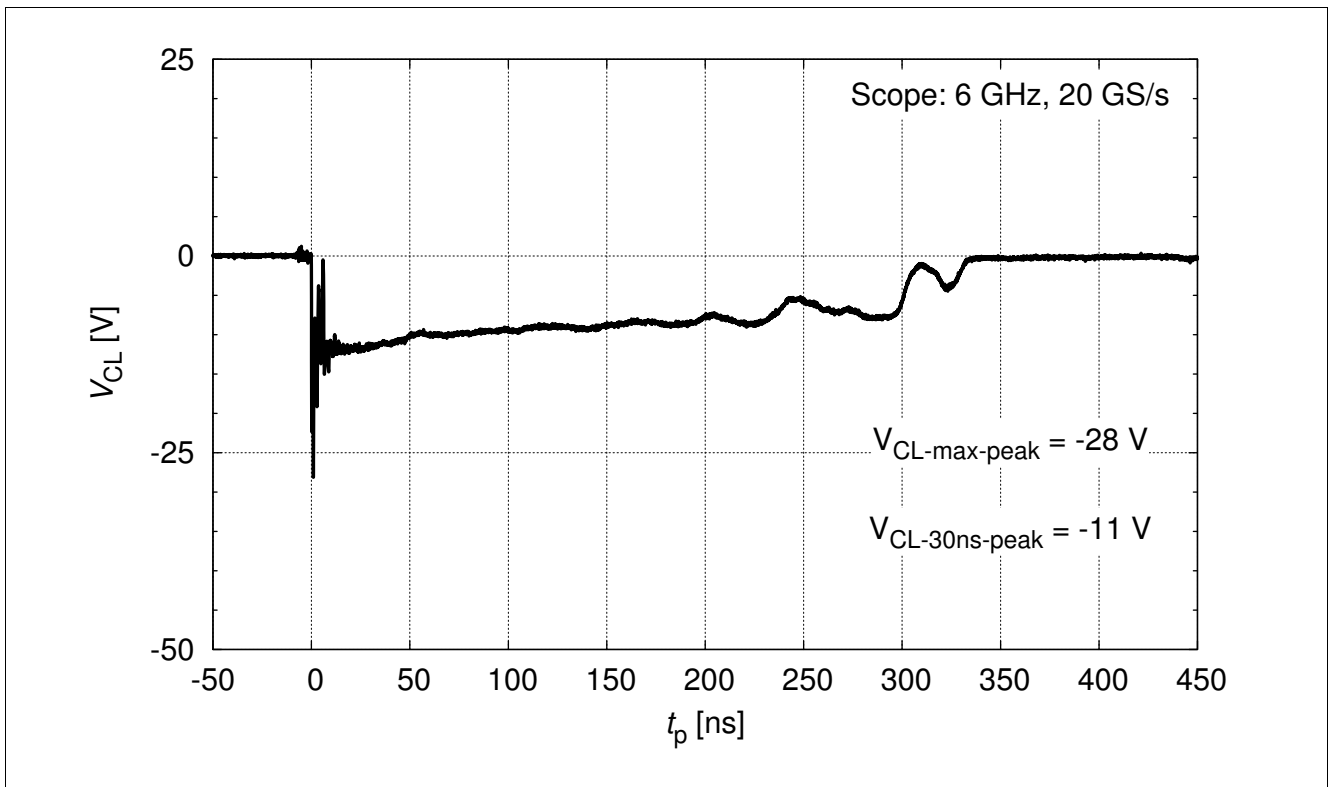


Figure 4-4 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 8 kV negative pulse



Typical Characteristics Diagrams

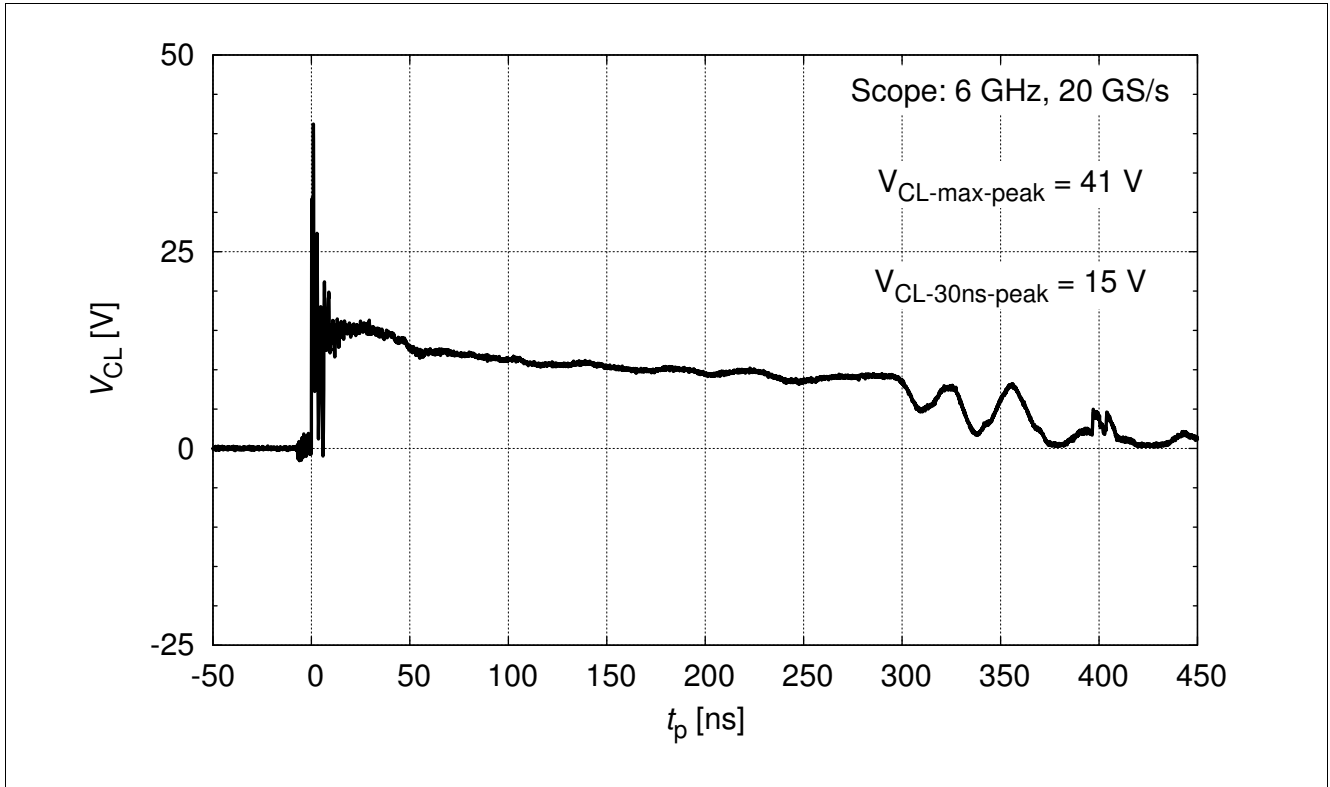


Figure 4-5 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV positive pulse

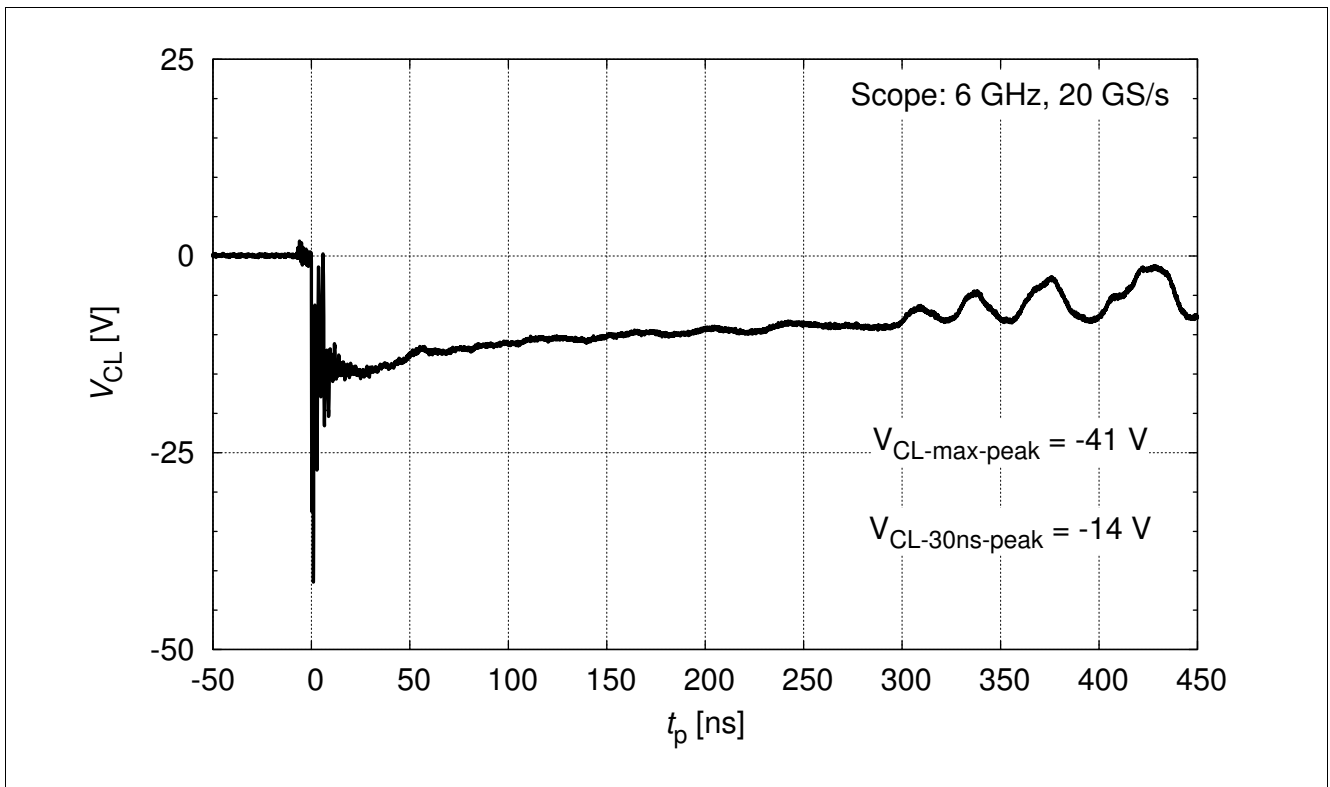


Figure 4-6 Clamping voltage (ESD):  $V_{CL} = f(t)$ , 15 kV negative pulse

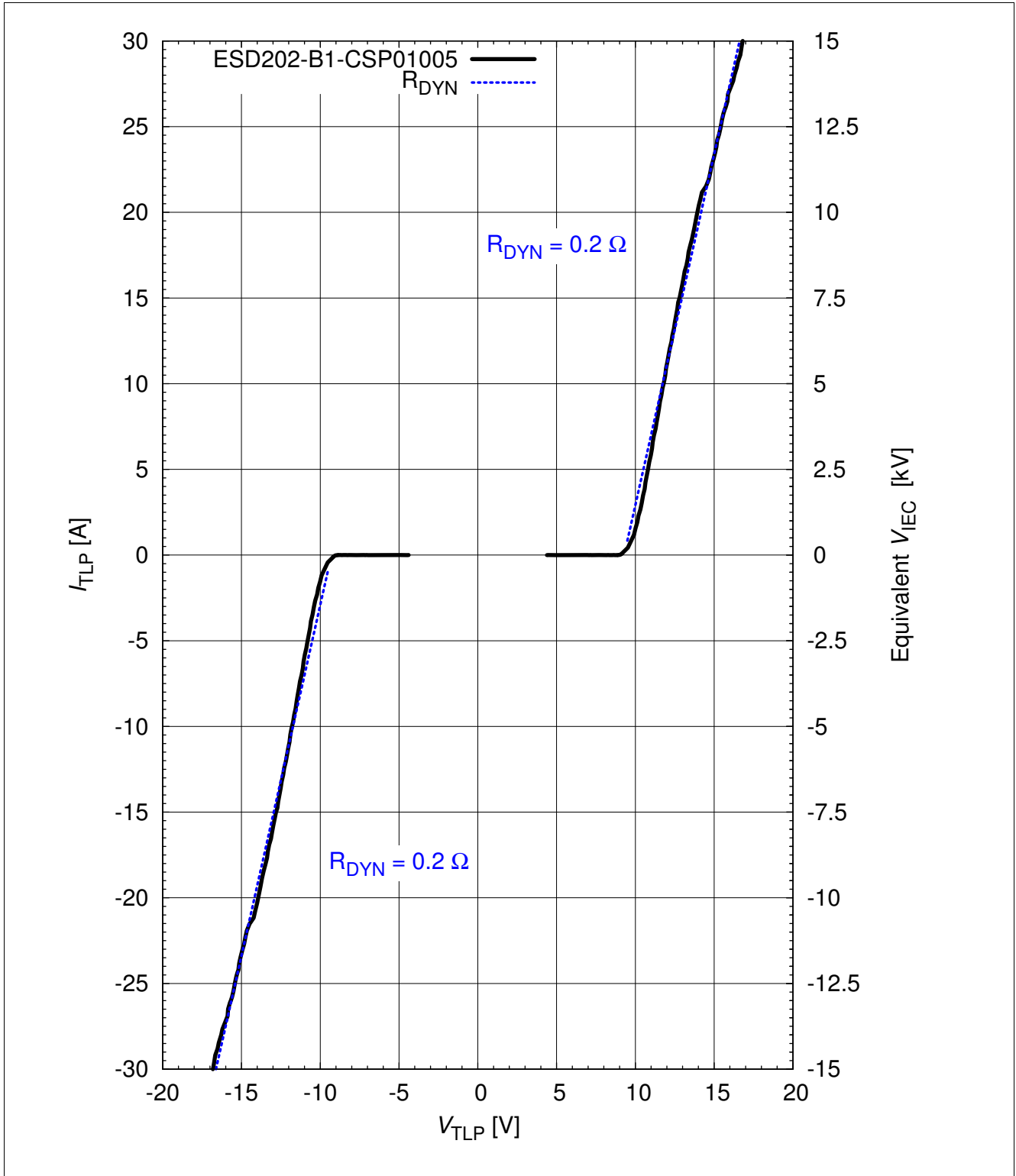


Figure 4-7 Clamping voltage (TLP):  $I_{TLP} = f(V_{TLP})$  [1]

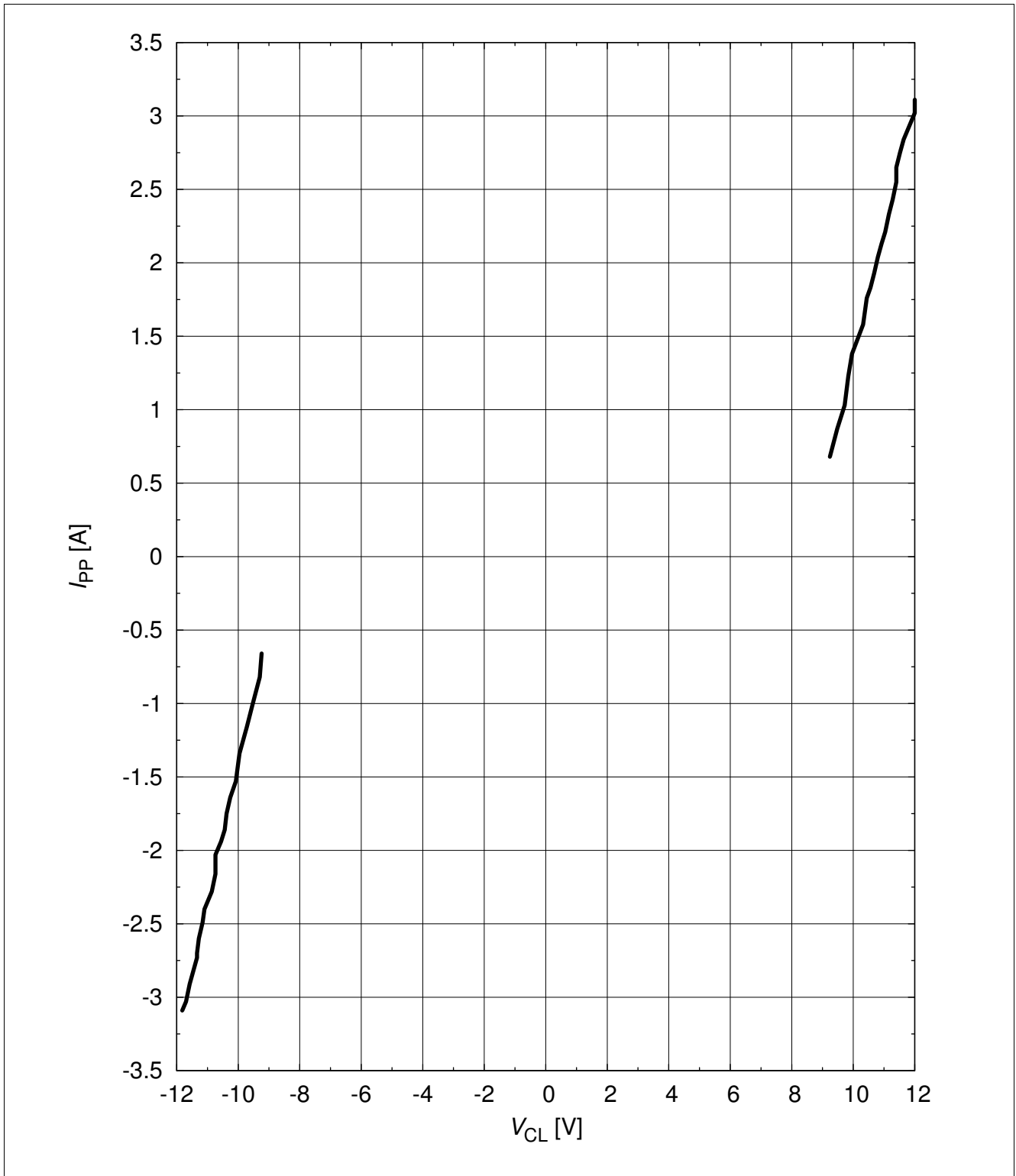


Figure 4-8 Clamping voltage (Surge):  $I_{PP} = f(V_{CL})$ [1]

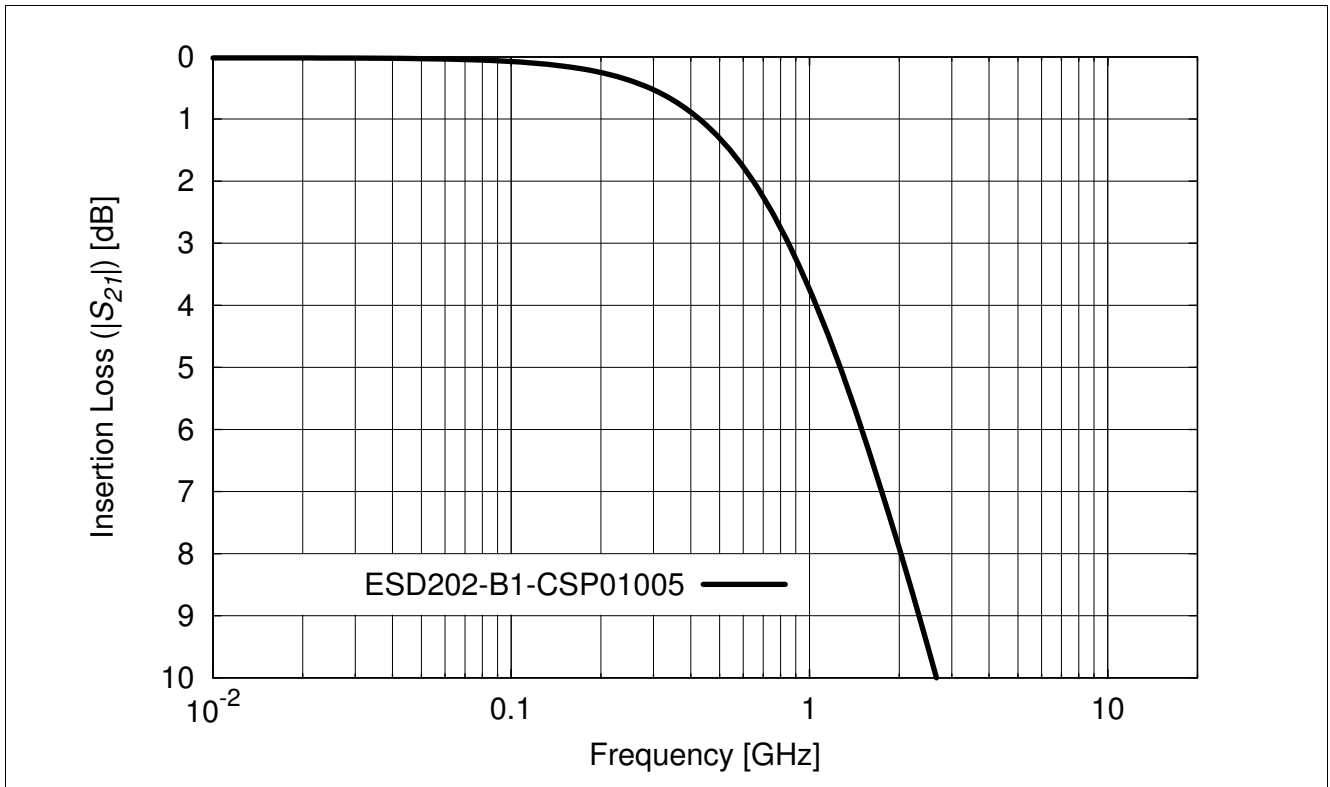


Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

## 5 Package Information

### 5.1 WLL-2-2

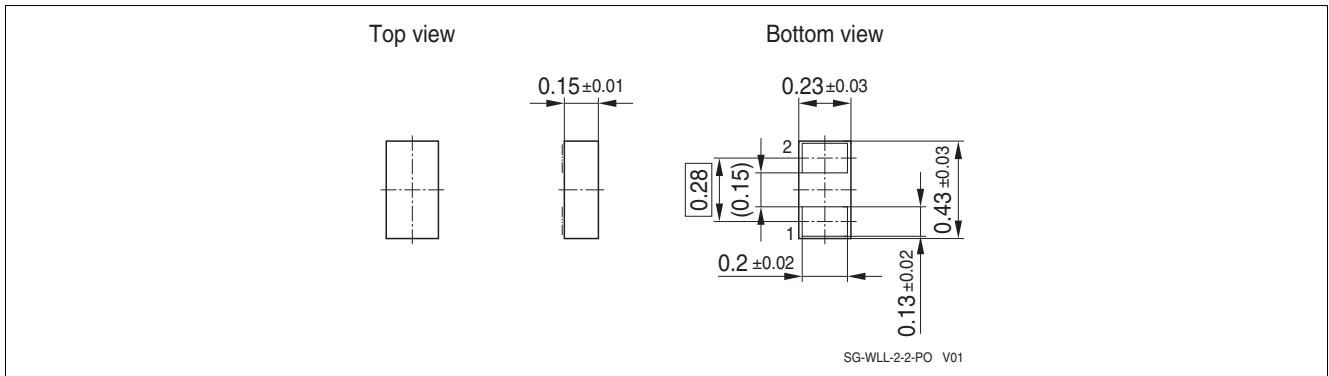


Figure 5-1 WLL-2-2: Package (dimension in mm)

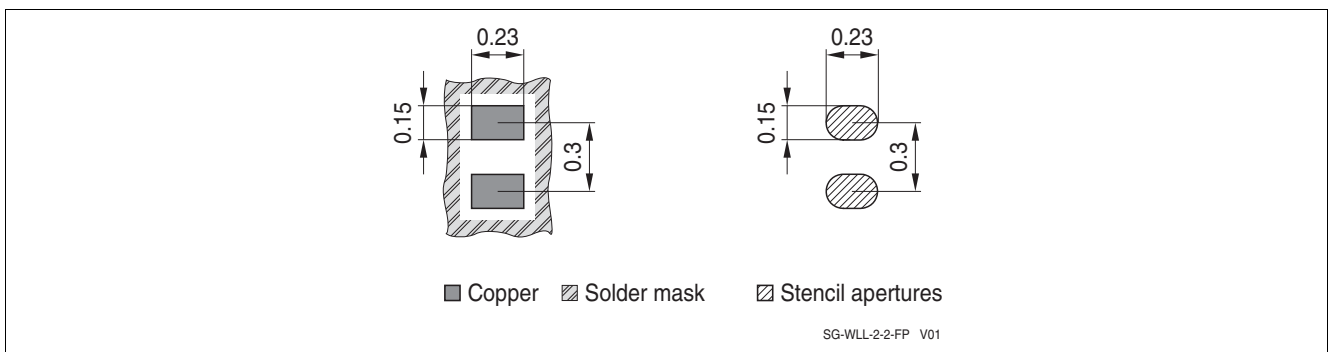


Figure 5-2 WLL-2-2 Footprint (dimension in mm) Recommendation for Printed Circuit Board Assembly<sup>[2]</sup>

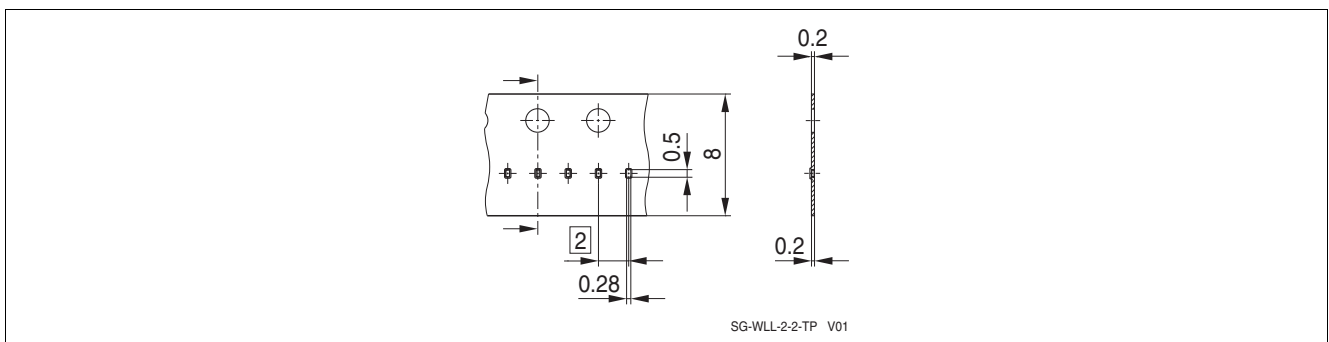


Figure 5-3 WLL-2-2: Packing (dimension in mm)

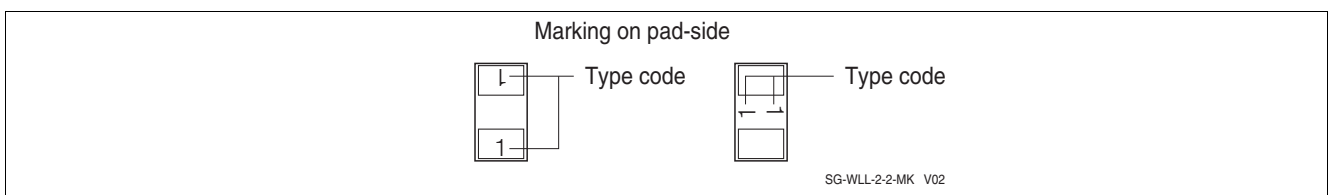


Figure 5-4 WLL-2-2: Marking example Table 1-1 "Part Information" on Page 3

## References

- [1] Infineon AG - **Application Note AN210**: Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology
- [2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages  
<http://www.infineon.com/dgdl/?fileId=db3a304344f7b4f9014503db540027c0>
- [3] Infineon AG - **Application Note AN392**: TVS Diodes in ChipScalePackage reduce size and save cost

**Revision History: Rev.1.3, 2016-02-05**

Page or Item	Subjects (major changes since previous revision)
<b>Revision 1.4, 2016-04-07</b>	
6	Update of Figure 4-2

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