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Protection Device

TVS (Transient Voltage Suppressor)

ESD231-B1-W0201

Bi-directional, 5.5 V, 3.5 pF, 0201, RoHS and Halogen Free compliant

ESD231-B1-W0201

Data Sheet

Revision 1.1, 2015-10-02
Final

Power Management & Multimarket

Edition 2015-10-02

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1 Product Overview

1.1 Features

- ESD / transient protection of susceptible I/O lines to:
  - **IEC61000-4-2 (ESD): ±30 kV (air/contact discharge)**
  - **IEC61000-4-4 (EFT): ±4 kV / ±80 A(5/50 ns)**
  - **IEC61000-4-5 (surge): ±12 A (8/20 µs)**
- Bi-directional working voltage up to: V_{RWM} **= ±5.5 V**
- Line capacitance: C_L **= 3.5 pF (typical) at** f **= 1 MHz**
- Clamping voltage: V_{CL} **= 12 V (typical) at** I_{TLP} **= 16 A** with R_{DYN} **= 0.3 Ω (typical)**
- Very low reverse current. I_R **< 1 nA (typical)**
- Minimized clamping overshoot due to extremely low parasitic inductance
- Small form factor SMD Size 0201 and low profile (0.58 mm x 0.28 mm x 0.15 mm)
- Bidirectional and symmetric I/V characteristics for optimized design and assembly
- Pb-free (RoHS compliant) and halogen free package

Guidelines for optimized PCB design and assembly process available [2]

RoHS

1.2 Application Examples

- USB 2.0 HA, MIPI, (µ)SD-card (UHS), SIM-card
- Control ports for DVI, HDMI, Display Port, and Thunderbolt
- Audio Line, Speaker, Headset, Microphone Protection
- Human Interface Devices (Keyboard, Touchpad, Buttons)

1.3 Product Description

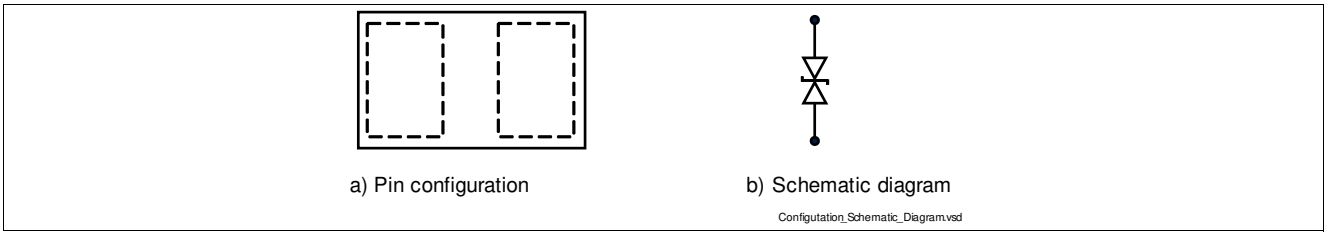

Figure 1-1 Pin Configuration and Schematic Diagram

Table 1-1 Part Information

Type	Package	Configuration	Marking code
ESD231-B1-W0201	WLL-2-1	1 line, bi-directional	M[1)]

1) The device does not have any marking or date code on the device backside. The Marking code is on pad side.

2 Maximum Ratings

Table 2-1 Maximum Rating *at T_A = 25 °C, unless otherwise specified*[1)]

Parameter	Symbol	Values	Unit
Reverse working voltage	V_{RWM}	±5.5	V
ESD air discharge[2)] ESD contact discharge[2)]	V_{ESD}	±30 ±30	kV
Peak pulse power[3)]	P_{PK}	132	W
Peak pulse current[3)]	I_{PP}	12	A
Operating temperature	T_{OP}	-55 to 125	°C
Storage temperature	T_{stg}	-65 to 150	°C

1) Device is electrically symmetrical
2) V_{ESD} according to IEC61000-4-2
3) Stress pulse: 8/20µs current waveform according to IEC61000-4-5

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component.

Table 2-2 Thermal Resistance

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
Junction - soldering point[1)]	R_{thJS}	-	30		K/W

1) For calculation of R_{thJA} please refer to Application Note [3] 077 Thermal Resistance Calculation.

3 Electrical Characteristics at T_A = 25 °C, unless otherwise specified

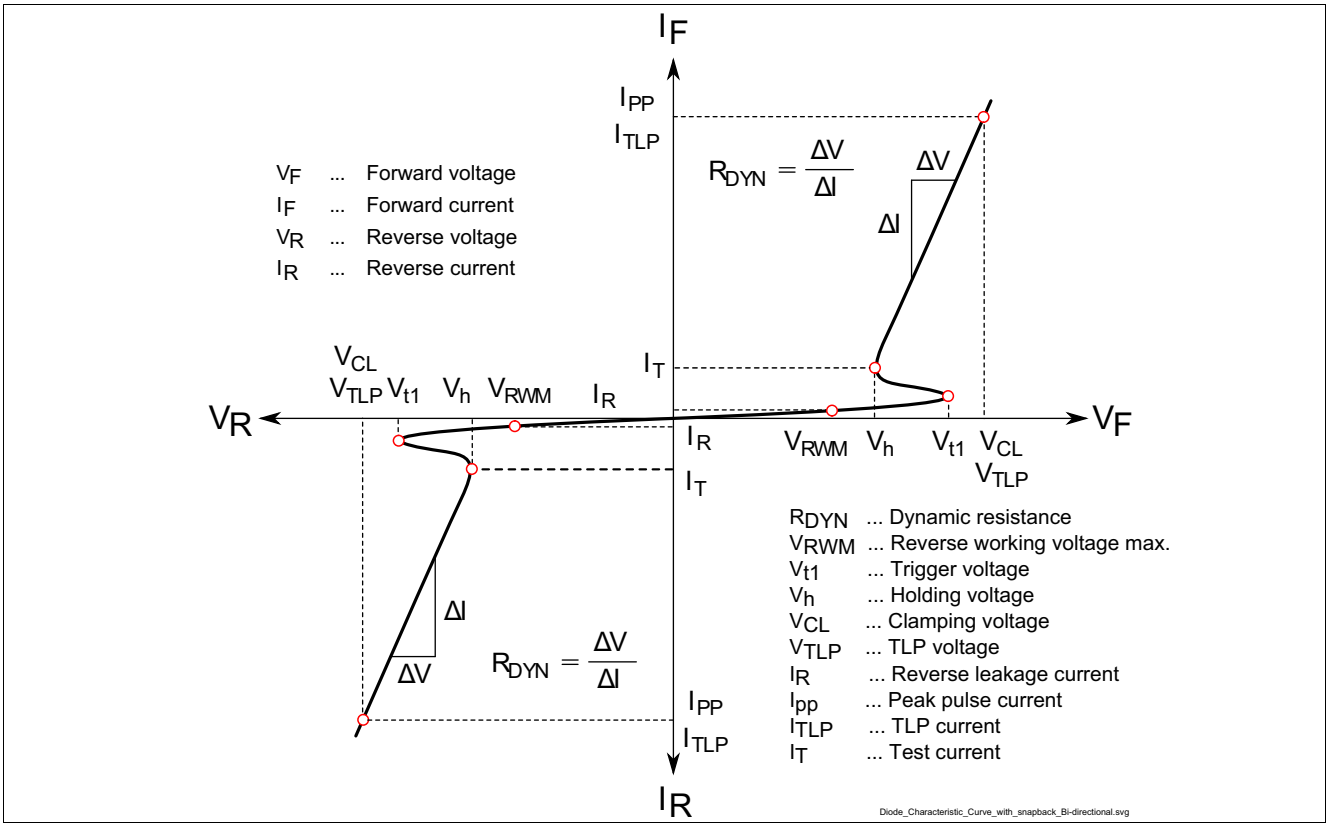

Figure 3-1 Definitions of electrical characteristics

Table 3-1 DC Characteristics at T_A = 25 °C, unless otherwise specified[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trigger voltage	V_{t1}	6.1	9.5	–	V	
Holding voltage	V_h	6.1	7.8	12.5	V	I_R = 10 mA
Reverse current	I_R	–	–	20	nA	V_R = 5.5 V

1) Device is electrically symmetrical

Table 3-2 RF Characteristics at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	3	3.5	4.1	pF	V_R = 0 V, f = 1 MHz
		–	3.2	–		V_R = 0 V, f = 1 GHz

Table 3-3 ESD and Surge Characteristics at T_A = 25 °C, unless otherwise specified [1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clamping voltage[2)]	V_{CL}	–	12	–	V	I_{TLP} = 16 A, t_p = 100 ns
		–	16	–		I_{TLP} = 30 A, t_p = 100 ns
Clamping voltage[3)]		–	8	–		I_{PP} = 2 A, t_p = 8/20 µs
		–	10	–		I_{PP} = 9 A, t_p = 8/20 µs
Dynamic resistance[2)]	R_{DYN}	–	0.3	–	Ω	t_p = 100 ns

1) Device is electrically symmetrical

2) Please refer to Application Note AN210[1].TLP parameter: Z_0 = 50 Ω , t_p = 100ns, t_r = 0.6 ns.

3) Stress pulse: 8/20µs current waveform according to IEC61000-4-5

4 Typical Characteristics Diagrams

Typical characteristics diagrams at T_A = 25°C, unless otherwise specified

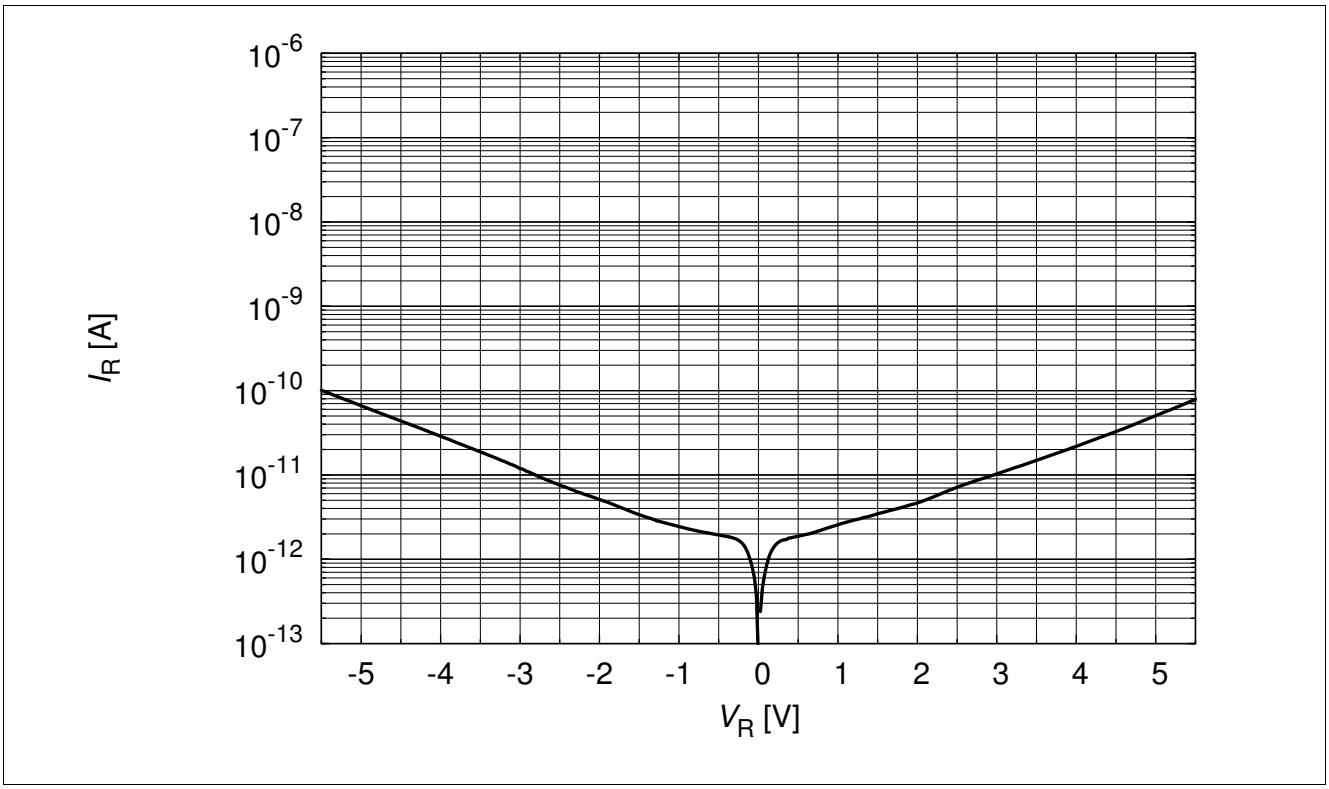

Figure 4-1 Reverse leakage current: $I_R = f(V_R)$

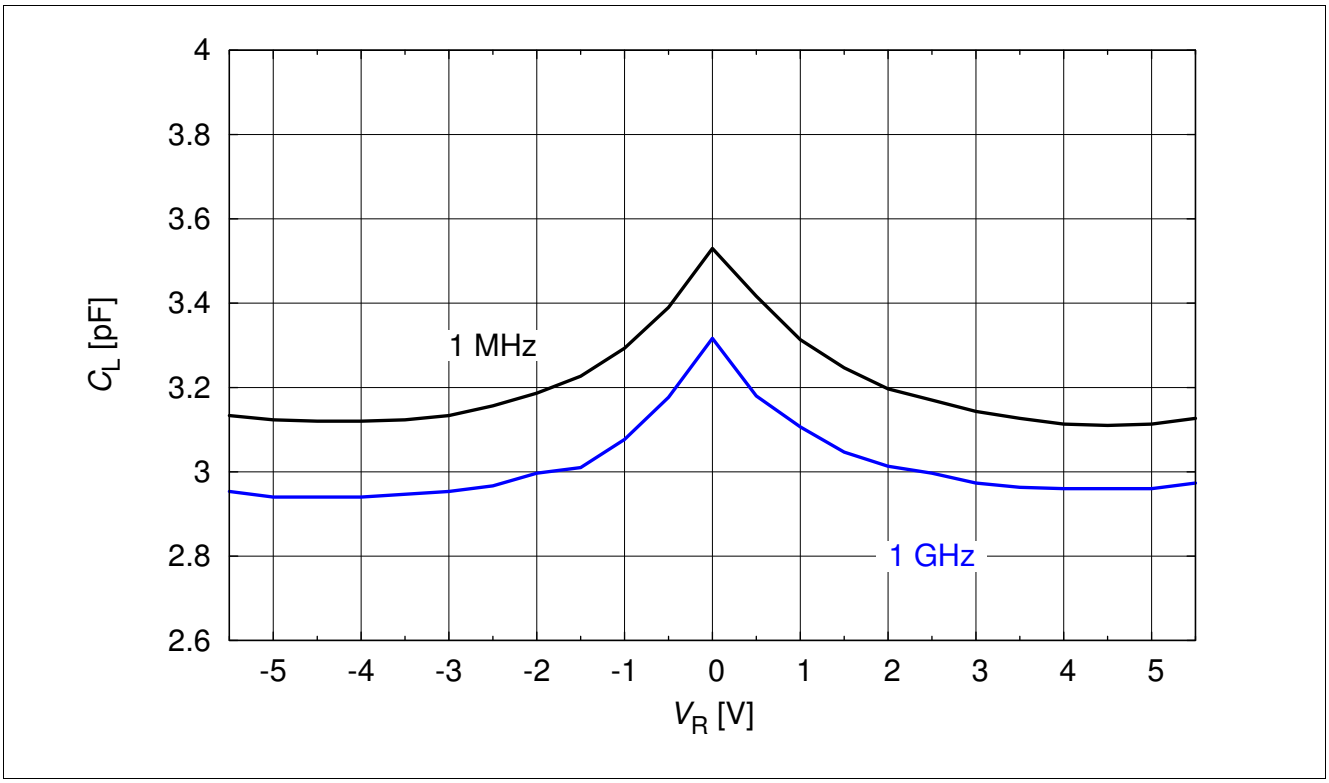

Figure 4-2 Line capacitance: $C_L = f(V_R)$

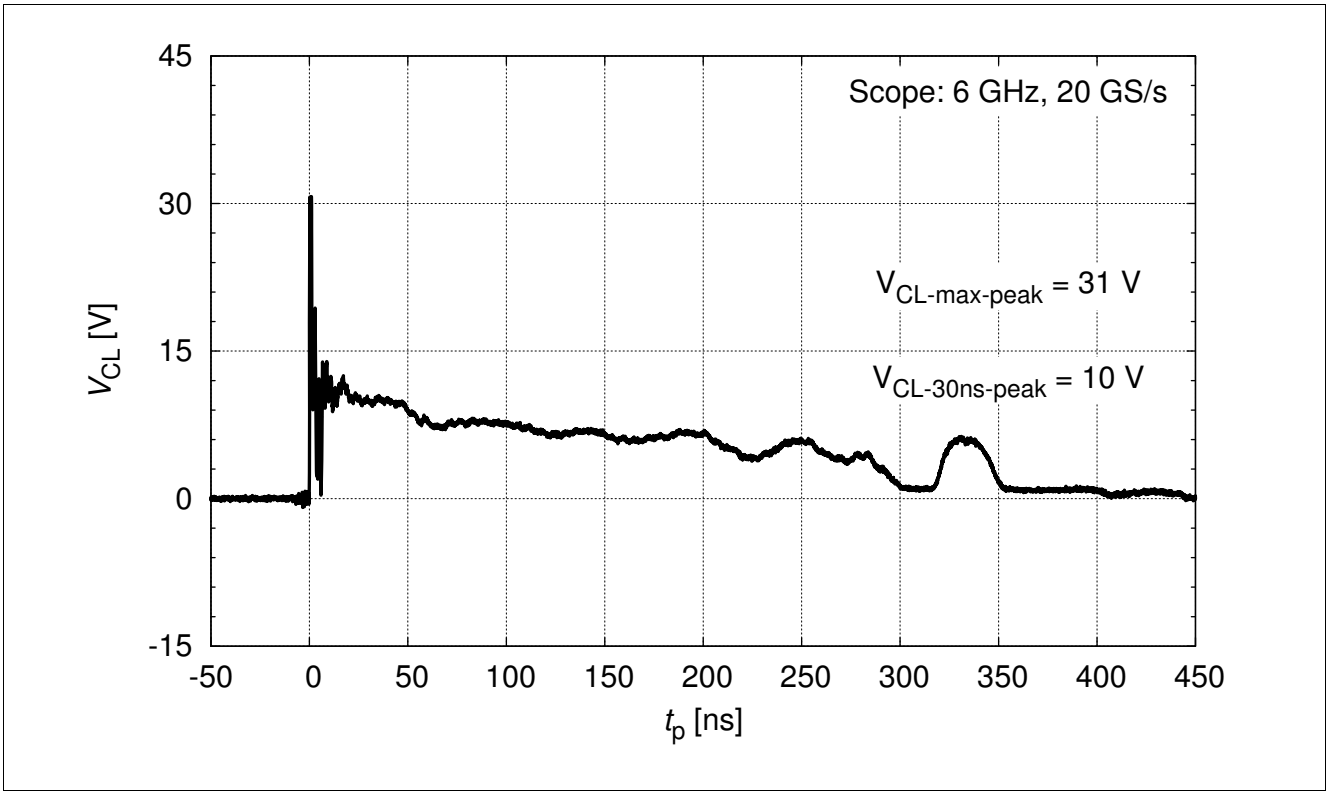

Figure 4-3 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV positive pulse

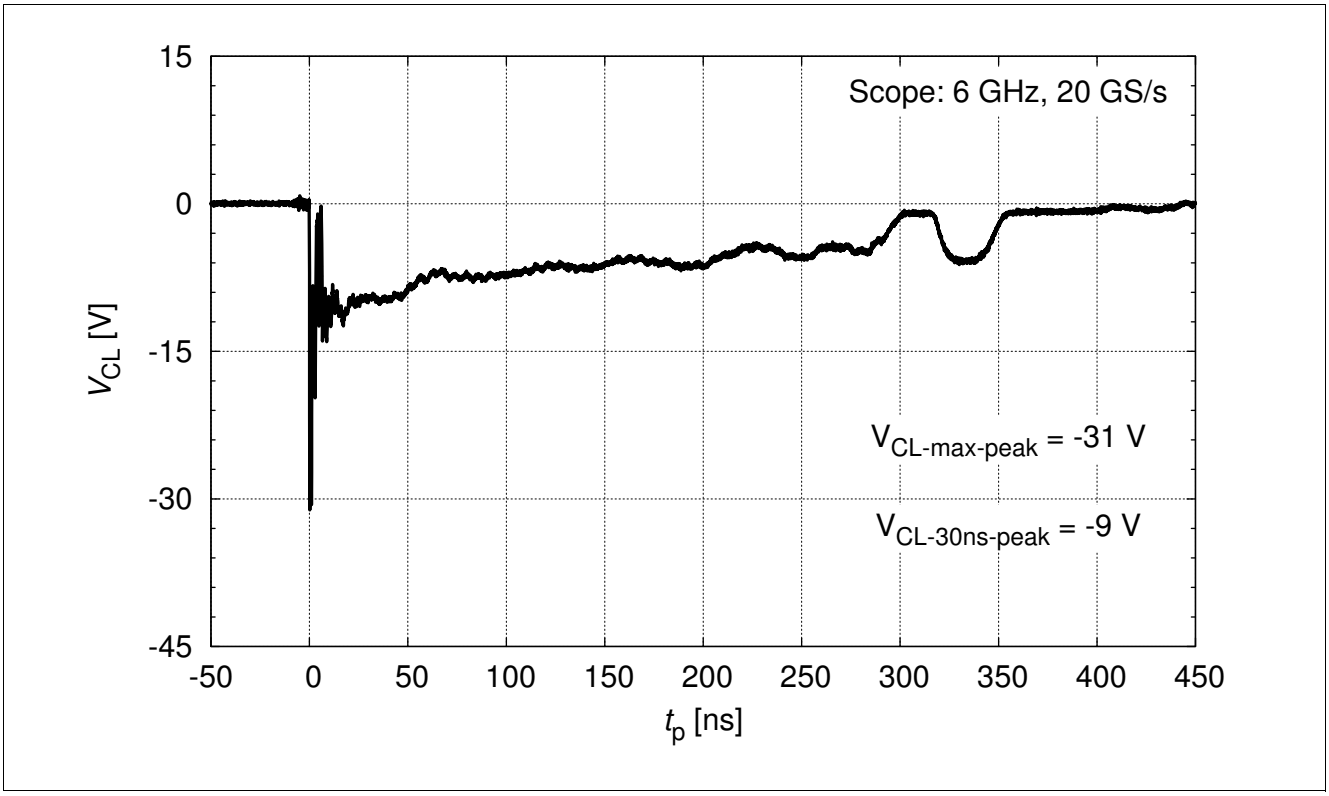

Figure 4-4 Clamping voltage (ESD): $V_{CL} = f(t)$, 8 kV negative pulse

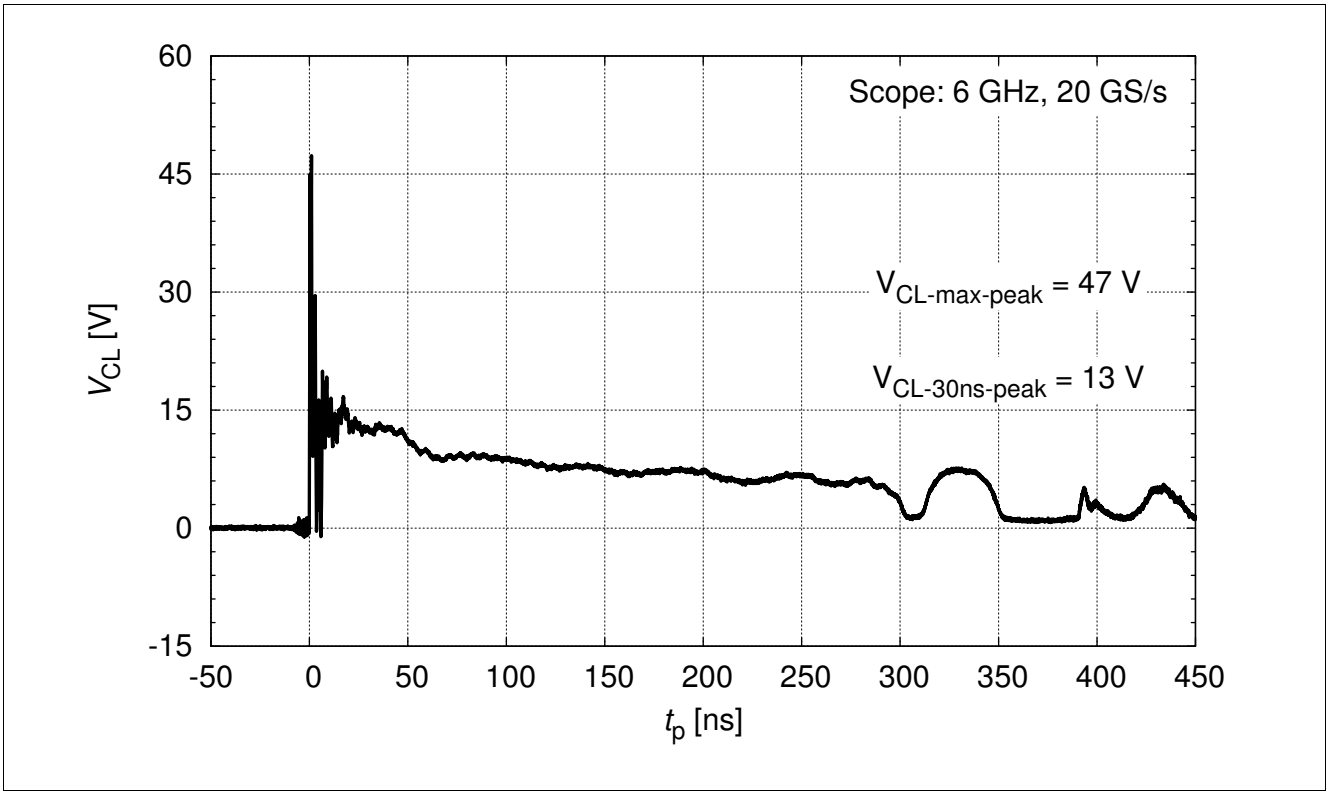

Figure 4-5 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV positive pulse

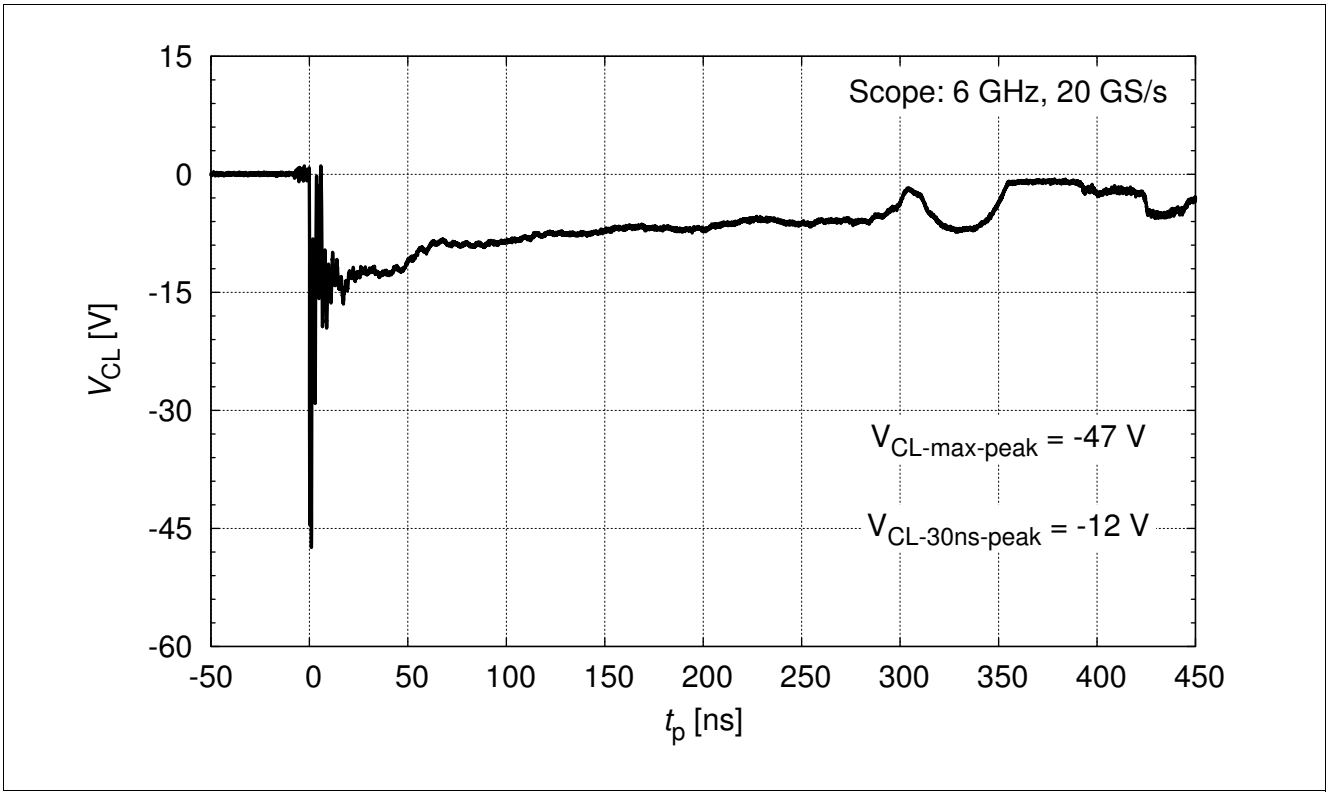

Figure 4-6 Clamping voltage (ESD): $V_{CL} = f(t)$, 15 kV negative pulse

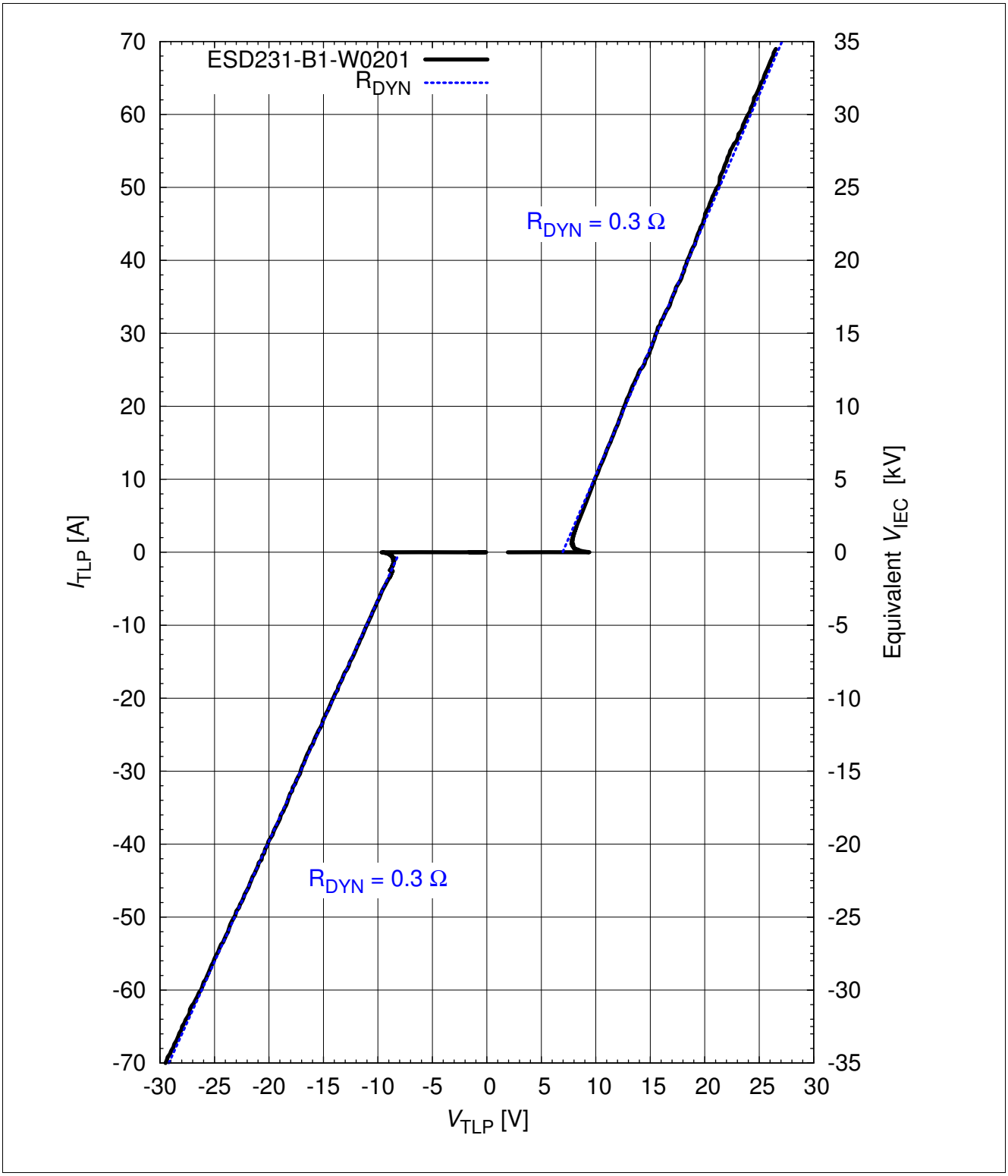

Figure 4-7 Clamping voltage (TLP): $I_{TLP} = f(V_{TLP})$ [1]

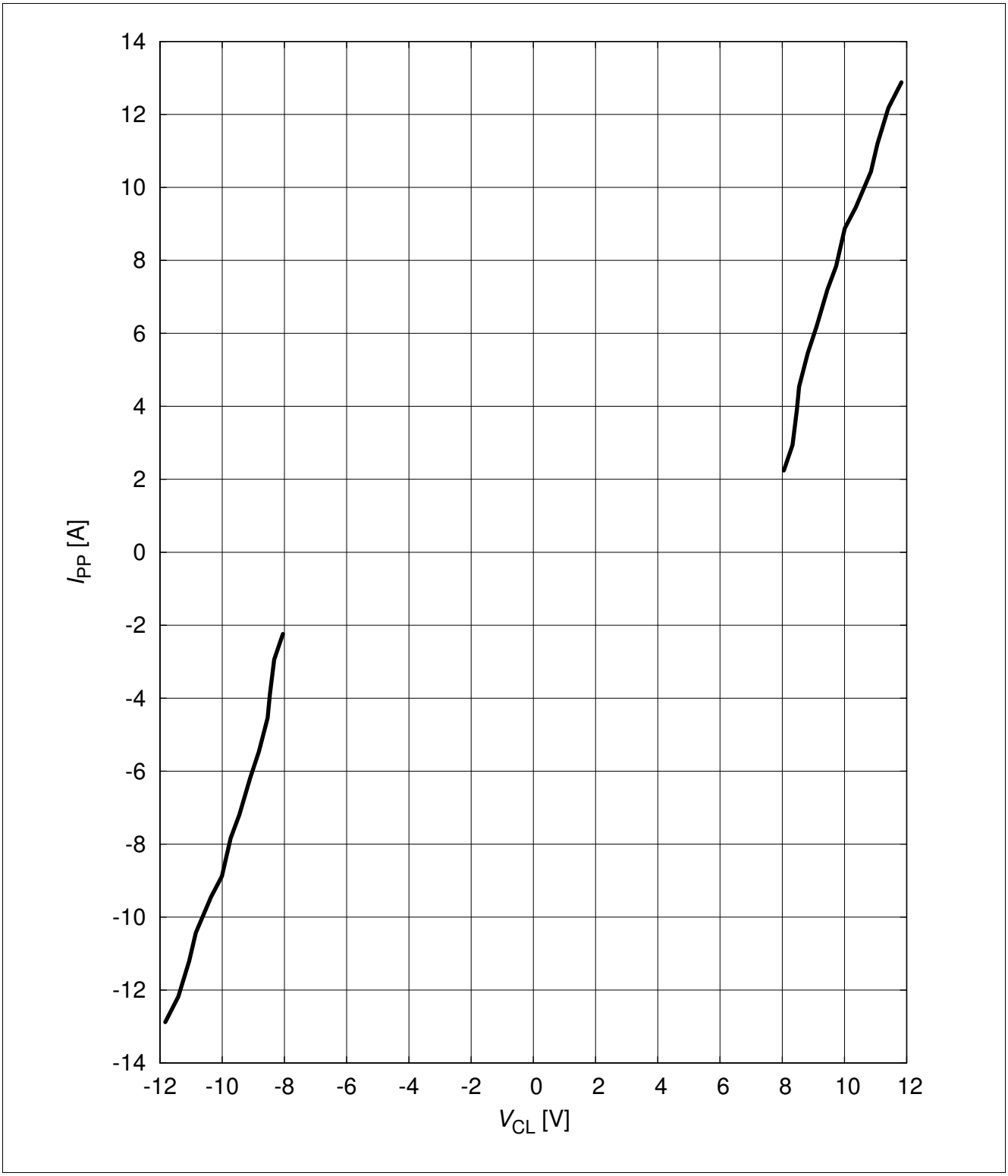

Figure 4-8 Clamping voltage (Surge): $I_{PP} = f(V_{CL})$[1]

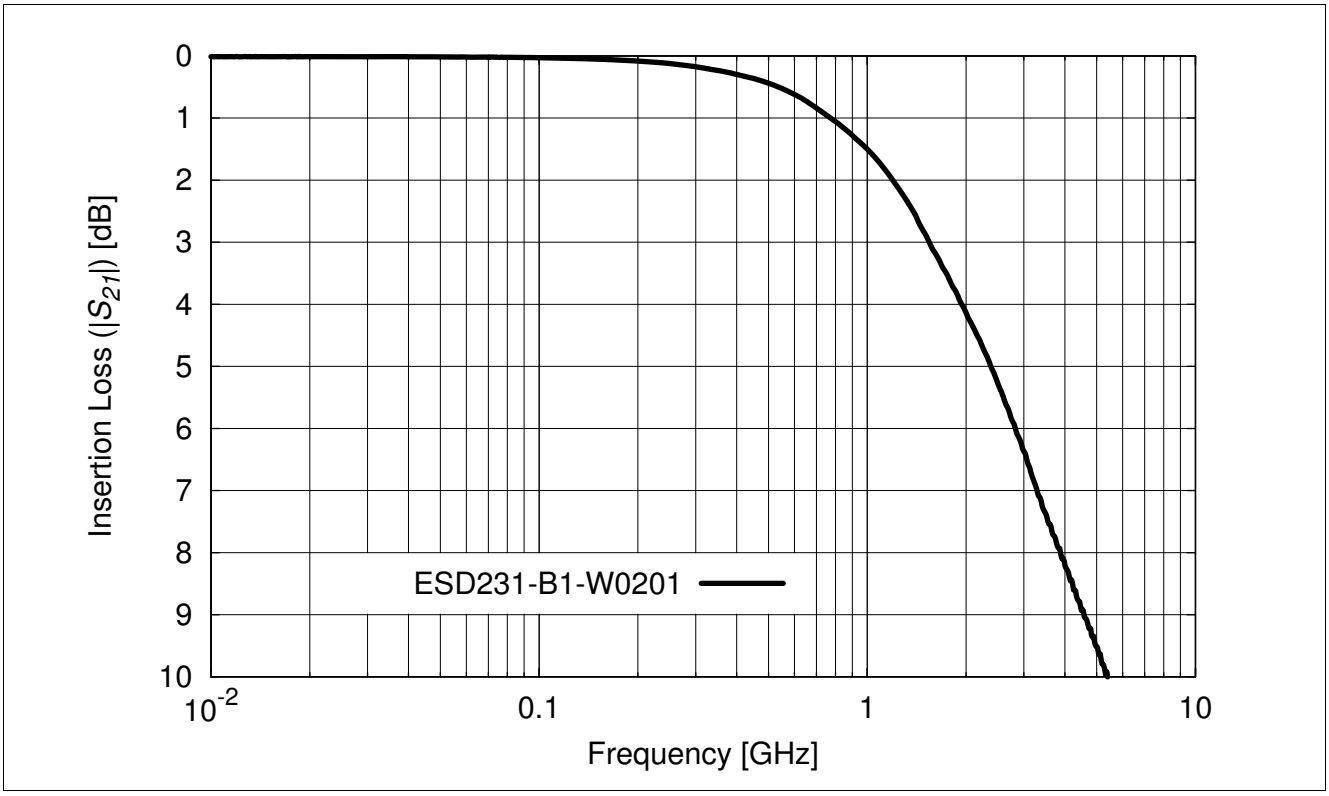

Figure 4-9 Insertion loss vs. frequency in a 50 Ω system

5 Package Information

5.1 WLL-2-1

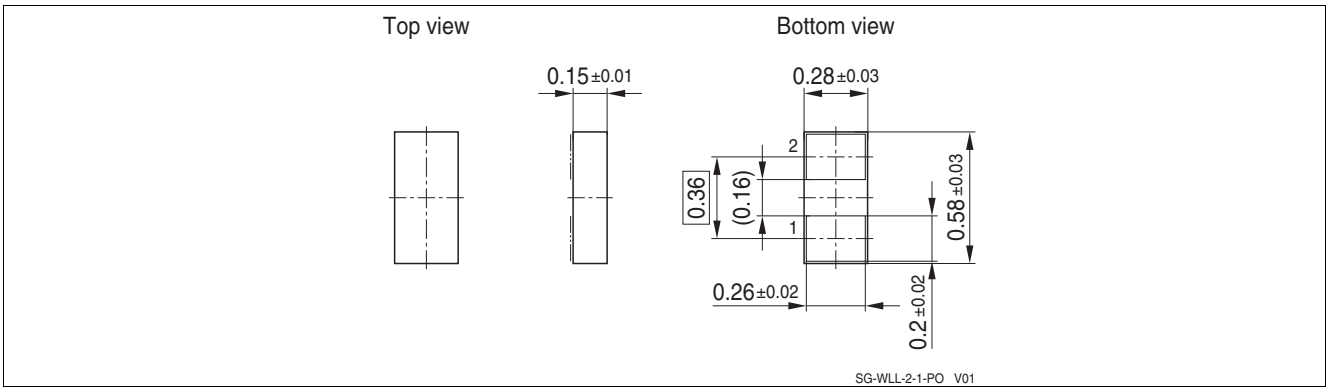

Figure 5-1 WLL-2-1 Package outline (dimension in mm)

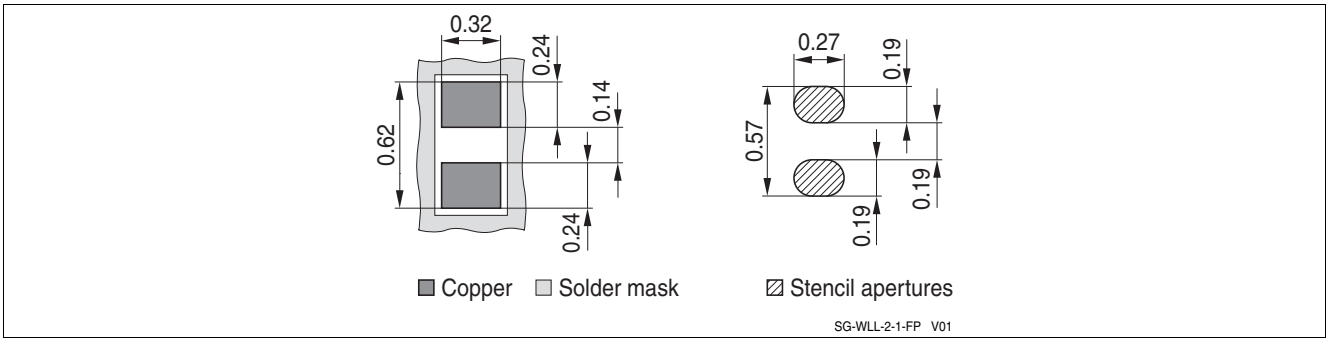

Figure 5-2 WLL-2-1 Footprint (dimension in mm) Recommendation for Printed Circuit Board Assembly[2]

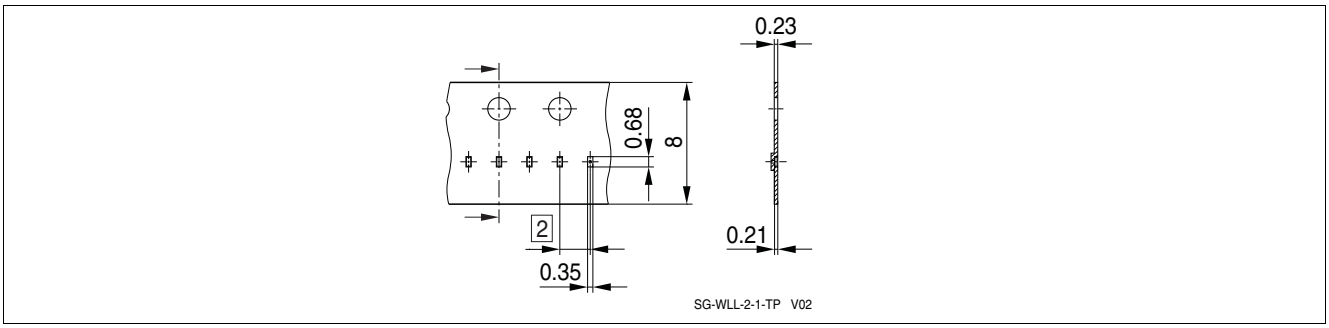

Figure 5-3 WLL-2-1 Packing (dimension in mm)

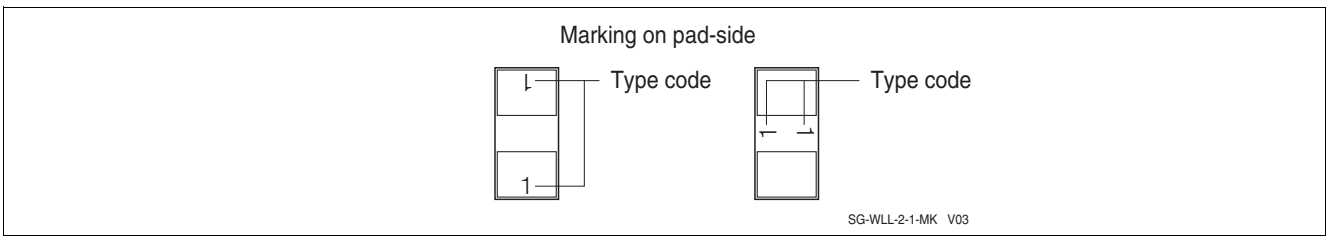

Figure 5-4 WLL-2-1 Marking example Table 1-1 “Part Information” on Page 3

References

[1] Infineon AG - **Application Note AN210:** Effective ESD Protection design at System Level Using VF-TLP Characterization Methodology

[2] Infineon AG - Recommendation for Printed Circuit Board Assembly of Infineon WLL Packages
http://www.infineon.com/dgdl/?fileId=db3a304344f7b4f9014503db540027c0

[3] Infineon AG - **Application Note AN077:** Thermal Resistance Calculation

Revision History: Rev. 1.0 2015-07-31	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2015-10-02	
All	Sales code change from ESD231-B1-CSP0201 to ESD231-B1-W0201

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