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TVS Diode

Transient Voltage Suppressor Diodes

ESD3V3XU1U Series

Uni-directional Ultra Low Capacitance ESD / Transient Protection Diode

ESD3V3XU1UL
ESD3V3XU1US

Data Sheet

Revision 1.1, 2011-10-19
Final

Industrial and Multi-Market

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Revision 1.1, 2011-10-19 Table3-2; Table3-4; Figure3-4 updated	
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Table of Contents

	Table of Contents	4
	List of Figures	5
	List of Tables	6
1	Uni-directional Ultra Low Capacitance ESD / Transient Protection Diode	7
1.1	Features	7
1.2	Application Examples	7
2	Product Description	7
3	Characteristics	8
3.1	Electrical Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified	8
3.2	Typical Characteristics at $T_A=25\text{°C}$, unless otherwise specified	10
4	Application Information	17
5	Package Information	18
5.1	PG-TSLP-2-17 (mm) [3]	18
5.2	PG-TSSLP-2-1 (mm) [3]	19
	References	20
	Terminology	21

List of Figures

Figure 2-1	Pin Configuration and Schematic Diagram	7
Figure 3-1	Definitions of electrical characteristics	8
Figure 3-2	Forward current, $I_F = (V_F)$	10
Figure 3-3	Reverse current, $I_R = (V_R)$	10
Figure 3-4	Reverse voltage characteristic, $I_R = (V_R)$	11
Figure 3-5	Reverse current $I_R = f(T_A)$, $V_R = 3.3\text{ V}$	11
Figure 3-6	Line capacitance $C_L = f(V_R)$, $f = 1\text{MHz}$, from pin 1 to pin 2	12
Figure 3-7	IEC61000-4-2 $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2	13
Figure 3-8	IEC61000-4-2 $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2	13
Figure 3-9	IEC61000-4-2 $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2	14
Figure 3-10	IEC61000-4-2 $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2	14
Figure 3-11	Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1 ^{Note: [2]}	15
Figure 3-12	Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2 ^{Note: [2]}	15
Figure 3-13	Forward clamping voltage $I_{PP} = f(V_{FC})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 μs)	16
Figure 3-14	Reverse clamping voltage $I_{PP} = f(V_{CL})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 μs)	16
Figure 4-1	Single line, uni-directional ESD / Transient protection	17
Figure 5-1	PG-TSLP-2-17: Package overview	18
Figure 5-2	PG-TSLP-2-17: Footprint	18
Figure 5-3	PG-TSLP-2-17: Packing	18
Figure 5-4	PG-TSLP-2-17: Marking (example)	18
Figure 5-5	PG-TSSLP-2-1: Package overview	19
Figure 5-6	PG-TSSLP-2-1: Footprint	19
Figure 5-7	PG-TSSLP-2-1: Packing	19
Figure 5-8	PG-TSSLP-2-1: Marking (example)	19

List of Tables

Table 2-1	Ordering Information	7
Table 3-1	Maximum Rating at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified	8
Table 3-2	DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified	8
Table 3-3	RF Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified	9
Table 3-4	ESD Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified	9

1 Uni-directional Ultra Low Capacitance ESD / Transient Protection Diode

1.1 Features

- ESD / transient protection of high speed data lines exceeding:
 - IEC61000-4-2 (ESD): ± 20 kV (air / contact)
 - IEC61000-4-4 (EFT): 2.5 kV / 50 A (5/50 ns)
 - IEC61000-4-5 (surge): 3 A (8/20 μ s)
- Maximum working voltage: $V_{RWM} = 3.3$ V
- Ultra low capacitance $C_L = 0.4$ pF (typical)
- Very low clamping voltage: $V_{CL} = 8$ V at $I_{PP} = 16$ A (typical) [2]
- Very low dynamic resistance: $R_{DYN} = 0.19$ Ω (typical) [2]
- Pb-free and halogen-free package (RoHS compliant)



1.2 Application Examples

- USB 3.0, 10/100/1000 Ethernet, Firewire, DVI, HDMI, S-ATA, DisplayPort
- Mobile HDMI Link, MDDI, MIPI, SWP / NFC

2 Product Description

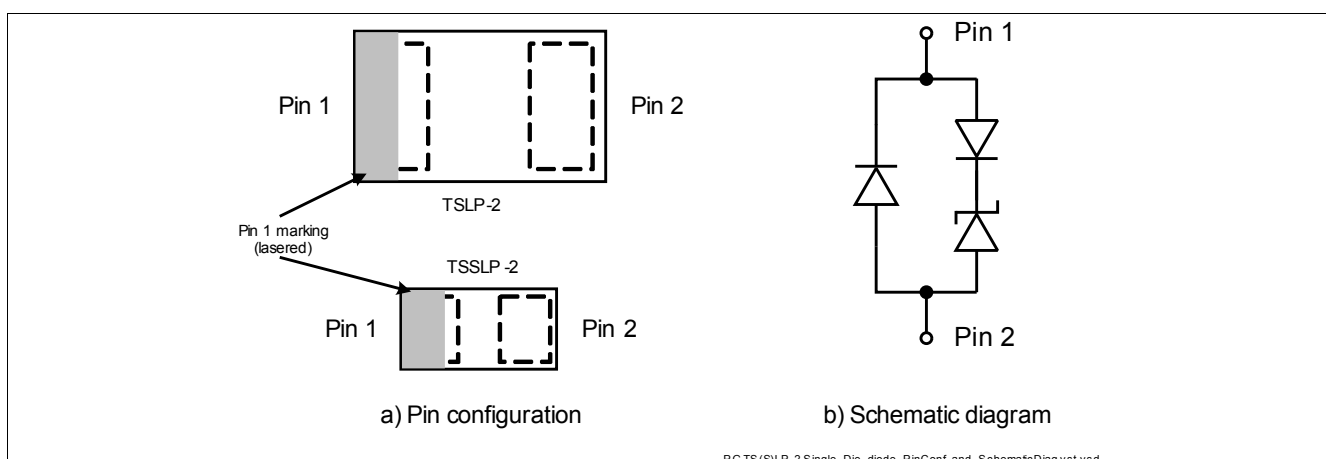


Figure 2-1 Pin Configuration and Schematic Diagram

Table 2-1 Ordering Information

Type	Package	Configuration	Marking code
ESD3V3XU1UL	PG-TSLP-2-17	1 line, uni-directional	X1
ESD3V3XU1US	PG-TSSLP-2-1	1 line, uni-directional	K

3 Characteristics

Table 3-1 Maximum Rating at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit
		Min.	Typ.	Max.	
ESD (air / contact) discharge ¹⁾	V_{ESD}	–	–	20	kV
Peak pulse current ($t_p = 8/20\ \mu\text{s}$) ²⁾	I_{PP}	–	–	3	A
Operating temperature range	T_{OP}	-40	–	125	$^\circ\text{C}$
Storage temperature	T_{stg}	-65	–	150	$^\circ\text{C}$

1) V_{ESD} according to IEC61000-4-2 ($R = 330\ \Omega$, $C = 150\ \text{pF}$)

2) I_{PP} according to IEC61000-4-5

3.1 Electrical Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

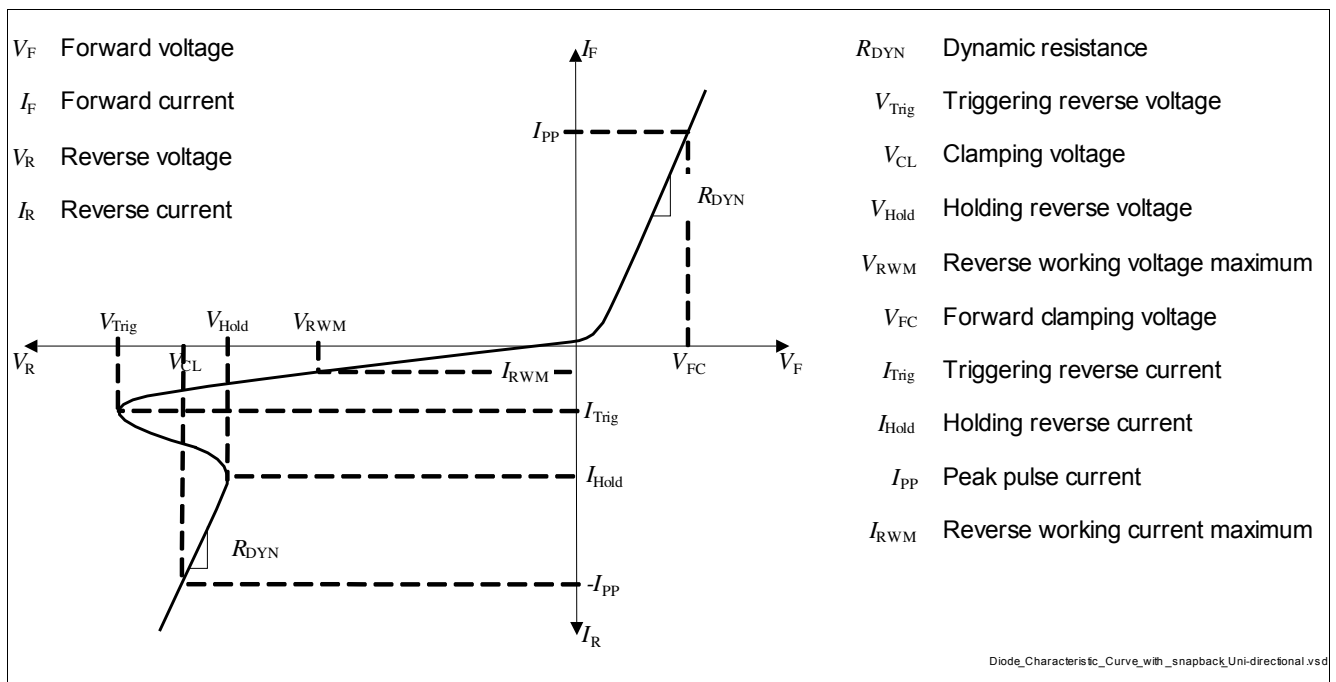


Figure 3-1 Definitions of electrical characteristics

Table 3-2 DC Characteristics at $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Reverse working voltage	V_{RWM}	–	–	3.3	V	Pin 1 to Pin 2
Reverse current	I_R	–	1	50	nA	$V_R = 3.3\ \text{V}$, from Pin 1 to Pin 2
Reverse breakdown voltage	V_{BR}	–	6.5	–	V	$I_R = 1\ \text{mA}$ from Pin 1 to Pin 2 voltage forced

Table 3-3 RF Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Line capacitance	C_L	–	0.4	0.65	pF	$V_R = 0\text{ V}, f = 1\text{ MHz}$
		–	0.4	0.65	pF	$V_R = 0\text{ V}, f = 1\text{ GHz}$
Series inductance	L_S	–	0.4	–	nH	ESD3V3XU1US
		–	0.2	–	nH	ESD3V3XU1UL

Table 3-4 ESD Characteristics at $T_A = 25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Trigger voltage ¹⁾ [2]	V_{TRIG}	–	7.2	–	V	TLP, from Pin 1 to Pin 2
Reverse clamping voltage ¹⁾ [2]	V_{CL}	–	8	–	V	TLP, $I_{PP} = 16\text{ A}$, from Pin 1 to Pin 2
		–	11	–	V	TLP, $I_{PP} = 30\text{ A}$, from Pin 1 to Pin 2
Forward clamping voltage ¹⁾ [2]	V_{FC}	–	6	–	V	TLP, $I_{PP} = 16\text{ A}$, from Pin 2 to Pin 1
		–	9	–	V	TLP, $I_{PP} = 30\text{ A}$, from Pin 2 to Pin 1
Dynamic resistance ¹⁾ [2]	R_{DYN}	–	0.19	–	Ω	TLP, Pin 1 to Pin 2
		–	0.23	–	Ω	TLP, Pin 2 to Pin 1

1)Please refer to Application Note AN210. ANSI/ESD STM5.5.1 - Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP), $t_p = 100\text{ ns}$, $t_r = 0.6\text{ ns}$, I_{TLP} and V_{TLP} averaging window: $t_1 = 30\text{ ns}$ to $t_2 = 60\text{ ns}$, extraction of dynamic TLP characteristic between $I_{PP1} = 10\text{ A}$ and $I_{PP2} = 40\text{ A}$.

3.2 Typical Characteristics at $T_A=25^\circ\text{C}$, unless otherwise specified

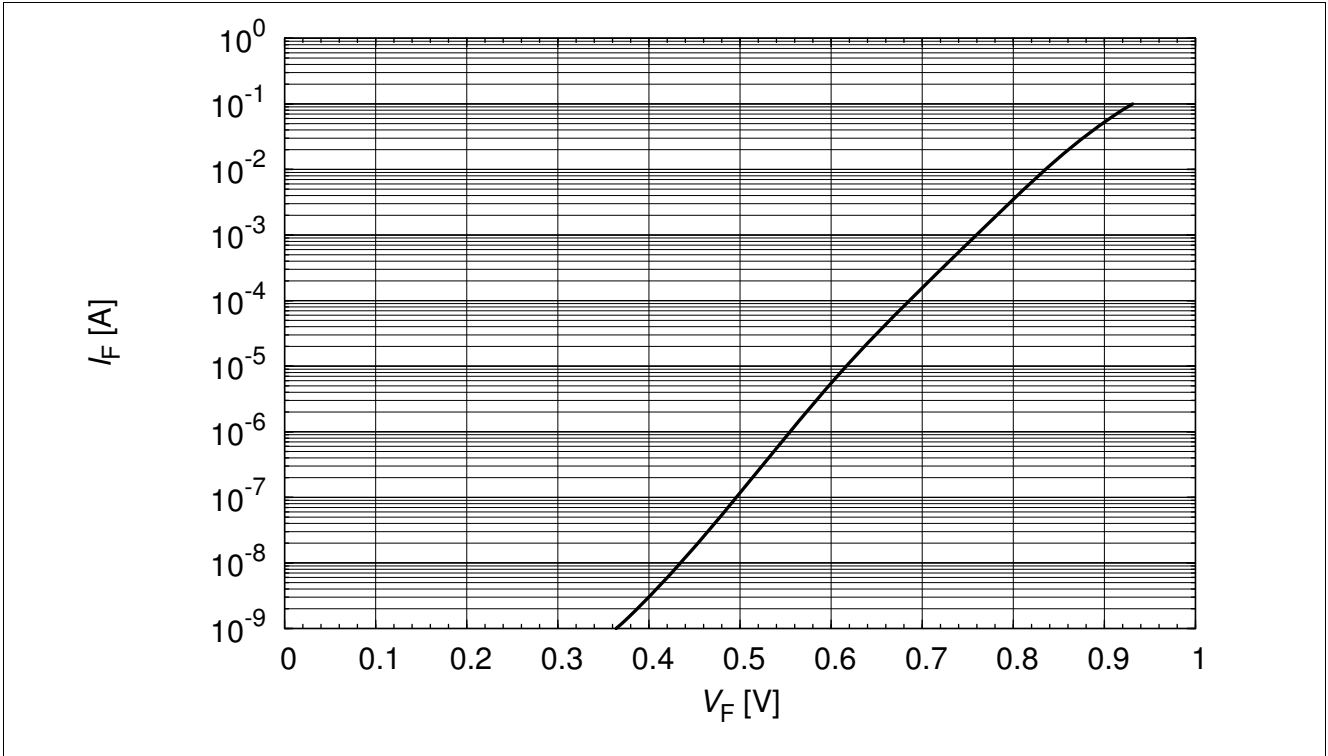


Figure 3-2 Forward current, $I_F = (V_F)$

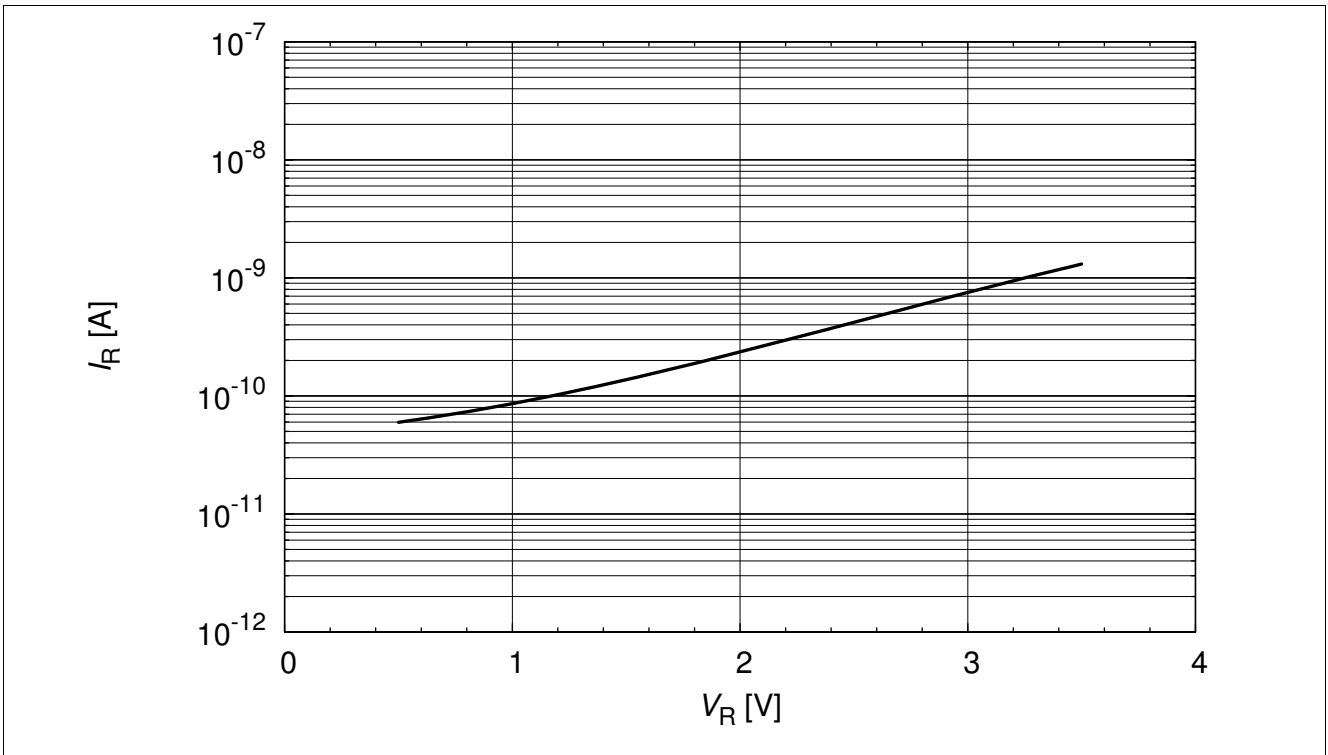


Figure 3-3 Reverse current, $I_R = (V_R)$

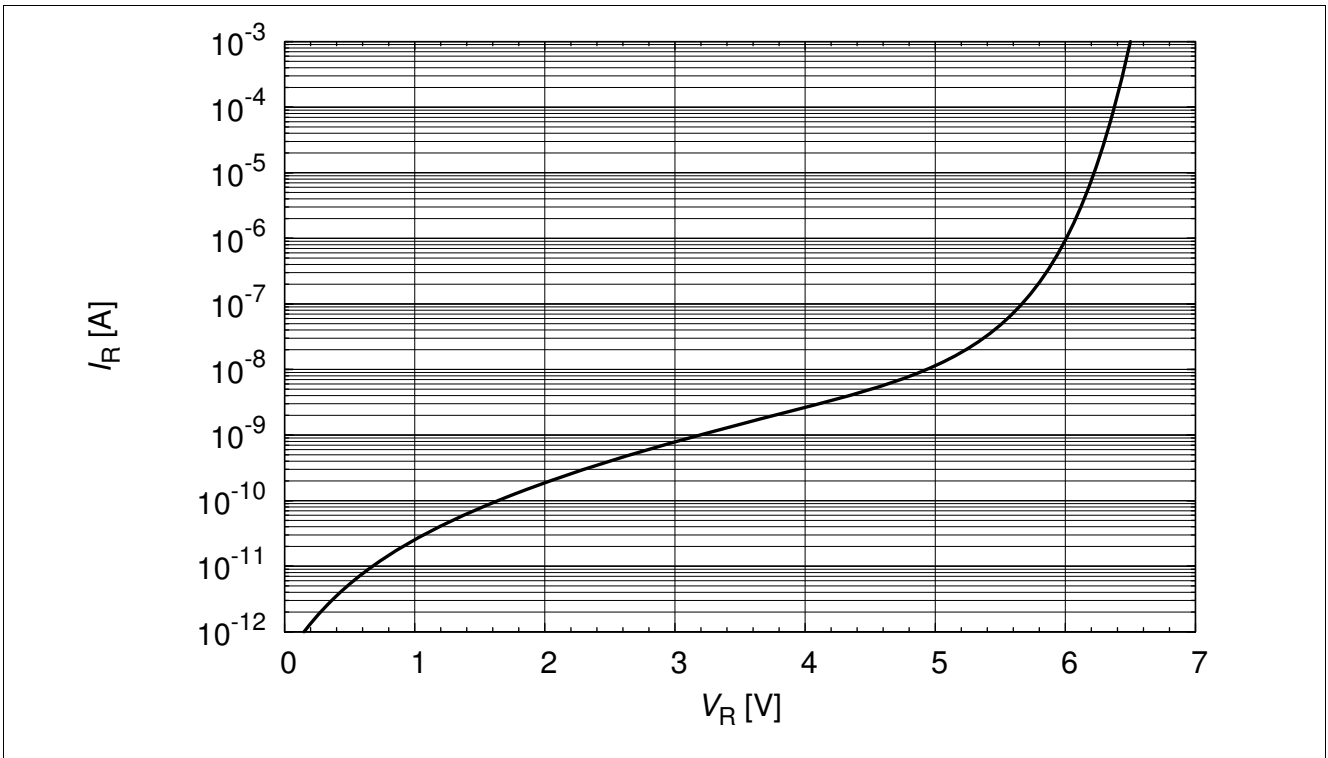


Figure 3-4 Reverse voltage characteristic, $I_R = (V_R)$

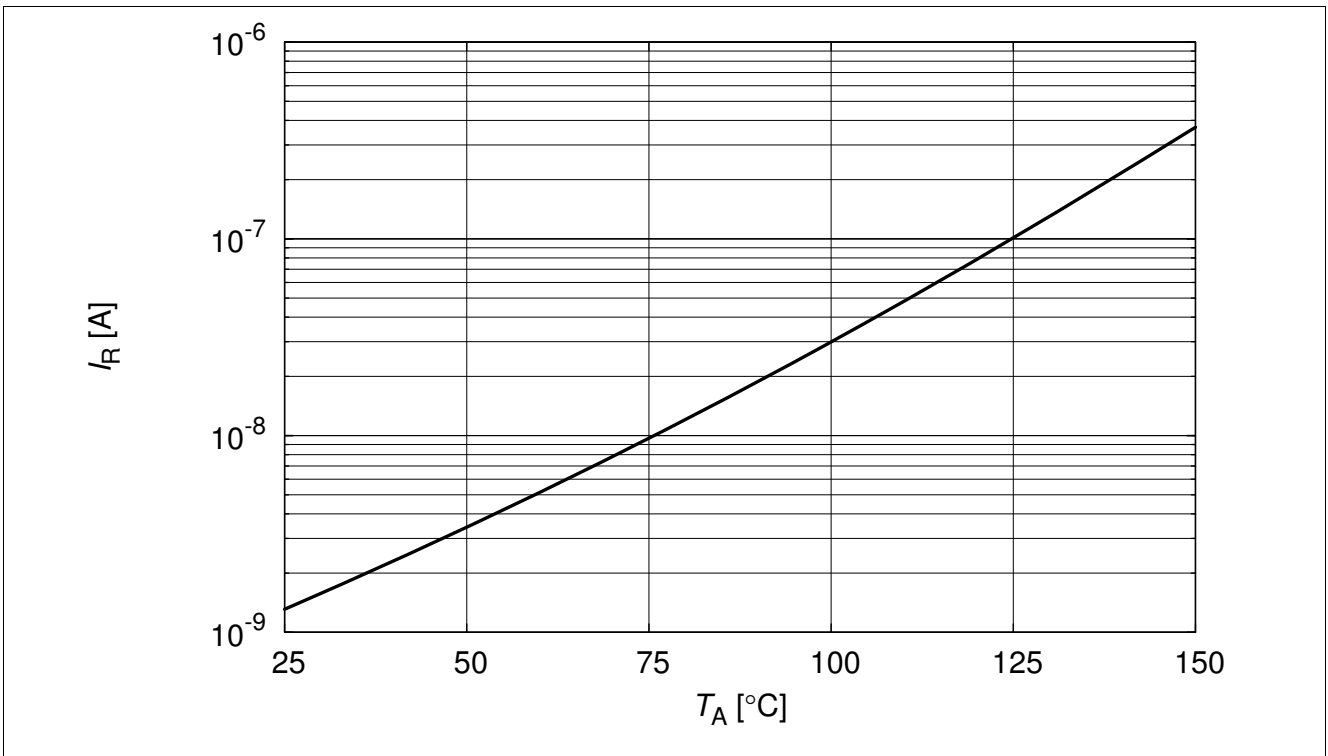


Figure 3-5 Reverse current $I_R = f(T_A)$, $V_R = 3.3$ V

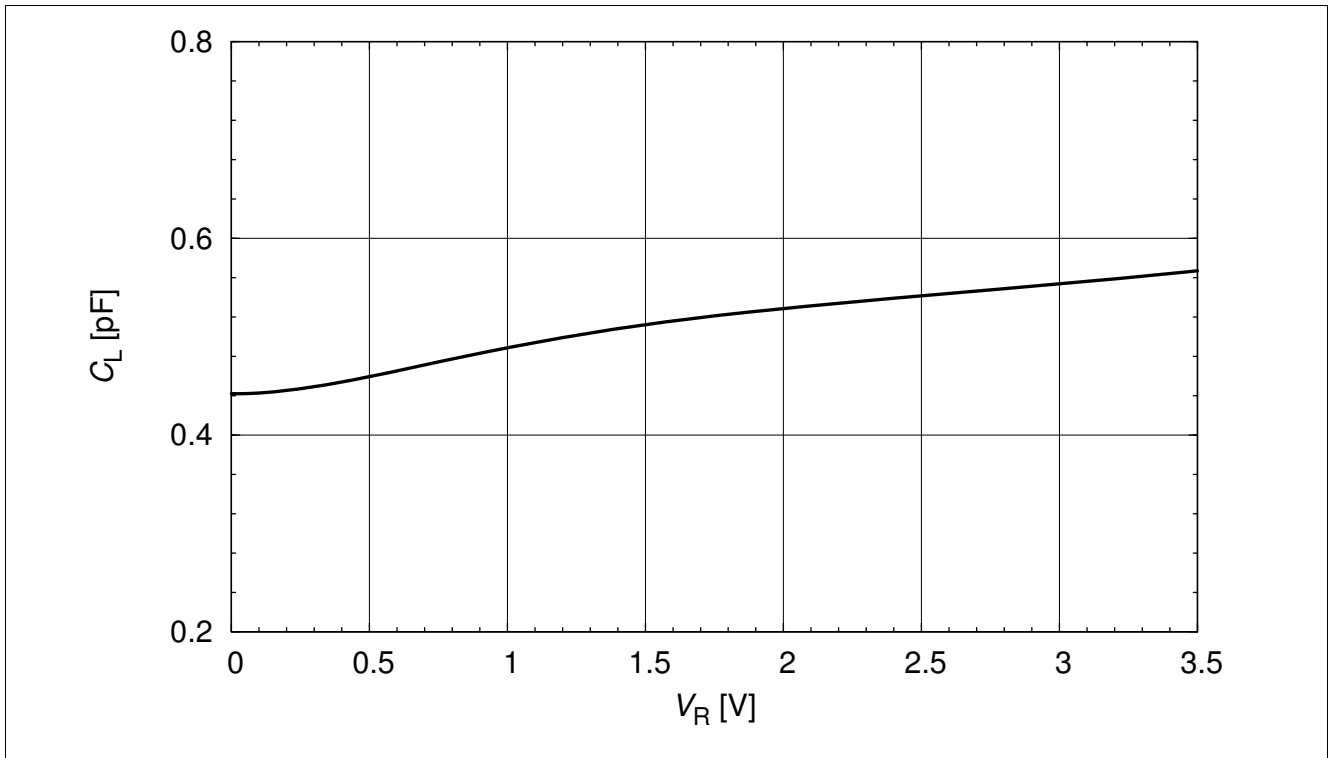


Figure 3-6 Line capacitance $C_L = f(V_R)$, $f = 1\text{MHz}$, from pin 1 to pin 2

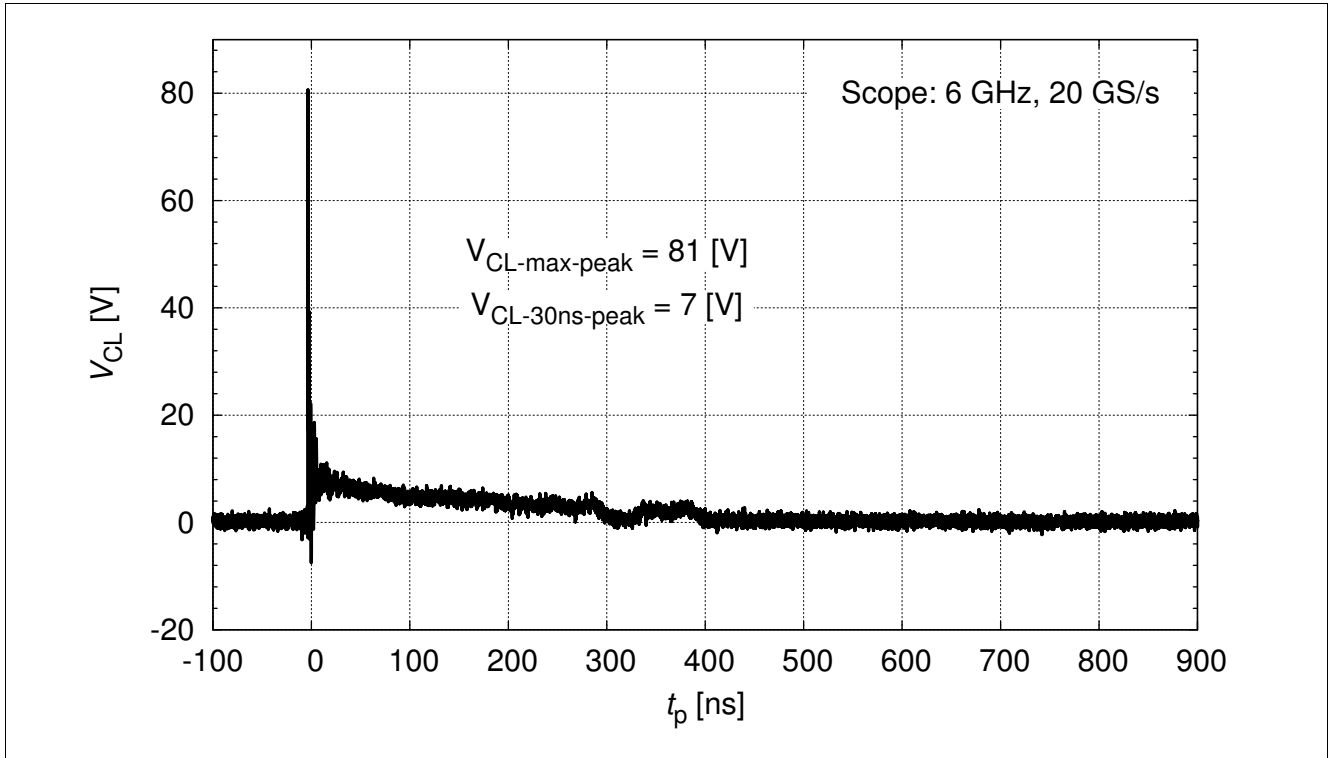


Figure 3-7 IEC61000-4-2 $V_{CL} = f(t)$, 8 kV positive pulse from pin 1 to pin 2

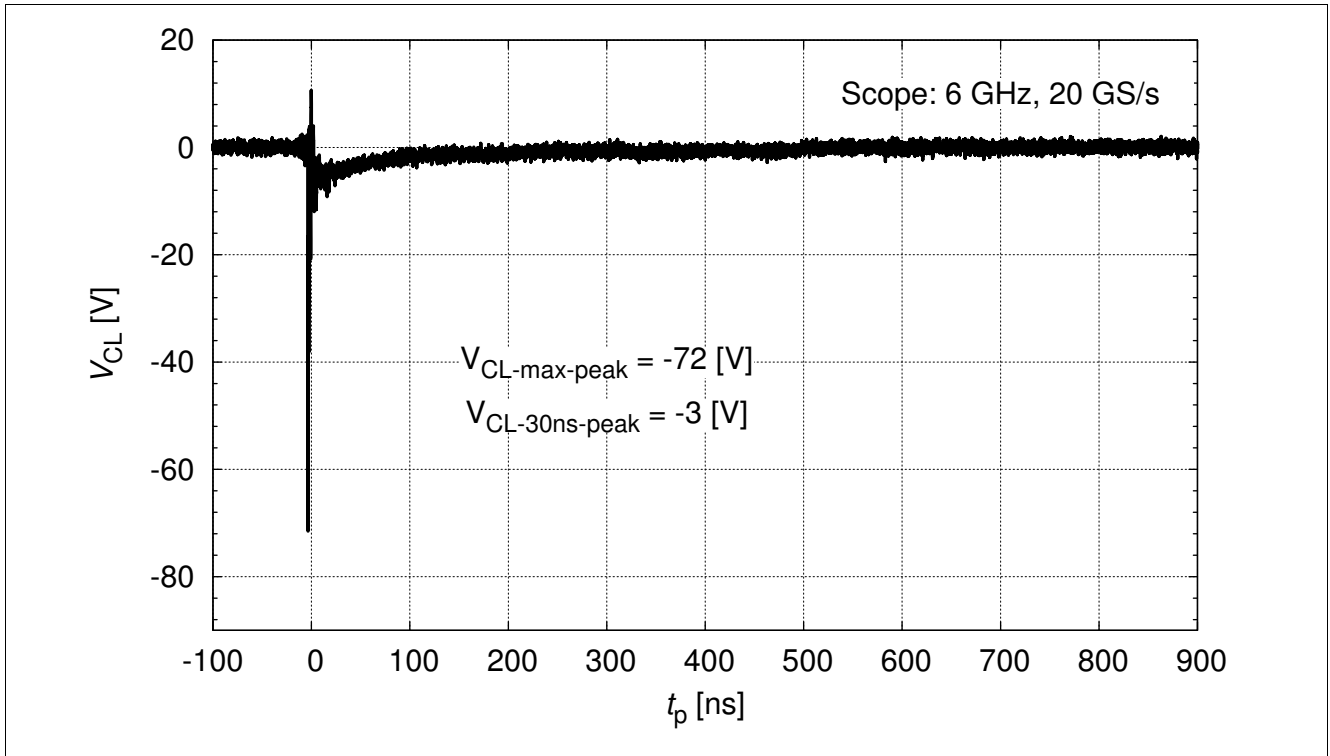


Figure 3-8 IEC61000-4-2 $V_{CL} = f(t)$, 8 kV negative pulse from pin 1 to pin 2

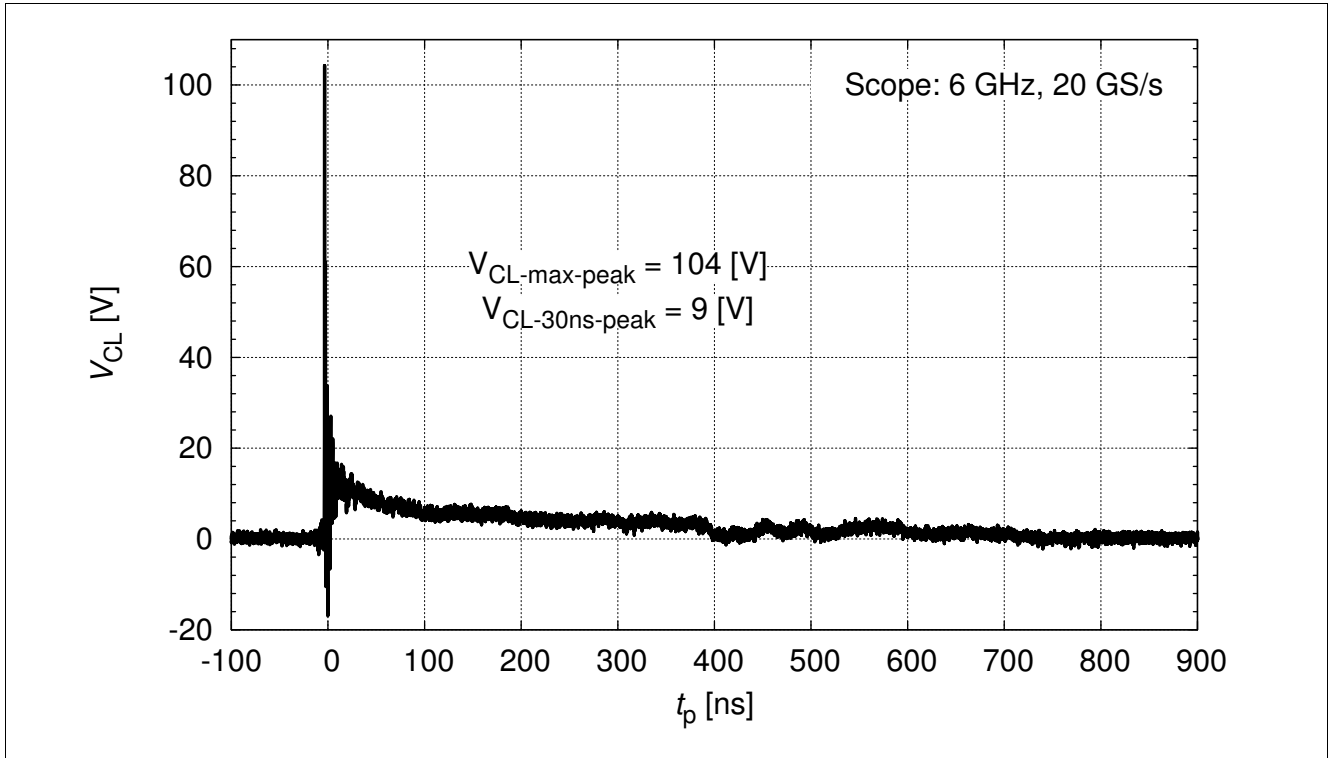


Figure 3-9 IEC61000-4-2 $V_{CL} = f(t)$, 15 kV positive pulse from pin 1 to pin 2

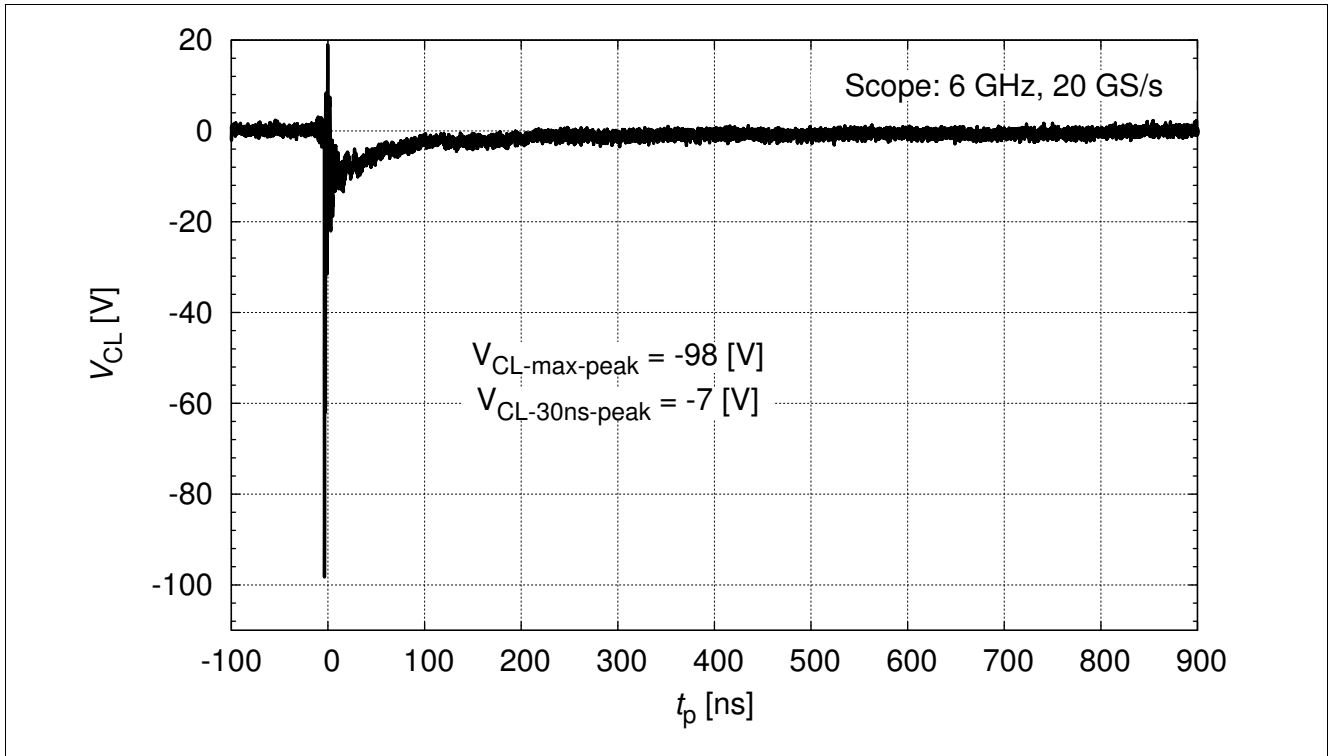


Figure 3-10 IEC61000-4-2 $V_{CL} = f(t)$, 15 kV negative pulse from pin 1 to pin 2

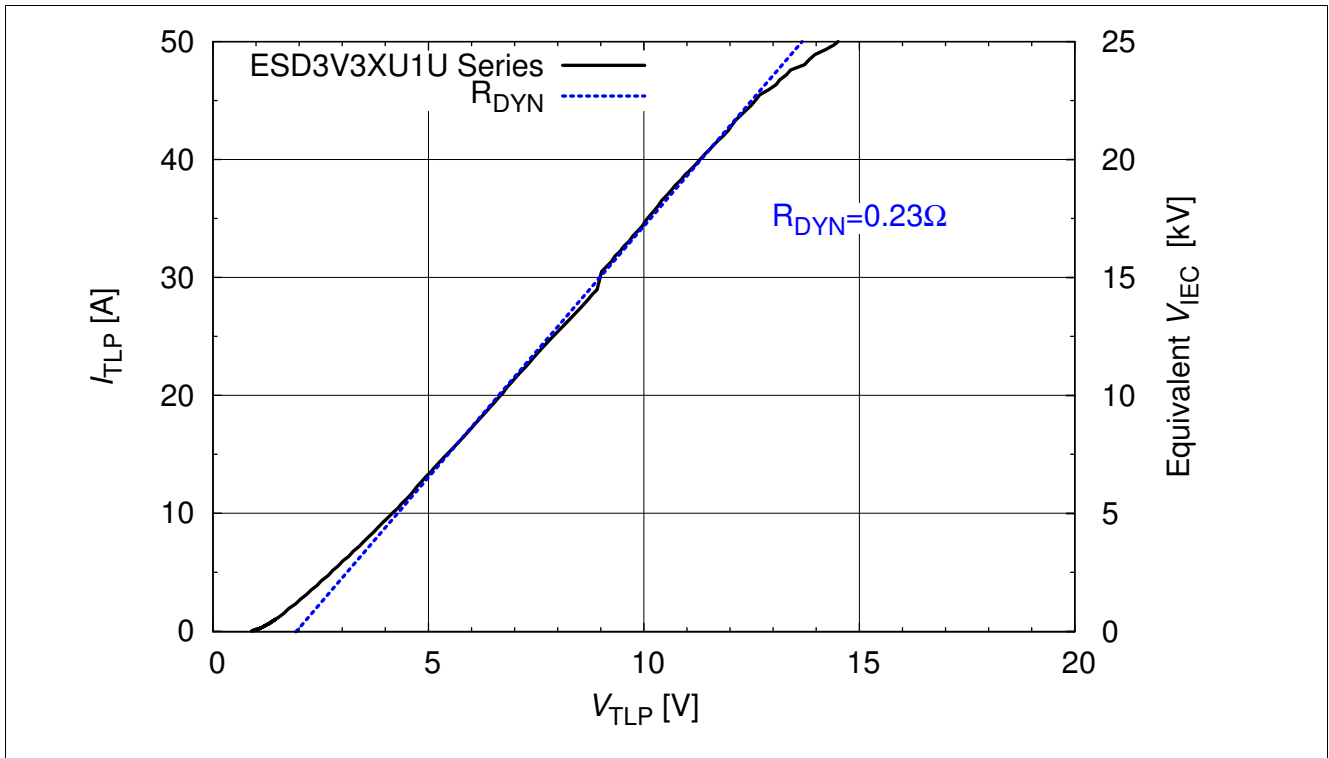


Figure 3-11 Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 2 to pin 1 ^{Note: [2]}

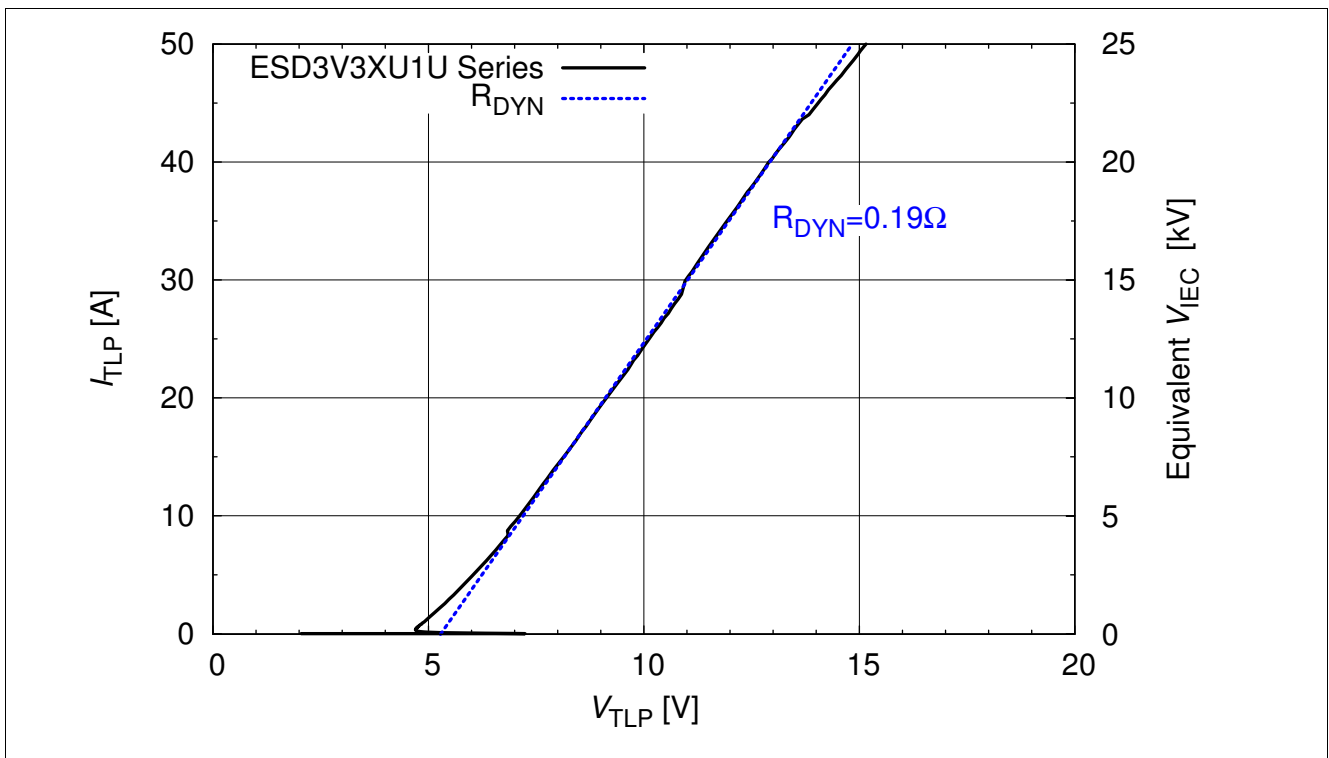


Figure 3-12 Clamping voltage $V_{TLP} = f(I_{TLP})$, from pin 1 to pin 2 ^{Note: [2]}

Note: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 600 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$, extraction of dynamic resistance using least squares fit of TLP characteristic between $I_{PP1} = 10 \text{ A}$ and $I_{PP2} = 40 \text{ A}$. The equivalent stress level V_{IEC} according IEC 61000-4-2 ($R = 330 \Omega$, $C = 150 \text{ pF}$) is calculated at the broad peak of the IEC waveform at $t = 30 \text{ ns}$ with 2 A/kV

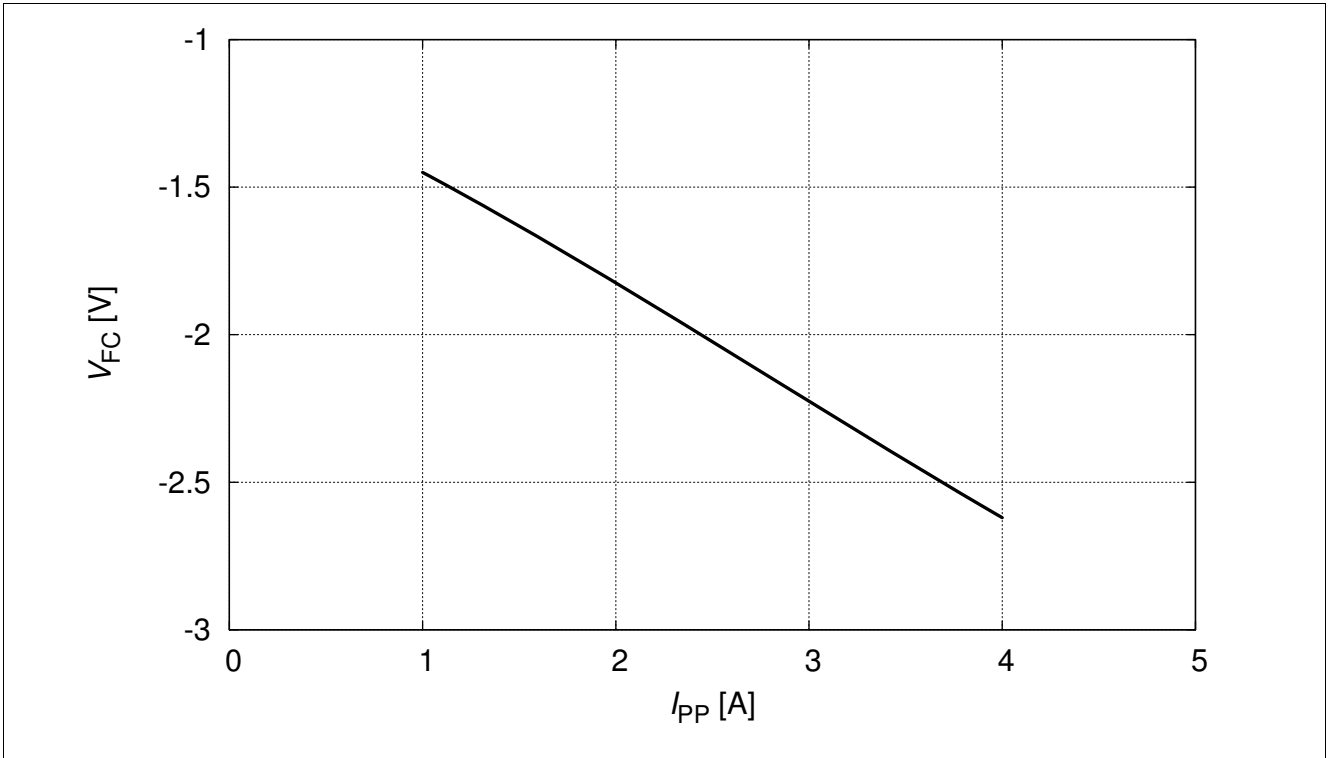


Figure 3-13 Forward clamping voltage $I_{PP} = f(V_{FC})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 μ s)

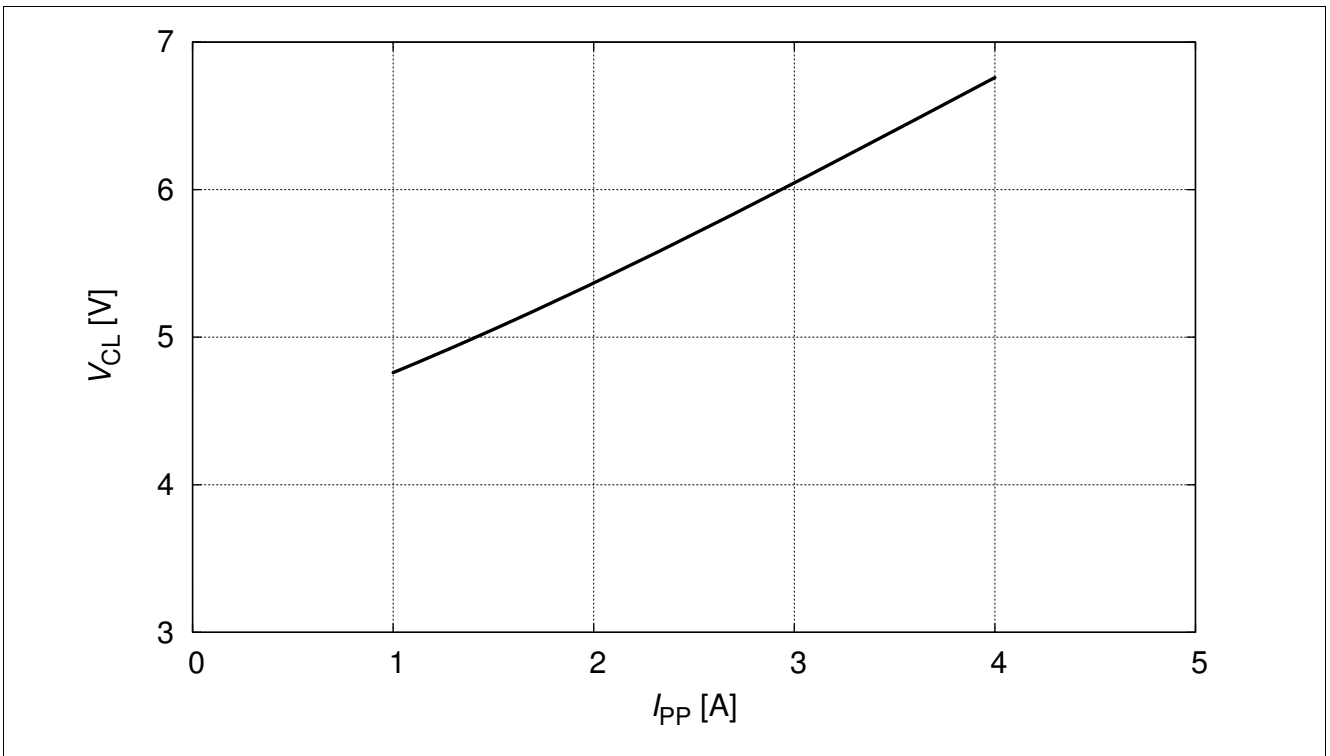


Figure 3-14 Reverse clamping voltage $I_{PP} = f(V_{CL})$, from pin 1 to pin 2 according to IEC61000-4-5 (8/20 μ s)

4 Application Information

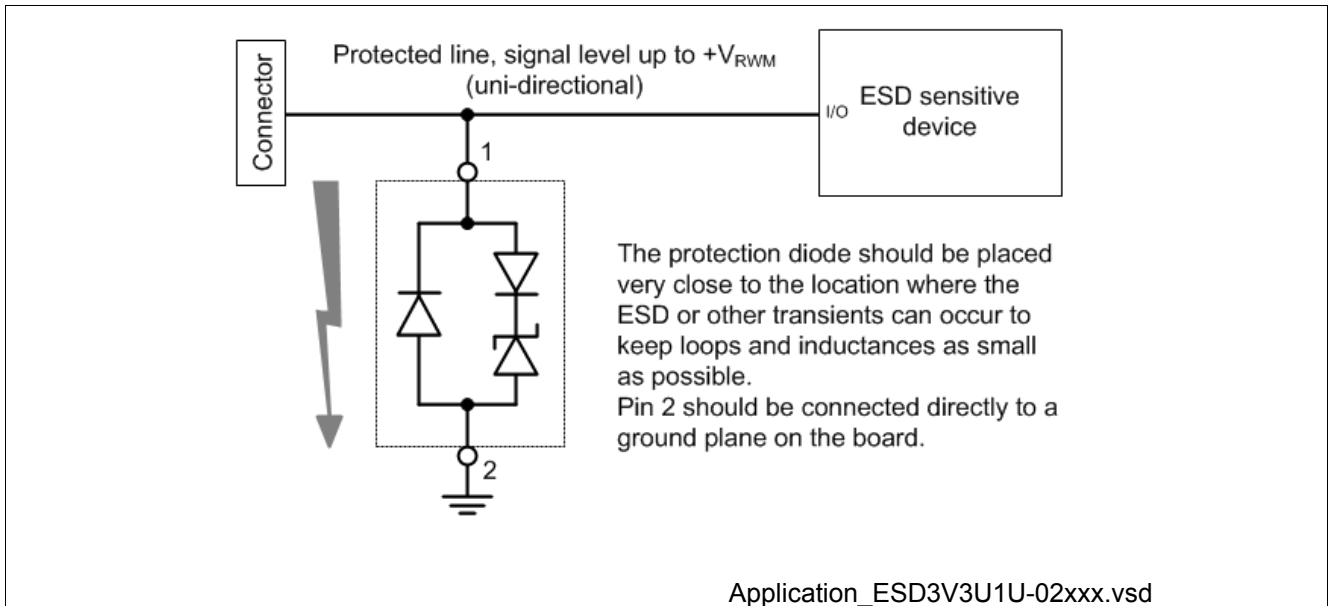


Figure 4-1 Single line, uni-directional ESD / Transient protection

5 Package Information

5.1 PG-TSLP-2-17 (mm) [3]

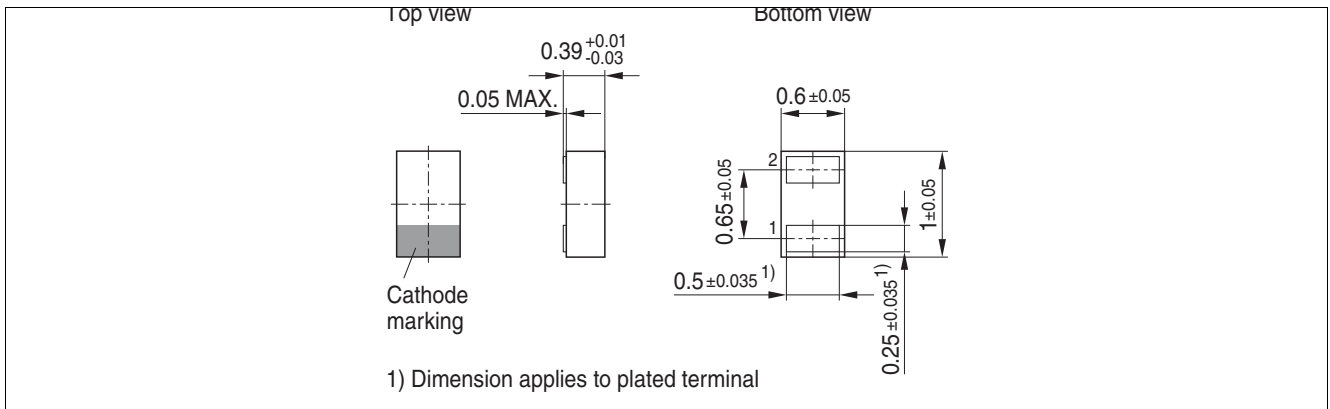


Figure 5-1 PG-TSLP-2-17: Package overview

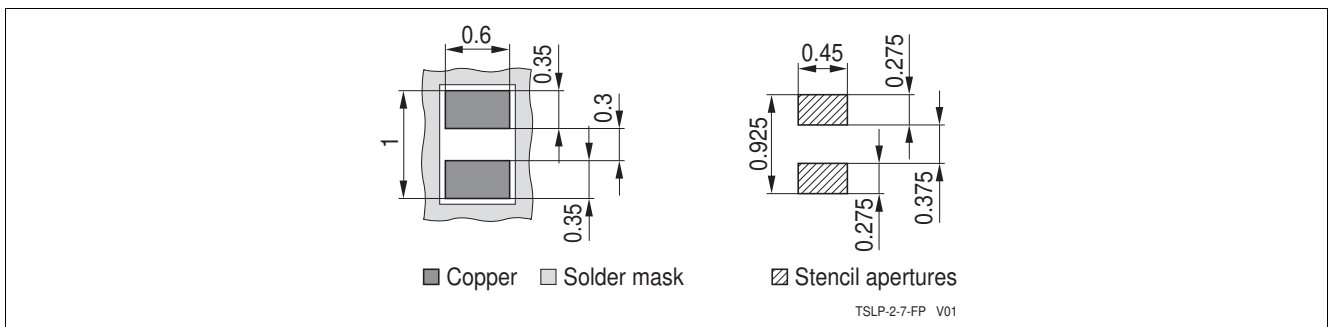


Figure 5-2 PG-TSLP-2-17: Footprint

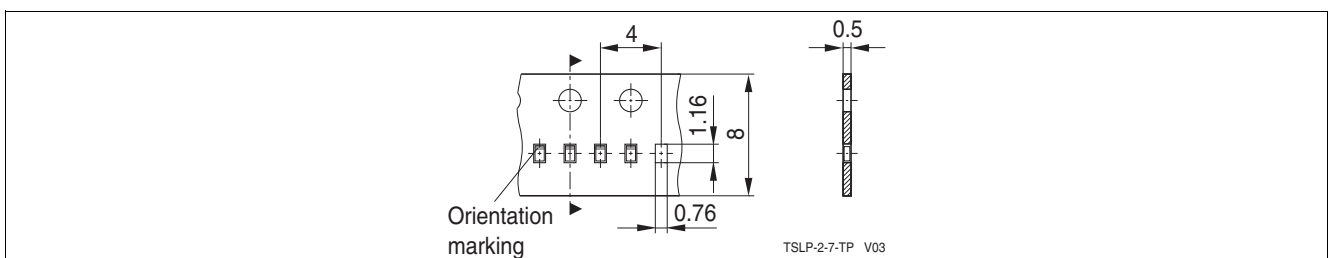


Figure 5-3 PG-TSLP-2-17: Packing

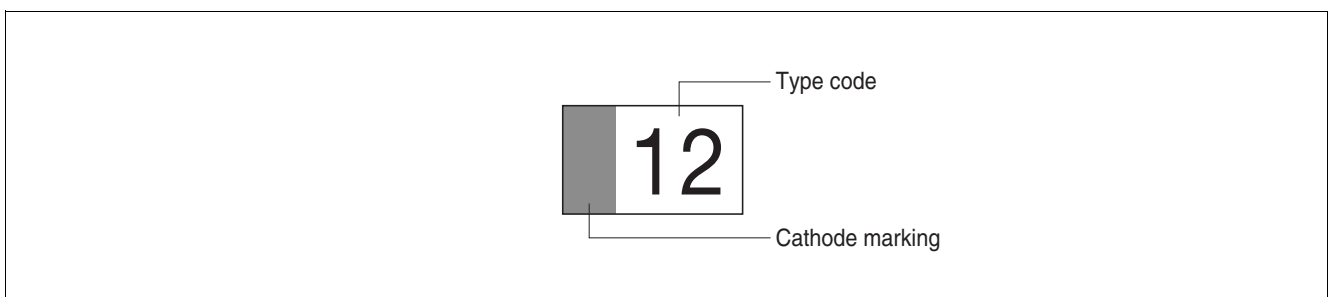


Figure 5-4 PG-TSLP-2-17: Marking (example)

5.2 PG-TSSLP-2-1 (mm) [3]

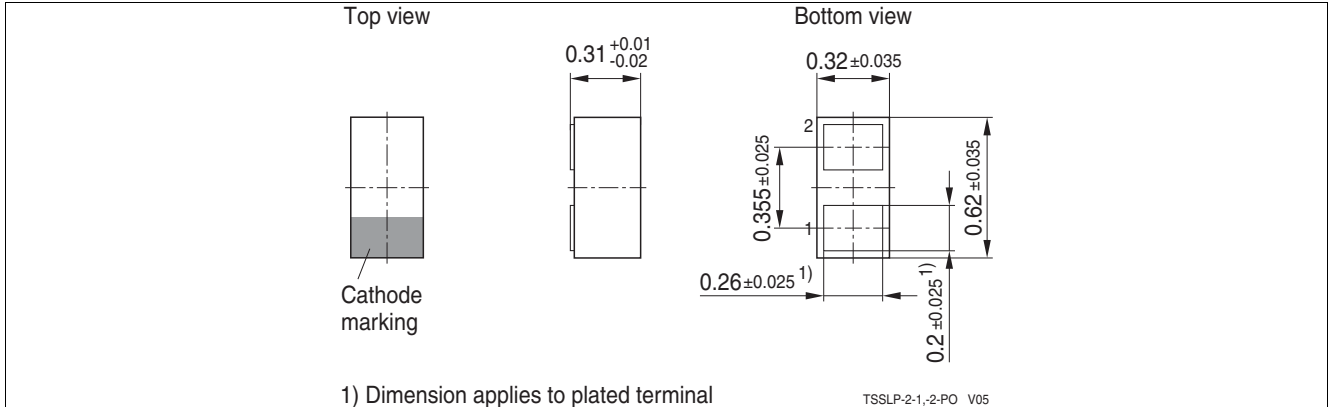


Figure 5-5 PG-TSSLP-2-1: Package overview

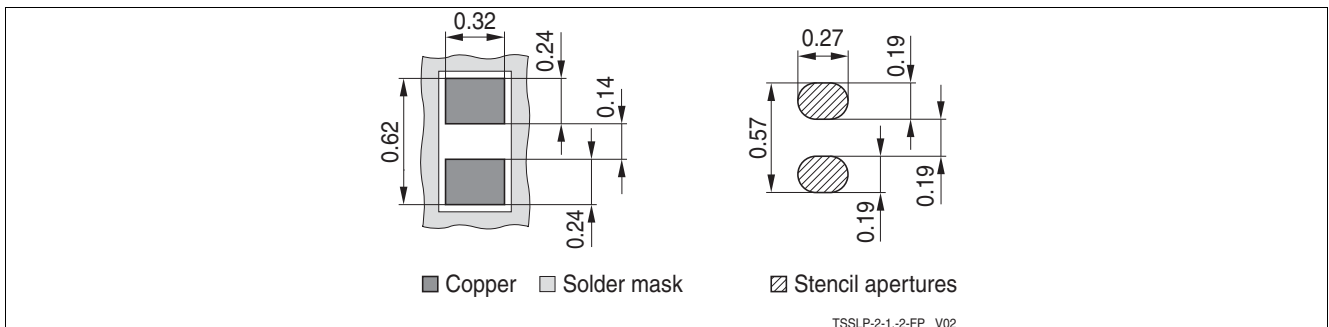


Figure 5-6 PG-TSSLP-2-1: Footprint

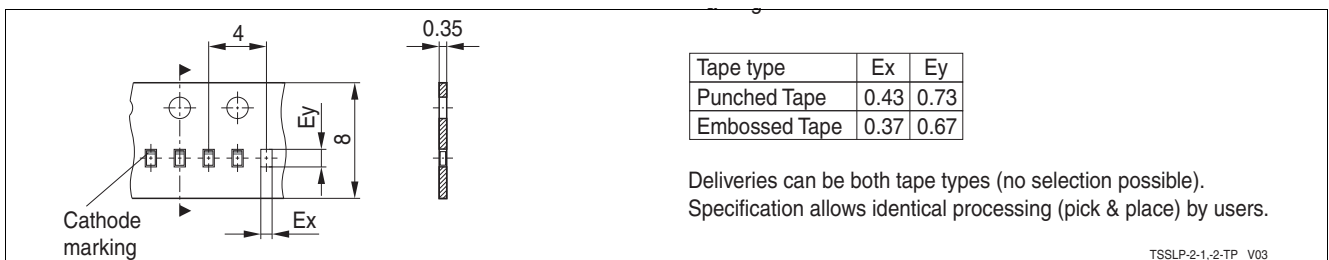


Figure 5-7 PG-TSSLP-2-1: Packing

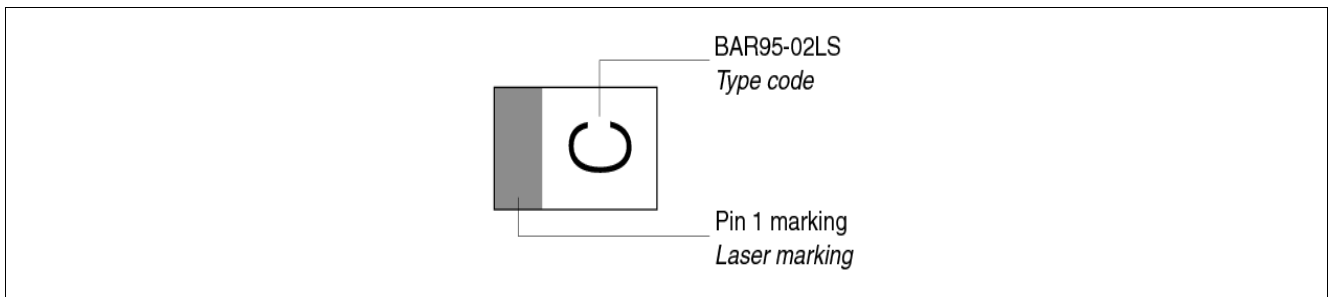


Figure 5-8 PG-TSSLP-2-1: Marking (example)

References

- [1] On-chip ESD protection for integrated circuits, Albert Z. H. Wang, ISBN:0-7923-7647-1
- [2] Infineon AG - **Application Note AN210: Effective ESD Protection Design at System Level Using VF-TLP Characterization Methodology**
- [3] Infineon AG - Recommendations for PCB Assembly of Infineon TSLP and TSSLP Package

Terminology

C_L	Line capacitance
DVI	Digital Visual Interface
EFT	Electrical Fast Transient
ESD	Electrostatic Discharge
HDMI	High Definition Multimedia Interface
IEC	International Electrotechnical Commission
I_{PP}	Peak pulse current
I_R	Reverse current
I_{RWM}	Reverse working current maximum
MDDI	Mobile Display Digital Interface
MIPI	Mobile Industrial Processor Interface
NFC	Near Field Communication
PCB	Printed Circuit Board
R_{DYN}	Dynamic resistance
RoHS	Restriction of Hazardous Substances Directive
S-ATA	Serial Advanced Technology Attachment
SWP	Single Wire Protocol
T_A	Ambient temperature
TLP	Transmission Line Pulse
T_{OP}	Operation temperature
t_p	Pulse duration
t_r	Pulse rise time
T_{stg}	Storage temperature
USB	Universal Serial Bus
V_{CL}	Reverse clamping voltage
V_{ESD}	Electrostatic discharge voltage
V_{FC}	Forward Clamping Voltage
V_{Hold}	Holding Voltage
V_{IEC}	Equivalent stress level according IEC61000-4-2 ($R = 330 \Omega$, $C = 150 \text{ pF}$)
V_R	Reverse voltage
V_{RWM}	Reverse working voltage maximum
V_{Trig}	Triggering Voltage
Z_0	Impedance

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