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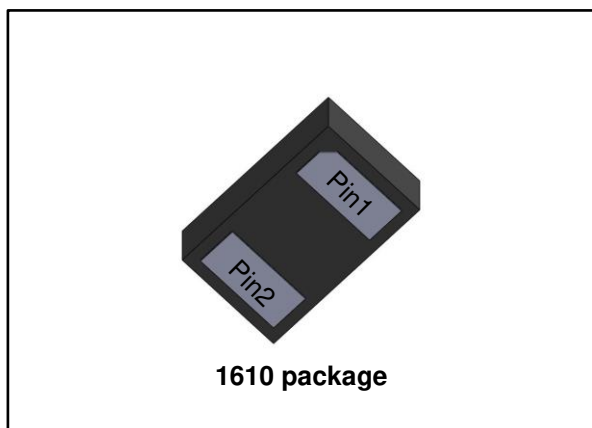
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**High power transient voltage suppressor**

Datasheet - production data

**Features**

- Low clamping voltage
- Peak pulse power: 1400 W (8/20  $\mu$ s)
- Stand-off voltage 5.5 V
- Unidirectional diode
- Low leakage current: 1.5  $\mu$ A at 25 °C
- Complies with IEC 61000-4-2 level 4
  - $\pm$ 30 kV (air discharge)
  - $\pm$ 30 kV (contact discharge)

**Applications**

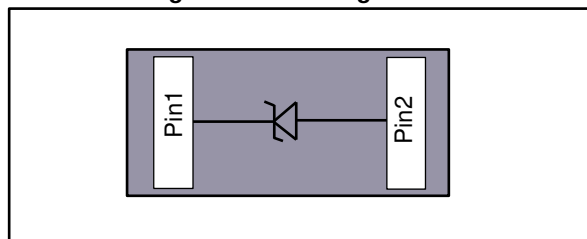
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Smartphones, mobile phones, tablets, portable multimedia
- USB  $V_{BUS}$  protection
- Power supply protection
- Battery protection

**Description**

The ESDA7P120-1U1M is a unidirectional single line TVS diode designed to protect the power line against EOS and ESD transients.

The device is ideal for applications where high power TVS and board space saving is required.

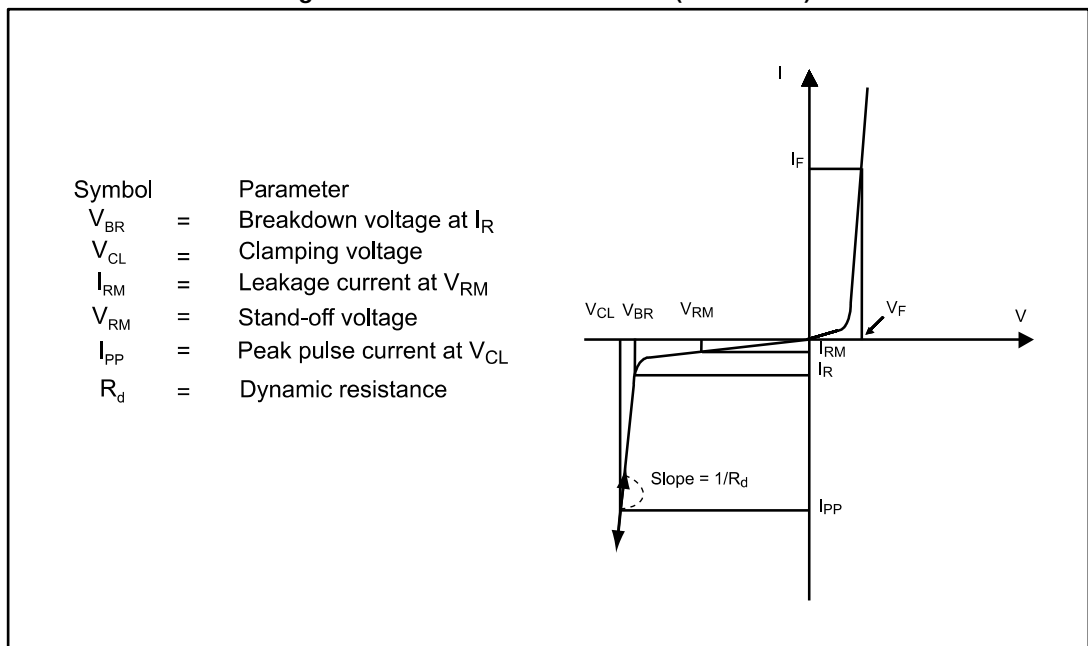
**Figure 1: Pin configuration**

# 1 Characteristics

**Table 1: Absolute maximum ratings (T<sub>amb</sub> = 25 °C)**

Symbol	Parameter		Value	Unit
V <sub>PP</sub>	Peak pulse voltage	IEC 61000-4-2: Contact discharge	>30	kV
		Air discharge	>30	
P <sub>PP</sub>	Peak pulse power	8/20µs	1400	W
I <sub>PP</sub>	Peak pulse current	8/20µs	120	A
T <sub>stg</sub>	Storage junction temperature range		-55 to +150	°C
T <sub>op</sub>	Operating junction temperature range		-55 to +150	

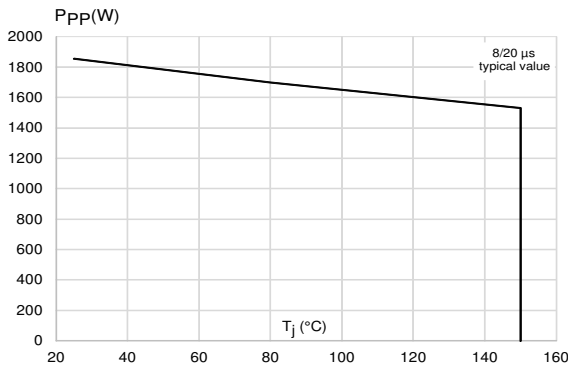
**Figure 2: Electrical characteristics (definitions)**



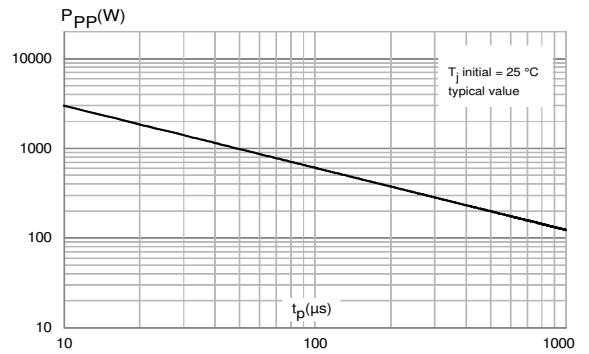
**Table 2: Electrical characteristics (T<sub>amb</sub> = 25 °C)**

Symbol	Test condition	Min.	Typ.	Max.	Unit
V <sub>BR</sub>	I <sub>R</sub> = 1 mA	6.4	6.8		V
I <sub>RM</sub>	V <sub>RM</sub> = 5 V			350	nA
I <sub>RM</sub>	V <sub>RM</sub> = 5.5 V			1.5	µA
R <sub>d</sub>	8/20 µs		0.035		Ω
V <sub>CL</sub>	I <sub>PP</sub> = 80 A, 8/20 µs		9.5	10.0	V
V <sub>CL</sub>	I <sub>PP</sub> = 100 A, 8/20 µs		10.2	10.7	V
V <sub>CL</sub>	I <sub>PP</sub> = 120 A, 8/20 µs		11	11.5	V

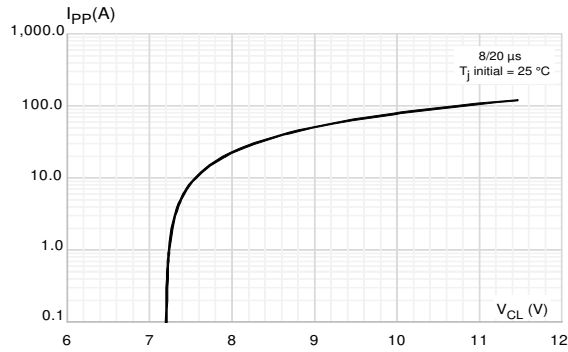
**Figure 3: Peak power dissipation versus initial temperature (typical value)**



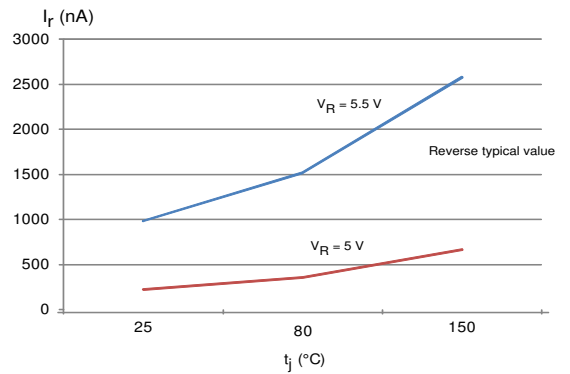
**Figure 4: Peak pulse power versus exponential pulse duration (typical value)**



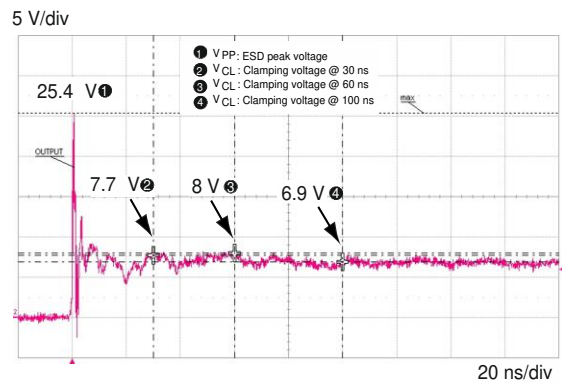
**Figure 5: Peak pulse current versus clamping voltage (maximum value)**



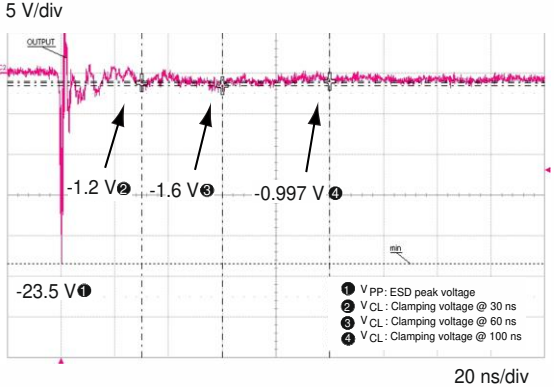
**Figure 6: Leakage current versus junction temperature (typical value)**



**Figure 7: ESD response to IEC 61000-4-2 (+8kV contact discharge)**



**Figure 8: ESD response to IEC 61000-4-2 (-8kV contact discharge)**





## 2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 2.1 QFN 1610 package information

Figure 9: QFN 1610 package outline

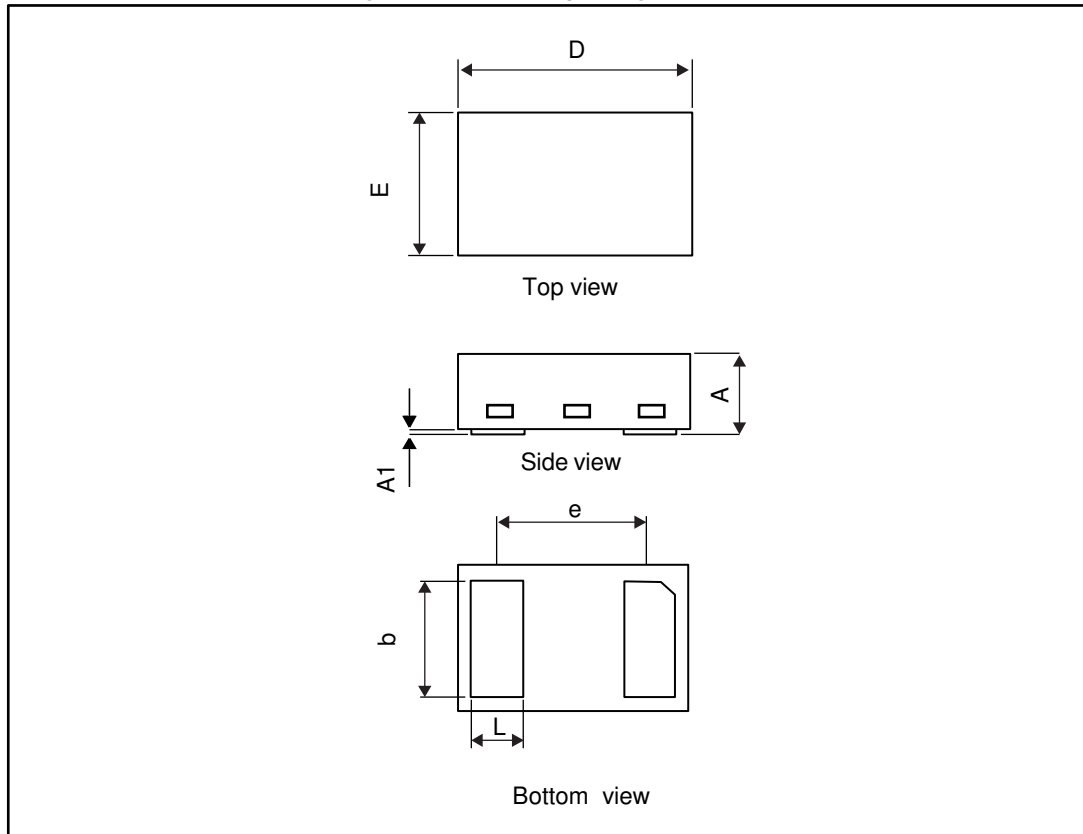
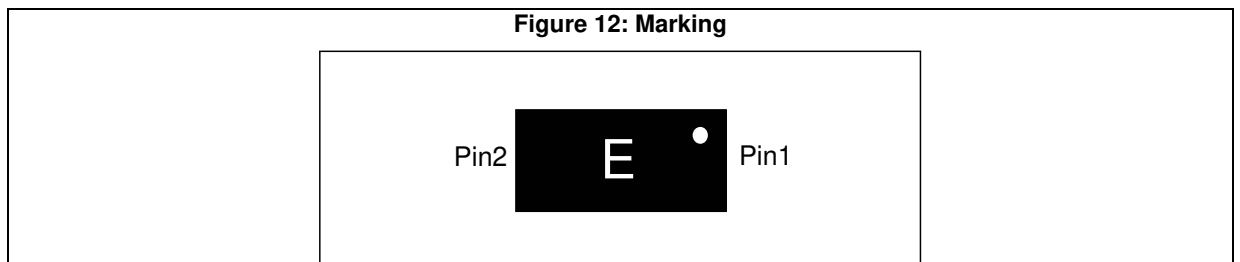
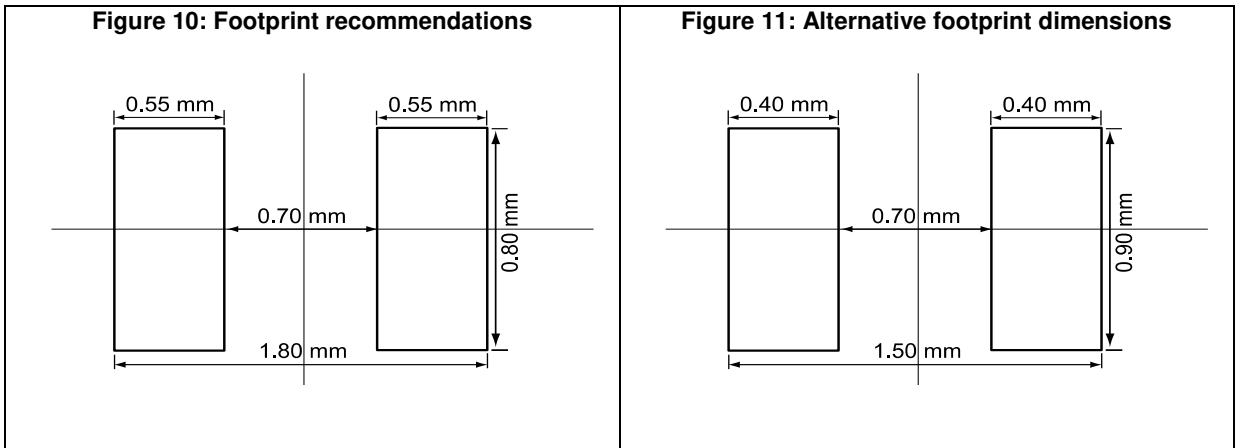
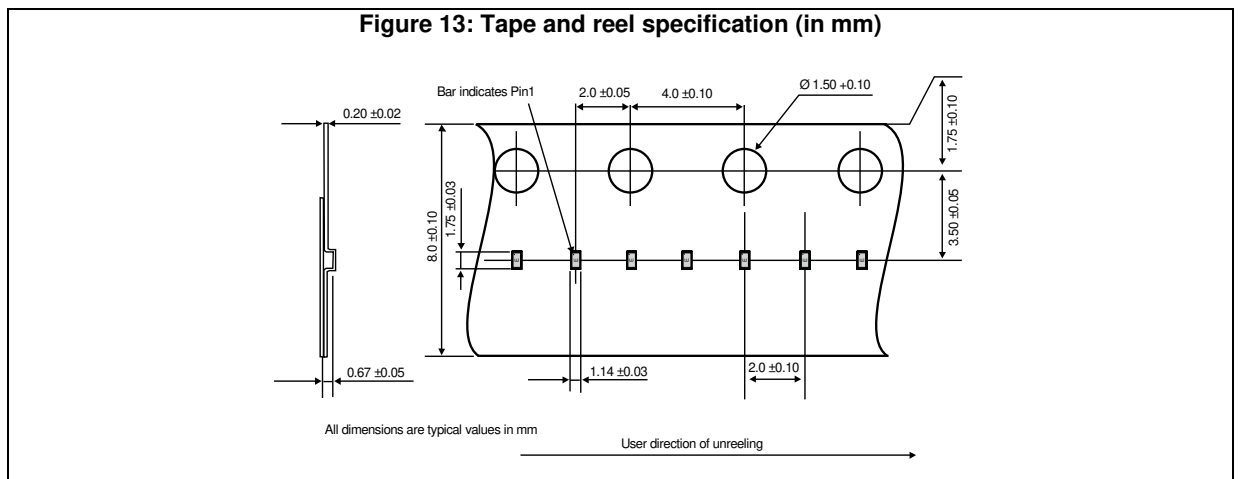


Table 3: QFN 1610 package mechanical data

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.0201	0.0217	0.0236
A1		0.02	0.05		0.0008	0.0020
b	0.75	0.80	0.85	0.0295	0.0315	0.0335
D		1.60			0.0630	
E		1.00			0.0394	
e		1.05			0.0413	
L	0.030	0.035	0.040	0.0118	0.0138	0.0157



Product marking may be rotated by multiples of 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.



### 3 PCB recommendation

#### 3.1 Stencil opening

1. General recommendation on stencil opening design
  - a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
  - a. Stencil thickness (T) = 75 ~ 125 μm
  - b. Aspect ratio =  $\frac{W}{T} \geq 1.5$
  - c. Aspect area =  $\frac{L \times W}{2T(L+W)} \geq 0.66$
3. Reference design
  - a. Stencil opening thickness: 100 μm
  - b. Stencil opening for leads: Opening to footprint ratio is 90%.

Figure 14: Stencil opening dimensions

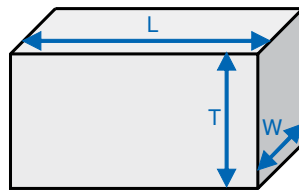


Figure 15: Recommended stencil window position

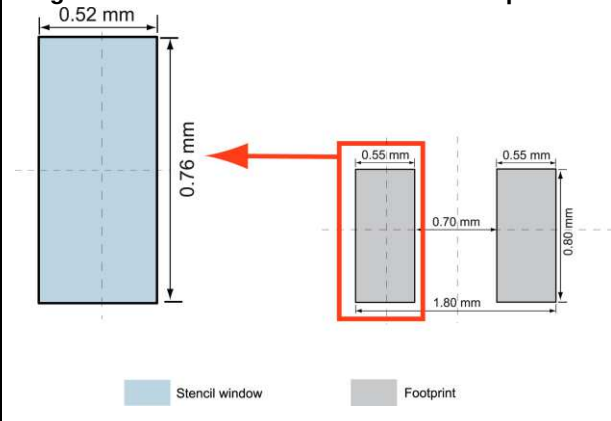
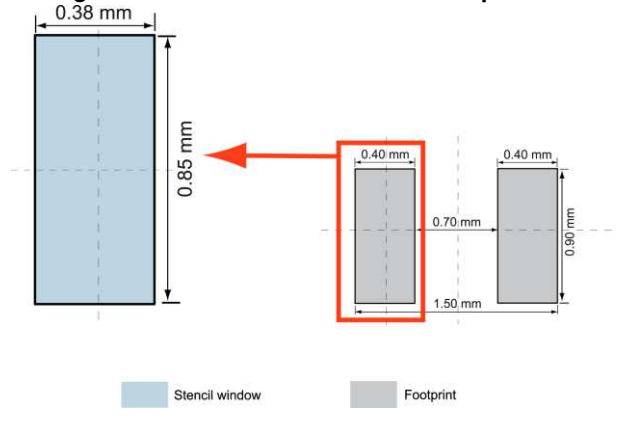


Figure 16: Alternative stencil window position



#### 3.2 Solder paste

1. Use halide-free flux, qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during PCB movement.
4. Solder paste with fine particles: powder particle size is 20-45 μm.

### 3.3 Placement

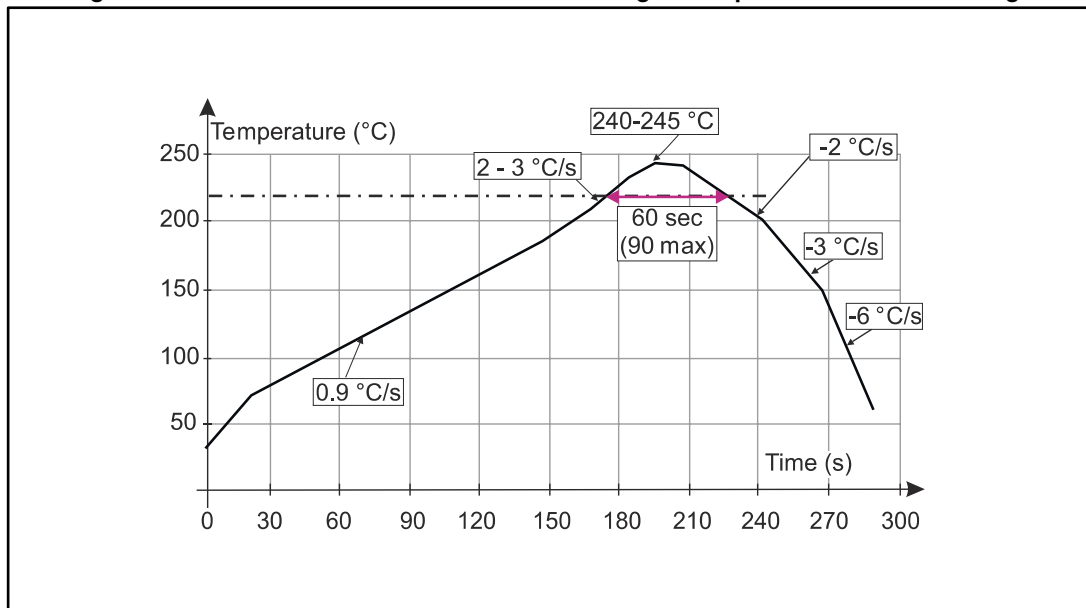
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of  $\pm 0.05$  mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

### 3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

### 3.5 Reflow

Figure 17: ST ECOPACK® recommended soldering reflow profile for PCB mounting



Minimize air convection currents in the reflow oven to avoid component movement.



## 4 Ordering information

Figure 18: Ordering information scheme

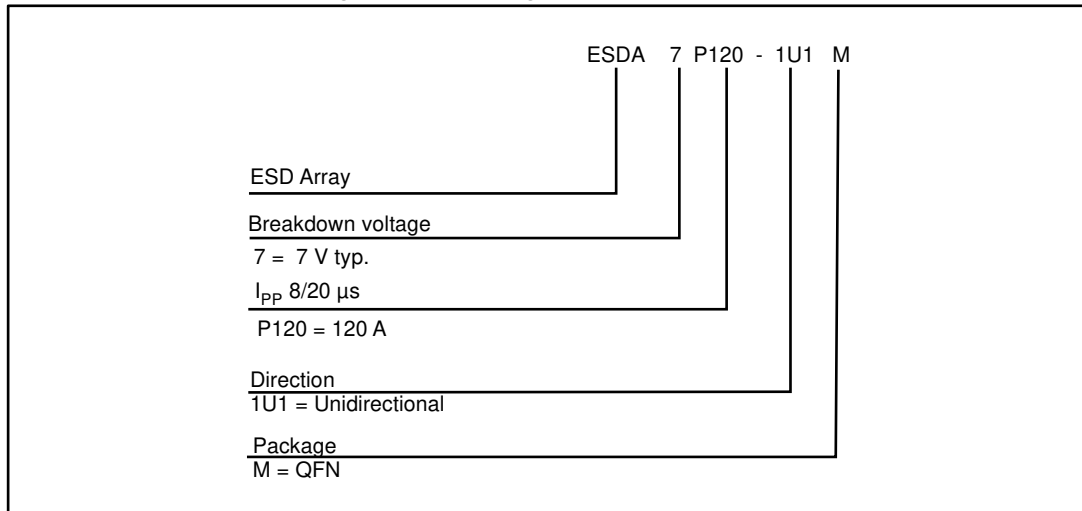


Table 4: Ordering information

Order code	Marking <sup>(1)</sup>	Package	Weight	Base qty.	Delivery mode
ESDA7P120-1U1M	E	QFN 1610	2.4 mg	8000	Tape and reel

**Notes:**

<sup>(1)</sup>The marking can be rotated by multiples of 90° to differentiate assembly location

## 5 Revision history

Table 5: Document revision history

Date	Revision	Changes
18-Jan-2017	1	Initial release.
09-Feb-2017	2	Updated <a href="#">Figure 1: "Pin configuration"</a>

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