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16-Bit Precision, Low Power Meter On A Chip with Cortex-M3 and Connectivity

Data Sheet **ADuCM350**

FEATURES

- Analog performance
  - 160 kSPS, 16-bit, precision analog-to-digital converter (ADC)
    - 4 dedicated voltage measurement channels
    - 8 current measurement channels
    - Impedance measurement engine
  - High precision voltage reference
  - Supply noise rejection filtering
  - Ultralow leakage configurable switch matrix
  - 12-bit digital-to-analog converter (DAC)
  - Precision instrumentation amplifier control loop
  - 6-channel CapTouch controller
  - Temperature sensor
- Analog hardware accelerators
  - Autonomous analog front-end (AFE) controller
    - Independent sequencer for AFE functions
  - Direct digital synthesizer (DDS)/arbitrary waveform generator
  - Receive filters
  - Complex impedance measurement (DFT) engine
- Processing
  - 16 MHz ARM Cortex-M3 processor
  - 384 kB of embedded flash memory
  - 32 kB system SRAM
  - 16 kB Flash configured EEPROM
  - Integrated full-speed USB 2.0 controller and PHY
  - Multilayer advanced microcontroller bus architecture (AMBA) bus matrix
  - Central direct memory access (DMA) controller
  - Real-time clock (RTC)
  - General-purpose, wake-up, and watchdog timers
- Communication
  - Input/output
    - I^2S and beeper interface
    - LCD display controller (parallel and serial)
    - LCD segment controller
    - SPI, I^2C, and UART peripheral interfaces
    - Programmable GPIOs
- Power
  - Coin cell battery compatible
  - 2.5 V to 3.6 V active measurement range
  - Power management unit (PMU)
  - Power-on reset (POR) and power supply monitor (PSM)
- Packages and temperature range
  - Operating temperature range: −40°C to +85°C
  - Package: 120-lead, 8 mm × 8 mm CSP_BGA

APPLICATIONS

- Point-of-care diagnostics
- Body-worn devices for monitoring vital signs
- Amperometric, voltametric, and impedometric measurements

FUNCTIONAL BLOCK DIAGRAM

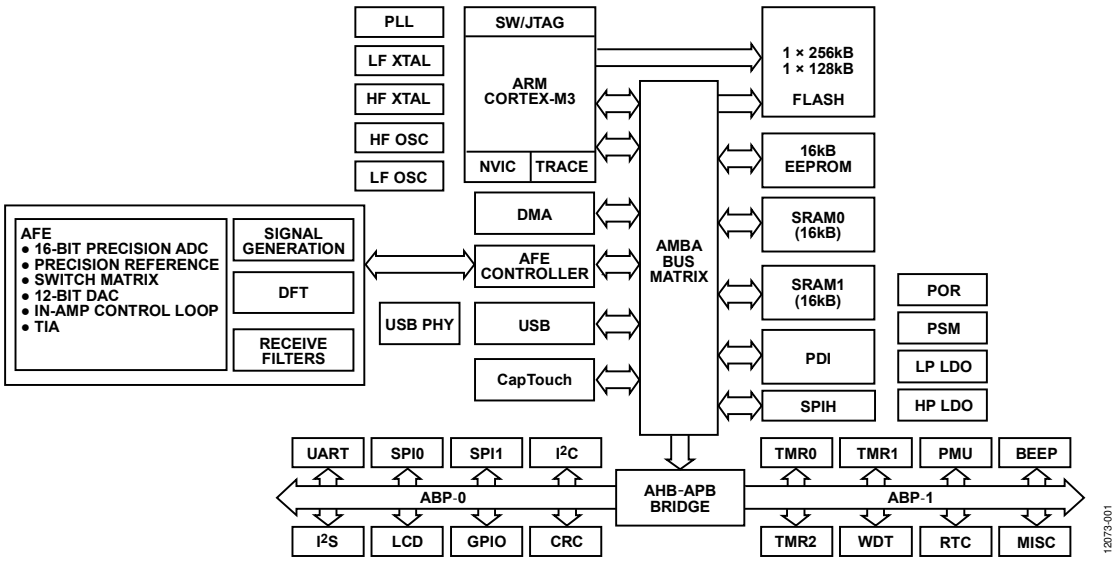

Figure 1.

Rev. A Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADuCM350 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1262: ADuCM350 Serial Download Protocol
- AN-1263: Security Integrity of the ADuCM350
- AN-1271: Optimizing the ADuCM350 for Impedance Conversion
- AN-1281: Amperometric/Potentiostat Measurements Using the ADuCM350
- AN-1282: Profiling the ADuCM350 Supply Current in an Example Application
- AN-1286: ADuCM350 Analog Front End Accuracy in a Noisy Digital Environment
- AN-1293: A Quick Guide to the ADuCM350 Sequencer
- AN-1302: Optimizing the ADuCM350 for 4-Wire, Bio-Isolated Impedance Measurement Applications

Data Sheet

- ADuCM350: 16-Bit Precision, Low Power Meter On A Chip with Cortex-M3 and Connectivity Data Sheet

User Guides

- UG-587: ADuCM350 Hardware Reference Manual
- UG-668: EVAL-ADuCM350EBZ User Guide
- UG-677: ADuCM350 Software Development Kit Quick Start Guide

REFERENCE MATERIALS

Technical Articles

- Home is Where the Heart Is

White Papers

- Operating the AD8233 with the ADuCM350

DESIGN RESOURCES

- ADUCM350 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADUCM350 EngineerZone Discussions.

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Visit the product page to see pricing options.

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REVISION HISTORY

5/14—Revision A: Initial Version

GENERAL DESCRIPTION

The ADuCM350 is a complete, coin cell powered, high precision, meter-on-chip for portable device applications for applications such as point-of-care diagnostics and body-worn devices for monitoring vital signs. The ADuCM350 is designed for high precision amperometric, voltametric, and impedometric measurement capabilities.

The ADuCM350 analog front end (AFE) features a 16-bit, precision, 160 kSPS analog-to-digital converter (ADC); 0.17% precision voltage reference; 12-bit, no missing codes digital-to-analog converter (DAC); and a reconfigurable ultralow leakage switch matrix. The ADuCM350 also includes an ARM® Cortex-M3-based processor, memory, and all I/O connectivity to support portable meters with display, USB communication, and active sensors. The ADuCM350 is available in a 120-lead, 8 mm × 8 mm CSP_BGA and operates from −40°C to +85°C.

To support extremely low dynamic and hibernate power management, the ADuCM350 provides a collection of power modes and features, such as dynamic and software controlled clock gating and power gating.

The AFE is connected to the ARM Cortex-M3 via an advanced high performance bus (AHB) slave interface on the advanced microcontroller bus architecture (AMBA) matrix, as well as direct memory access (DMA) and interrupt connections.

SPECIFICATIONS

All characterization is at VCCM = 2.5 V to 3.6 V, specifications below 2.5 V are for functionality only, all minimum and maximum specifications are specified for a temperature range of −40°C to +85°C, unless otherwise noted.

ANALOG FRONT-END SPECIFICATIONS

AFE LDO Specifications

Table 1. AFE LDO Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
VOLTAGE					
Output Voltage	1.71	1.8	1.89	V	Measured with a load capacitance (C_{LOAD}) = 0.47 µF; measured with 1 mA load current on AVDD_RX/TX; all AFE blocks powered down
Dropout		150	200	mV	10 mA load applied; no AFE blocks enabled
REGULATION					
Line		1080		µV/V	10 mA load applied
Load		0.65		mV/mA	10 mA load applied
POWER UP					
Power-Up Time		500		µs	Measured with a C_{LOAD} = 0.47 µF; current limit enabled

High Precision Internal Reference Specifications

Table 2. High Precision Internal Reference Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC V_{REF}					
Reference Voltage Initial Accuracy[1]	1.797	1.8	1.803	V	For a temperature range of 0°C to 50°C
	1.79	1.8	1.803	V	For a temperature range of −40°C to +85°C
Output Impedance			570	mΩ	LDO and reference enabled; all other AFE blocks disabled; reference loaded with 50 µA on VREF
Temperature Coefficient[2]	−52		+90	ppm/°C	For a temperature range of −40°C to +85°C, maximum value from −40°C to +25°C, and from +25°C to +85°C specified
	−45		+48	ppm/°C	For a temperature range of 0°C to 50°C, maximum value from −40°C to +25°C, and from 25°C to 85°C specified
VREF Thermal Hysteresis		50		ppm	
REF_EXCITE Switching Load	1.789	1.793	1.797	V	I_{LOAD} = 200 µA; internal ADC measurement
Line Regulation		50		µV/V	V_{CCM1} = 2.5 V, V_{CCM2} = 3.6 V; reference loaded with 300 µA
Short-Circuit Current to Ground		10		mA	Current limit off
DAC V_{REF}					
Reference Voltage	1.77	1.8	1.83	V	
VBIAS					
VBIAS Voltage	1.095	1.1	1.102	V	Measured with a C_{LOAD} = 0.47 µF; no current load

[1] Reference voltage is trimmed unloaded. Measured with C_{LOAD} = 4.7 µF. Measured at 25°C.
[2] Guaranteed by design and/or characterization.

DAC/RCF/PGA Specifications

Table 3. DAC/PGA/RCF Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
DAC					
Output Range	−600		+600	mV	As seen by sensor
Resolution			12	Bits	
Integral Nonlinearity (INL)		±0.85		LSB	Measured at an output of the excitation loop, using gain = 1 and default DAC clock (16 MHz ÷ 49 DAC clock speed)
Differential Nonlinearity (DNL)	−1		+1	LSB	Measured at an output of the excitation loop, using gain = 1 and default DAC clock (16 MHz ÷ 49 DAC clock speed)
Full-Scale Error					
Positive		±0.2		% FSR	PGA (gain = 1), measured at an output of the excitation loop, DAC code = 0xE00
		±1		% FSR	PGA (gain = 0.025), measured at an output of the excitation loop, DAC code = 0xE00
Negative		±0.2		% FSR	PGA (gain = 1), measured at an output of the excitation loop, DAC code = 0x200
		±1		% FSR	PGA (gain = 0.025), measured at an output of the excitation loop, DAC code = 0x200
Offset Error, Midscale		±1		mV	PGA (gain = 1 or gain = 0.025), measured at an output of the excitation loop across RCAL
Clocking Frequency	280.7	320	380.95	kHz	
PROGRAMMABLE GAIN AMPLIFIER (PGA)					
Gain from PGA in State 0		1			Covered by DAC full-scale error measured on an output of the excitation loop
Gain from PGA in State 1		0.025			Covered by DAC full-scale error measured on an output of the excitation loop
RECONSTRUCTION FILTER (RCF)					
3 dB Corner Frequency		50		kHz	

[1] There may be some system offsets and gain errors that can be calibrated at the system level to improve dc accuracy. Hence, the voltage swing at the output of the DAC is ±800 mV to guarantee ±600 mV swing on the sensor.

SWITCH MATRIX SPECIFICATIONS

Table 4. Switch Matrix Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
R_{ON}[1]					
Current Carrying Switches					
Dx, DR1, Tx, and TR2		40	50	Ω	
IVS		40	75	Ω	
Noncurrent Carrying Switches					
Px, Nx, and NR2	600		900	Ω	
PR1	600		950	Ω	
NL	260		350	Ω	
PL	210		260	Ω	
DC OFF LEAKAGE[2]					
T and N Switches		370		pA	Sum value of four T switches and four N switches
P Switches		340		pA	Sum value of four P switches
D Switches		350		pA	Sum value of four D switches

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DC ON LEAKAGE[2]					
T, N, and P Switches		530		pA	Sum value for 25 switches, including NL
D Switches		340		pA	Sum value for eight switches

[1] R_{ON} characterized with a voltage sweep from 0 V to VCCM. Production tested at 1.8 V.
[2] See Figure 38 as a reference. The AFE x pin is driven to 0.2 V.

TRANSIMPEDANCE AMPLIFIER SPECIFICATIONS

Table 5. Transimpedance Amplifier Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TRANSIMPEDANCE AMPLIFIER					
Maximum Current Sink/Source		±5		mA	Ensure an R_{TIA} selection to generate ±750 mV swing for optimal linearity performance
Short-Circuit Protection Functionality		10		mA	

ADC SPECIFICATIONS

Table 6. ADC Specifications[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADC					
Input Range	0.35		1.85	V	Internal reference
No Missing Codes		16		Bits	
DNL		±0.9		LSB	
INL		±0.7		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from 0°C to 50°C
		±1		LSB	@ 160 kSPS with respect to an optimal voltage range of ±750 mV, from −40°C to +85°C
Sample Rate After Decimation		160		kSPS	
3 dB Bandwidth		54		kHz	

[1] R_{TIA} = 7.5 kΩ, C_{TIA} = 220 pF; ±100 µA current measurement.

TEMPERATURE SENSOR SPECIFICATIONS

Table 7. Temperature Sensor Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
TEMPERATURE SENSOR					
Accuracy		±1		°C	0°C to 50°C, trimmed at 25°C
		±2		°C	−40°C to +85°C, trimmed at +25°C

CapTouch

Table 8. CapTouch Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CapTouch™ CHARACTERISTICS					
Core Resolution		14		Bits	
Core SNR	60			dB	1 kHz test tone, input range of ADC = 1.8 V
CAPT_x		±10		nA	GPIO leakage test
Update Rate	7.5		1E6	µs	Programmable, dependent on configuration
Update Rate per Sensor	7.5			µs	No filtering enabled, clock = 16 MHz
CAPT_x Input Range		±8		pF	ΔC_{IN} is register programmable from 0.5 pF to 9.3 pF
CAPT_x Offset (CapDAC) Range		75		pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CapDAC Resolution		0.1		pF	
Output Noise					
Peak-to-Peak		8		Codes	
RMS		1.3		Codes	

DFT-BASED IMPEDANCE MEASUREMENTS

Table 9. DFT-Based Impedance Measurements[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
IMPEDANCE					
Accuracy[2]					
Magnitude			0.33	%	Standard deviation as a percent of Z
Phase			0.17	Degrees	Standard deviation of Z
Precision[3]					
Magnitude			0.17	%	Standard deviation as a percent of Z
Phase			0.08	Degrees	Standard deviation of Z

[1] For a Z of 181 Ω (0.02% tolerant resistor). Excitation frequency = 20 kHz, sine amplitude = 9 mV_{RMS}, R_{CAL} = 1 kΩ, R_{TIA} = 7.5 kΩ, C_{TIA} = 220 pF. Measurements at 25°C. Single DFT measurement.
[2] Device-to-device repeatability for 1000 devices.
[3] Single device, repeatable measurements.

DIGITAL PLATFORM

Digital LDO

Table 10. Digital LDO Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE	1.71	1.8	1.89	V	Measured with a C_{LOAD} = 0.47 µF, measured with a 10 mA load current on DVDD
DROPOUT		150	200	mV	10 mA load applied, no AFE blocks enabled
REGULATION					
Line		1.4		mV/V	10 mA load current on DVDD
Load		0.41		mV/mA	0 mA to 10 mA load current
POWER-UP TIME		42		µs	Time taken from LDO enable to when LDO voltage is within specification, C_{LOAD} = 0.47 µF, regulator unloaded

Low Power LDO

Table 11. Low Power LDO Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
OUTPUT VOLTAGE	1.71	1.8	1.89	V	
REGULATION					
Line		0.45		mV/V	VCCM = 2.0 V to 3.6 V
Load		28.5		mV/mA	0 µA to 100 µA load

Flash/General-Purpose Flash

Table 12. Flash/General-Purpose Flash Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FLASH/GP FLASH					
Endurance[1]	20,000			Cycles	
Erase Time		20		ms	@ 1.8 V
Program Time		20		µs	@ 1.8 V
Data Retention[2]		100		Years	Below room temperature

[1] Endurance is qualified to 10,000 cycles as per JEDEC Std. 22 Method A117 and measured at −40°C, +25°C, and +125°C. Typical endurance at 25°C is 170,000 cycles.
[2] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Std. 22 Method A117. Retention lifetime derates with junction temperature.

Digital Inputs/Outputs: Specified

Specified pin supply range from 2.5 V to 3.6 V.

Table 13. Digital Inputs and Outputs[1] Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	2.5	3	3.6	V	
Impedance					
Pull-Down		20		kΩ	I_{SINK} < 10 µA
Pull-Up		15		kΩ	I_{SOURCE} < 10 µA
Internal Pull-Up/Pull-Down Enabled Leakage[2]		200		µA	
Digital I/O Leakage Current		.01	1	µA	
Input Capacitance		10		pF	
Input Voltage					
Low (V_{INL})			0.3 × pin supply	V	
High (V_{INH})	0.7 × pin supply			V	
Output Voltage					
Low (V_{OL})			0.4	V	I_{SINK} = 1.0 mA
V_{OL} High Drive		0.4		V	I_{SINK} = 1.6 mA
High (V_{OH})[3]	Pin supply − 0.4			V	I_{SOURCE} = 1.0 mA
V_{OH} High Drive		2.4		V	I_{SOURCE} = 1.6 mA

[1] Includes GPIO, debug, SPI, I²C, PDI, LCD, I²S, and beeper.
[2] See Table 35 for details regarding bumps/pins that have pull-up resistors.
[3] I²C does not drive out a high voltage; it uses external pull-up resistors.

Digital Inputs/Outputs: Functional

Functional pin supply range from 1.65 V to 2.5 V.

Table 14. Digital Inputs/Outputs: Functional Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
PIN SUPPLY	1.65		2.5	V	
Input Voltage					
Low (V_{INL})		0.3 × pin supply		V	
High (V_{INH})		0.7 × pin supply		V	
Output Voltage					
Low (V_{OL})		0.45		V	I_{SINK} = 1.0 mA
High (V_{OH})[1]		Pin supply − 0.5		V	I_{SOURCE} = 1.0 mA

[1] I²C does not drive out a high voltage; it uses external pull-up resistors.

Universal Serial Bus Regulator Specifications

Table 15. Universal Serial Bus Regulator Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SERIAL BUS REGULATOR					
Input Voltage Range	3.6		5.25	V	
Regulated Output Voltage	3.2		3.4	V	
Dropout		440		mV	40 mA continuous current
Regulation					
Line		0.0043		%/V	4.5 V to 5.5 V
Load		0.0093		%/mA	@ 5 V, 220 nF ceramic decoupling capacitor
Power-Up Time		37		µs	

Universal Serial Bus DC Specifications

Table 16. Universal Serial Bus DC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
RECEIVER					
Single-Ended Input Voltage (Driven)					
High	2.0			V	
Low			0.8	V	
Differential Receiver Input					
Common Mode	0.8		2.5	V	
Sensitivity	0.2			V	V(USB DP) – V(USB DM)
TRANSMITTER					
Output Voltage					
Low (V_{OL})	0		0.3	V	Pull-up resistor asserted on the USB pin, USB DP, R_{PU} to AVDD
High (V_{OH})	2.8		3.6	V	Pull-down resistor asserted on USB DP and USB DM (15 kΩ to GND)
Driver Output Impedance	28		44	Ω	R_{DRIVER} + R_{SERIES}
Term Series Resistor		40		Ω	
Pull-Up Resistor (D+ High)	1.425	1.5	3.095	kΩ	Termination voltage = USB regulator voltage
Pull-Up Resistor (D+ Low)	0.9		1.575	kΩ	Termination voltage = USB regulator voltage
Pull-Down Resistors	14.25	15	24.8	kΩ	

Universal Serial Bus AC Specifications

Meeting USB 2.0 compliance electrical tests.

Table 17. Universal Serial Bus AC Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FULL SPEED DRIVER TIMING					C_{LOAD} = 50 pF
Signaling Rate	11.988	12		MHz	
Output Time					
Rise	4		20	ns	V_{OH} – V_{OL} (10% to 90%), C_{LOAD} = 50 pF
Fall	4		20	ns	V_{OH} – V_{OL} (10% to 90%), C_{LOAD} = 50 pF
Rise and Fall Matching	90		111.1	%	Exclude transition from idle
Output Voltage Crossover	1.3		2.0	V	Exclude transition from idle
FULL SPEED JITTER					C_{LOAD} = 50 pF
Driver Jitter Generated	−2		+2	ns	Next transitions
	−1		+1	ns	Paired transitions
Load Capacitance			50	pF	Testing slew rate

LCD, Charge Pump

Table 18. LCD, Charge Pump Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CAPACITANCE					
Reservoir Capacitance Between VLCDVDD and VLCD_GND	0.47	1		µF	
Flying Capacitance	2.2		4.7	nF	Between VLCD FLY1 and VLCD FLY2
VLCD					
Switching Voltage					
VLCD FLY1	−0.7		VLCD + 0.2	V	Top of flying capacitor
VLCD FLY2	0		VCCM	V	Bottom of flying capacitor
VLCD Charge Pump Switching Frequency		32		kHz	
Minimum VLCD with Respect to VCCM_ANA and VCCM_DIG	2.1			V	When <2.1 V after 62.5 ms elapses indicates fault condition
VLCDVDD					
VLCDVDD Voltage Range	2.4		3.65	V	5-bit programmable in steps of 40 mV
VLCDVDD Pin Leakage		3		nA	To VCCM
		0.2		nA	To GND
VLCDVDD Start-Up Time		5		ms	VLCDVDD = 0 V to 3.6 V, reservoir = 1 µF, flying capacitor = 2.2 nF (minimum) and 4.7 nF (maximum)
VLCDVDD Line Regulation		0.32		%	
V_LCD_xx VOLTAGE RANGE					
V_LCD_13 Voltage Range	VLCD ÷ 3 − 10		VLCD ÷ 3 + 10	mV	
V_LCD_23 Voltage Range	2/3 VLCD − 13		2/3 VLCD + 13	mV	
COMx PINS					
DC Voltage Across Segment and COMx Pins			50	mV	
PIN OUTPUT IMPEDANCE					
Segment		2000		Ω	
Common		130		Ω	

SYSTEM CLOCKS/TIMERS

The following tables document the system clock specifications in the ADuCM350.

Platform External Crystal Oscillator

Table 19. Platform External Crystal Oscillator Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOW FREQUENCY					
$C_{EXT}1 = C_{EXT}2$	12	15	18	pF	External capacitor, C1 = C2 (symmetrical load)
Frequency		32,768		Hz	
HIGH FREQUENCY					
$C_{EXT}1 = C_{EXT}2$	10	12	15	pF	External capacitor
Frequency		8 or 16		MHz	

On-Chip RC Oscillators

Table 20. On-Chip RC Oscillators Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
HIGH FREQUENCY RC OSCILLATOR					
Frequency		16		MHz	
Accuracy	−5		+5	%	
Start-Up Time		35		µs	
LOW FREQUENCY RC OSCILLATOR					
Frequency		32,768		Hz	
Accuracy	−20		+20	%	
Start-Up Time		980		µs	

PLLs

Table 21. PLL Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM PLL					
Input Frequency	8	16		MHz	
Output Frequency		16	32	MHz	
Frequency Error			2500	ppm	
RMS Jitter			92	ps	@ 32 MHz, external XTAL
USB PLL					
Input Frequency	8	16		MHz	
Output Frequency	16		60	MHz	16 MHz input
Frequency Error			2500	ppm	
Period Jitter			68	ps	@ 60 MHz, external XTAL

Watchdog, Wake-Up, and General-Purpose Timers

Table 22. Watchdog, Wake-Up, and General-Purpose Timers Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
WATCHDOG TIMERS					
Timeout Period					
Shortest		0.03		ms	32,768 Hz clock, prescaler = 1
Longest		8191		sec	32,768 Hz clock, prescaler = 4096
WAKE-UP TIMERS					
Timeout Period					
Shortest		62.5		ns	16 MHz clock, prescaler = 1
Longest		136		Years	32,768 Hz clock, prescaler = 32,768
GENERAL-PURPOSE TIMER × 3					
Timeout Period					
Shortest		62.5		ns	16 MHz clock, prescaler = 1
Longest		65,535		sec	32,768 Hz clock, prescaler = 32,768
Timer Output PWM Frequency	1		16	MHz	

[1] Guaranteed by design.

POWER MANAGEMENT SPECIFICATIONS

The following tables cover the specifications for the power management section of the ADuCM350.

Power Supplies

Table 23. Power Supplies Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLIES					
VCCM_ANA/VCCM_DIG	2		3.6	V	VCCM_x pins connected to the CR2032 battery, main supply for ADuCM350
VCCM_ANA/VCCM_DIG	2.5		3.6	V	Battery operating range
VBACK	1.62		3.6	V	Super capacitor pin, back-up mode supply
VBUS	4.75	5	5.25	V	USB 5 V supply
VDD_IO	1.8		3.6	V	Supply for some digital I/O pads; see Table 35, I/O supply column for details
VLCDVDD	1.8		3.6	V	Supply for LCD I/O

Power Supply Monitoring

Table 24. Power Supply Monitoring Specifications

Parameter[1]	Min	Typ	Max	Unit	Test Conditions/Comments
VCCM PSM					
Voltage Detection Range	1.7		3.2	V	100 mV step size
Hysteresis	±10		±100	mV	
Trip Point Detection Accuracy			Hysteresis + 70	mV	
VRTC PSM					
Voltage Detection Range	1.55		1.7	V	100 mV step size
Hysteresis	±25		±100	mV	
Trip Point Detection Accuracy			Hysteresis + 70	mV	
VBACK PSM					
Voltage Detection Range	1.7		3.2	V	100 mV step size
Hysteresis			±100	mV	
Trip Point Detection Accuracy			Hysteresis + 70	mV	

[1] For details regarding these parameters, see the UG-587 hardware reference manual.

TRICKLE CHARGER

Table 25. Trickle Charger Specifications

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CURRENT					
Charge Current		0.48		mA	Limits load on button cell at power-up
Reverse Current			1	µA	
VOLTAGE					
Forward Voltage		40	120	mV	Where forward current reduces to zero

TIMING CHARACTERISTICS

LCD Segment/Common Timing Specifications

Table 26. LCD Segment/Common Timing Specifications[1, 2]

				Static Mux		4× Mux	
FRAMESEL[3]	FRAMESEL[2]	FRAMESEL[1]	FRAMESEL[0]	f_{LCD} (Hz)	Frame Rate (Hz)	f_{LCD} (Hz)	Frame Rate (Hz)
0	0	0	0	256	128	1024	128
0	0	0	1	204.8	102.4	819.2	102.4
0	0	1	0	170.7	85.3	682.7	85.3
0	0	1	1	146.3	73.1	585.1	73.1
0	1	0	0	128	64	512	64
0	1	0	1	113.8	56.9	455.1	56.9
0	1	1	0	102.4	51.2	409.6	51.2
0	1	1	1	93.1	46.5	372.4	46.5
1	0	0	0	85.3	42.7	341.3	42.7
1	0	0	1	78.8	39.4	315.1	39.4
1	0	1	0	73.1	36.6	292.6	36.6
1	0	1	1	68.3	34.1	273.1	34.1
1	1	0	0	64	32	256	32
1	1	0	1	60.2	30.1	240.9	30.1
1	1	1	0	56.9	28.4	227.6	28.4
1	1	1	1	53.9	26.9	215.6	26.9

[1] $f_{LCD} = f_{BCLK}/(FRAMESEL + 4)$. See the UG-587 hardware reference manual for details
[2] FRAMESEL[3], FRAMESEL[2], FRAMESEL[1], and FRAMESEL[0] indicate the bit numbers in the LCD_COM register.

I²C Timing

Capacitive load for each of the I²C bus lines (C_B) = 400 pF maximum as per I²C bus specifications; I²C timing is guaranteed by design and not production tested.

Table 27. I²C Timing in Fast Mode (400 kHz)

Parameter	Description	Min	Max	Unit
t_L	Clock low pulse width	1300		ns
t_H	Clock high pulse width	600		ns
t_{SHD}	Start condition hold time	600		ns
t_{DSU}	Data setup time	100		ns
t_{DHD}[1]	Data hold time	0		ns
t_{RSU}	Setup time for repeated start	600		ns
t_{PSU}	Stop condition setup time	600		ns
t_{BUF}	Bus-free time between a stop condition and a start condition	1.3		µs
t_R	Rise time for both clock and data	20 + 0.1 Cb	300	ns
t_F	Fall time for both clock and data	20 + 0.1 Cb	300	ns
t_{SUP}	Pulse width of spike suppressed	0	50	ns

[1] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{INH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Table 28. I²C Timing in Standard Mode (100 kHz)

Parameter	Description	Min	Max	Unit
t_L	Clock low pulse width	4.7		µs
t_H	Clock high pulse width	4.0		ns
t_{SHD}	Start condition hold time	4.7		µs
t_{DSU}	Data setup time	250		ns
t_{DHD}[1]	Data hold time	0		µs
t_{RSU}	Setup time for repeated start	4.0		µs

Parameter	Description	Min	Max	Unit
t_{PSU}	Stop condition setup time	4.0		µs
t_{BUF}	Bus-free time between a stop condition and a start condition	4.7		µs
t_R	Rise time for both clock and data		1	µs
t_F	Fall time for both clock and data		300	ns

[1] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the V_{INH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.

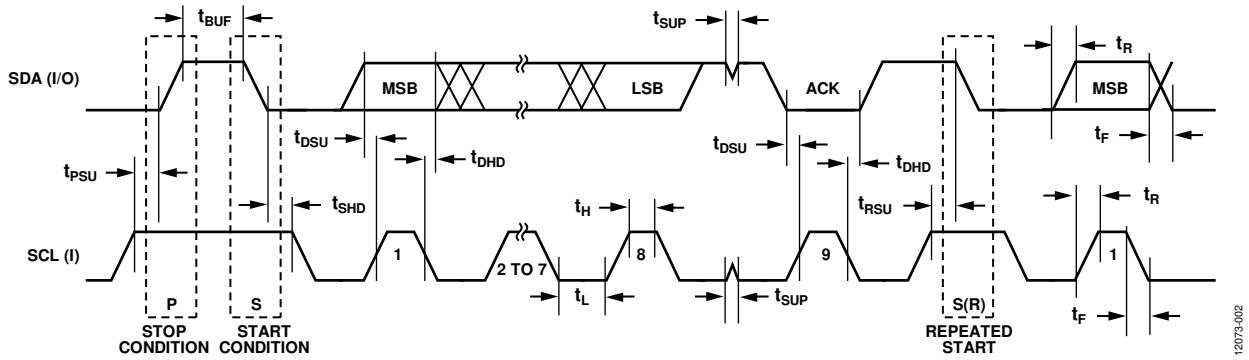

Figure 2. I²C-Compatible Interface Timing

I²S Timing Specifications

I²S timing is guaranteed by design and not production tested; timing specifications are given for a standard I²S data rate of 2.5 MHz; the I²S bus is designed to operate up to 25 MHz.

Table 29. I²S Timing: Master Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
I²S MASTER TRANSMITTER TIMING						
SCLK Period	T	360	400	440	ns	
Minimum Clock Period	T_{TR}	360			ns	T_{TR} is the minimum allowed clock period for the transmitter, $T > T_{TR}$
Clock High Period	t_{HC}	160			ns	Minimum > 0.35 × T = 140 ns
Clock Low Period	t_{LC}	160			ns	Minimum > 0.35 × T = 140 ns
Delay	t_{DTR}			300	ns	Minimum < 0.80 × T = 320 ns
Data Hold Time	t_{HTR}	100			ns	Minimum > 0 ns
Clock Rise Time	t_{RC}			60	ns	Minimum > 0.15 × T_{TR} = 54 ns (slave mode only)

[1] T refers to the typical value listed for the SCLK period; therefore, T = 400 ns in this case.

Table 30. I²S Timing: Slave Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments[1]
I²S SLAVE RECEIVER TIMING						
SCLK Period	T	360	400	440	ns	T_{TR} = 360 ns
Clock High Period	t_{HC}	110			ns	Minimum < 0.35 × T = 126 ns
Clock Low Period	t_{LC}	160			ns	Minimum < 0.35 × T = 126 ns
Data Setup Time	t_{SR}			300	ns	Minimum < 0.20 × T = 72 ns
Data Hold Time	t_{HTR}	100			ns	Minimum < 0 ns

[1] T refers to the typical value listed for the SCLK period; therefore, T = 400 ns in this case.

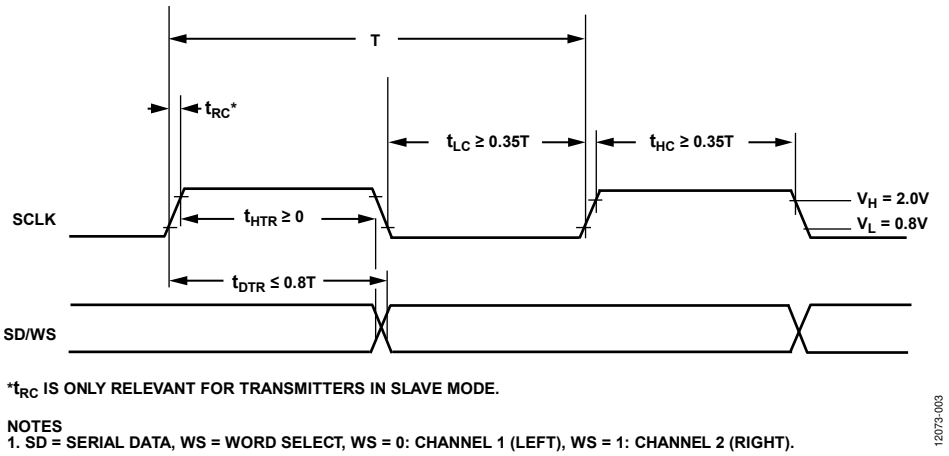

Figure 3. I²S-Compatible Interface Transmitter Timing

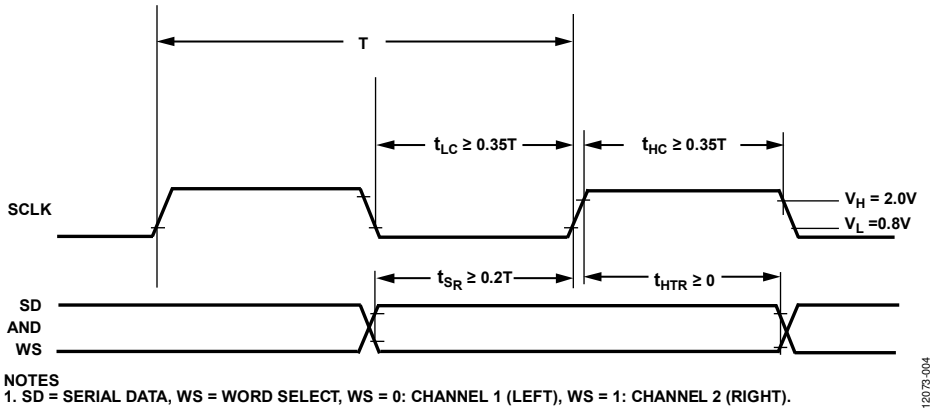

Figure 4. I²S-Compatible Interface Receiver Timing

SPI Timing

SPIH can be used for high data rate peripherals.

Table 31. SPI Master Mode Timing[1]

Parameter	Description	Min	Typ	Max	Unit
t_{SL}	SCLK low pulse width[2]		(SPIXDIV[5:0] + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[2]		(SPIXDIV[5:0] + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge		0	35.5	ns
t_{DOSU}	Data output setup before SCLK edge[2]	(SPIDIV + 1) × t_{UCLK}			ns
t_{DSU}	Data input setup time before SCLK edge	58.7			ns
t_{DHD}	Data input hold time after SCLK edge	16			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns

[1] Guaranteed by design.
[2] t_{UCLK} = 62.5 ns. It corresponds to the maximum internal clock frequency before clock dividers.

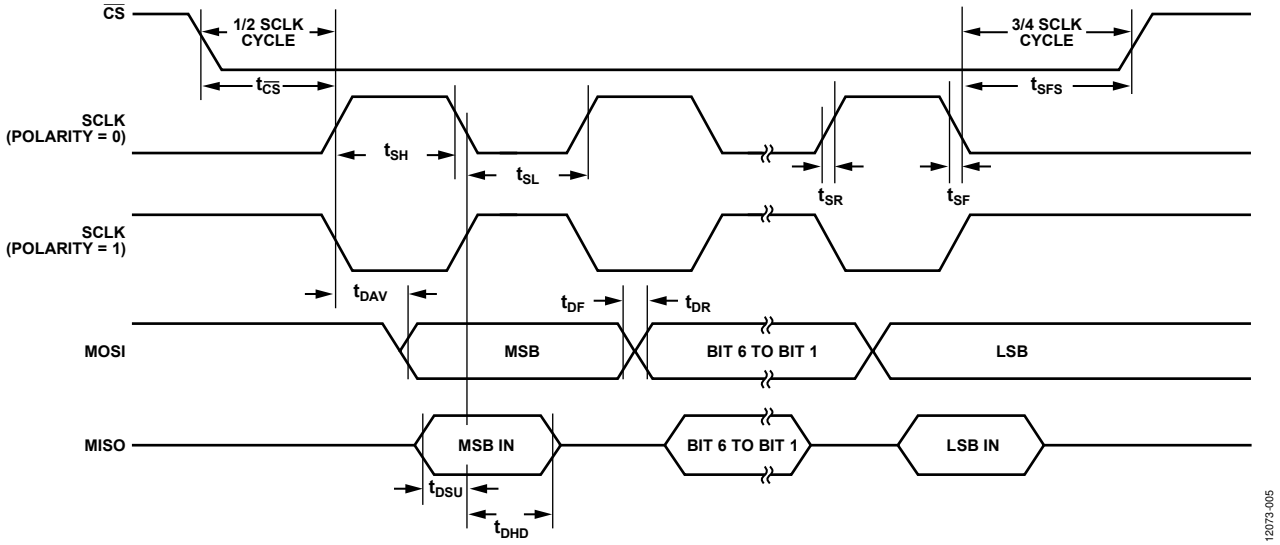

Figure 5. SPI Master Mode Timing (Phase Mode = 1)

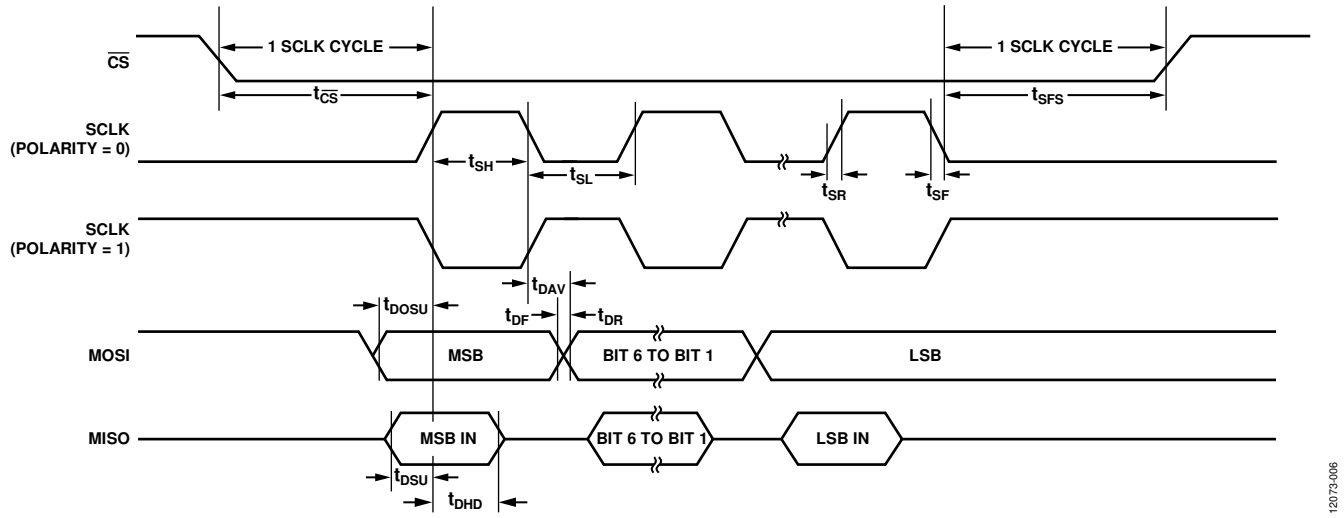

Figure 6. SPI Master Mode Timing (Phase Mode = 0)

Table 32. SPI Slave Mode Timing

Parameter	Description	Min	Typ	Max	Unit
$t_{\overline{CS}}$	$\overline{CS}$ to SCLK edge	38			ns
t_{SL}	SCLK low pulse width[1]		(SPIXDIV[5:0] + 1) × t_{UCLK}		ns
t_{SH}	SCLK high pulse width[1]	62.5	(SPIDIV[5:0] + 1) × t_{UCLK}		ns
t_{DAV}	Data output valid after SCLK edge			49.1	ns
t_{DSU}	Data input setup time before SCLK edge	20.2			ns
t_{DHD}	Data input hold time after SCLK edge	10.1			ns
t_{DF}	Data output fall time		12	35.5	ns
t_{DR}	Data output rise time		12	35.5	ns
t_{SR}	SCLK rise time		12	35.5	ns
t_{SF}	SCLK fall time		12	35.5	ns
t_{DOCS}	Data output valid after $\overline{CS}$ edge			25	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	0			ns

[1] t_{UCLK} = 62.5 ns. It corresponds to the maximum internal clock frequency before clock dividers.

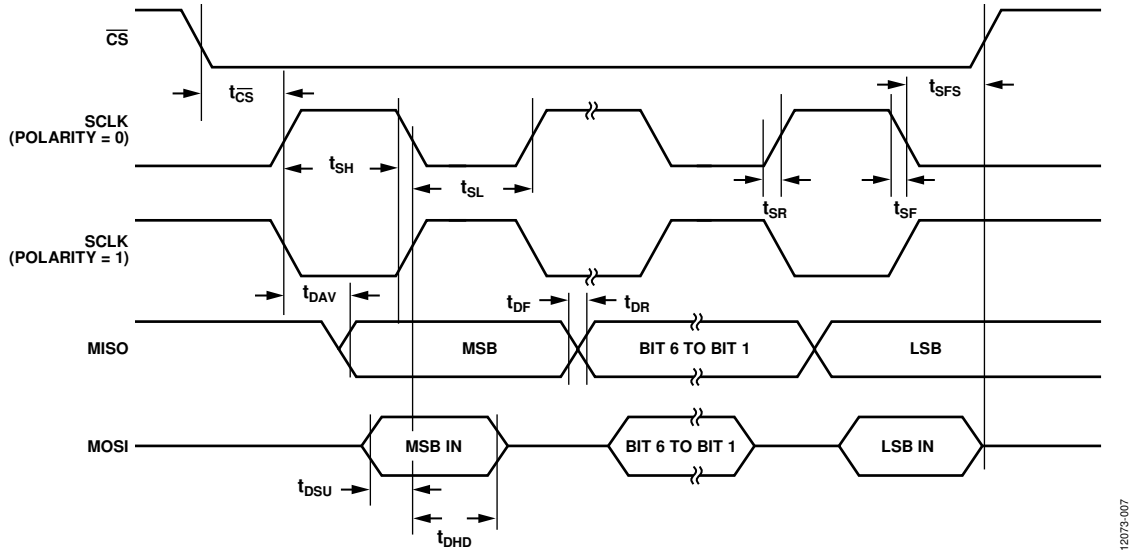

Figure 7. SPI Slave Mode Timing (Phase Mode = 1)

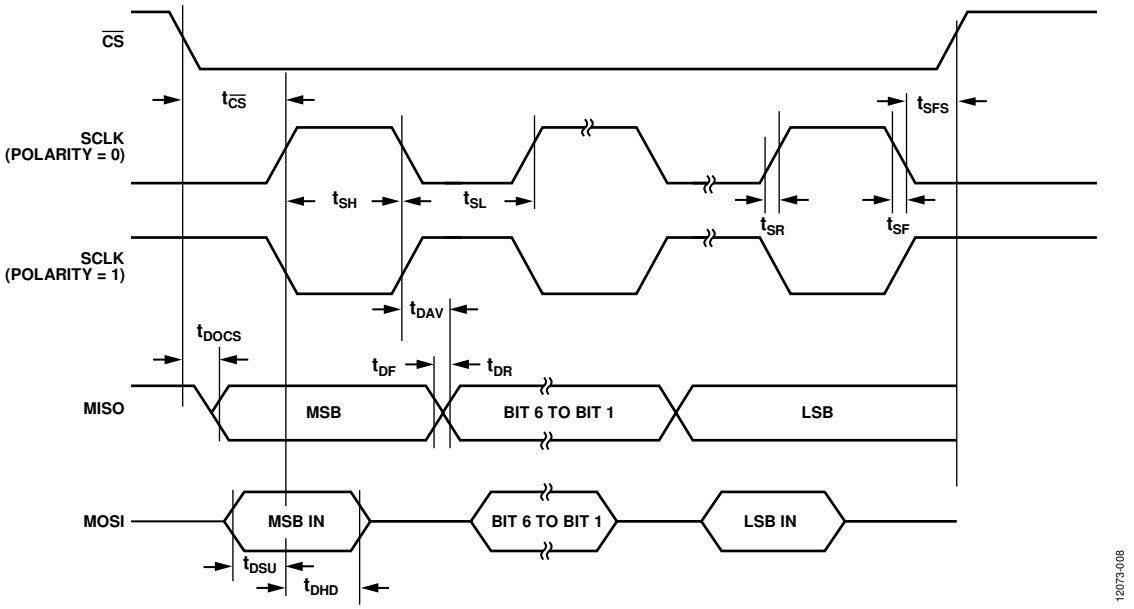

Figure 8. SPI Slave Mode Timing (Phase Mode = 0)

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 33.

Parameter	Rating
Supplies	
VCCM_ANA, VCCM_DIG, VLCDVDD, VDD_IO, VBACK to AGND_x/DGNDx	−0.3 V to +3.6 V
Decoupling	
DVDD, AVDD_RX/TX, VBIAS, VREF, VUSB	−0.3 V to +2.0 V
Digital Input/Output	
P0.x, P1.x, P2.x, P3.x, P4.x, BOOT, RESETX	−0.3 V to +3.6 V
TRACEx	−0.3 V to +3.6 V
Switch Matrix (RCAL 1, RCAL 2, AFE x)	−0.3 V to +3.6 V
TIA (TIA_I, TIA_O)	−0.3 V to +3.6 V
Analog Inputs (AN_x)	−0.3 V to +3.6 V
REF_EXCITE	−0.3 V to +1.98 V
VLCD FLY1, VLCD FLY2	−0.3 V to +3.6 V
V_LCD_13, V_LCD_23	−0.3 V to +3.6 V
VBUS to DGND	−0.3 V to +5.25 V
USB DM, USB DP to DGND	−0.3 V to +3.6 V
HF_XTALx, LF_XTALx	−0.3 V to +1.98 V
Analog Ground to Digital Ground	
AGND CTOUCH, AGND_RX/TX, AGND_REF to DGND, DGND1, DGND2, DGND USB	−0.3 V to +0.3 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages; assumes use of a JEDEC 4-layer board.

Table 34. Thermal Resistance

Package Type	θ_{JA}	Unit
CSP_BGA	35	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A	DNC	P2.1/ COM1/ RESX	P2.3/ COM3/ DCX	P2.5/S2/ ECLOCK-WRX	P1.0/S3/ D0/SCL	P1.2/S5/ D2/DIN	P1.4/S7/ D4	P1.6/S9/ D6	P1.8/S11/ D8	P1.10/ S13/D10	P1.12/ S15/D12	P1.14/ S17/D14	P2.10/S23	P2.9/S22	P2.15/S28
B	V_LCD_23	P2.0/ COM0	P2.2/ COM2/ CSX	P2.4/S1/ RWX-RDX	P1.1/S4/ D1/DOUT	P1.3/S6/ D3	P1.5/S8/ D5	P1.7/S10/ D7	P1.9/S12/ D9	P1.11/ S14/D11	P1.13/ S16/D13	P1.15/ S18/D15	P2.11/S24	P2.12/S25	P2.8/S21
C	HF_XTAL2	V_LCD_13												P3.10/S31	P2.7/S20/ TOUTA
D	HF_XTAL1	VLCDVDD												P2.13/S26	P2.6/ S19/TE
E	VUSB	VLCD FLY1												P3.11/S32	P2.14/S27
F	USB DM	VLCD FLY2				DGND USB	DGND2/ LCD_GND	P3.8/S29	P3.9/S30	P3.3/ SPI0_CS				P3.0/ SPI0_SCLK	P3.2/ SPI0_MOSI
G	USB DP	VBUS				DGND1				P3.4/ I2CSCL/ SPI1_SCLK				P3.1/ SPI0_MISO	P3.6/UTX/ TOUTB/ SPI1_MOSI
H	TMS-SWDIO/ P0.8	TCK-SWCLK/ P0.9				VCCM_ DIG				P3.5/ I2CSD/ SPI1_MISO				DGND	VDD_IO
J	TDO-SWO/ P0.6/UTX	TDI/P0.7/ URX				P3.14/ LRCLK				P3.7/URX/ TOUTC/ SPI1_CS				P0.4/ CAPT_E	P0.1/ CAPT_B
K	DVDD	P0.11				P3.12/ BEEP/ BMCLK	P3.13/ BEEPX/ SDATA	RESETX	AGND_RX/ AGND_TX	AGND_REF				P0.3/ CAPT_D	P0.0/ CAPT_A
L	P4.0/ I2CSCL	P4.1/ I2CSD												P0.5/ CAPT_F	P0.2/ CAPT_C
M	VBACK	P0.15/ SPIH_CS												TRACE0	TRACECLK
N	LF_XTAL2	BOOT												TRACE2	TRACE1
P	LF_XTAL1	P0.13/ SPIH_MISO	P0.14/ SPIH_MOSI	VCCM_ ANA	RCAL 1	AFE 2	AFE 4	AFE 6	AFE 8	VBIAS	TIA_I	AN_A	AN_B	AGND CTOUCH	TRACE3
R	P4.2/ TOUTB	P0.10/ TOUTC	P0.12/ SPIH_SCLK	AVDD_RX/ AVDD_TX	RCAL 2	AFE 1	AFE 3	AFE 5	AFE 7	VREF	TIA_O	REF_ EXCITE	AN_C	AN_D	TRST

12073-009

Figure 9. Bump Location (Top View Looking Through Device, Bumps Not to Scale)

Table 35. Pin Function Descriptions

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
Power and Ground					
P4	VCCM_ANA	S	VCCM_ANA	N/A	Battery Connection and Analog Circuit Power. Connect VCCM_ANA to the CR2032 battery. VCCM_ANA powers the analog circuits. This pin is connected to VCCM_DIG internally.
H6	VCCM_DIG	S	VCCM_DIG	N/A	Battery Connection and Digital Circuit Power. Connect VCCM_DIG to the CR2032 battery. VCCM_DIG powers the digital circuits. This pin is connected to VCCM_ANA internally.
G2	VBUS	S	VBUS	N/A	5 V USB Supply Voltage.
M1	VBACK	S	VBACK	N/A	RTC Supply. Connect VBACK to the super capacitor.
H15	VDD_IO	S	VDD_IO	N/A	VDD_IO Supply.
E1	VUSB	A	VUSB	N/A	Regulated USB 3.6 V Supply.
R10	VREF	A	N/A	N/A	1.8 V Reference Voltage Decoupling Capacitor Pin.
P10	VBIAS	A	N/A	N/A	1.1 V Bias Voltage Decoupling Capacitor Pin.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
K1	DVDD	A	N/A	N/A	1.8 V Digital Regulator Decoupling Capacitor Pin.
R4	AVDD_RX/AVDD_TX	A	AVDD TX/RX	N/A	1.8 V Analog Regulator Decoupling Capacitor Pin for Receiver (Rx)/Transmitter (Tx) Circuits.
K9	AGND_RX/AGND_TX	G	N/A	N/A	Rx/Tx Analog Ground.
K10	AGND_REF	G	N/A	N/A	Reference Ground.
H14	DGND	G	N/A	N/A	Digital Ground.
G6	DGND1	G	N/A	N/A	Digital Ground.
F7	DGND2/LCD_GND	G	N/A	N/A	Digital Ground/Ground for LCD.
F6	DGND USB	G	N/A	N/A	USB Ground. Connect DGND USB to the digital ground plane.
AFE Pins					
P12	AN_A	A	VCCM_ANA	N/A	ADC Mux Input.
P13	AN_B	A	VCCM_ANA	N/A	ADC Mux Input.
R13	AN_C	A	VCCM_ANA	N/A	ADC Mux Input.
R14	AN_D	A	VCCM_ANA	N/A	ADC Mux Input.
P5	RCAL 1	A	VCCM_ANA	N/A	Terminal A of Calibration Resistor. Connect RCAL 1 to the switch matrix.
R5	RCAL 2	A	VCCM_ANA	N/A	Terminal B of Calibration Resistor. Connect RCAL 2 to the switch matrix.
R6	AFE 1	A	VCCM_ANA	N/A	Uncommitted AFE Pin 1.
P6	AFE 2	A	VCCM_ANA	N/A	Uncommitted AFE Pin 2.
R7	AFE 3	A	VCCM_ANA	N/A	Uncommitted AFE Pin 3.
P7	AFE 4	A	VCCM_ANA	N/A	Uncommitted AFE Pin 4.
R8	AFE 5	A	VCCM_ANA	N/A	Uncommitted AFE Pin 5.
P8	AFE 6	A	VCCM_ANA	N/A	Uncommitted AFE Pin 6.
R9	AFE 7	A	VCCM_ANA	N/A	Uncommitted AFE Pin 7.
P9	AFE 8	A	VCCM_ANA	N/A	Uncommitted AFE Pin 8.
P11	TIA_I	A	VCCM_ANA	N/A	Transimpedance Amplifier Input. Connect the IV resistor to this pin.
R11	TIA_O	A	VCCM_ANA	N/A	Transimpedance Amplifier Output. Connect the IV resistor to this pin.
R12	REF_EXCITE	A	VCCM_ANA	N/A	Gated Precision Reference Voltage.
Debug Interface					
J1	TDO-SWO/P0.6/UTX	I/O	VCCM_DIG	Pull-up	JTAG Serial Data Output or Serial Wire Trace Output/GPIO/UART_TX. This is a multifunction pin.
J2	TDI/P0.7/URX	I/O	VCCM_DIG	Pull-up	JTAG Serial Data Input/GPIO/UART_RX. This is a multifunction pin.
H1	TMS-SWDIO/P0.8	I/O	VCCM_DIG	Pull-up	JTAG Test Mode Select or Serial Wire Data/GPIO. This is a multifunction pin.
H2	TCK-SWCLK/P0.9	I/O	VCCM_DIG	Pull-down	JTAG Test Clock or Serial Wire Clock/GPIO. This is a multifunction pin.
R15	TRST	I	VCCM	N/A	Trace Reset.
M15	TRACECLK	O	VCCM	N/A	Trace Clock.
M14	TRACE0	O	VCCM	N/A	Trace Data 0.
N15	TRACE1	O	VCCM	N/A	Trace Data 1.
N14	TRACE2	O	VCCM	N/A	Trace Data 2.
P15	TRACE3	O	VCCM	N/A	Trace Data 3.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
SPI H					
R3	P0.12/SPIH_SCLK	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H Clock. This is a dual function pin.
P2	P0.13/SPIH_MISO	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H MISO. This is a dual function pin.
P3	P0.14/SPIH_MOSI	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H MOSI. This is a dual function pin.
M2	P0.15/SPIH_CS	I/O	VCCM_DIG	Pull-up	GPIO/Serial Port H Chip Select (Active Low). This is a dual function pin.
Other Serial Ports					
F14	P3.0/SPI0_SCLK	I/O	VDD_IO	Pull-up	GPIO/SPI 0 SCLK. This is a dual function pin.
G14	P3.1/SPI0_MISO	I/O	VDD_IO	Pull-up	GPIO/SPI 0 MISO. This is a dual function pin.
F15	P3.2/SPI0_MOSI	I/O	VDD_IO	Pull-up	GPIO/SPI 0 MOSI. This is a dual function pin.
F10	P3.3/SPI0_CS	I/O	VDD_IO	Pull-up	GPIO/SPI 0 Chip Select (Active Low). This is a dual function pin.
G10	P3.4/I2CSCL/SPI1_SCLK	I/O	VDD_IO	Pull-up	GPIO (External Interrupt 7)/I^2C Clock/SPI 1 SCLK. This is a multifunction pin.
H10	P3.5/I2CSD/SPI1_MISO	I/O	VDD_IO	Pull-up	GPIO/I2C Data/SPI 1 MISO. This is a multifunction pin.
G15	P3.6/UTX/TOUTB/SPI1_MOSI	I/O	VDD_IO	Pull-up	GPIO/UART Tx/Timer B Output/SPI 1 MOSI. This is a multifunction pin.
J10	P3.7/URX/TOUTC/SPI1_CS	I/O	VDD_IO	Pull-up	GPIO/UART Rx/Timer C Output/SPI 1 Chip Select (Active Low). This is a multifunction pin.
USB					
F1	USB DM	I/O	VCCM_DIG	N/A	USB Data −.
G1	USB DP	I/O	VCCM_DIG	N/A	USB Data +.
CapTouch Interface					
K15	P0.0/CAPT_A	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 1)/CapTouch A. This is a dual function pin.
J15	P0.1/CAPT_B	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 2)/CapTouch B. This is a dual function pin.
L15	P0.2/CAPT_C	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 3)/CapTouch C. This is a dual function pin.
K14	P0.3/CAPT_D	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 4)/CapTouch D. This is a dual function pin.
J14	P0.4/CAPT_E	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 5)/CapTouch E. This is a dual function pin.
L14	P0.5/CAPT_F	A	VCCM_DIG	Pull-up	GPIO (External Interrupt 6)/CapTouch F. This is a dual function pin.
P14	AGND CTOUCH	G	N/A	N/A	Capacitance to Digital Converter AC Shield.
System Clocks					
P1	LF_XTAL1	A	RTC_VBACK	N/A	32 kHz XTAL Pin.
N1	LF_XTAL2	A	RTC_VBACK	N/A	32 kHz XTAL Pin.
D1	HF_XTAL1	A	DVDD	N/A	16 MHz XTAL Pin.
C1	HF_XTAL2	A	DVDD	N/A	16 MHz XTAL Pin.
Display					
E2	VLCD FLY1	A	VLCD VDD	N/A	LCD Flying Capacitor Top Plate.
F2	VLCD FLY2	A	VLCD VDD	N/A	LCD Flying Capacitor Bottom Plate.
D2	VLCDVDD	S	N/A	N/A	Full-Scale LCD Voltage Output or VLCD Supply.
C2	V_LCD_13	A	VLCD VDD	N/A	One-Third (1/3) LCD Voltage. Leave this pin as no connect.
B1	V_LCD_23	A	VLCD VDD	N/A	Two-Thirds (2/3) LCD Voltage. Leave this pin as no connect.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
B2	P2.0/COM0	I/O	VLCD VDD	Pull-up	GPIO/Common Output 0 for LCD Back Plane (COM 0). This is a dual function pin.
A2	P2.1/COM1/RESX	I/O	VLCD VDD	Pull-up	GPIO/COM 1/Parallel Display Interface (PDI) Reset. This is a multifunction pin.
B3	P2.2/COM2/CSX	I/O	VLCD VDD	Pull-up	GPIO/COM 2/PDI Chip Select. This is a multifunction pin.
A3	P2.3/COM3/DCX	I/O	VLCD VDD	Pull-up	GPIO/COM 3/PDI Data Select. This is a multifunction pin.
B4	P2.4/S1/RWX-RDX	I/O	VLCD VDD	Pull-up	GPIO/Segment Driver 1 (SEG 1)/PDI R/WX or RDX. This is a multifunction pin.
A4	P2.5/S2/ECLOCK-WRX	I/O	VLCD VDD	Pull-up	GPIO/SEG 2/PDI E Clock Output (Motorola Bus Mode) or PD Write Select (Intel® Bus Mode). This is a multifunction pin.
A5	P1.0/S3/D0/SCL	I/O	VLCD VDD	Pull-down	GPIO/SEG 3/PDI D0/PDI Serial Port Clock. This is a multifunction pin.
B5	P1.1/S4/D1/DOUT	I/O	VLCD VDD	Pull-down	GPIO/SEG 4/PDI D1/PDI Serial Port Data Output. This is a multifunction pin.
A6	P1.2/S5/D2/DIN	I/O	VLCD VDD	Pull-down	GPIO/SEG 5/PDI D2/PDI Serial Port Data Input. This is a multifunction pin.
B6	P1.3/S6/D3	I/O	VLCD VDD	Pull-down	GPIO/SEG 6/PDI D3. This is a multifunction pin.
A7	P1.4/S7/D4	I/O	VLCD VDD	Pull-down	GPIO/SEG 7/PDI D4. This is a multifunction pin.
B7	P1.5/S8/D5	I/O	VLCD VDD	Pull-down	GPIO/SEG 8/PDI D5. This is a multifunction pin.
A8	P1.6/S9/D6	I/O	VLCD VDD	Pull-down	GPIO/SEG 9/PDI D6. This is a multifunction pin.
B8	P1.7/S10/D7	I/O	VLCD VDD	Pull-down	GPIO/SEG 10/PDI D7/System Clock Output. This is a multifunction pin.
A9	P1.8/S11/D8	I/O	VLCD VDD	Pull-down	GPIO/SEG 11/PDI D8. This is a multifunction pin.
B9	P1.9/S12/D9	I/O	VLCD VDD	Pull-down	GPIO/SEG 12/ PDI D9. This is a multifunction pin.
A10	P1.10/S13/D10	I/O	VLCD VDD	Pull-down	GPIO/SEG 13/PDI D10. This is a multifunction pin.
B10	P1.11/S14/D11	I/O	VLCD VDD	Pull-down	GPIO/SEG 14/PDI D11. This is a multifunction pin.
A11	P1.12/S15/D12	I/O	VLCD VDD	Pull-down	GPIO/SEG 15/PDI D12. This is a multifunction pin.
B11	P1.13/S16/D13	I/O	VLCD VDD	Pull-down	GPIO/SEG 16/PDI D13. This is a multifunction pin.
A12	P1.14/S17/D14	I/O	VLCD VDD	Pull-down	GPIO/SEG 17/PDI D14. This is a multifunction pin.
B12	P1.15/S18/D15	I/O	VLCD VDD	Pull-down	GPIO/SEG 18/PDI D15. This is a multifunction pin.
D15	P2.6/S19/TE	I/O	VLCD VDD	Pull-down	GPIO/SEG 19/TE. This is a multifunction pin.
C15	P2.7/S20/TOUTA	I/O	VLCD VDD	Pull-down	GPIO/SEG 20/Timer A Output. This is a multi-function pin.
B15	P2.8/S21	I/O	VLCD VDD	Pull-down	GPIO/SEG 21. This is a dual function pin.
A14	P2.9/S22	I/O	VLCD VDD	Pull-down	GPIO/SEG 22. This is a dual function pin.
A13	P2.10/S23	I/O	VLCD VDD	Pull-down	GPIO/SEG 23. This is a dual function pin.
B13	P2.11/S24	I/O	VLCD VDD	Pull-down	GPIO/SEG 24. This is a dual function pin.
B14	P2.12/S25	I/O	VLCD VDD	Pull-up	GPIO/SEG 25. This is a dual function pin.
D14	P2.13/S26	I/O	VLCD VDD	Pull-up	GPIO/SEG 26. This is a dual function pin.
E15	P2.14/S27	I/O	VLCD VDD	Pull-up	GPIO/SEG 27. This is a dual function pin.
A15	P2.15/S28	I/O	VLCD VDD	Pull-up	GPIO/SEG 28. This is a dual function pin.
F8	P3.8/S29	I/O	VLCD VDD	Pull-up	GPIO/SEG 29. This is a dual function pin.
F9	P3.9/S30	I/O	VLCD VDD	Pull-up	GPIO/SEG 30. This is a dual function pin.
C14	P3.10/S31	I/O	VLCD VDD	Pull-up	GPIO/SEG 31. This is a dual function pin.
E14	P3.11/S32	I/O	VLCD VDD	Pull-up	GPIO/SEG 32. This is a dual function pin.

Pin No.	Mnemonic	I/O[1]	I/O Supply[2]	GPIO Pull-Up/Down[2]	Description
Miscellaneous Digital Input/Output					
K8	RESETX	I	VCCM_DIG	Pull-up	Reset Pin (Active Low).
L1	P4.0/I2CSCL	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 0)/I²C Clock. This is a dual function pin.
L2	P4.1/I2CSD	I/O	VCCM_DIG	Pull-up	GPIO/I²C Data. This is a dual function pin.
R1	P4.2/TOUTB	I/O	VCCM_DIG	Pull-up	GPIO/Timer B Output. This is a dual function pin.
R2	P0.10/TOUTC	I/O	VCCM_DIG	Pull-up	GPIO (External Interrupt 8)/Timer C Output. This is a dual function pin.
K2	P0.11	I/O	VCCM_DIG	Pull-up	GPIO (External Clock Input Pin).
N2	BOOT	I	VCCM_DIG	Pull-down	The device enters serial download mode if this pin is held high during, and for a short time after, a reset. It executes user code after any reset event or if the pin is low.
A1	DNC		N/A	N/A	Do Not Connect. Leave this pin floating.
Audio					
K6	P3.12/BEEP/BMCLK	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Positive/I²S Bit Clock. This is a multifunction pin.
K7	P3.13/BEEPX/SDATA	I/O	VCCM_DIG	Pull-down	GPIO/Beeper Output Negative/I²S Serial Data Output. This is a multifunction pin.
J6	P3.14/LRCLK	I/O	VCCM_DIG	Pull-down	GPIO/I²S Frame Clock. This is a dual function pin.

[1] S is supply, A is analog input, I is digital input, O is digital output, I/O is digital input/output, and G is ground.
[2] N/A means not applicable.