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Evaluating the AD1974 Four ADC with PLL 192 kHz, 24-Bit Codec

EVAL-AD1974AZ PACKAGE CONTENTS

AD1974 evaluation board
USBi control interface board
USB cable

OTHER SUPPORTING DOCUMENTATION

AD1974 data sheet

EVALUATION BOARD OVERVIEW

This document explains the design and setup of the evaluation board for the AD1974. The evaluation board must be connected to an external ±12 V dc power supply and ground. On-board regulators derive the 3.3 V supplies for the AD1974. The AD1974 is controlled through an SPI interface. A small external interface board, EVAL-ADUSB2EBZ (also called USBi), connects to a PC USB port and provides SPI access to the evaluation board through a ribbon cable. A graphical user interface (GUI) program is provided for easy programming of the chip in a Microsoft® Windows® PC environment. The evaluation board allows demonstration and performance testing of most AD1974 features, including the four ADCs, as well as the digital audio ports.

Additional analog circuitry (ADC input filter/buffer) and digital interfaces such as S/PDIF are provided to ease product evaluation.

All analog audio interfaces are accessible with stereo audio 3.5 mm TRS connectors.

FUNCTIONAL BLOCK DIAGRAM

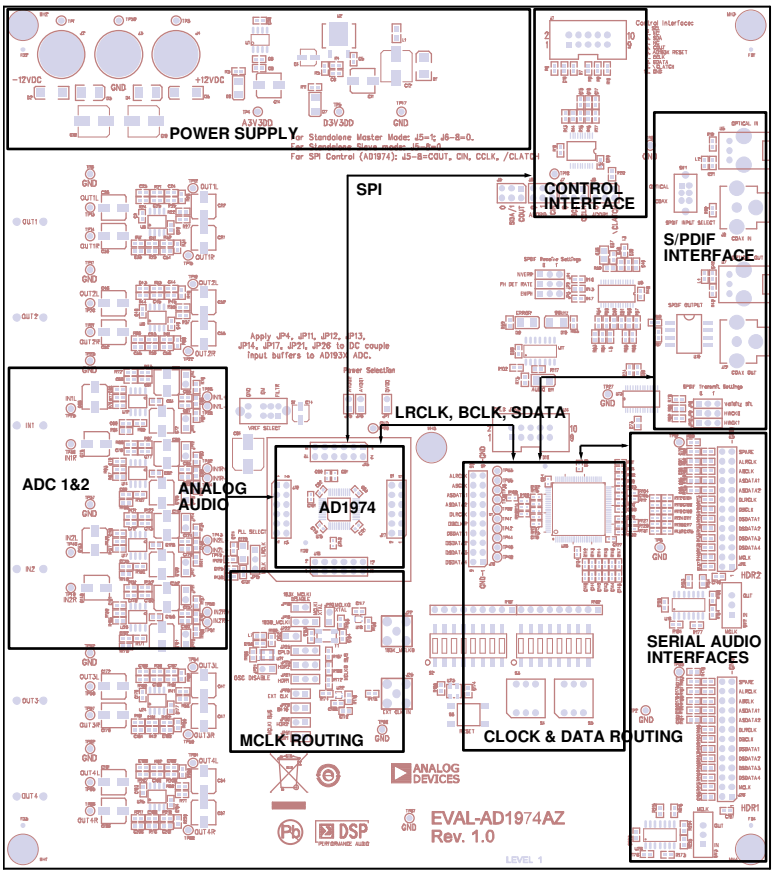

Figure 1.

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REVISION HISTORY

2/10—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

STANDALONE MODE

It is possible to run the board and the AD1974 ADC in standalone mode, which fixes the functionality of the AD1974 into the I²S data format, running at 256 × f_S (default register condition). The ADC BCLK and LRCLK ports are flipped between slave and master (input and output) by tying COUT (Pin 24) to low or high. This is accomplished by moving the J5 jumper to either 0 or SDA/1 (see Figure 2 and Figure 3 for the correct settings).

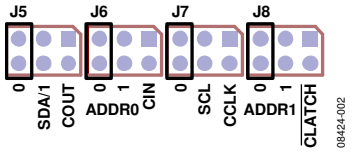

Figure 2. Standalone Slave Mode

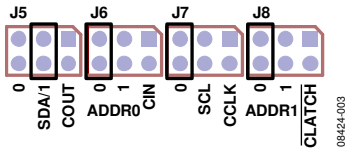

Figure 3. Standalone Master Mode

With the control jumpers set to standalone master mode, the S2 DIP switches set to on, the S3 DIP switch sets to off, and both rotary hex mode switches, S4 and S5, set to 0, the AD1974 is the LRCLK, BCLK, and SDATA source. The default MCLK jumper setting uses the on-board oscillator as MCLK for the AD1974 as well as the S/PDIF transmitter and HDR1 port. The board passes analog audio from the IN1 stereo to the S/PDIF and HDR1 output ports. IN2 can be selected by changing S3, Position 8, to on. Other serial audio clock and data routing configurations are described in the Switch and Jumper Settings section.

SPI CONTROL

The evaluation board can be configured for interactive control of the registers in the AD1974 by connecting the SPI port to the USBi. The SPI jumper settings are shown in Figure 4.

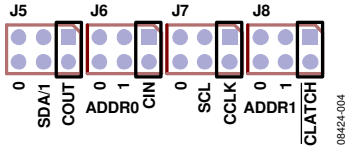

Figure 4. SPI Control

The **Automated Register Window Builder** software controls the AD1974 and is available at www.analog.com/AD1974.

AUTOMATED REGISTER WINDOW BUILDER SOFTWARE INSTALLATION

The **Automated Register Window Builder** is a program that launches a graphical user interface for direct, live control of the AD1974 registers. The GUI content for the part is defined in a part-specific .xml file; this file is included in the software installation. To install the **Automated Register Window Builder** software, follow these steps:

1. At **www.analog.com/AD1974**, find the **Resources & Tools** list.
2. In the list, find **Evaluation Boards & Development Kits** and click **Evaluation Boards/Tools** to open the provided **ARWBvXX.zip** file.
3. Double-click the provided **.msi** file to extract the files to an empty folder on your PC.
4. Then double-click **setup.exe** and follow the prompts to install the **Automated Register Window Builder**. A computer restart is not required.
5. Copy the .xml file for the AD1974 from the extraction folder into the **C:\Program Files\Analog Devices Inc\AutomatedRegWin** folder, if it does not appear in the folder after installation.

HARDWARE SETUP, USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into the J1 control interface header.
2. Connect the USB cable to your computer and to the USBi.
3. When prompted for drivers, follow these steps:
   a. Choose **Install from a list or a specific location**.
   b. Choose **Search for the best driver in these locations**.
   c. Check the box for **Include this location in the search**.
   d. Find the USBi driver in **C:\Program Files\ Analog Devices Inc\AutomatedRegWin\USB drivers**.
   e. Click **Next**.
   f. If prompted to choose a driver, select **CyUSB.sys**.
   g. If the PC is running Windows XP and you receive a message that the software has not passed Windows logo testing, click **Continue Anyway**.

You can now open the **Automated Register Window Builder** application and load the .xml file for the part onto your evaluation board.

POWERING THE BOARD

The AD1974 evaluation board requires power supply input of ±12 V dc and ground to the three binding posts; +12 V draws ~250 mA and −12 V draws~100mA. The on-board regulators provide two 3.3 V rails, one each for AVDD and DVDD for the AD1974. DVDD also supplies power for the active peripheral components on the board. Jumpers are provided to allow access to the power connections of the AD1974. These are convenient points to insert a current measuring device. The only components on the AD1974 side of the jumper are the part itself and the local power supply decoupling. The jumper blocks are shown in Figure 5.

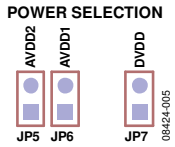

Figure 5. AD1974 Power Jumpers

SETTING UP THE MASTER CLOCK (MCLK)

The AD1974 evaluation board has a series of jumpers that give the user great flexibility in the MCLK clock source for the AD1974. MCLK can come from five sources: passive crystal, active oscillator, external clock in, and two header connections. Note that the CPLD on the board must have a valid clock source; the frequency is not critical. These jumper blocks can assign this CPLD clock. Most applications of the board use MCLK from either the oscillator or one of the header (HDR) inputs. Figure 6 to Figure 7 show the on-board active oscillator disabled so that it does not interfere with the selected clock. The clock feed to the CPLD comes directly from the clock source.

Note that, if the HDR connectors are to be driven with MCLK from a source on the evaluation board, SW2 and/or SW3 must be switched from the IN position to the OUT position.

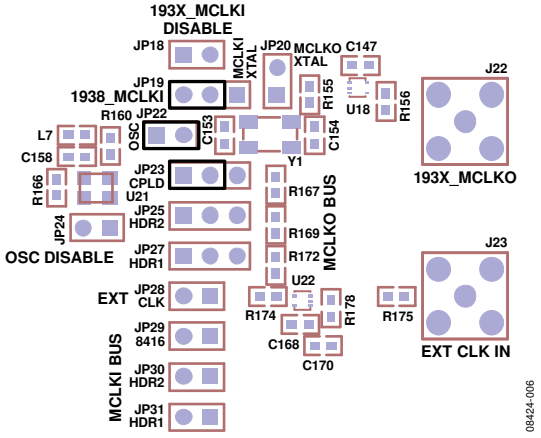

Figure 6. Active On-Board Oscillator as Master; the AD1974 and CPLD as Slaves

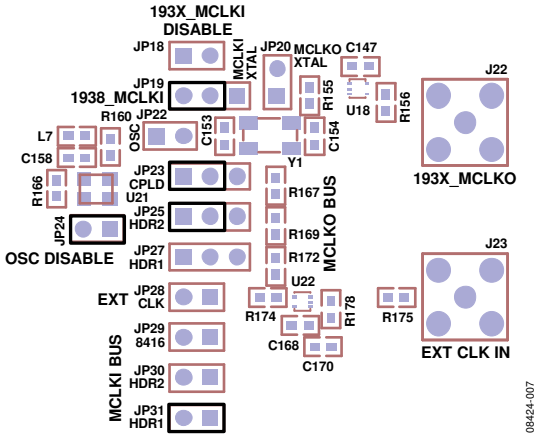

Figure 7. HDR1 as MCLK Master; the AD1974, CPLD, and HDR2 as Slaves

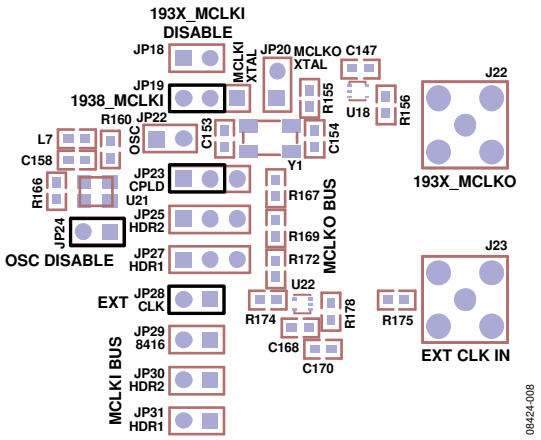

Figure 8. External Clock In as Master; the AD1974 and CPLD as Slaves

The MCLK configurations shown in Figure 9 and Figure 10 use the AD1974 MCLKO port to drive the CPLD and, possibly, the HDRs. The passive crystal runs the AD1974 at 12.288 MHz. Figure 10 shows the MCLKI shut off; this is the case when the PLL is set to LRCLK instead of to MCLK.

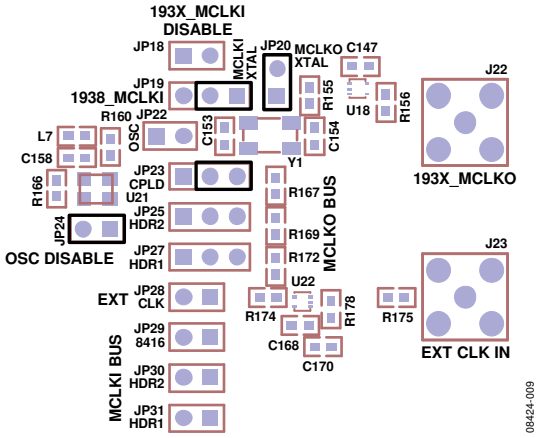

Figure 9. Passive Crystal; the AD1974 Is Master; the CPLD Is Slave from the MCLKO Port

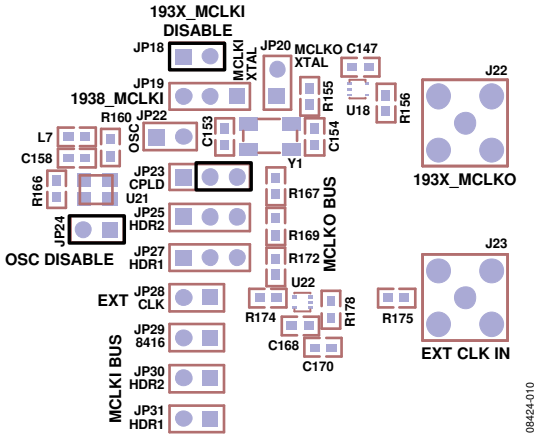

Figure 10. LRCLK Is the Master Clock Using the PLL; MCLKI Is Disabled, and CPLD Is Slave to the MCLKO Port

CONFIGURING THE PLL FILTER

The PLL for the AD1974 can run from either MCLK or LRCLK, according to its setting in the PLL and Clock Control 0 register, Bits[6:5]. The matching RC loop filter must be connected to LF (Pin 47) using JP15. See Figure 11 and Figure 12 for the jumper positions.

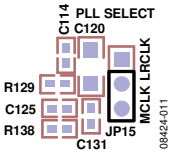

Figure 11. MCLK Loop Filter Selected

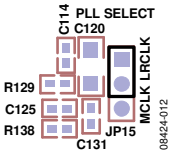

Figure 12. LRCLK Loop Filter Selected

Normally, the MCLK filter is the default selection; it is also possible to use the register control window to program the PLL to run from the LRCLK. In this case, the jumper must be changed as shown in Figure 12.

CONNECTING AUDIO CABLES

Analog Audio

The analog inputs and outputs use 3.5 mm TRS jacks; they are configured in the standard configuration: tip = left, ring = right, sleeve = ground. The analog inputs to IN1 and IN2 generate 0 dBFS from a 1 V rms analog signal. The on-board buffer circuit creates the differential signal to drive the ADC with 2 V rms at the maximum level. There are test points that allow direct access to the ADC pins; note that the ADC pins have a common mode voltage of 1.5 V dc. These test points require proper care so that improper loading does not drag down the common-mode voltage, and the headroom and performance of the part do not suffer.

The ADC buffer circuit has been designed with a switch (S1) that allows the user to change the voltage reference for all of the amplifiers. GND, CM and FILTR can be selected as a reference; it is advisable to shut down the power to the board before changing this switch. The CM and FILTR lines are very sensitive and do not react well to a change in load while the AD1974 is active. A series of jumpers allows the user to dc-couple the buffer circuit to the ADC analog port in when CM and FILTR are selected (see Figure 13).

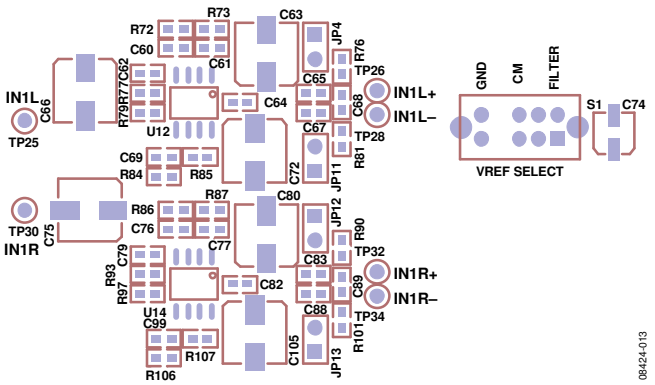

Figure 13. VREF Selection and DC Coupling Jumpers

Digital Audio

There are two types of digital interfacing, S/PDIF and discrete serial. The S/PDIF transmitter port has both optical and coaxial connectors that can be used simultaneously. The serial audio connectors use 1 × 2 100 mil spaced headers, signal and ground. The LRCLK, BCLK, and SDATA paths are available for the ADC on the HDR1 and HDR2 connectors. Each has a connection for MCLK; each HDR MCLK interface has a switch to set the port as an input or output, depending on the configuration of the evaluation board.

SWITCH AND JUMPER SETTINGS

Clock and Control

The AD1974 is designed to run in standalone mode at a sample rate (f_S).of 48 kHz, with an MCLK of 12.288 MHz (256 × f_S). In standalone slave mode, the ADC port must receive valid BCLK and LRCLK. The AD1974 can be clocked from the HDR1 connector; the ADC BCLK and LRCK port sources are selected with S2, Position 2 and Position 3. For HDR1 as master, S2, Position 3, should be on (see the detail in Figure 14 and Figure 15). Note that HDR2 is not implemented in the CPLD routing code.

It is also possible to configure the AD1974 ADC BCLK and LRCK ports to run in standalone master mode; moving J5 to SDA/1, as shown in Figure 3, changes the state of the AD1974. Setting S2, Position 2, to on selects the proper routing to both the S/PDIF transmitter and the HDR1 connector. In this mode, the AD1974 ADC port generates BCLK and LRCLK when given a valid MCLK.

For the full flexibility of the AD1974, the part can be put in SPI control mode and programmed with the **Automated Register Window Builder** application (see Figure 4 for the appropriate jumper settings). Changing the registers and setting the DIP switches allow many possible configurations. In the various master and slave modes, the AD1974 takes MCLK from a selected source and can be set to generate or receive either BCLK or LRCLK to or from either the ADC or the DAC port, depending on the settings and requirements.

As an example, to set the ADC port as master, switch the ADC Control Register 2 bits for BCLK and LRCLK to master and change S2, Position 2, and S2, Position 5, to on. In this mode, the board is configured so that the ADC BCLK and LRCLK pins are the clock source for both the ADC destination and the DAC data source. For the DAC port to be the master, the DAC Control Register 1 bits for BCLK and LRCLK must be changed to master, and S2, Position 2 and Position 3, and S2, Position 5 and Position 6, must all be on. On this evaluation board, these settings allow the master port on the AD1974 to drive both the S/PDIF and the HDR connections. Many combinations of master and slave are possible (see Figure 14 and Figure 15 for the correct settings).

S/PDIF Audio

The settings in Figure 14 and Figure 15 show the details of clock routing and control for the ADC port. The board is shipped with the IN1 analog port selected as default feed to the S/PDIF transmitter; the hex switches are set to 0 and only the S2, Position 2, DIP switch is on. All other switches are set to off. The evaluation board is shipped in standalone master mode (see Figure 3); the BCLK and LRCLK signals run from the ADC port of the AD1974 to the S/PDIF transmitter and HDR1.

In this default configuration, IN1 analog is routed through the AD1974 ADC ASDATA1 path to the S/PDIF output. By changing DIP switch S3, Position 8, from 0 to 1, IN2 is selected.

HDR Connectors—Serial Audio

Routing of serial audio to the HDR1 connector is controlled by DIP S3, Position 6 and Position 7. The default condition routes IN1 to ASDATA1 and IN2 to ASDATA2.

Other Options

To use other f_S rates, the USBi must be connected and the AD1974 registers must be programmed accordingly. For example, adjusting the f_S rate to 96 kHz requires that the ADC Control 0 register have the sample rate set to 96 kHz (see Figure 14 and Figure 15 for the complete list of options).

The CPLD code is presented in the CPLD Code section and is included with the evaluation board; alterations and additions to the functionality of the CPLD are possible by altering the code and reprogramming the CPLD.

ROTARY AND DIP SWITCH SETTINGS

AD1974/ADAU132X Rev-E Evaluation Board Configuration: (* indicates default setting)

1) DIP Switch S2 Position-8 (SPDIF_RX_TX reset) must be toggled after power-up for proper operation of the SPDIF receiver and transmitter.
2) The AD1974 evalution board defaults the AD1974 codec to standalone mode preventing SPI/I²C operation. The J5, J6, J7, and J8 header jumpers can be changed for SPI/I²C operation.

ADC and DAC Serial Clock (BCLK, LRCLK) Source Selection and Routing (Switch S2)

1) DIP Switch S2 controls the AD1974 ADC and DAC serial clock source selection. One of four clock sources is selected based on the setting. SPDIF Receiver CS8416, Header Connector HDR1, ADC serial clocks, or DAC serial clock can be the clock source. ADC and DAC serial clock selection is controlled independently.
2) The AD1974 master clock source should be selected using the JP28, JP29, JP30, and JP31 header jumpers such that the MCLK source is in sync with the DAC/ADC serial clock and data source.

DIP Switch S2 position: Position-1 ADC- ABCLK, ALRCLK Clock Disable		Description
Off*	Enable	Enable ADC clocks
On	Disable	Tristate ADC clocks

Position-2	Position-3							
ADC - ABCLK, ALRCLK Source Selection		ABCLK Source	ALRCLK Source	SPDIF_Rx Clocks	SPDIF_Tx Clocks	HDR1 Clocks	ADC Clocks	DAC Clocks
Off*	Off*	SPDIF_RX_8416	SPDIF_RX_8416	Master	Slave	Slave	Slave	N/A
Off	On	HDR1_ABCLK	HDR1_ALRCLK	Slave	Slave	Master	Slave	N/A
On	Off	ADC-ABCLK	ADC-ALRCLK	Slave	Slave	Slave	Master	N/A
On	On	DAC-DBCLK	DAC-DLRCLK	Slave	Slave	Slave	Slave	Master

Position-4 DAC – DBCLK, DLRCLK Clock Disable		Description
Off*	Enable	Enable DAC clocks
On	Disable	Tristate DAC clocks

Position-5	Position-6							
DAC - DBCLK, DLRCLK Source Selection		DBCLK Source	DLRCLK Source	SPDIF_Rx Clocks	SPDIF_Tx Clocks	HDR1 Clocks	ADC Clocks	DAC Clocks
Off*	Off*	SPDIF_RX_8416	SPDIF_RX_8416	Master	Slave	Slave	N/A	Slave
Off	On	HDR1_DBCLK	HDR1_DLRCLK	Slave	Slave	Master	N/A	Slave
On	Off	ADC-ABCLK	ADC-ALRCLK	Slave	Slave	Slave	Master	Slave
On	On	DAC-DBCLK	DAC-DLRCLK	Slave	Slave	Slave	N/A	Master

Position-7 SPDIF_RX-TX Clock Rate Selection	Description SPDIF_RX_TX MCLK Rate	SPDIF_TX CS8406 MCLK Jumper Settings JP10	JP9
Off*	SPDIF_RX_TX MCLK Rate = 256xf_S	0	0
On	SPDIF_RX_TX MCLK Rate = 128xf_S	0	1

Position-8 SPDIF_RX_TX /RESET	Description SPDIF_TX_RX RESETB	
Off*	SPDIF_RX_TX in active mode	(Note: This position must be toggled after power-up for proper operation.)
On	SPDIF_RX_TX in reset mode	

SPDIF RX - CS8416 Jumpers JP1	JP2	JP3
0 = Normal update rate phase detector, increased clock jitter	0 = NVERR selected	0 = Emphasis audio match off
1 = High update rate phase detector, low clock jitter	1 = RERR selected	1 = Emphasis audio match on

SPDIF TX - CS8406 Jumpers JP18	SPDIF_TX CS8406 MCLK Rate Jumper Settings JP10	JP9	
0 = the V pin input determines the state of the validity bit in the outgoing AES3 transmitted data	0	0	SPDIF_TX MCLK Rate = 256xf_S
1 = the V pin input determines the state of the validity bit in the outgoing AES3 transmitted data	0	1	SPDIF_TX MCLK Rate = 128xf_S

08424-014

Figure 14. Settings Chart 1

DAC and ADC Serial Data (DSDATA/ASDATA) Source Selection and Routing (Switch S4 and Switch S3)

Rotary hex Switch S4 selects the AD1974 DAC serial data source. The DAC data source can be either SPDIF Receiver CS8416 or can be provided by the Header Connector HDR1. It is important to note that the DAC data source should be in sync with the DAC serial port clock source(set by DIP Switch S2, Positions [5:6]. DIP Switch S3 routes the ADC serial data among AD193x, SPDIF Transmitter CS8406, and Header Connector HDR1 in stereo, TDM, and aux mode.

***** Signal sources to the DAC data lines (DSDATA1/2/3/4) fill the columns, column header is the destination ******

S4 Position	DAC Serial Format	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	Description
0*	Stereo	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416	SPDIF_RX_8416 stereo data to all eight DAC channels
1	Stereo	SPDIF_RX_8416	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	SPDIF_RX_8416 stereo data to DAC1 only, rest DACs2/3/4 data from HDR1 connector
2	Stereo	HDR1_DSDATA1	SPDIF_RX_8416	HDR1_DSDATA3	HDR1_DSDATA4	SPDIF_RX_8416 data to DAC2 only, rest DACs1/3/4 data from HDR1 connector
3	Stereo	HDR1_DSDATA1	HDR1_DSDATA2	SPDIF_RX_8416	HDR1_DSDATA4	SPDIF_RX_8416 data to DAC3 only, rest DACs1/2/4 data from HDR1 connector
4	Stereo	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	SPDIF_RX_8416	SPDIF_RX_8416 data to DAC4 only, rest DACs1/2/3 data from HDR1 connector
5	N/A	N/A	N/A	N/A	N/A	
6	N/A	N/A	N/A	N/A	N/A	
7	Stereo/TDM	ZERO DATA	ZERO DATA	ZERO DATA	ZERO DATA	Source zero data to all eight DAC channels
8	Stereo	HDR1_DSDATA1	HDR1_DSDATA1	HDR1_DSDATA1	HDR1_DSDATA1	HDR1 Connector Signal HDR1_D SDATA1 drives all four DAC pairs
9	Stereo	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive corresponding DAC data lines
A	TDM	HDR1_DSDATA1	DAC_TDM_OUT			HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
B	Dual- Line TDM	HDR1_DSDATA1	DAC_TDM_OUT	HDR1_DSDATA3	DAC_TDM_OUT	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
C	DAC aux mode	HDR1_DSDATA1	Aux ADC1 input	Aux ADC2 input	Aux DAC2 output	HDR1 Connector Data Lines DSDATA1, DSDATA2... so on drive/receive corresponding DAC data lines in TDM mode
D						
E						
F	Stereo/TDM	TRISTATE	TRISTATE	TRISTATE	TRISTATE	Tristate all DAC data lines, DSDATA1, DSDATA2, DSDATA3, and DSDATA4

***** Column content indicates the direction of the DAC data pins and corresponding HDR1 connector DAC data pins *******

S4 Position	DAC1 (DSDATA1)	DAC2 (DSDATA2)	DAC3 (DSDATA3)	DAC4 (DSDATA4)	HDR1_DSDATA1	HDR1_DSDATA2	HDR1_DSDATA3	HDR1_DSDATA4	SPDIF_Rx Data	HDR1 Data
0*	Input	Input	Input	Input	N/A	N/A	N/A	N/A	Master	
1	Input	Input	Input	Input	N/A	Input	Input	Input	Master	
2	Input	Input	Input	Input	Input	N/A	Input	Input	Master	
3	Input	Input	Input	Input	Input	Input	N/A	Input	Master	
4	Input	Input	Input	Input	Input	Input	Input	N/A	Master	
5										
6										
7	Input	Input	Input	Input	Output	Output	Output	Output	N/A	N/A
8	Input	Input	Input	Input	Input	Input	Input	Input		Master
9	Input	Input	Input	Input	Input	Input	Input	Input		Master
A	Input	Output			Input	Output				Master
B	Input	Output	Input	Output	Input	Output	Input	Output		Master
C	Input	Input	Input	Output	Input	Input	Input	Output		Master
D										
E										
F	TRISTATE	TRISTATE	TRISTATE	TRISTATE						

DIP Switch S3 Position:

Position-6	Position-7	ADC Serial Format	HDR1_ASDATA1	HDR1_ASDATA2	Description (HDR1 ADC Data Source Selection)
Off*	Off*	Stereo	ASDATA1	ASDATA2	HDR1 Connector ADC Data Lines ASDATA1 and ASDATA2 receive corresponding ADC data stream
Off	On	Stereo	ASDATA2	ASDATA2	HDR1 Connector ADC Data Line ASDATA1 receive ADC2 data line ASDATA2
On	Off	TDM	ASDATA1	ADC TDM input stream	HDR1 Connector ADC Data Line ASDATA1 receive ADC TDM out data stream
On	On	ADC Aux *(see note)*	ASDATA1	ADC TDM input stream	HDR1 Connector ADC Data Line ASDATA1 receive ADC TDM out data stream

NOTE: ADC AUX mode overrides the DAC data configuration rotary Switch S2 setting.

DIP Switch S3 Position:

Position-6	Position-7	HDR1_ASDATA1	HDR1_ASDATA2	ADC1 (ASDATA1)	ADC2 (ASDATA2)
Off*	Off*	Output	Output	Output	Output
Off	On	Output	Output	Output	Output
On	Off	Output	Input	Output	Input
On	On	Output	Input	Output	Input

DIP Switch S3 Position:

Position-8	
Off*	ADC1 Data Stream ASDATA1 is sourced to the SPDIF_Tx_8406.
On	ADC2 Data Stream ASDATA2 is sourced to the SPDIF_Tx_8406.

Figure 15. Settings Chart 2

08424-015

SCHEMATICS AND ARTWORK

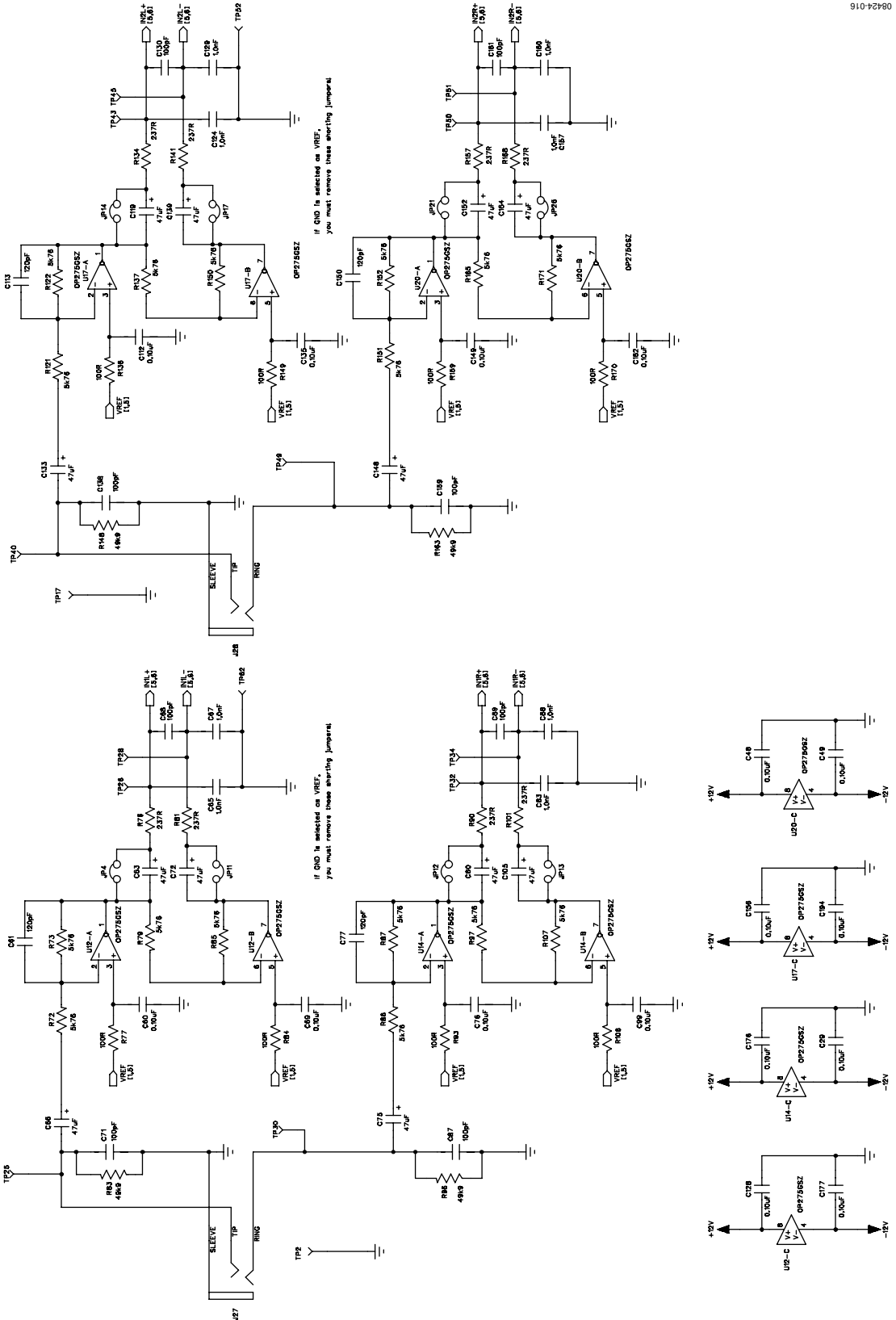

Figure 16. Board Schematics, Page 1—ADC Buffer Circuits

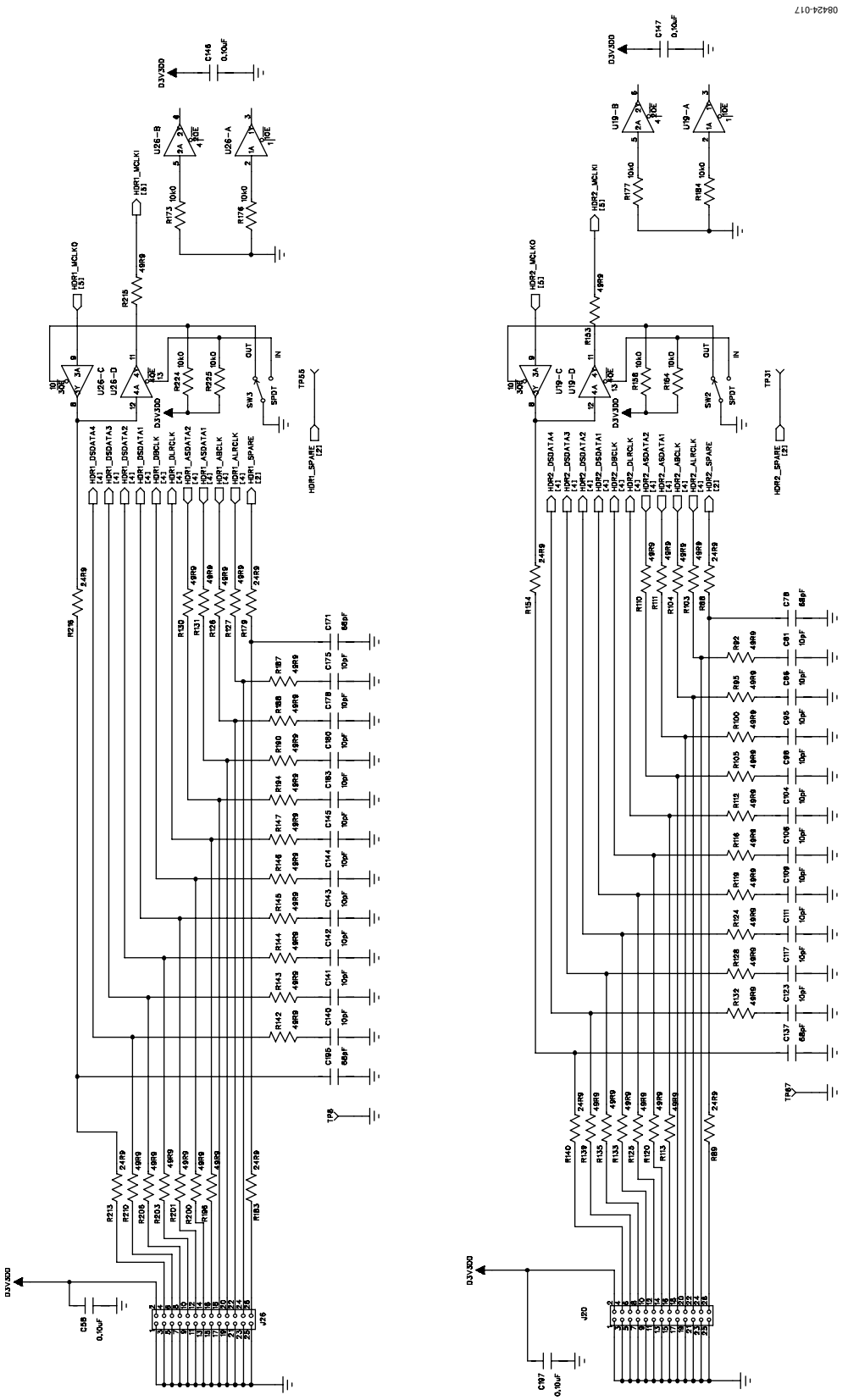

Figure 17. Board Schematics, Page 2—Serial Digital Audio Interface Headers with MCLK Direction Switching

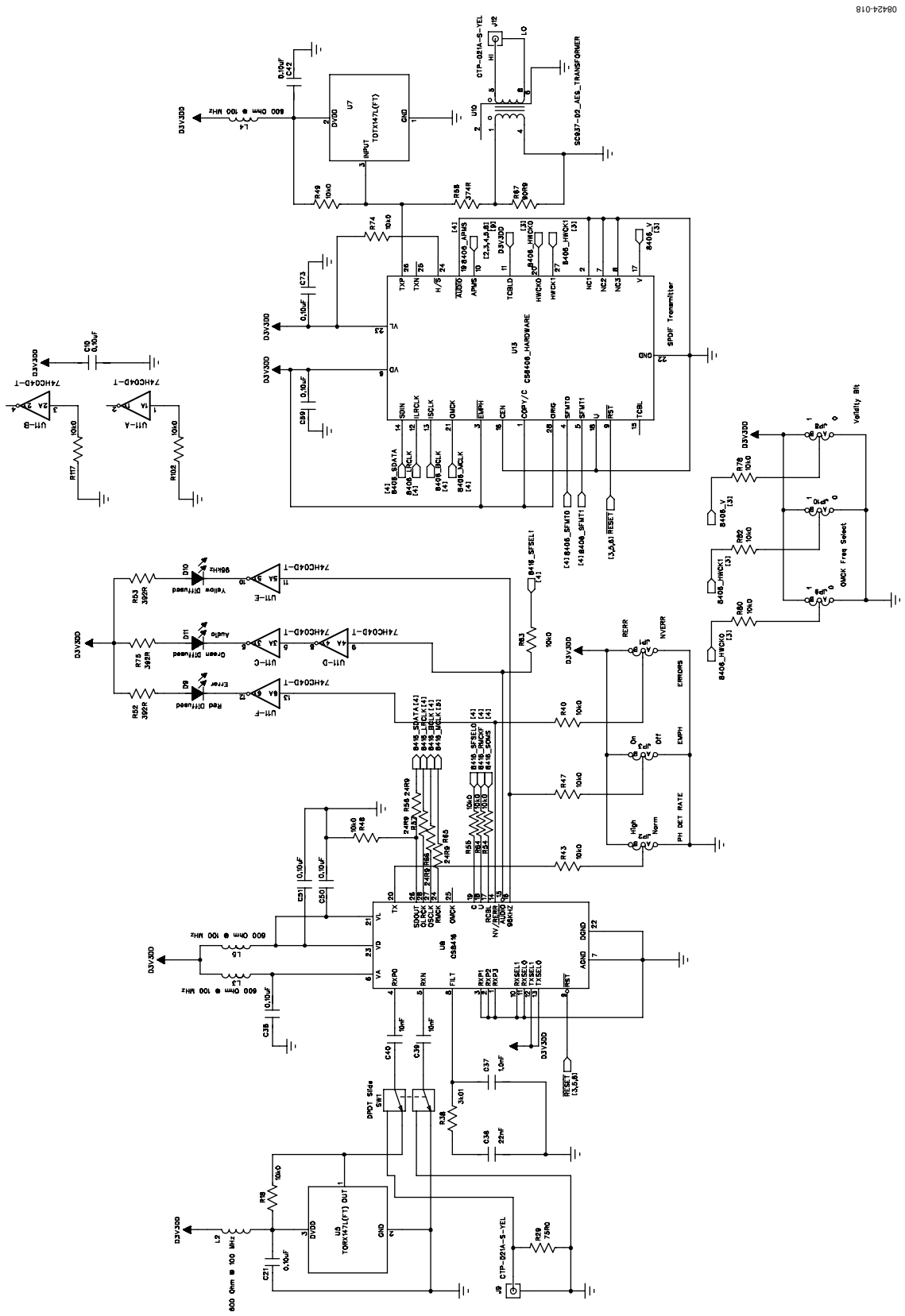

Figure 18. Board Schematics, Page 3—S/PDIF Receive and Transmit Interfaces

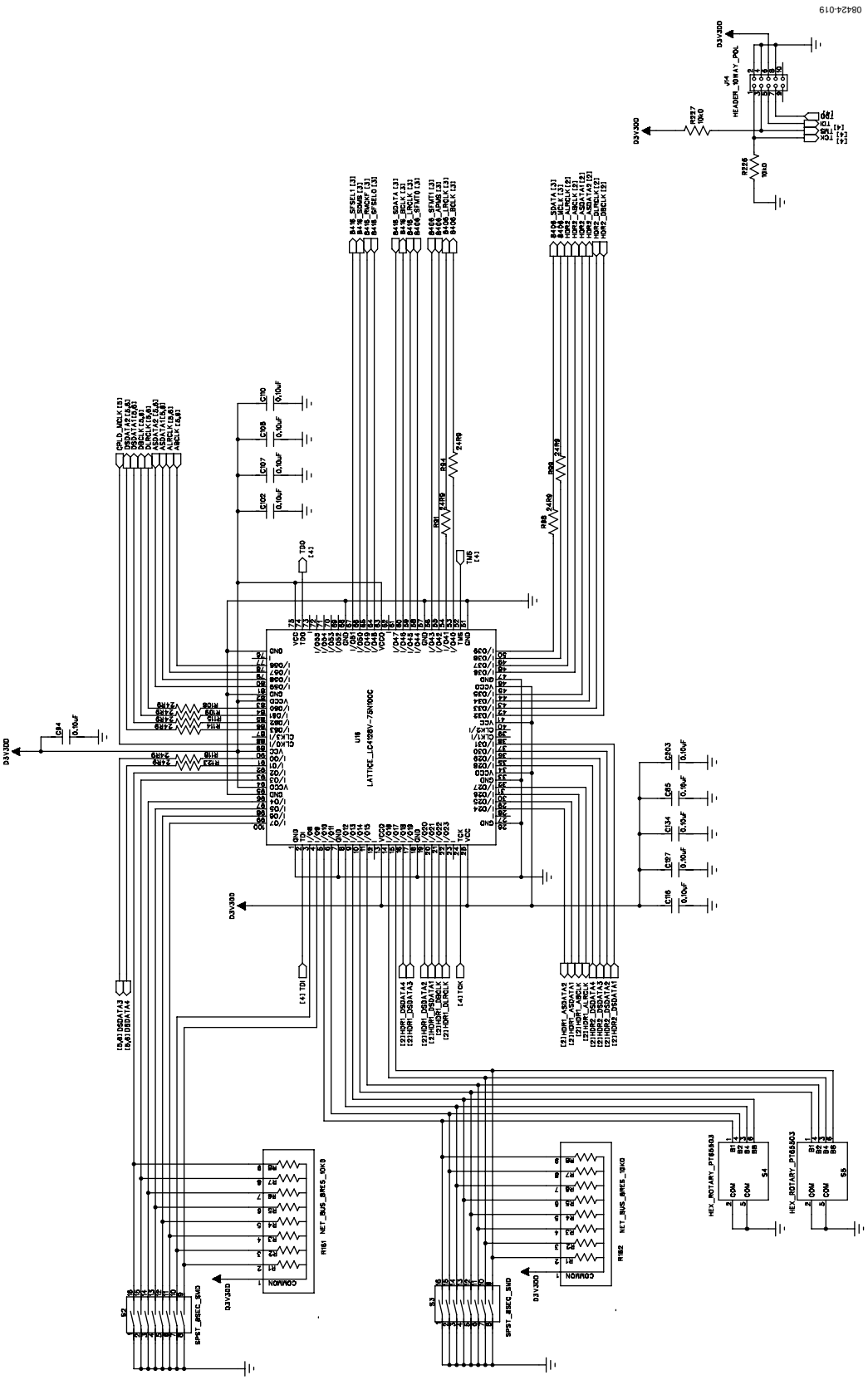

Figure 19. Board Schematics, Page 4—Serial Digital Audio Routing and Control CPLD

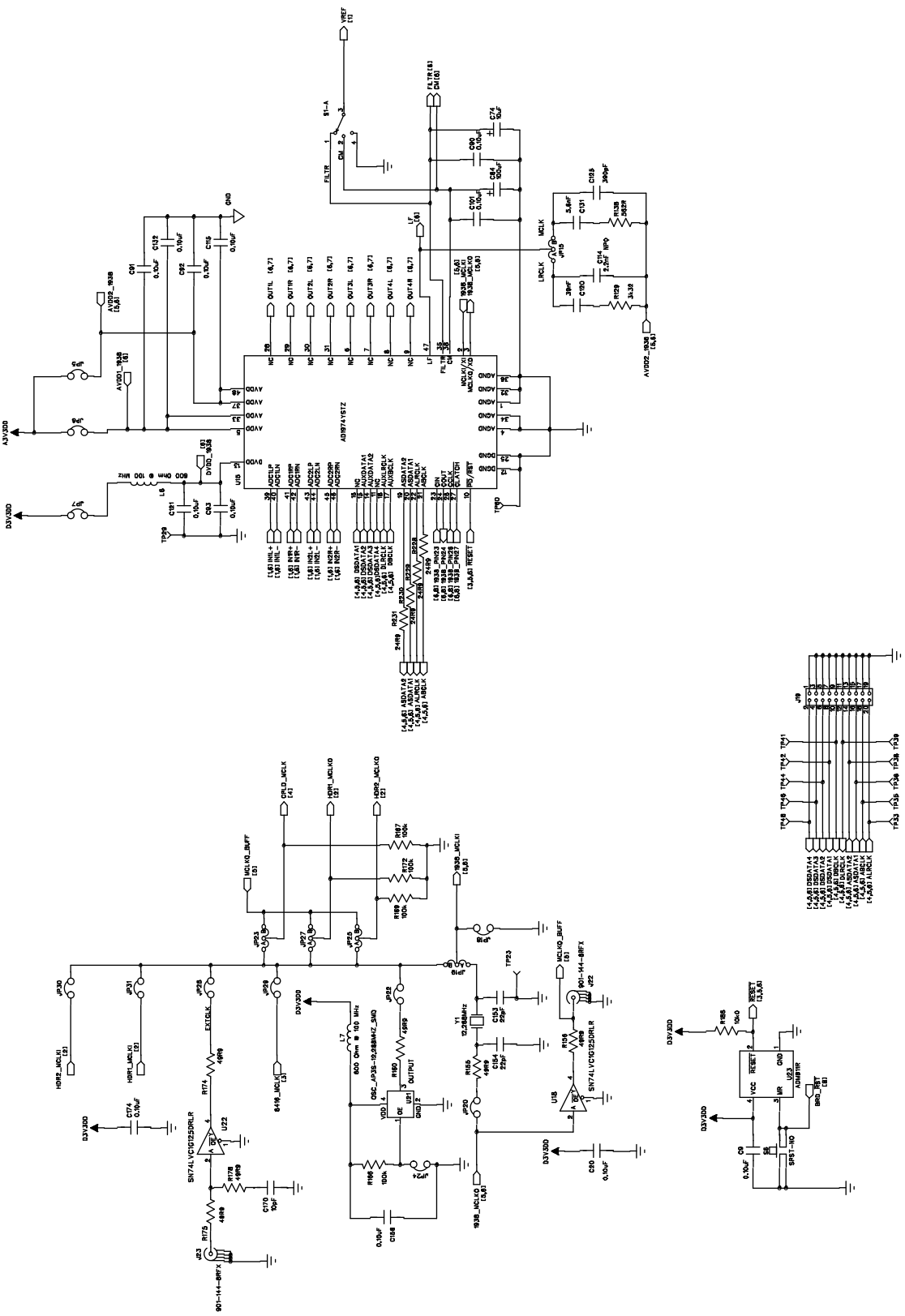

Figure 20. Board Schematic, Page 5—AD1974 with MCLK Selection Jumpers

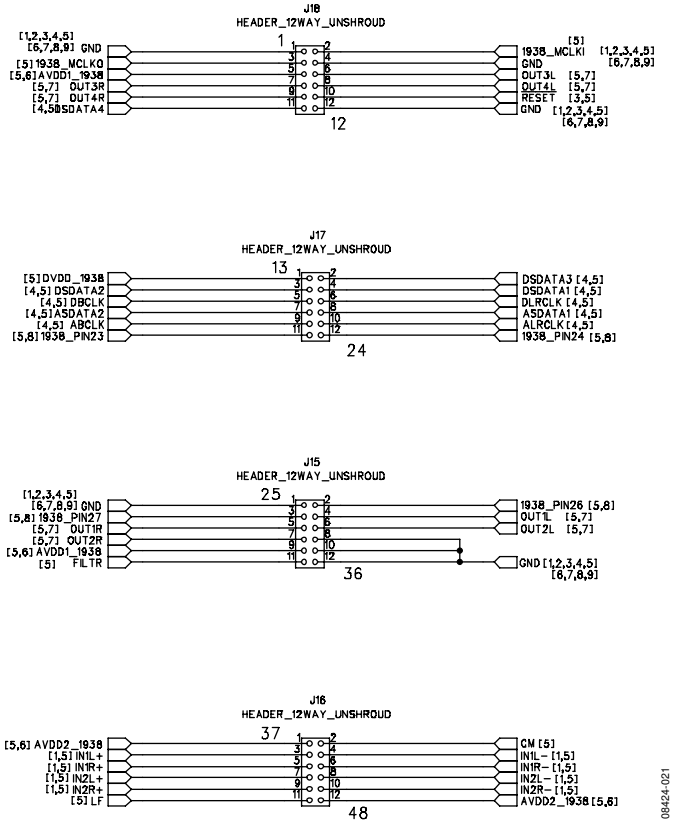

Figure 21. Board Schematics, Page 6—Daughter Card Interface, Useful as Test Points

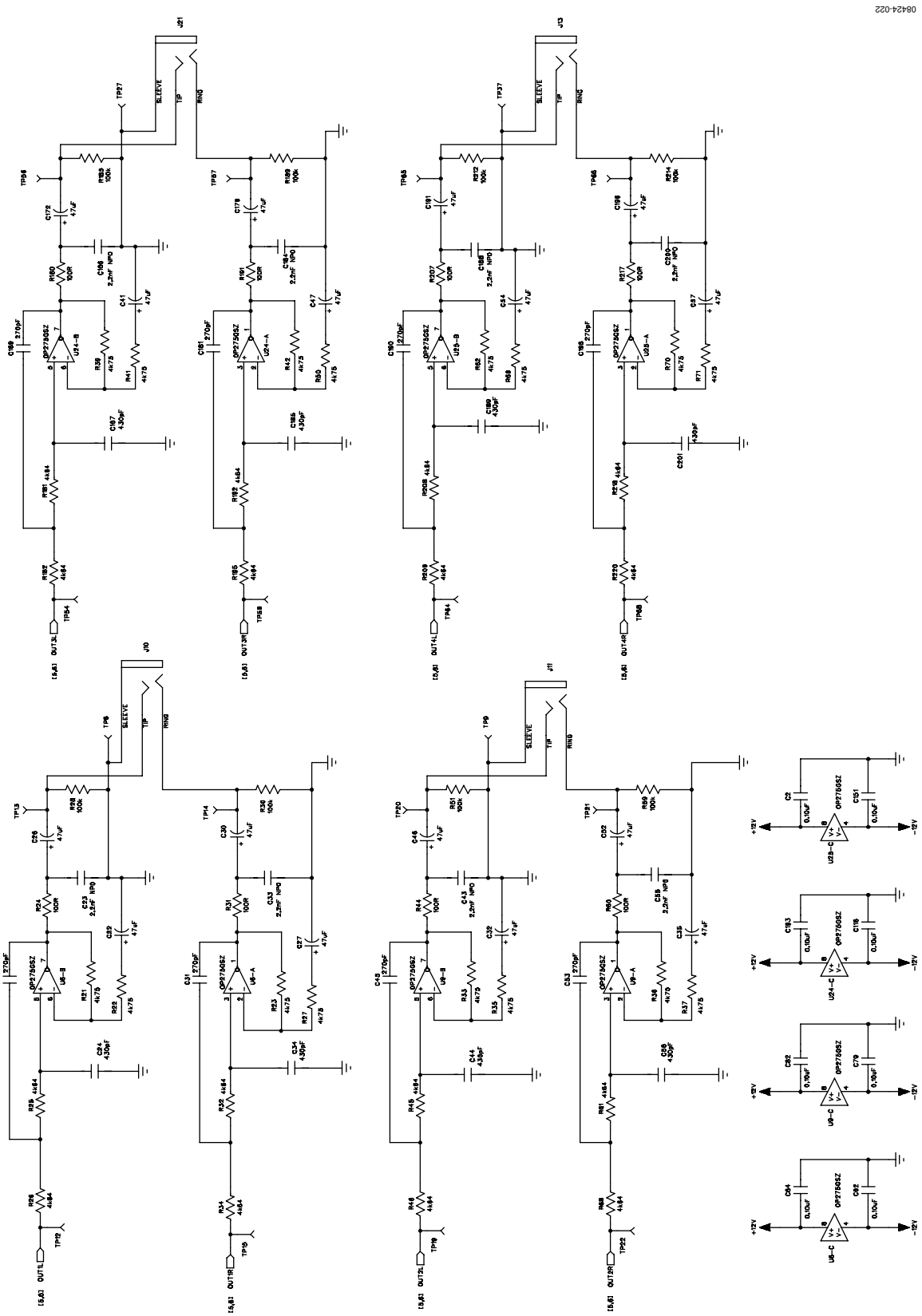

Figure 22. Board Schematics, Page 7—DAC Buffer Circuits

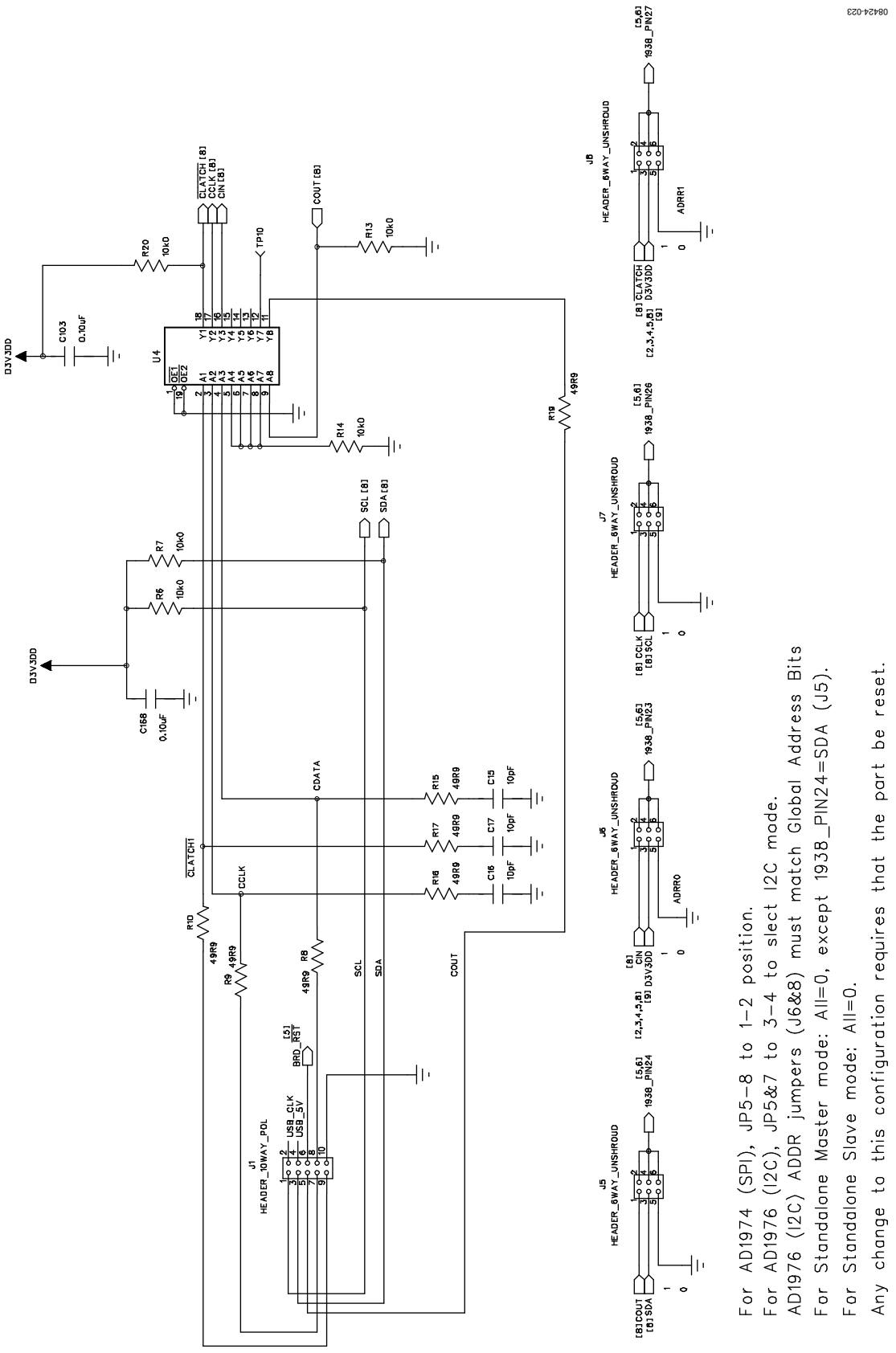

Figure 23. Board Schematics, Page 8—SPI Control Interface

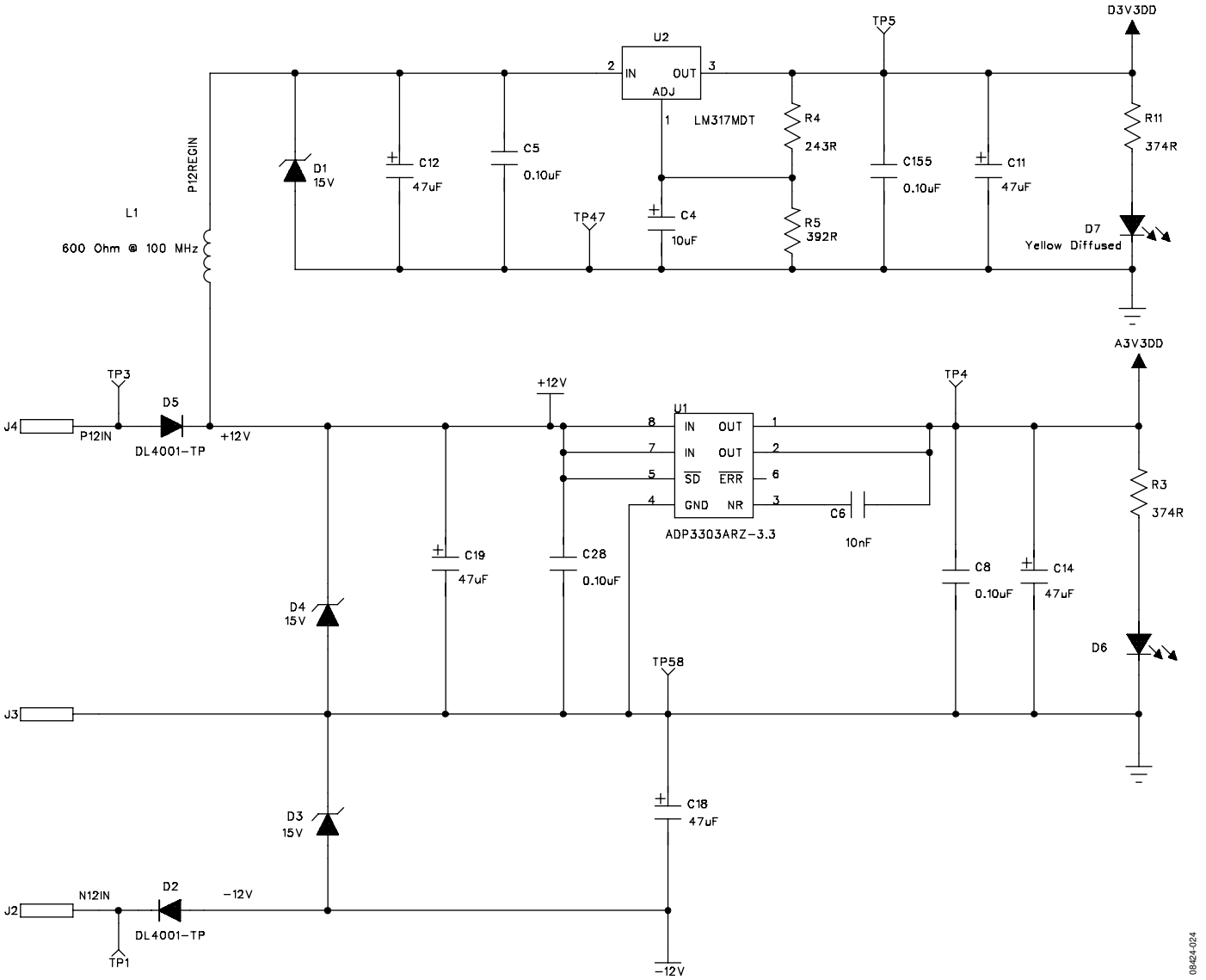

Figure 24. Board Schematics, Page 9—Power Supply

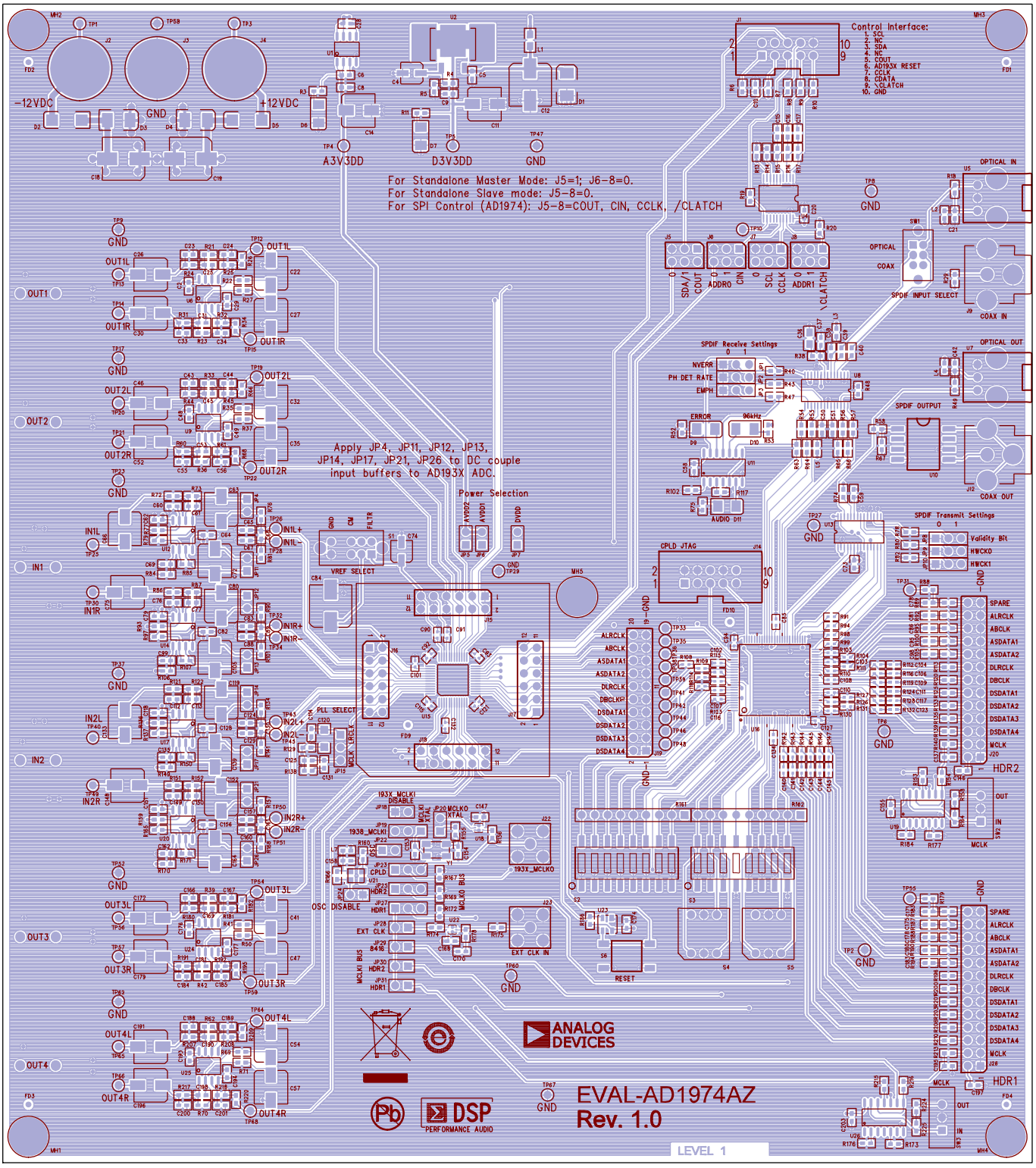

Figure 25. Top Assembly Layer

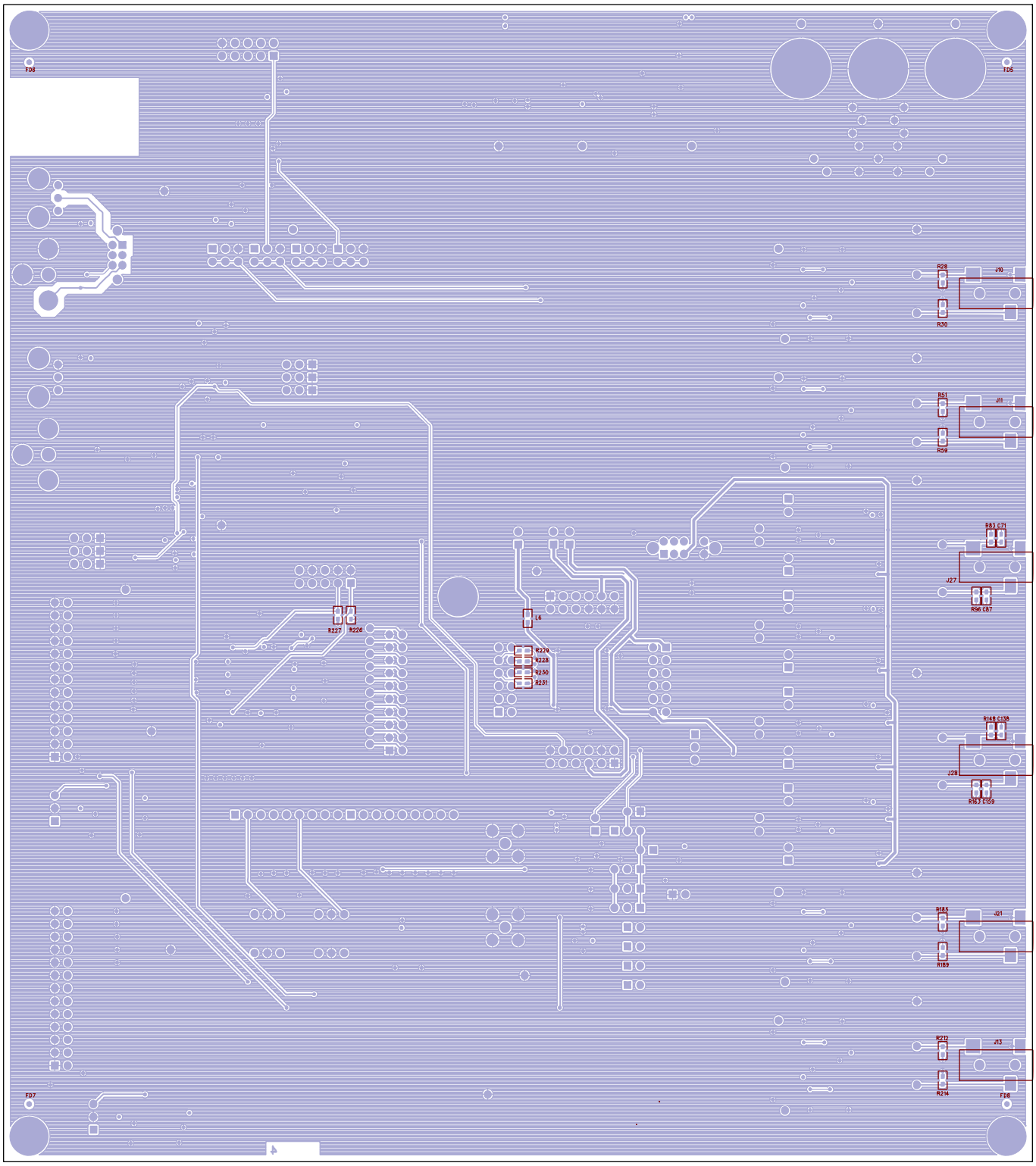

Figure 26. Bottom Assembly Layer

CPLD CODE

```
MODULE                    IF_Logic
TITLE   'AD1974 EVB Input Interface Logic'
//=============================================================================
//  FILE:                                          AD1974_pld_revE.abl
//  REVISION DATE:        04-16-09 (rev-E)
//  REVISION:                                      E
//  DESCRIPTION:
//=============================================================================

LIBRARY 'MACH';

"INPUTS  ------------------------------------------------------------------
// AD1974 CODEC pins
DSDATA1,DSDATA2           pin 86, 87 istype 'com';
DSDATA3,DSDATA4           pin 91, 92 istype 'com';
DBCLK,DLRCLK              pin 85, 84 istype 'com';
ASDATA1,ASDATA2           pin 80, 81 istype 'com';
ABCLK,ALRCLK              pin  78, 79 istype 'com';

// 25-pin header connector HDR1 pins
HDR1_DSDATA1              pin 20 istype 'com';
HDR1_DSDATA2              pin 19 istype 'com';
HDR1_DSDATA3              pin 17 istype 'com';
HDR1_DSDATA4              pin 16 istype 'com';
HDR1_DBCLK                pin 21 istype 'com';
HDR1_DLRCLK               pin 22 istype 'com';
HDR1_ASDATA1              pin 29 istype 'com, buffer';
HDR1_ASDATA2              pin  28 istype 'com, buffer';
HDR1_ABCLK                pin  30 istype 'com';
HDR1_ALRCLK               pin  31 istype 'com';

// 25-pin header connector HDR2 pins
HDR2_DSDATA1              pin  37 istype 'com';
HDR2_DSDATA2              pin 36 istype 'com';
HDR2_DSDATA3              pin 35 istype 'com';
HDR2_DSDATA4              pin 34 istype 'com';
HDR2_DBCLK                pin  41 istype 'com';
HDR2_DLRCLK               pin  42 istype 'com';
HDR2_ASDATA1              pin 44 istype 'com';
HDR2_ASDATA2              pin 43 istype 'com, buffer';
HDR2_ABCLK                pin  47 istype 'com';
HDR2_ALRCLK               pin  48 istype 'com';

// S/PDIF Rx CS8414 pins
SDATA_8416                pin 61 istype 'com';
```

```
BCLK_8416                  pin 60 istype 'com';
LRCLK_8416                 pin 59 istype 'com';
SOMS_RX,SFSEL1_RX,SFSEL0_RX,RMCKF_RX  pin 66,67,64,65 istype 'com';

// S/PDIF Tx CS8404 pins
SDATA_8406                                                          pin 50 istype
'com';
BCLK_8406,LRCLK_8406                              pin 53, 54 istype 'com';
MCLK_8406                                                           pin 49 istype
'com';
APMS_TX,SFMT1_TX,SFMT0_TX  pin 55,56,58 istype 'com';
CPLD_MCLK                                                           pin  89 istype
'com';

// AD1974 SPI port pins
//CCLK,CDATA,CLATCH                               pin 84, 83, 85 istype 'com';
//COUT
                           pin 82 istype 'com';
//CLATCH2,CLATCH3,CLATCH4                         pin 86, 56, 4 istype 'com';
//CONTROL_ENB                                                       pin 81 istype
'com';

S/PDIF_RESET_OUT                                                    pin 69 istype
'com';

// Switch S1, S2, S3 and S4 pins
ADC_CLK_OFF                                                         pin 93 istype
'com';                     // S2-1
ADC_CLK_SRC1                                    pin 94 istype 'com';       // S2-2
ADC_CLK_SRC0                                    pin 97 istype 'com';       // S2-3
DAC_CLK_OFF                                                         pin 98 istype
'com';                     // S2-4
DAC_CLK_SRC1                                    pin 99 istype 'com';       // S2-5
DAC_CLK_SRC0                                    pin 100 istype 'com';   // S2-6
S/PDIF_MCLK_RATE     pin 3 istype 'com';        // S2-7
S/PDIF_RESET_IN                                 pin 4 istype 'com';        // S2-8

MODE11,MODE12,MODE13,MODE14                          pin 5,6,8,9 istype 'com'; // S4
STAND_ALONE,MODE22,MODE23,MODE24     pin 10,11,14,15 istype 'com'; // S5

"NODES
I_DSDATA1, I_DSDATA2, I_DSDATA3, I_DSDATA4          node istype 'com';
I_DBCLK, I_DLRCLK
                           node istype 'com';
I_ASDATA1, I_ASDATA2
                           node istype 'com, buffer';
I_ABCLK, I_ALRCLK
                           node istype 'com';
Qdivide                                  node istype 'reg, buffer';
```

```
//=============================================================================
"MACROS

// Switch S3, DIP POSITIONS 6 AND 7

    ADC_HDR_NORMAL      = ( MODE22 &  MODE23);
    ADC_HDR_DATA2_DATA1 = ( MODE22 & !MODE23);
    ADC_HDR_TDM         = (!MODE22 &  MODE23);
    ADC_HDR_AUX         = (!MODE22 & !MODE23);

    S/PDIF_OUT_MUX = MODE24;

// HEX Switch S4

                          // S4 position 0,
   DAC_RX_ALL  =   ( MODE14 & MODE13 &  MODE12 &  MODE11);

                          // S4 position 1,
   DAC_RX_1    =  ( MODE14 & MODE13 &  MODE12 &  !MODE11);

                          // S4 position 2,
   DAC_RX_2    =  ( MODE14 & MODE13 &  !MODE12 &  MODE11);

                          // S4 position 3,
   DAC_RX_3    =  ( MODE14 & MODE13 &  !MODE12 &  !MODE11);

                          // S4 position 4,
   DAC_RX_4 =  ( MODE14 & !MODE13 &  MODE12 &  MODE11);

                          // S4 position 5,
   NA1  =  ( MODE14 & !MODE13 &  MODE12 &  !MODE11);

                          // S4 position 6,
   NA2  =  ( MODE14 & !MODE13 &  !MODE12 &  MODE11);

                          // S4 position 7,
   DAC_DATA_ZERO  =  ( MODE14 & !MODE13 &  !MODE12 &  !MODE11);

                          // S4 position 8,
   DAC_HDR1_ALL  =  ( !MODE14 & MODE13 &  MODE12 &  MODE11);

                          // S4 position 9,
   DAC_HDR1_IND  =  ( !MODE14 & MODE13 &  MODE12 &  !MODE11);

                          // S4 position A,
   DAC_HDR1_TDM  =  ( !MODE14 & MODE13 &  !MODE12 &  MODE11);
```

```
                        // S4 position B,
   DAC_DUAL_TDM  =  ( !MODE14 & MODE13 &  !MODE12 &  !MODE11);

                        // S4 position C,
   DAC_HDR1_AUX  =  ( !MODE14 & !MODE13 &  MODE12 &  MODE11);

                        // S4 position D,
   NA3  =           ( !MODE14 & !MODE13 &  MODE12 &  !MODE11);

                        // S4 position E,
   NA4  =           ( !MODE14 & !MODE13 &  !MODE12 &  MODE11);

                        // S4 position F,
   DAC_DATA_HIZ  =  ( !MODE14 & !MODE13 &  !MODE12 &  !MODE11);


// Switch S2

   DAC_S/PDIF = (DAC_CLK_SRC1 & DAC_CLK_SRC0);
   DAC_HDR1  = (DAC_CLK_SRC1 & !DAC_CLK_SRC0);
   DAC_ADC   = (!DAC_CLK_SRC1 & DAC_CLK_SRC0);
   DAC_DAC   = (!DAC_CLK_SRC1 & !DAC_CLK_SRC0);

   ADC_S/PDIF = (ADC_CLK_SRC1 & ADC_CLK_SRC0);
   ADC_HDR1  = (ADC_CLK_SRC1 & !ADC_CLK_SRC0);
   ADC_ADC   = (!ADC_CLK_SRC1 & ADC_CLK_SRC0);
   ADC_DAC   = (!ADC_CLK_SRC1 & !ADC_CLK_SRC0);

 "================================================================================
EQUATIONS

S/PDIF_RESET_OUT = S/PDIF_RESET_IN;

// Configuration of the CS8416, changes active on reset, BCLK_8416 and LRCLK_8416 are bi-
directional signals.
   SOMS_RX                 =                              DAC_S/PDIF;

                                                        // SOMS = Serial Output Master/Slave Select
   SFSEL1_RX               =                              0; //DIR_RJ # DIR_RJ16;
                           // SFSEL1 = Serial Format Select 1
   SFSEL0_RX               =                              1; //DIR_I2S # DIR_DSP;
                           // SFSEL0 = Serial Format Select 0
   RMCKF_RX                =                              !S/PDIF_MCLK_RATE;
                                                                                    // RMCKF =
Receive Master Clock Frequency

 //   M0_8414 = (0 # !DAC_S/PDIF);
 //   M1_8414 = 1;
 //   M2_8414 = 0;
```

```
 //  M3_8414 = 0;

// CS8404 Tx interface mode select
                          APMS_TX = 0; // Tx serial port is always slave in this application
                          SFMT1_TX = 0;  // Tx data format is I2S always
                          SFMT0_TX = 1;

 //   M0_8404 = 0;
 //   M1_8404 = 0;
 //   M2_8404 = 1;  // I2S format only

// divide 256Fs clock by 2 for 128Fs clock to the the S/PDIF Tx
//    Qdivide.clk =  CPLD_MCLK;
//   Qdivide.d = !Qdivide;

//    MCLK_8406 = Qdivide;
                          MCLK_8406 = CPLD_MCLK;
    BCLK_8406 = I_ABCLK;
    LRCLK_8406 = I_ALRCLK;
    SDATA_8406 = (ASDATA1 & S/PDIF_OUT_MUX) # (ASDATA2 & !S/PDIF_OUT_MUX);

// For SPI mode, let external port drive the SPI port

    DBCLK.oe  = (DAC_S/PDIF  # DAC_HDR1 # DAC_ADC # !DAC_DAC) & (DAC_CLK_OFF);
    DLRCLK.oe = (DAC_S/PDIF  # DAC_HDR1 # DAC_ADC # !DAC_DAC) & (DAC_CLK_OFF);
    ABCLK.oe  = (ADC_S/PDIF  # ADC_HDR1 # !ADC_ADC # ADC_DAC) & (ADC_CLK_OFF);
    ALRCLK.oe = (ADC_S/PDIF  # ADC_HDR1 # !ADC_ADC # ADC_DAC) & (ADC_CLK_OFF);

    HDR1_DBCLK.oe  = (DAC_S/PDIF  # !DAC_HDR1 # DAC_ADC # DAC_DAC);
    HDR1_DLRCLK.oe = (DAC_S/PDIF  # !DAC_HDR1 # DAC_ADC # DAC_DAC);
    HDR1_ABCLK.oe  = (ADC_S/PDIF  # !ADC_HDR1 # ADC_ADC # ADC_DAC);
    HDR1_ALRCLK.oe = (ADC_S/PDIF  # !ADC_HDR1 # ADC_ADC # ADC_DAC);

    BCLK_8416.oe  = (!DAC_S/PDIF);
    LRCLK_8416.oe = (!DAC_S/PDIF);
    BCLK_8416     = I_DBCLK;
    LRCLK_8416    = I_DLRCLK;

    DSDATA1.oe  = (!DAC_DATA_HIZ);
    DSDATA2.oe  = (!(DAC_HDR1_TDM # DAC_DUAL_TDM # DAC_DATA_HIZ));  //DSDATA2 is output in DAC
TDM-daisy chain mode
    DSDATA3.oe  = (!DAC_DATA_HIZ);
    DSDATA4.oe  = (!(DAC_DUAL_TDM # ADC_HDR_AUX # DAC_HDR1_AUX # DAC_DATA_HIZ));   // SECOND
TDM-OUT IN DUAL LINE DAC TDM MODE
    ASDATA2.oe  = (ADC_HDR_TDM);  //ASDATA2 is input in ADC TDM mode

    HDR1_DSDATA2.oe = (DAC_HDR1_TDM # DAC_DUAL_TDM);
```

```
    HDR1_DSDATA4.oe = (DAC_DUAL_TDM # ADC_HDR_AUX # DAC_HDR1_AUX);
    HDR1_ASDATA2.oe = (!ADC_HDR_TDM);

    DBCLK    = I_DBCLK;
    DLRCLK   = I_DLRCLK;
    ABCLK    = I_ABCLK;
    ALRCLK   = I_ALRCLK;

    DSDATA1  = (HDR1_DSDATA1 & (DAC_HDR1_ALL # DAC_HDR1_IND # DAC_RX_2 # DAC_RX_3 # DAC_RX_4 #
DAC_HDR1_TDM # DAC_DUAL_TDM # ADC_HDR_AUX))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_1)) # (0 & DAC_DATA_ZERO);
    DSDATA2  = (HDR1_DSDATA1 & DAC_HDR1_ALL) # (HDR1_DSDATA2 & (DAC_HDR1_IND # ADC_HDR_AUX #
DAC_HDR1_AUX # DAC_RX_1 # DAC_RX_3 # DAC_RX_4))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_2)) # (0 & DAC_DATA_ZERO);
    DSDATA3  = (HDR1_DSDATA1 & (DAC_HDR1_ALL)) # (HDR1_DSDATA3 & (DAC_HDR1_IND # DAC_DUAL_TDM #
ADC_HDR_AUX # DAC_HDR1_AUX # DAC_RX_1 # DAC_RX_2 # DAC_RX_4))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_3)) # (0 & DAC_DATA_ZERO);
    DSDATA4  = (HDR1_DSDATA1 & (DAC_HDR1_ALL)) # (HDR1_DSDATA4 & (DAC_HDR1_IND # DAC_RX_1 #
DAC_RX_2 # DAC_RX_3))
              # (SDATA_8416 & (DAC_RX_ALL # DAC_RX_4)) # (0 & DAC_DATA_ZERO);

    HDR1_DBCLK  = I_DBCLK;
    HDR1_DLRCLK = I_DLRCLK;
    HDR1_ABCLK  = I_ABCLK;
    HDR1_ALRCLK = I_ALRCLK;

    HDR1_ASDATA1 = (ASDATA1 & (ADC_HDR_NORMAL # ADC_HDR_TDM # ADC_HDR_AUX # DAC_HDR1_AUX )) #
(ASDATA2 & ADC_HDR_DATA2_DATA1);
    HDR1_ASDATA2 = ASDATA2;
    ASDATA2 = HDR1_ASDATA2;

    HDR1_DSDATA2 = DSDATA2;
    HDR1_DSDATA4 = DSDATA4;

// Internal node signals
    I_DBCLK   = (BCLK_8416 & DAC_S/PDIF) # (HDR1_DBCLK & DAC_HDR1) # (DBCLK & DAC_DAC) #
(I_ABCLK & DAC_ADC);

    I_DLRCLK  = (LRCLK_8416 & DAC_S/PDIF) # (HDR1_DLRCLK & DAC_HDR1) # (DLRCLK & DAC_DAC) #
(I_ALRCLK & DAC_ADC);

    I_ABCLK   = (BCLK_8416 & ADC_S/PDIF) # (HDR1_ABCLK & ADC_HDR1) # (ABCLK & ADC_ADC) #
(I_DBCLK & ADC_DAC);

    I_ALRCLK  = (LRCLK_8416 & ADC_S/PDIF) # (HDR1_ALRCLK & ADC_HDR1) # (ALRCLK & ADC_ADC) #
(I_DLRCLK & ADC_DAC);
"================================================================================

END IF_Logic
```