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32-Channel, 3 V/5 V, Single-Supply, 14-Bit *dense*DAC

Data Sheet

AD5382

FEATURES

- Guaranteed monotonic
- INL error: ±4 LSB max
- On-chip 1.25 V/2.5 V, 10 ppm/°C reference
- Temperature range: −40°C to +85°C
- Rail-to-rail output amplifier
- Power-down mode
- Package type: 100-lead LQFP (14 mm × 14 mm)
- User interfaces
  - Parallel
  - Serial (SPI®-/QSPI™-/MICROWIRE™-/DSP-compatible, featuring data readback)
  - I²C-compatible
- Robust 6.5 kV HBM and 2 kV FICDM ESD rating

INTEGRATED FUNCTIONS

- Channel monitor
- Simultaneous output update via $\overline{\text{LDAC}}$
- Clear function to user-programmable code
- Amplifier boost mode to optimize slew rate
- User-programmable offset and gain adjust
- Toggle mode enables square wave generation
- Thermal monitor

APPLICATIONS

- Variable optical attenuators (VOAs)
- Level setting (ATE)
- Optical micro-electro-mechanical systems (MEMS)
- Control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

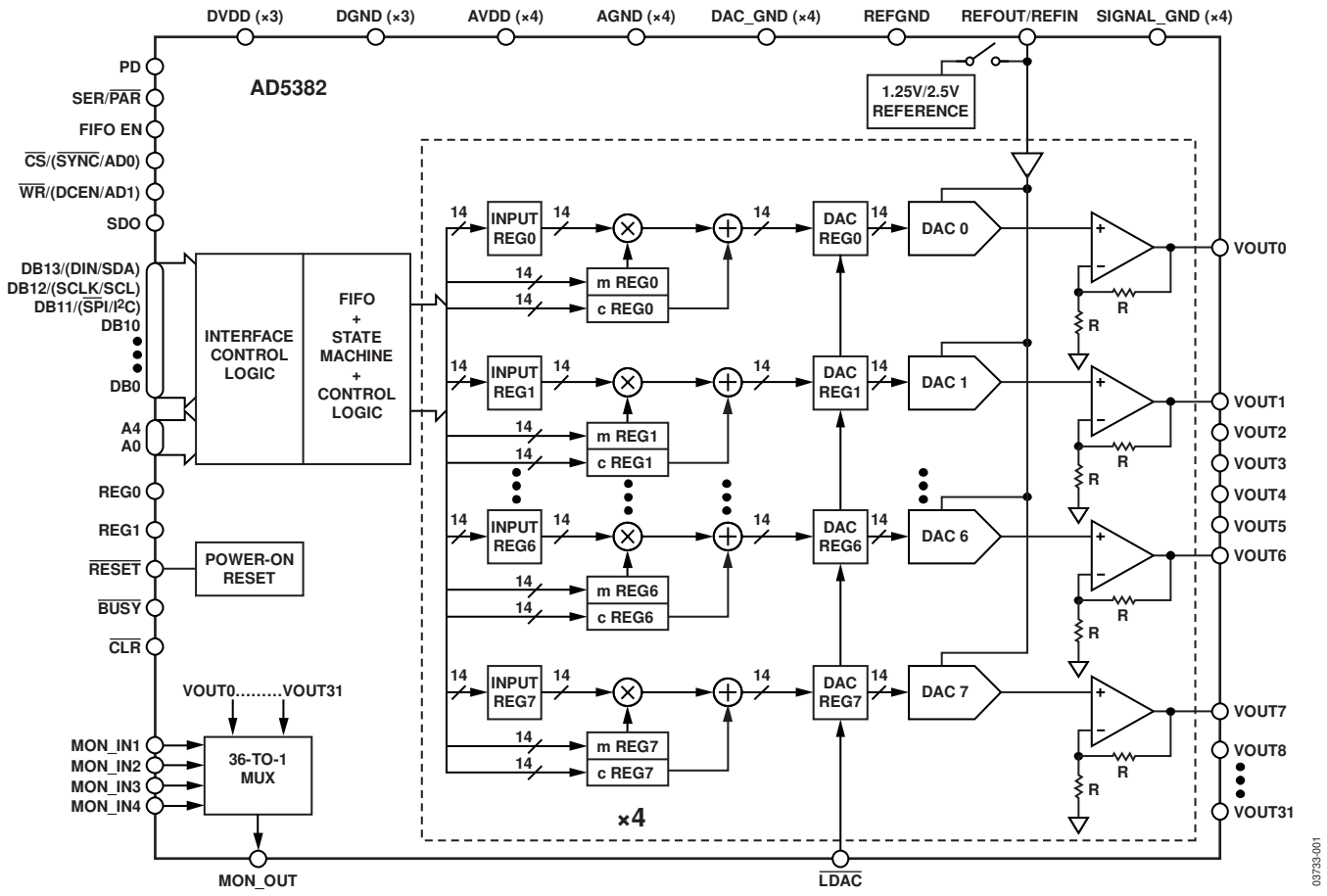

Figure 1.

Rev. D Document Feedback

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COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD5382 Evaluation Board

DOCUMENTATION

Application Notes

- AN-1225: 32 Channels of Programmable Voltage with Excellent Temperature Drift Performance Using the AD5382 DAC
- AN-1226: AD5382 Channel Monitor Function

Data Sheet

- AD5382: 32-Channel, 3 V/5 V, Single-Supply, 14-Bit *dense*DAC Data Sheet

Product Highlight

- Extending the *dense*DAC™ Multichannel D/As

User Guides

- UG-757: Evaluating the AD5380/AD5382 40-/32-Channel, 14-Bit Voltage Output DACs with On-Chip Reference

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD5380 IIO Multi-Channel DAC Linux Driver

REFERENCE MATERIALS

Solutions Bulletins & Brochures

- Digital to Analog Converters ICs Solutions Bulletin

Technical Articles

- Software Calibration Reduces D/A Converter Offset and Gain Errors

DESIGN RESOURCES

- AD5382 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

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Changes to Table 6 12
Changes to Soft Reset Section 23
Changes to Reset Function Section 26
Changes to Figure 37 33
Added Power Supply Sequencing Section, Table 18, Figure 38, and Figure 39; Renumbered Sequentially 34
Added Figure 40 and Figure 41 35
Changed ADR280 to ADR3412, Typical Configuration Circuit Section 35

10/12—Rev. B to Rev. C

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5/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5382 is a complete, single-supply, 32-channel, 14-bit *dense*DAC® available in a 100-lead LQFP package. All 32 channels have an on-chip output amplifier with rail-to-rail operation. The AD5382 includes an internal software-selectable 1.25 V/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that allows optimization of the amplifier slew rate.

The AD5382 contains a double-buffered parallel interface, which features a 20 ns $\overline{WR}$ pulse width, an SPI-, QSPI-, MICROWIRE-, DSP-compatible serial interface with interface speeds in excess of 30 MHz and an I²C®-compatible interface that supports a 400 kHz data transfer rate.

An input register followed by a DAC register provides double buffering, allowing the DAC outputs to be updated independently or simultaneously using the $\overline{LDAC}$ input.

Each channel has a programmable gain and offset adjust register that allows the user to fully calibrate any DAC channel. Power consumption is typically 0.25 mA per channel when operating with boost mode disabled.

SPECIFICATIONS

AD5382-5 SPECIFICATIONS

AVDD = 4.5 V to 5.5 V; DVDD = 2.7 V to 5.5 V, AGND = DGND = 0 V; External REFIN = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD5382-5[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy[2] (INL)	±4	LSB max	
Differential Nonlinearity (DNL)	−1/+2	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at Code 32 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.05	% FSR max	At 25°C
	±0.06	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	1	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	2.5	V	±1% for specified performance, AVDD = 2xREFIN + 50 mV
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to AVDD/2	V min/max	
Reference Output[4]			Enabled via CR10 in the AD5382 control register; CR12 selects the reference voltage
Output Voltage	2.495/2.505	V min/max	At ambient; CR12 = 1; optimized for 2.5 V operation
	1.22/1.28	V min/max	1.25 V reference selected; CR12 = 0
Reference TC	±10	ppm/°C max	Temperature range: +25°C to +85°C
	±15	ppm/°C max	Temperature range: –40°C to +85°C
Output Impedance	800	Ω typ	
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	0/AVDD	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.6	Ω max	
MONITOR PIN			
Output Impedance	1	kΩ typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DVDD = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage			
DVDD > 3.6 V	0.8	V max	
DVDD ≤ 3.6 V	0.6	V max	
Input Current	±1	µA max	Total for all pins, $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	

Parameter	AD5382-5[1]	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL ONLY)[3]			
V_{IH}, Input High Voltage	0.7 × DVDD	V min	SMBus-compatible at DVDD < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DVDD	V max	SMBus-compatible at DVDD < 3.6 V
I_{IN}, Input Leakage Current	±1	µA max	
V_{HYST}, Input Hysteresis	0.05 × DVDD	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	DVDD = 5 V ± 10%, sinking 200 µA
V_{OH}, Output High Voltage	DVDD – 1	V min	DVDD = 5 V ± 10%, sourcing 200 µA
V_{OL}, Output Low Voltage	0.4	V max	DVDD = 2.7 V to 3.6 V, sinking 200 µA
V_{OH}, Output High Voltage	DVDD – 0.5	V min	DVDD = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AVDD	4.5/5.5	V min/max	
DVDD	2.7/5.5	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	–85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded, boost off. 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded, boost on. 0.325 mA/channel typ
DI_{DD}	1	mA max	V_{IH} = DVDD, V_{IL} = DGND.
AI_{DD} (Power-Down)	20	µA max	Typically 100 nA
DI_{DD} (Power-Down)	20	µA max	Typically 1 µA
Power Dissipation	65	mW max	Outputs unloaded, boost off, AVDD = DVDD = 5 V

[1] AD5382-5 is calibrated using an external 2.5 V reference. Temperature range for all versions: –40°C to +85°C.
[2] Accuracy guaranteed from VOUT = 10 mV to AVDD – 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5382-5 is 2.5 V. Programmable to 1.25 V via CR12 in the AD5382 control register; operating the AD5382-5 with a 1.25 V reference leads to degraded accuracy specifications.

AD5382-3 SPECIFICATIONS

AVDD = 2.7 V to 3.6 V; DVDD = 2.7 V to 5.5 V, AGND = DGND = 0 V; external REFIN = 1.25 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	AD5382-3[1]	Unit	Test Conditions/Comments
ACCURACY			
Resolution	14	Bits	
Relative Accuracy[2] (INL)	±4	LSB max	
Differential Nonlinearity (DNL)	−1/+2	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	mV max	
Offset Error	±4	mV max	Measured at Code 64 in the linear region
Offset Error TC	±5	µV/°C typ	
Gain Error	±0.05	% FSR max	At 25°C
	±0.1	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[3]	2	ppm FSR/°C typ	
DC Crosstalk[3]	1	LSB max	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	1.25	V	±1% for specified performance
DC Input Impedance	1	MΩ min	Typically 100 MΩ
Input Current	±1	µA max	Typically ±30 nA
Reference Range	1 to AVDD/2	V min/max	
Reference Output[4]			Enabled via CR10 in the AD5382 control register, CR12 selects the reference voltage
Output Voltage	1.245/1.255	V min/max	At ambient; CR12 = 0; optimized for 1.25 V operation
	2.47/2.53	V min/max	2.5 V reference selected; CR12 = 1
Reference TC	±10	ppm/°C max	Temperature Range: +25°C to +85°C
	±15	ppm/°C max	Temperature Range: −40°C to +85°C
Output Impedance	800	Ω typ	
OUTPUT CHARACTERISTICS[3]			
Output Voltage Range[2]	0/AVDD	V min/max	
Short-Circuit Current	40	mA max	
Load Current	±1	mA max	
Capacitive Load Stability			
$R_L = \infty$	200	pF max	
R_L = 5 kΩ	1000	pF max	
DC Output Impedance	0.6	Ω max	
MONITOR PIN (MON OUT)			
Output Impedance	1	kΩ typ	
Three-State Leakage Current	100	nA typ	
LOGIC INPUTS (EXCEPT SDA/SCL)[3]			DVDD = 2.7 V to 3.6 V
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage			
DVDD > 3.6 V	0.8	V max	
DVDD ≤ 3.6 V	0.6	V max	
Input Current	±1	µA max	Total for all pins, $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	pF max	
LOGIC INPUTS (SDA, SCL ONLY)[3]			
V_{IH}, Input High Voltage	0.7 × DVDD	V min	SMBus-compatible at DVDD < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DVDD	V max	SMBus-compatible at DVDD < 3.6 V
I_{IN}, Input Leakage Current	±1	µAmax	
V_{HYST}, Input Hysteresis	0.05 × DVDD	V min	
C_{IN}, Input Capacitance	8	pF typ	
Glitch Rejection	50	ns max	Input filtering suppresses noise spikes of less than 50 ns

Parameter	AD5382-3[1]	Unit	Test Conditions/Comments
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[3]			
V_{OL}, Output Low Voltage	0.4	V max	Sinking 200 µA
V_{OH}, Output High Voltage	DVDD – 0.5	V min	Sourcing 200 µA
High Impedance Leakage Current	±1	µA max	SDO only
High Impedance Output Capacitance	5	pF typ	SDO only
LOGIC OUTPUT (SDA)[3]			
V_{OL}, Output Low Voltage	0.4	V max	I_{SINK} = 3 mA
	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	µA max	
Three-State Output Capacitance	8	pF typ	
POWER REQUIREMENTS			
AVDD	2.7/3.6	V min/max	
DVDD	2.7/5.5	V min/max	
Power Supply Sensitivity[3]			
ΔMidscale/ΔAV_{DD}	–85	dB typ	
AI_{DD}	0.375	mA/channel max	Outputs unloaded; boost off; 0.25 mA/channel typ
	0.475	mA/channel max	Outputs unloaded; boost on; 0.325 mA/channel typ
DI_{DD}	1	mA max	V_{IH} = DVDD V_{IL} = DGND
AI_{DD} (Power-Down)	20	µA max	Typically 100 nA
DI_{DD} (Power-Down)	20	µA max	Typically 1 µA
Power Dissipation	39	mW max	Outputs unloaded; boost off; AVDD = DVDD = 3 V

[1] AD5382-3 is calibrated using an external 1.25 V reference. Temperature range is –40°C to +85°C.
[2] Accuracy guaranteed from VOUT = 10 mV to AVDD – 50 mV.
[3] Guaranteed by characterization, not production tested.
[4] Default on the AD5382-5 is 2.5 V. Programmable to 1.25 V via CR12 in the AD5382 control register; operating the AD5382-5 with a 1.25 V reference leads to degraded accuracy specifications.

AC CHARACTERISTICS[1]

AVDD = 4.5 V to 5.5 V or 2.7 V to 3.6 V; DVDD = 2.7 V to 5.5 V; AGND = DGND= 0 V.

Table 3.

Parameter	All	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time[2]			1/4 scale to 3/4 scale change settling to ±1 LSB
	3	µs typ	
	8	µs max	
Slew Rate[2]	1.5	V/µs typ	Boost mode off, CR11 = 0
	2.5	V/µs typ	Boost mode on, CR11 = 1
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
DAC-to-DAC Crosstalk	1	nV-s typ	See the Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz	15	µV p-p typ	External reference, midscale loaded to DAC
	40	µV p-p typ	Internal reference, midscale loaded to DAC
Output Noise Spectral Density			
At 1 kHz	150	nV/√Hz typ	
At 10 kHz	100	nV/√Hz typ	

[1] Guaranteed by design and characterization, not production tested.
[2] The slew rate can be programmed via the current boost control bit (CR11) in the AD5382 control register.

TIMING CHARACTERISTICS

SPI-, QSPI-, MICROWIRE-, OR DSP-COMPATIBLE SERIAL INTERFACE

DVDD = 2.7 V to 5.5 V; AVDD = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5 [4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ falling edge
t_6 [4]	33	ns min	Minimum $\overline{SYNC}$ low time
t_7	10	ns min	Minimum $\overline{SYNC}$ high time
t_{7A}	140	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_8	5	ns min	Data setup time
t_9	4.5	ns min	Data hold time
t_{10}[4]	36	ns max	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{11}	670	ns max	$\overline{BUSY}$ pulse width low (single channel update)
t_{12} [4]	20	ns min	24th SCLK falling edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	100/2000	ns min/max	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	3	µs typ	DAC output settling time; boost mode off
t_{18}	20	ns min	$\overline{CLR}$ pulse width low
t_{19}	40	µs max	$\overline{CLR}$ pulse activation time
t_{20}[5]	30	ns max	SCLK rising edge to SDO valid
t_{21}[5]	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{22}[5]	8	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{23}	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_r = t_f = 5$ ns (10% to 90% of V_{CC}) and are timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.
[4] Standalone mode only.
[5] Daisy-chain mode only.

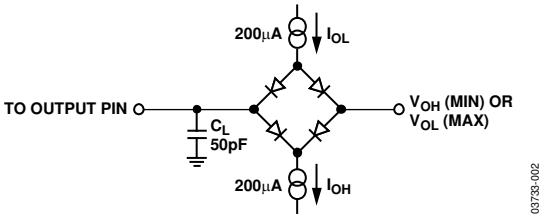

Figure 2. Load Circuit for SDO Timing Diagram (Serial Interface, Daisy-Chain Mode)

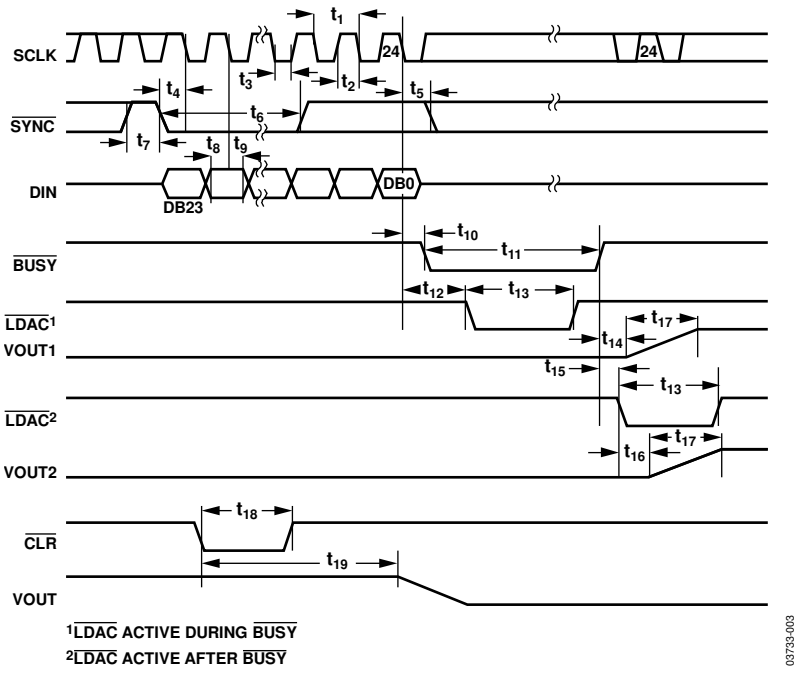

Figure 3. Serial Interface Timing Diagram (Standalone Mode)

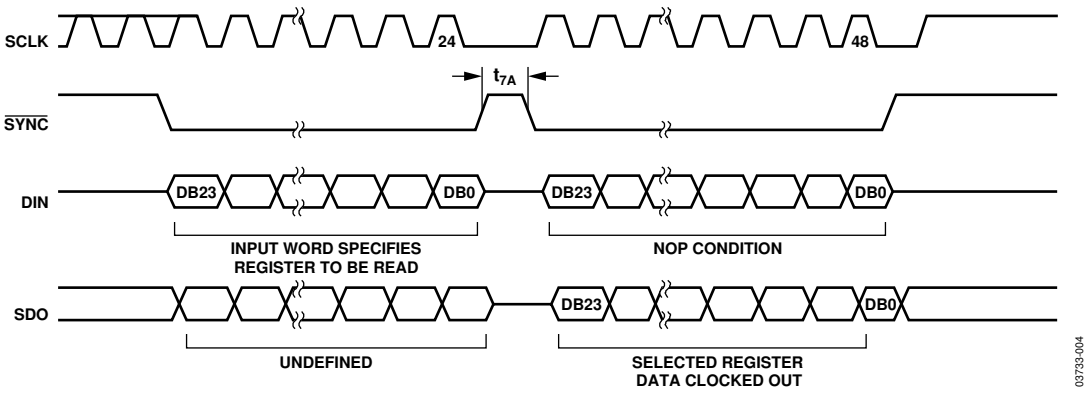

Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

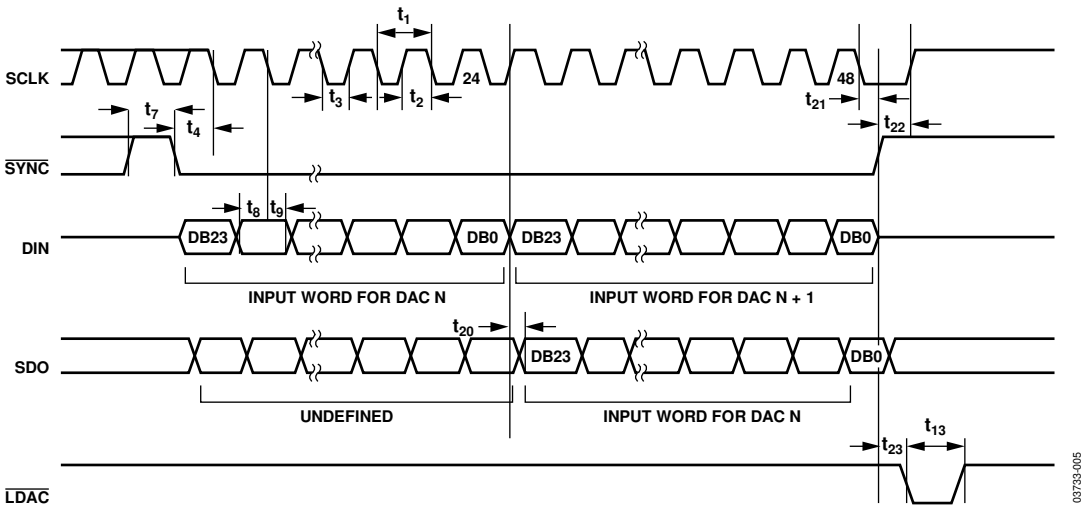

Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

I²C SERIAL INTERFACE

DVDD = 2.7 V to 5.5 V; AVDD = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
f_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD,STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU,DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD,DAT}$, data hold time
	0	µs min	$t_{HD,DAT}$, data hold time
t_7	0.6	µs min	$t_{SU,STA}$, setup time for repeated start
t_8	0.6	µs min	$t_{SU,STO}$, stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_R, rise time of SCL and SDA when receiving
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS-compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS-compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	$20 + 0.1C_b$[4]	ns min	t_F, fall time of SCL and SDA when transmitting
C_b	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization, not production tested.
[2] See Figure 6.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of SCL's falling edge.
[4] C_b is the total capacitance, in pF, of one bus line. t_R and t_F are measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

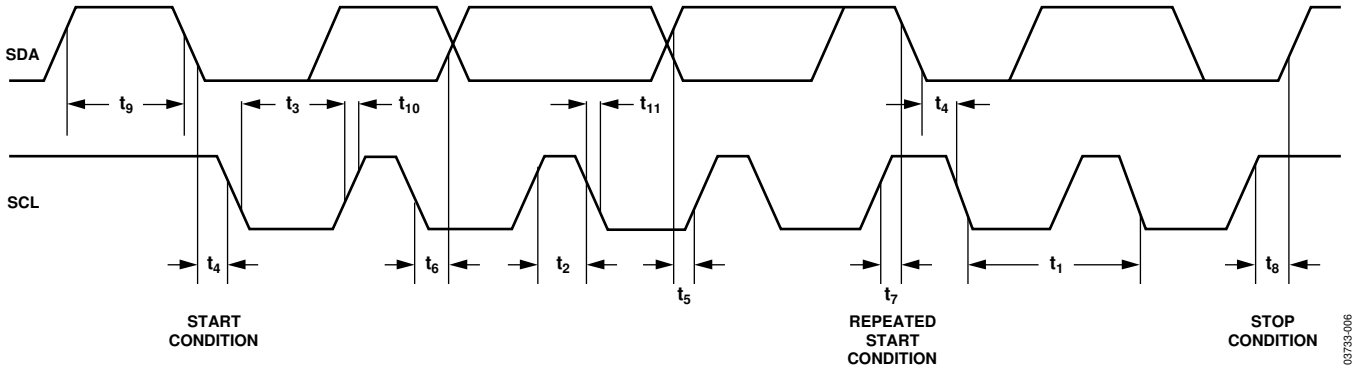

Figure 6. I²C-Compatible Serial Interface Timing Diagram

PARALLEL INTERFACE

DVDD = 2.7 V to 5.5 V; AVDD = 4.5 V to 5.5 V or 2.7 V to 3.6 V; AGND = DGND = 0 V; all specifications Tmin to Tmax, unless otherwise noted.

Table 6.

Parameter[1, 2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_0	4.5	ns min	REG0, REG1, address to $\overline{WR}$ rising edge setup time
t_1	4.5	ns min	REG0, REG1, address to $\overline{WR}$ rising edge hold time
t_2	20	ns min	$\overline{CS}$ pulse width low
t_3	20	ns min	$\overline{WR}$ pulse width low
t_4	0	ns min	$\overline{CS}$ to $\overline{WR}$ falling edge setup time
t_5	0	ns min	$\overline{WR}$ to $\overline{CS}$ rising edge hold time
t_6	4.5	ns min	Data to $\overline{WR}$ rising edge setup time
t_7	4.5	ns min	Data to $\overline{WR}$ rising edge hold time
t_8	20	ns min	$\overline{WR}$ pulse width high
t_9[4]	700	ns min	Minimum $\overline{WR}$ cycle time (single-channel write)
t_{10}[4]	30	ns max	$\overline{WR}$ rising edge to $\overline{BUSY}$ falling edge
t_{11}[4, 5]	670	ns max	$\overline{BUSY}$ pulse width low (single-channel update)
t_{12}	30	ns min	$\overline{WR}$ rising edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	20	ns min	$\overline{LDAC}$ rising edge to $\overline{WR}$ rising edge
t_{16}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{17}	100/2000	ns min/max	$\overline{LDAC}$ falling edge to DAC output response time
t_{18}	2	µs typ	DAC output settling time
t_{19}	20	ns min	$\overline{CLR}$ pulse width low
t_{20}	40	µs max	$\overline{CLR}$ pulse activation time

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with $t_R = t_R = 5$ ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.2 V.
[3] See Figure 7.
[4] See Figure 28.
[5] Measured with the load circuit of Figure 2.

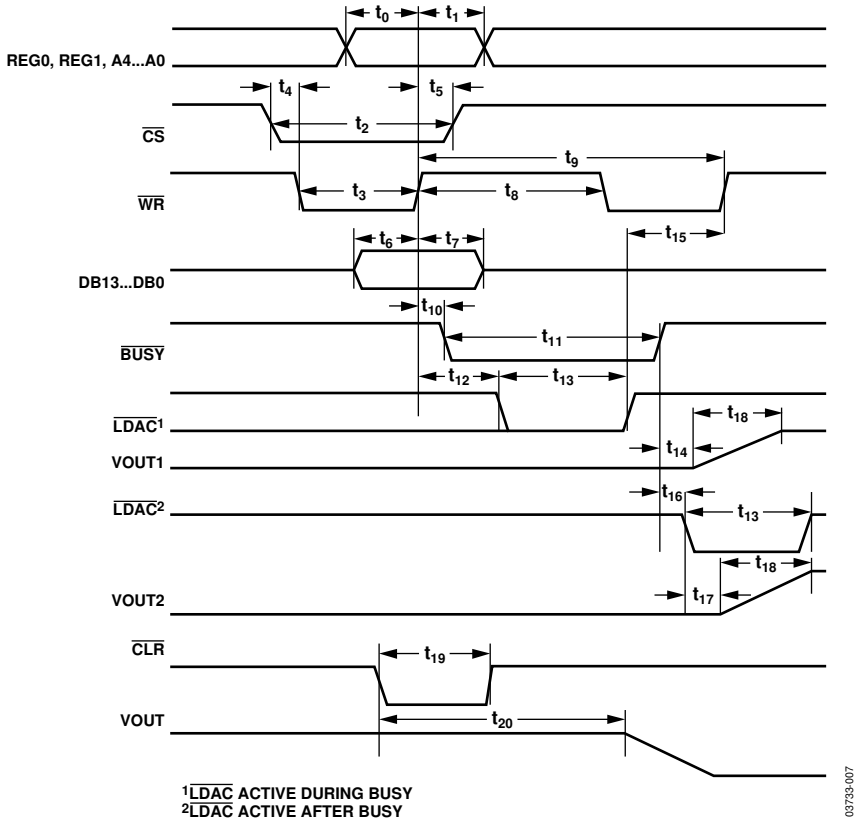

Figure 7. Parallel Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted[1].

Table 7.

Parameter	Rating
AVDD to AGND	–0.3 V to +7 V
DVDD to DGND	–0.3 V to +7 V
Digital Inputs to DGND	–0.3 V to DVDD + 0.3 V
SDA/SCL to DGND	–0.3 V to + 7 V
Digital Outputs to DGND	–0.3 V to DVDD + 0.3 V
REFIN/REFOUT to AGND	–0.3 V to AVDD + 0.3 V
AGND to DGND	–0.3 V to +0.3 V
VOUTx to AGND	–0.3 V to AVDD+ 0.3 V
Analog Inputs to AGND	–0.3 V to AVDD + 0.3 V
MON_IN Inputs to AGND	–0.3 V to AVDD + 0.3 V
MON_OUT to AGND	–0.3 V to AVDD + 0.3 V
Operating Temperature Range	
Commercial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	150°C
100-lead LQFP Package	
θ_{JA} Thermal Impedance	44°C/W
Reflow Soldering	
Peak Temperature	230°C
ESD	
HBM	6.5 kV
FICDM	2 kV

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

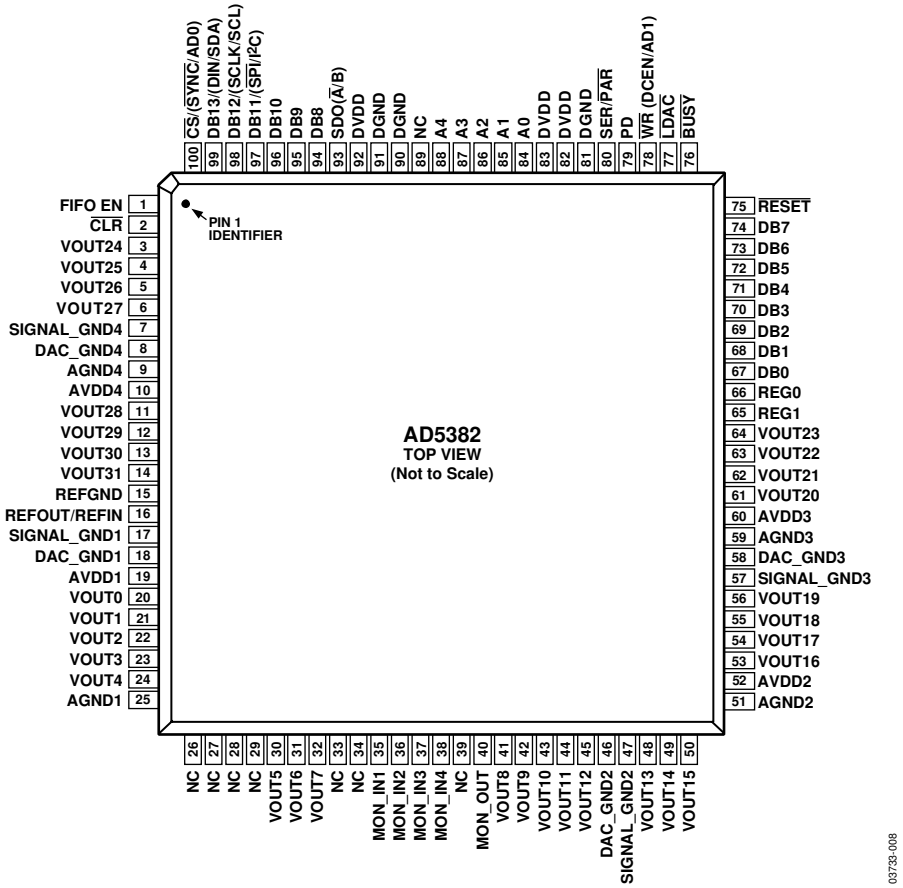

Figure 8. 100-Lead LQFP Pin Configuration

Table 8. Pin Function Descriptions

Mnemonic	Function
VOUTx	Buffered Analog Outputs for Channel x. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
SIGNAL_GND(1–4)	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GND pins are tied together internally and should be connected to the AGND plane as close as possible to the AD5382.
DAC_GND(1–4)	Ground Reference point for the Internal 14-Bit DAC. Each group of eight channels contains a DAC_GND pin. These pins should be connected to the AGND plane.
AGND(1–4)	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AVDD(1–4)	Analog Supply Pins. Each group of eight channels has a separate AVDD pin. These pins are internally shorted and should be decoupled with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range for the AD5382-5 is 4.5 V to 5.5 V; operating range for the AD5382-3 is 2.7 V to 3.6 V.
DGND	Ground for All Digital Circuitry.
DVDD	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. It is recommended that these pins be decoupled with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
REFGND	Ground Reference Point for the Internal Reference.
REFOUT/REFIN	Reference Output when the Internal Reference is Selected. The AD5382 contains a common REFOUT/REFIN pin. If the application requires an external reference, it can be applied to this pin, and the internal reference can be disabled via the control register. The default for this pin is a reference input.
MON_OUT	Monitor Output. When the monitor function is enabled, this pin acts as the output of a 36-to-1 channel multiplexer that can be programmed to multiplex one of Channels 0 to 31 or any of the monitor input pins (MON_IN1 to MON_IN4) to the MON_OUT pin. The MON_OUT pin's output impedance is typically 500 Ω and is intended to drive a high input impedance like that exhibited by SAR ADC inputs.

Mnemonic	Function
MON_INx	Monitor Input Pins. The AD5382 contains four monitor input pins that allow the user to connect input signals, within the maximum ratings of the device, to these pins for monitoring purposes. Any of the signals applied to the MON_IN pins, along with the 32 output channels, can be switched to the MON_OUT pin via software. For example, an external ADC can be used to monitor these signals.
SER/$\overline{PAR}$	Interface Select Input. This pin allows the user to select whether the serial or parallel interface is used. If it is tied high, the serial interface mode is selected and Pin 97 ($\overline{SPI}$/I²C) is used to determine if the interface mode is SPI or I²C. Parallel interface mode is selected when SER/$\overline{PAR}$ is low.
$\overline{CS}$/($\overline{SYNC}$/AD0)	In parallel interface mode, this pin acts as the chip select input (level sensitive, active low). When low, the AD5382 is selected. In serial interface mode, this is the frame synchronization input signal for the serial clocks before the addressed register is updated. In I²C mode, this pin acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I²C bus.
$\overline{WR}$/(DCEN/AD1)	Multifunction Pin. In parallel interface mode, this pin acts as write enable. In serial interface mode, this pin acts as a daisy-chain enable in SPI mode and as a hardware address pin in I²C mode. Parallel Interface Write Input (Edge Sensitive). The rising edge of $\overline{WR}$ is used in conjunction with $\overline{CS}$ low, and the address bus inputs to write to the selected device registers. Serial Interface. Daisy-chain select input (level sensitive, active high). When high, this signal is used in conjunction with SER/$\overline{PAR}$ high to enable the SPI serial interface daisy-chain mode. I²C Mode. This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I²C bus.
DB13–DB0	Parallel Data Bus. DB13 is the MSB and DB0 is the LSB of the input data-word on the AD5382.
A4–A0	Parallel Address Inputs. A4 to A0 are decoded to address one of the AD5382s 40 input channels. Used in conjunction with the REG1 and REG0 pins to determine the destination register for the input data.
REG1, REG0	In parallel interface mode, REG1 and REG0 are used in decoding the destination registers for the input data. REG1 and REG0 are decoded to address the input data register, offset register, or gain register for the selected channel and are also used to decide the special function registers.
SDO/($\overline{A}$/B)	Serial Data Output in Serial Interface Mode. Three-stateable CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK, and is valid on the falling edge of SCLK. In parallel interface mode, this pin acts as the A or B data register select when writing data to the AD5382s data registers with toggle mode selected (see the Toggle Mode Function section). In toggle mode, the $\overline{LDAC}$ is used to switch the output between the data contained in the A and B data registers. All DAC channels contain two data registers. In normal mode, Data Register A is the default for data transfers.
$\overline{BUSY}$	Digital CMOS Output. $\overline{BUSY}$ goes low during internal calculations of the data (x2) loaded to the DAC data register. During this time, the user can continue writing new data to the x1, c, and m registers, but no further updates to the DAC registers and DAC outputs can take place. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is low, this event is stored. $\overline{BUSY}$ also goes low during power-on reset, and when the $\overline{RESET}$ pin is low. During this time, the interface is disabled and any events on $\overline{LDAC}$ are ignored. A $\overline{CLR}$ operation also brings $\overline{BUSY}$ low.
$\overline{LDAC}$	Load DAC Logic Input (Active Low). If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is inactive (high), the contents of the input registers are transferred to the DAC registers, and the DAC outputs are updated. If $\overline{LDAC}$ is taken low while $\overline{BUSY}$ is active and internal calculations are taking place, the $\overline{LDAC}$ event is stored and the DAC registers are updated when $\overline{BUSY}$ goes inactive. However, any events on $\overline{LDAC}$ during power-on reset or on $\overline{RESET}$ are ignored.
$\overline{CLR}$	Asynchronous Clear Input. The CLR input is falling edge sensitive. When $\overline{CLR}$ is activated, all channels are updated with the data in the $\overline{CLR}$ code register. $\overline{BUSY}$ is low for 35 µs while all channels are being updated with the $\overline{CLR}$ code.
$\overline{RESET}$	Asynchronous Digital Reset Input (Falling Edge Sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence takes 270 µs. The falling edge of $\overline{RESET}$ initiates the $\overline{RESET}$ process and $\overline{BUSY}$ goes low for the duration, returning high when $\overline{RESET}$ is complete. While $\overline{BUSY}$ is low, all interfaces are disabled and all $\overline{LDAC}$ pulses are ignored. When $\overline{BUSY}$ returns high, the part resumes normal operation, and the status of the $\overline{RESET}$ pin is ignored until the next falling edge is detected.
PD	Power Down (Level Sensitive, Active High). PD is used to place the device in to low power mode where the device consumes 2 µA AIDD and 20 µA DIDD. In power-down mode, all internal analog circuitry is placed in low power mode, and the analog output is configured as a high impedance output or provides a 100 kΩ load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.

Mnemonic	Function
FIFO EN	FIFO Enable (Level Sensitive, Active High). When connected to DVDD, the internal FIFO is enabled, allowing the user to write to the device at full speed. FIFO is available only in parallel interface mode. The status of the FIFO EN pin is sampled on power-up, and also following a CLEAR or RESET, to determine if the FIFO is enabled. In either serial or I^2C interface modes, the FIFO EN pin should be tied low.
DB11/($\overline{SPI}$/I^2C)	Multifunction Input Pin. In parallel interface mode, this pin acts as DB11 of the parallel input data-word. In serial interface mode, this pin acts as serial interface mode select. When serial interface mode is selected (SER/$\overline{PAR}$ = 1) and this input is low, SPI mode is selected. In SPI mode, DB12 is the serial clock (SCLK) input and DB13 is the serial data (DIN) input. When serial interface mode is selected (SER/$\overline{PAR}$ = 1) and this input is high, I^2C mode is selected. In this mode, DB12 is the serial clock (SCL) input and DB13 is the serial data (SDA) input.
DB12/(SCLK/SCL)	Multifunction Input Pin. In parallel interface mode, this pin acts as DB12 of the parallel input data-word. In serial interface mode, this pin acts as a serial clock input. Serial Interface Mode. In serial interface mode, data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 50 MHz. I^2C Mode. In I^2C mode, this pin performs the SCL function, clocking data into the device. The data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
DB13/(DIN/SDA)	Multifunction Data Input Pin. In parallel interface mode, this pin acts as DB13 of the parallel input data-word. Serial Interface Mode. In serial interface mode, this pin acts as the serial data input. Data must be valid on the falling edge of SCLK. I^2C Mode. In I^2C mode, this pin is the serial data pin (SDA) operating as an open-drain input/output.
NC	No Connect. The user is advised not to connect any signals to these pins.

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error, and is expressed in LSB.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and m = all 1s, c = 2^{n-1}

$$VOUT_{(Zero\text{-}Scale)} = 0 \text{ V}$$

Zero-scale error is a measurement of the difference between VOUT (actual) and VOUT (ideal), expressed in mV. It is mainly due to offsets in the output amplifier.

Offset Error
Offset error is a measurement of the difference between VOUT (actual) and VOUT (ideal) in the linear region of the transfer function, expressed in mV. Offset error is measured on the AD5382-5 with Code 32 loaded into the DAC register, and on the AD5382-3 with Code 64.

Gain Error

Gain error is specified in the linear region of the output range between VOUT= 10 mV and VOUT = AVDD – 50 mV. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed in %FSR with the DAC output unloaded.

DC Crosstalk
This is the dc change in the output level of one DAC at midscale in response to a full-scale code (all 0s to all 1s, and vice versa) and output change of all other DACs. It is expressed in LSB.

DC Output Impedance
This is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time
This is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change, and is measured from the $\overline{\text{BUSY}}$ rising edge.

Digital-to-Analog Glitch Energy
This is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one DAC due to both the digital change and to the subsequent analog output change at another DAC. The victim channel is loaded with midscale. DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
This is a measurement of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz in a 1 Hz bandwidth at 10 kHz.

TYPICAL PERFORMANCE CHARACTERISTICS

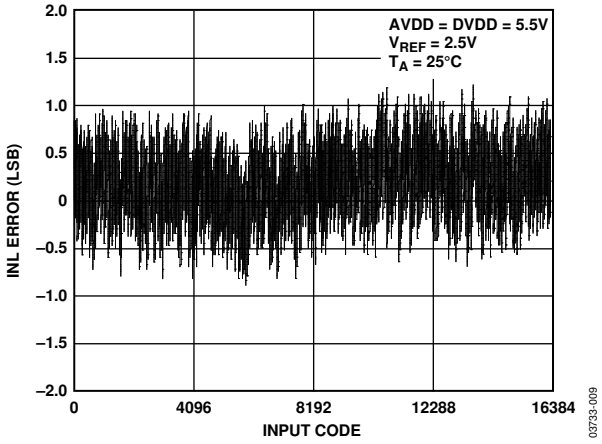

Figure 9. Typical AD5382-5 INL Plot

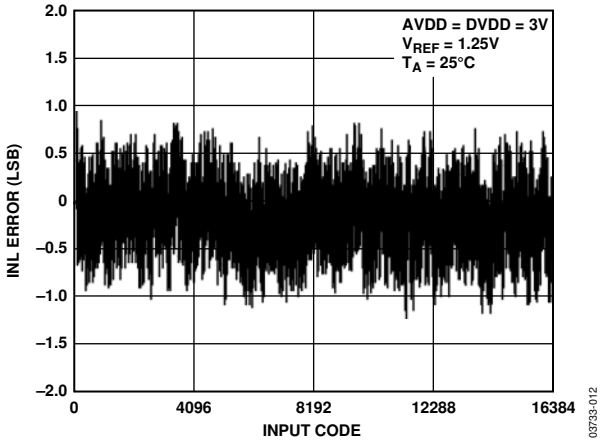

Figure 12. Typical AD5382-3 INL Plot

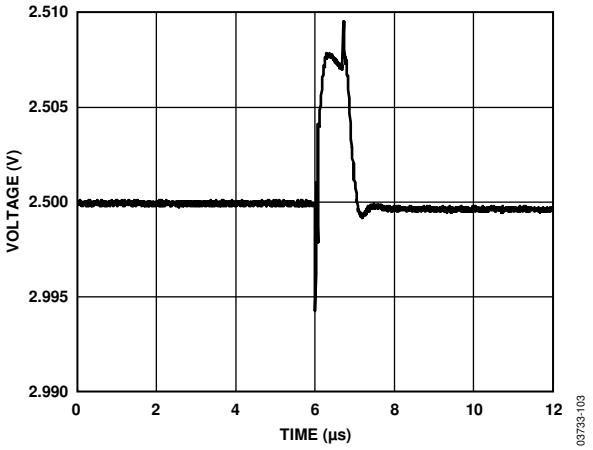

Figure 10. AD5382-5 Glitch Impulse

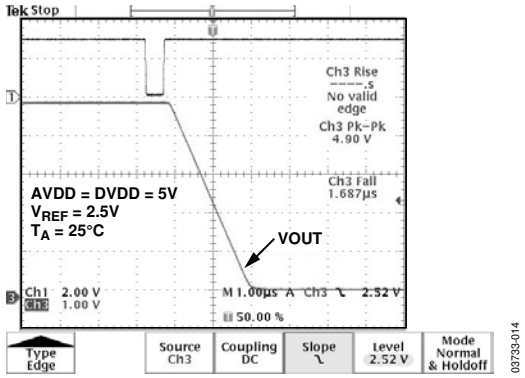

Figure 13. Slew Rate with Boost On

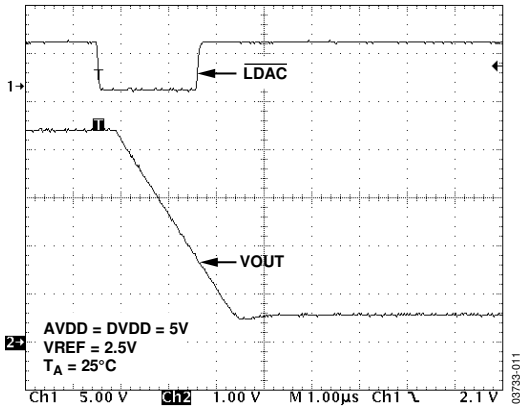

Figure 11. Slew Rate with Boost Off

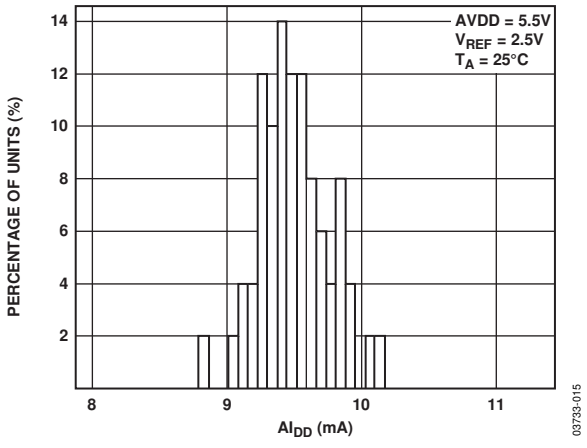

Figure 14. AI_{DD} Histogram

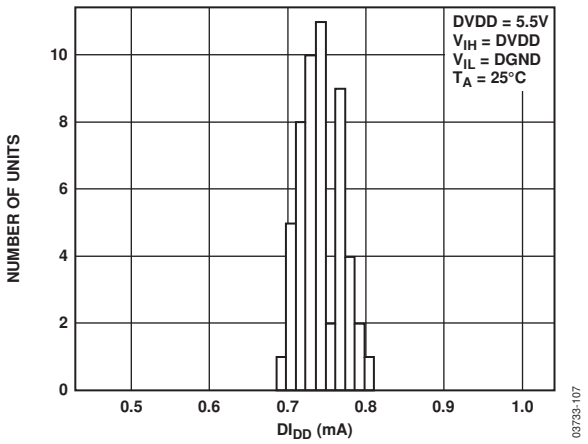

Figure 15. DI_{DD} Histogram

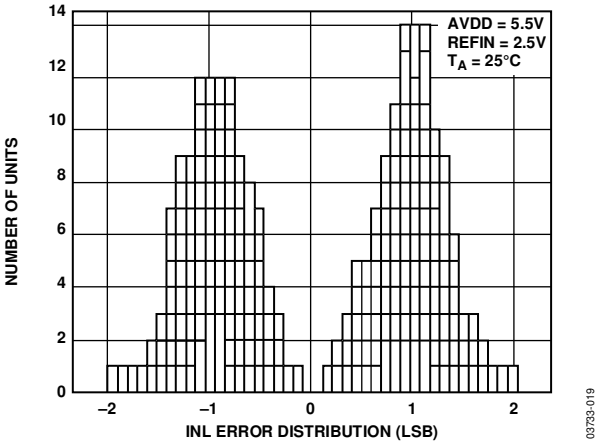

Figure 18. INL Error Distribution

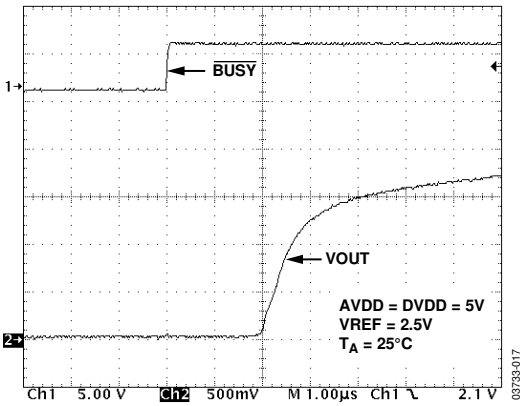

Figure 16. Exiting Soft Power-Down

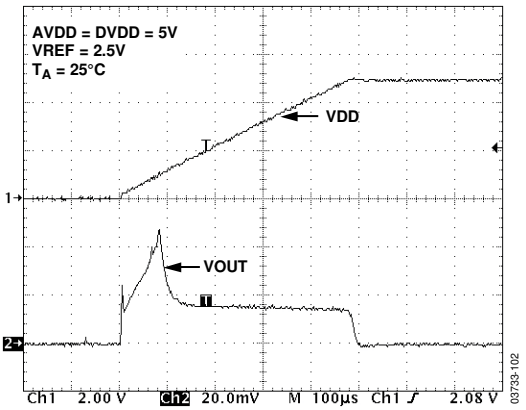

Figure 19. Exiting Hardware Power-Down

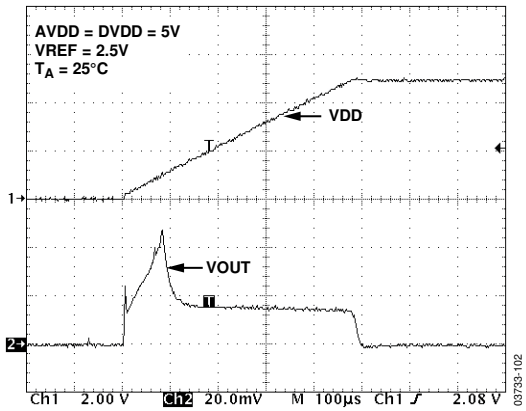

Figure 17. Power-Up Transient

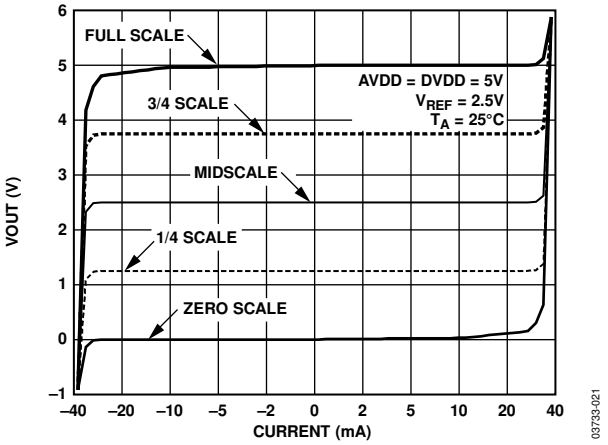

Figure 20. AD5382-5 Output Amplifier Source and Sink Capability

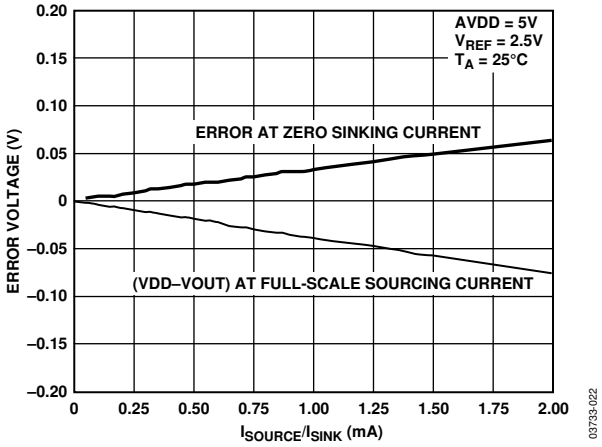

Figure 21. Headroom at Rails vs. Source/Sink Current

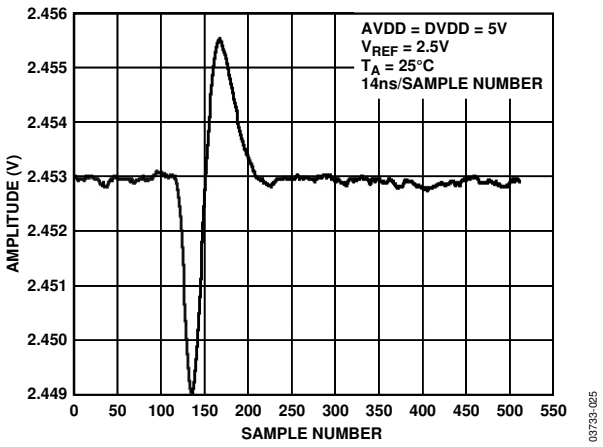

Figure 24. Adjacent Channel DAC-to-DAC Crosstalk

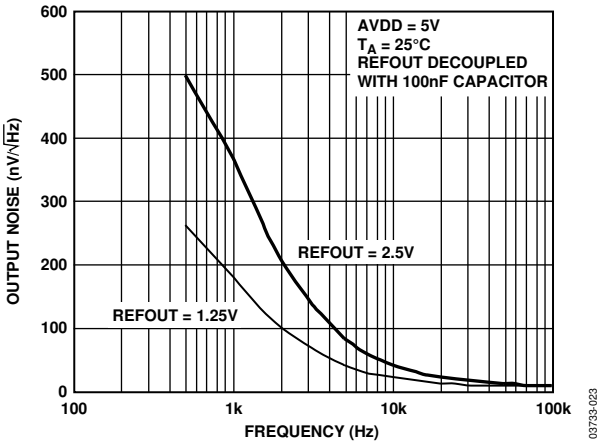

Figure 22 REFOUT Noise Spectral Density

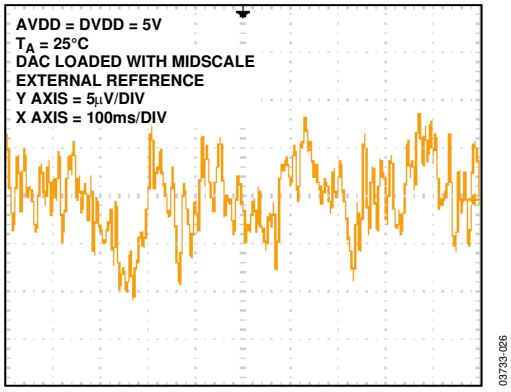

Figure 25. 0.1 Hz to 10 Hz Noise Plot

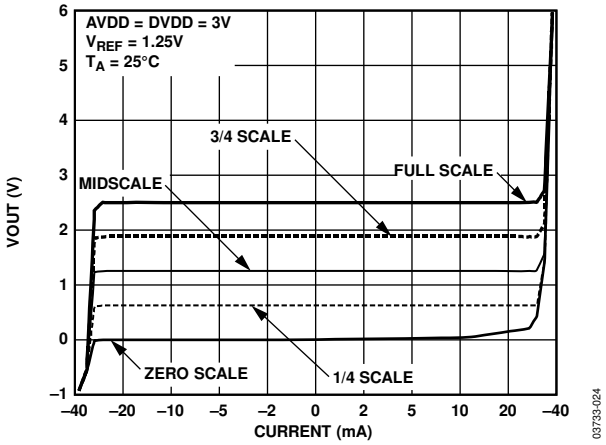

Figure 23. AD5382-3 Output Amplifier Source and Sink Capability

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5382 is a complete, single-supply, 32-channel voltage output DAC that offers 14-bit resolution. The part is available in a 100-lead LQFP package and features both a parallel and a serial interface. This product includes an internal, software-selectable, 1.25 V/2.5 V, 10 ppm/°C reference, which can be used to drive the buffered reference inputs; alternatively, an external reference can be used to drive these inputs. Internal/external reference selection is via the CR10 bit in the control register; CR12 selects the reference magnitude if the internal reference is selected. All channels have an on-chip output amplifier with rail-to-rail output capable of driving 5 kΩ in parallel with a 200 pF load.

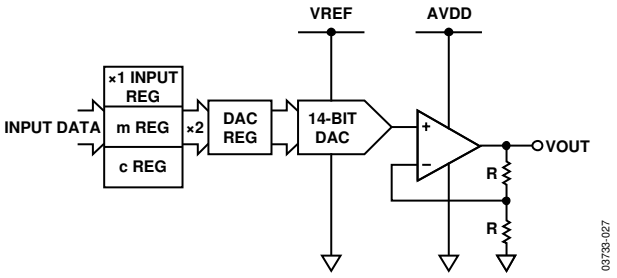

Figure 26. Single-Channel Architecture

The architecture of a single DAC channel consists of a 14-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor-string architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independent offset and gain control registers that allow the user to digitally trim offset and gain. These registers give the user the ability to calibrate out errors in the complete signal chain, including the DAC, using the internal m and c registers, which hold the correction factors. All channels are double buffered, allowing synchronous updating of all channels using the $\overline{\text{LDAC}}$ pin. Figure 26 shows a block diagram of a single channel on the AD5382. The digital input transfer function for each DAC can be represented as

$$x2 = [(m + 2)/2^n \times x1] + (c - 2^{n-1})$$

where:
x2 is the data-word loaded to the resistor string DAC.
x1 is the 14-bit data-word written to the DAC input register.
m is the gain coefficient (default is 0x3FFE on the AD5382). The gain coefficient is written to the 13 most significant bits (DB13 to DB1) and LSB (DB0) is a zero.
n = DAC resolution (*n* = 14 for AD5382).
c is the14-bit offset coefficient (default is 0x2000).

The complete transfer function for these devices can be represented as

$$VOUT = 2 \times V_{REF} \times x2/2^n$$

where:
x2 is the data-word loaded to the resistor string DAC, and V_{REF} is the internal reference voltage, or the reference voltage externally applied to the DAC REFOUT/REFIN pin. For specified performance, an external reference voltage of 2.5 V is recommended for the AD5382-5, and 1.25 V for the AD5382-3.

DATA DECODING

The AD5382 contains a 14-bit data bus, DB13–DB0. Depending on the value of REG1 and REG0 (see Table 9), this data is loaded into the addressed DAC input registers (x1), offset (c) registers, or gain (m) registers. The format data, offset (c), and gain (m) register contents are shown in Table 10 to Table 12.

Table 9. Register Selection

REG1	REG0	Register Selected
1	1	Input Data Register (x1)
1	0	Offset Register (c)
0	1	Gain Register (m)
0	0	Special Function Registers (SFRs)

Table 10. DAC Data Format (REG1 = 1, REG0 = 1)

DB13 to DB0				DAC Output (V)
11	1111	1111	1111	$2 V_{REF} \times (16383/16384)$
11	1111	1111	1110	$2 V_{REF} \times (16382/16384)$
10	0000	0000	0001	$2 V_{REF} \times (8193/16384)$
10	0000	0000	0000	$2 V_{REF} \times (8192/16384)$
01	1111	1111	1111	$2 V_{REF} \times (8191/16384)$
00	0000	0000	0001	$2 V_{REF} \times (1/16384)$
00	0000	0000	0000	0

Table 11. Offset Data Format (REG1 = 1, REG0 = 0)

DB13 to DB0				Offset (LSB)
11	1111	1111	1111	+8191
11	1111	1111	1110	+8190
10	0000	0000	0001	+1
10	0000	0000	0000	0
01	1111	1111	1111	–1
00	0000	0000	0001	–8191
00	0000	0000	0000	–8192

Table 12. Gain Data Format (REG1 = 0, REG0 = 1)

DB13 to DB0				Gain Factor
11	1111	1111	1110	1
10	1111	1111	1110	0.75
01	1111	1111	1110	0.5
00	1111	1111	1110	0.25
00	0000	0000	0000	0

ON-CHIP SPECIAL FUNCTION REGISTERS (SFR)

The AD5382 contains a number of special function registers (SFRs), as outlined in Table 13. SFRs are addressed with REG1 = REG0 = 0 and are decoded using Address Bits A4 to A0.

Table 13. SFR Register Functions (REG1 = 0, REG0 = 0)

R/$\overline{W}$	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	NOP (No Operation)
0	0	0	0	0	1	Write Clear Code
0	0	0	0	1	0	Soft Clear
0	0	1	0	0	0	Soft Power-Down
0	0	1	0	0	1	Soft Power-Up
0	0	1	1	0	0	Control Register Write
1	0	1	1	0	0	Control Register Read
0	0	1	0	1	0	Monitor Channel
0	0	1	1	1	1	Soft Reset

SFR COMMANDS

NOP (No Operation)

REG1 = REG0 = 0, A4–A0 = 00000

Performs no operation but is useful in serial readback mode to clock out data on D_{OUT} for diagnostic purposes. $\overline{BUSY}$ pulses low during a NOP operation.

Write Clear Code

REG1 = REG0 = 0, A4–A0 = 00001
DB13–DB0 = Contain the clear code data

Bringing the $\overline{CLR}$ line low or exercising the soft clear function loads the contents of the DAC registers with the data contained in the user-configurable Clear register, and sets VOUT0 to VOUT31 accordingly. This can be very useful for setting up a specific output voltage in a clear condition. It is also beneficial for calibration purposes; the user can load full scale or zero scale to the clear code register and then issue a hard-ware or software clear to load this code to all DACs, removing the need for individual writes to each DAC. Default on power-up is all zeros.

Soft Clear

REG1 = REG0 = 0, A4–A0 = 00010
DB13–DB0 = Don't Care

Executing this instruction performs a software clear, which is functionally the same as that provided by the external $\overline{CLR}$ pin. The DAC outputs are loaded with the data in the Clear Code. register (Table 13). It takes 35 µs to fully execute the Soft Clear and is indicated by the $\overline{BUSY}$ low time.

Soft Power-Down

REG1 = REG0 = 0, A4–A0 = 01000
DB13–DB0 = Don't Care

Executing this instruction performs a global power-down feature that puts all channels into a low power mode that reduces the analog supply current to 2 µA max and the digital current to 20 µA max. In power-down mode, the output amplifier can be configured as a high impedance output or provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. No register can be written to while in power-down.

Soft Power-Up

REG1 = REG0 = 0, A4–A0 = 01001
DB13–DB0 = Don't Care

This instruction is used to power up the output amplifiers and the internal reference. The time to exit power-down is 8 µs. The hardware power-down and software functions are internally combined in a digital OR function.

Soft RESET

REG1 = REG0 = 0, A4–A0 = 01111
DB13–DB0 = Don't Care

This instruction is used to implement a software reset. All internal registers are reset to their default values, which correspond to m at full-scale and c at zero. The contents of the DAC registers are cleared, setting all analog outputs to 0 V. The soft reset activation time is 135 µs max. Only perform a soft reset when the AD5382 is not in power-down mode.

Table 14. Control Register Contents

MSB													LSB
CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Control Register Write/Read

REG1 = REG0 = 0, A4–A0 = 01100, R/$\overline{W}$ status determines if the operation is a write (R/$\overline{W}$ = 0) or a read (R/$\overline{W}$ = 1). DB13 to DB0 contain the control register data.

Control Register Contents

CR13: Power-Down Status. This bit is used to configure the output amplifier state in power-down.

CR13 = 1. Amplifier output is high impedance (default on power-up).

CR13 = 0. Amplifier output is 100 kΩ to ground.

CR12: REF Select. This bit selects the operating internal reference for the AD5382.

CR12 = 1: Internal reference is 2.5 V (AD5382-5 default), the recommended operating reference for AD5382-5.

CR12 = 0: Internal reference is 1.25 V (AD5382-3 default), the recommended operating reference for AD5382-3.

CR11: Current Boost Control. This bit is used to boost the current in the output amplifier, thereby altering its slew rate.

CR11 = 1: Boost Mode On. This maximizes the bias current in the output amplifier, optimizing its slew rate but increasing the power dissipation.

CR11 = 0: Boost Mode Off (default on power-up). This reduces the bias current in the output amplifier and reduces the overall power consumption.

CR10: Internal/External Reference. This bit determines if the DAC uses its internal reference or an externally applied reference.

CR10 = 1: Internal Reference Enabled. The reference output depends on data loaded to CR12.

CR10 = 0: External Reference Selected (default on power-up).

CR9: Channel Monitor Enable (see Channel Monitor Function)

CR9 = 1: Monitor Enabled. This enables the channel monitor function. After a write to the monitor channel in the SFR register, the selected channel output is routed to the MON_OUT pin.

CR9 = 0: Monitor Disabled (default on power-up). When the monitor is disabled, MON_OUT is three-stated.

CR8: Thermal Monitor Function. This function is used to monitor the AD5382's internal die temperature when enabled.

The thermal monitor powers down the output amplifiers when the temperature exceeds 130°C. This function can be used to protect the device when power dissipation may be exceeded if a number of output channels are simultaneously short-circuited. A soft power-up re-enables the output amplifiers if the die temperature drops below 130°C.

CR8 = 1: Thermal Monitor Enabled.

CR8 = 0: Thermal Monitor Disabled (default on power-up).

CR7 and CR6: Don't Care.

CR5 to CR2: Toggle Function Enable. This function allows the user to toggle the output between two codes loaded to the A and B register for each DAC. Control Register Bits CR5 to CR2 are used to enable individual groups of eight channels for operation in toggle mode. A Logic 1 written to any bit enables a group of channels; a Logic 0 disables a group. $\overline{LDAC}$ is used to toggle between the two registers. Table 15 shows the decoding for toggle contains Channels 24 to 31, CR5 = 1 enables these channels.

Table 15.

CR Bit	Group	Channels
CR5	3	24–31
CR4	2	16–23
CR3	1	8–15
CR2	0	0–7

CR1 and CR0: Don't Care.

Channel Monitor Function

REG1 = REG0 = 0, A4–A0 = 01010

DB13–DB8 = Contain data to address the monitored channel

A channel monitor function is provided on the AD5382. This feature, which consists of a multiplexer addressed via the interface, allows any channel output or the signals connected to the MON_IN inputs to be routed to the MON_OUT pin for monitoring using an external ADC. The channel monitor function must be enabled in the control register before any channels are routed to MON_OUT. On the AD5382, DB13 to DB8 contain the channel address for the monitored channel. Selecting channel address 63 three-states MON_OUT.