Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

8-/16-Channel, 3 V/5 V, Serial Input, Single-Supply, 12-/14-Bit Voltage Output

Data Sheet

AD5390/AD5391/AD5392

FEATURES

- AD5390: 16-channel, 14-bit voltage output DAC
- AD5391: 16-channel, 12-bit voltage output DAC
- AD5392: 8-channel, 14-bit voltage output DAC
- Guaranteed monotonic
- INL
  - ±1 LSB max (AD5391)
  - ±3 LSB max (AD5390-5/AD5392-5)
  - ±4 LSB max (AD5390-3/AD5392-3)
- On-chip 1.25 V/2.5 V, 10 ppm/°C reference
- Temperature range: −40°C to +85°C
- Rail-to-rail output amplifier
- Power-down mode
- Package types
  - 64-lead LFCSP (9 mm × 9 mm)
  - 52-lead LQFP (10 mm × 10 mm)
- User interfaces
- Serial SPI-, QSPI-, MICROWIRE-, and DSP-compatible (featuring data readback)
- I²C-compatible interface
- Integrated functions
  - channel monitor
  - simultaneous output update via $\overline{\text{LDAC}}$
  - clear function to user-programmable code
  - amplifier boost mode to optimize slew rate
  - user-programmable offset and gain adjust
  - toggle mode enables square wave generation
  - thermal monitor
- Robust 6.5 kV HBM and 2 kV FICDM ESD rating

APPLICATIONS

- Instrumentation and industrial control
- Power amplifier control
- Level setting (ATE)
- Control systems
- Microelectromechanical systems (MEMs)
- Variable optical attenuators (VOAs)
- Optical transceivers (MSA 300, XFP)

FUNCTIONAL BLOCK DIAGRAM

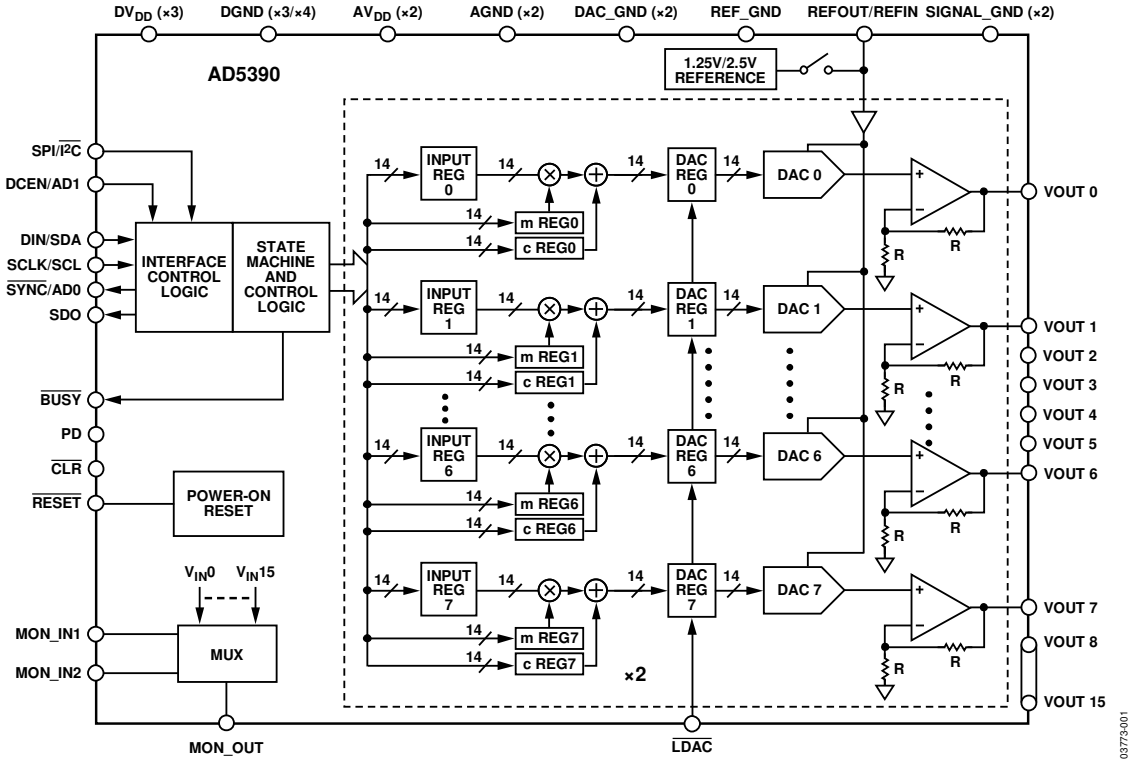


Figure 1.

Rev. F

Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

Technical Support
www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

6/14—Rev. E to Rev. F

Deleted Table 1; Renumbered Sequentially 4
Changed AD5390-3/AD5391-3/AD5392-3 Input Current from ±10 μA (max) to ±1 μA (max); Table 3 8
Changes to Table 5 11
Changes to Soft Reset Section 31
Changes to Reset Function Section 35
Replaced ADSP2101 with ADSP-BF527 36
Added Power Supply Sequencing Section 38
Changes to Ordering Guide 43

6/12—Rev. D to Rev. E

Changes to Table 1 4
Change to Accuracy Parameter, Gain Error, Table 2 5
Change to Accuracy Parameter, Gain Error, Table 4 8
Added Exposed Pad Notation to Figure 7 and Figure 8 15

5/12—Rev. C to Rev. D

Changes to Product Title and Features Section 1
Changes to Table 2 4
Changes to Table 3 6
Changes to Table 4 7
Changes to Table 5 9
Changes to Table 6 10
Changes to Table 8 13
Changes to Figure 8 and Figure 10 14
Changes to Table 9 16
Changes to Figure 17, Figure 18, Figure 19, And Figure 22 19
Changes to Figure 23, Figure 24, Figure 25, and Figure 26 20
Changes to Table 26 32
Changes to Ordering Guide 40

1/09—Rev. B to Rev. C

Updated Format ....Universal
Changes to Figure 33 27
Added Figure 34 and Renumbered Sequentially 27
Changes to Figure 34 28
Changes to Table 28 33
Change order of Figure 41 and Figure 42 36
Changes to Toggle Mode Function Section 37

3/06—Rev. A to Rev. B

Changes to Figure 1 1
Changes to Table 9 14
Changes to Table 12 and Table 15 23
Updated Outline Dimensions 39
Changes to Ordering Guide 40

10/04—Rev. 0 to Rev. A

Changes to Features 1
Changes to Table 1 3
Changes to Table 2 4
Changes to Table 3 6
Changes to Table 4 7
Changes to Figure 36 35
Changes to Figure 37 36
Changes to Figure 38 36
Changes to Ordering Guide 41

4/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5390/AD5391 are complete single-supply, 16-channel, 14-bit and 12-bit DACs, respectively. The AD5392 is a complete single-supply, 8-channel, 14-bit DAC. The devices are available in either a 64-lead LFCSP or a 52-lead LQFP. All channels have an on-chip output amplifier with rail-to-rail operation. All devices include an internal 1.25/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that optimizes the output amplifier slew rate.

The AD5390/AD5391/AD5392 contain a 3-wire serial interface with interface speeds in excess of 30 MHz that are compatible with SPI®, QSPI™, MICROWIRE™, and DSP interface standards and an I²C-compatible interface supporting a 400 kHz data transfer rate.

An input register followed by a DAC register provides double-buffering, allowing DAC outputs to be updated independently or simultaneously using the $\overline{\text{LDAC}}$ input. Each channel has a programmable gain and offset adjust register, letting the user fully calibrate any DAC channel.

Power consumption is typically 0.25 mA per channel.

SPECIFICATIONS

AD5390-5/AD5391-5/AD5392-5 SPECIFICATIONS

AV_{DD} = 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V; REFIN = 2.5 V external. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	AD5390-5[1] AD5392-5[1]	AD5391-5[1]	Unit	Test Conditions/Comments
ACCURACY				
Resolution	14	12	Bits	
Relative Accuracy	±3	±1	LSB max	
Differential Nonlinearity	−1/+2	±1	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	4	mV max	
Offset Error	±4	±4	mV max	Measured at Code 32 in the linear region (AD5390-5/AD5391-5); measured at Code 8 in the linear region (AD5391-5)
Offset Error TC	±5	±5	µV/°C typ	
Gain Error	±0.05	±0.05	% FSR max	At 25°C T_{MIN} to T_{MAX}
	±0.06	±0.06	% FSR max	
Gain Temperature Coefficient[2]	2	2	ppm FSR/°C typ	
DC Crosstalk[2]	1	1	LSB max	
REFERENCE INPUT/OUTPUT				
Reference Input[2]				
Reference Input Voltage	2.5	2.5	V	±1% for specified performance, $AV_{DD} = 2 \times REFIN + 50$ mV
DC Input Impedance	1	1	MΩ min	Typically 100 MΩ
Input Current	±1	±1	µA max	Typically ±30 nA
Reference Range	1 V to $AV_{DD}/2$	1 V to $AV_{DD}/2$	V min/max	
Reference Output[3]				Enabled via internal/external bit in control register; REF select bit in control register selects the reference voltage
Output Voltage	2.495/2.505	2.495/2.505	V min/max	At ambient, optimized for 2.5 V operation
	1.22/1.28	1.22/1.28	V min/max	At ambient when 1.25 V reference is selected
Reference TC	±10	±10	ppm max	Temperature range: 25°C to 85°C
	±15	±15	ppm max	Temperature range: −40°C to +85°C
Output Impedance	800	800	Ω typ	
OUTPUT CHARACTERISTICS[2]				
Output Voltage Range[4]	$0/AV_{DD}$	$0/AV_{DD}$	V min/max	
Short-Circuit Current	40	40	mA max	
Load Current	±1	±1	mA max	
Capacitive Load Stability				
$R_L = \infty$	200	200	pF max	
R_L = 5 kΩ	1000	1000	pF max	
DC Output Impedance	0.6	0.6	Ω max	
MONITOR OUTPUT PIN				
Output Impedance	1000	1000	Ω typ	
Three-State Leakage Current	100	100	nA typ	
LOGIC INPUTS[2]				DV_{DD} = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	2	V min	
V_{IL}, Input Low Voltage				
DVDD > 3.6 V	0.8	0.8	V max	
DVDD ≤ 3.6 V	0.6	0.6	V max	
Input Current	±10	±10	µA max	Total for all pins, $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	10	pF max	

Parameter	AD5390-5[1] AD5392-5[1]	AD5391-5[1]	Unit	Test Conditions/Comments
LOGIC INPUTS (SCL, SDA Only)				
V_{IH}, Input High Voltage	0.7 × DV_{DD}	0.7 × DV_{DD}	V min	SMBus-compatible at DV_{DD} < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DV_{DD}	0.3 × DV_{DD}	V max	SMBus-compatible at DV_{DD} < 3.6 V
I_{IN}, Input Leakage Current	±1	±1	µA max	
V_{HYST}, Input Hysteresis	0.05 × DV_{DD}	0.05 × DV_{DD}	V min	
C_{IN}, Input Capacitance	8	8	pF typ	
Glitch Rejection	50	50	ns max	Input filtering suppresses noise spikes of <50 ns
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[2]				
Output Low Voltage	0.4	0.4	V max	DV_{DD} = 5 V ± 10%, sinking 200 µA
Output High Voltage	DV_{DD} − 1	DV_{DD} − 1	V min	DV_{DD} = 5 V ± 10%, SDO only, sourcing 200 µA
Output Low Voltage	0.4	0.4	V max	DV_{DD} = 2.7 V to 3.6 V, sinking 200 µA
Output High Voltage	DV_{DD} − 0.5	DV_{DD} − 0.5	V min	DV_{DD} = 2.7 V to 3.6 V SDO only, sourcing 200 µA
High Impedance Leakage Current	±1	±1	µA max	
High Impedance Output Capacitance	5	5	pF typ	
LOGIC OUTPUT (SDA)[2]				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 3 mA
	0.6	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	±1	µA max	
Three-State Output Capacitance	8	8	pF typ	
POWER REQUIREMENTS				
AV_{DD}	4.5/5.5	4.5/5.5	V min/max	
DV_{DD}	2.7/5.5	2.7/5.5	V min/max	
Power Supply Sensitivity[2]				
ΔMidscale/ΔAV_{DD}	−85	−85	dB typ	
AI_{DD}	0.375	0.375	mA/channel max	Outputs unloaded, boost off, 0.25 mA/channel typ
AI_{DD}	0.475	0.475	mA/channel max	Outputs unloaded, boost on, 0.325 mA/channel typ
DI_{DD}	1	1	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)	20	20	µA max	Typically 100 nA
DI_{DD} (Power-Down)	20	20	µA max	Typically 1 µA
Power Dissipation	35	35	mW max	AD5390/AD5391 with outputs unloaded, AV_{DD} = DV_{DD} = 5 V, boost off
	20	20	mW max	AD5392 with outputs unloaded, AV_{DD} = DV_{DD} = 5 V, boost off

[1] The AD5390-5/AD5391-5/AD5392-5 are calibrated with a 2.5 V reference. Temperature range for all versions: −40°C to +85°C.
[2] Guaranteed by characterization, not production tested.
[3] Programmable either to 1.25 V typical or 2.5 V typical via the AD5390/AD5391/AD5392 control register. Operating the AD5390-5/AD5391-5/AD5392-5 with a reference of 1.25 V leads to a degradation in performance accuracy.
[4] Accuracy guaranteed from VOUT = 10 mV to AV_{DD} − 50 mV.

AD5390-5/AD5391-5/AD5392-5 AC CHARACTERISTICS

AV_{DD} = 4.5 V to 5.5 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V.

Table 2.

Parameter	All[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time			¼ scale to ¾ scale change settling to ±1 LSB
AD5390/AD5392	3	µs typ	Boost mode off, CR11 = 0
	8	µs max	Boost mode off, CR11 = 0
AD5391	3	µs typ	Boost mode off, CR11 = 0
	8	µs max	Boost mode off, CR11 = 0
Slew rate[2]	2.5	V/µs typ	Boost mode on
	1.5	V/µs typ	Boost mode off
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
Channel-to-Channel Isolation	100	dB typ	See the Terminology section
DAC-to-DAC Crosstalk	1	nV-s typ	See the Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
Output Noise (0.1 Hz to 10 Hz)	15	µV p-p typ	External reference midscale loaded to DAC
	40	µV p-p typ	Internal reference midscale loaded to DAC
Output Noise Spectral Density			
@ 1 kHz	150	nV/(Hz)$^{1/2}$ typ	
@ 10 kHz	100	nV/(Hz)$^{1/2}$ typ	

[1] Guaranteed by characterization, not production tested.
[2] The slew rate can be adjusted via the current boost control bit in the DAC control register.

AD5390-3/AD5391-3/AD5392-3 SPECIFICATIONS

AV_{DD} = 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V; REFIN = 1.25 V external. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	AD5390-3[1] AD5392-3[1]	AD5391-3[1]	Unit	Test Conditions/Comments
ACCURACY				
Resolution	14	12	Bits	
Relative Accuracy	±4	±1	LSB max	
Differential Nonlinearity	−1/+2	±1	LSB max	Guaranteed monotonic over temperature
Zero-Scale Error	4	4	mV max	
Offset Error	±4	±4	mV max	Measured at code 64 in the linear region
Offset Error TC	±5	±5	µV/°C typ	
Gain Error	±0.05	±0.05	% FSR max	At 25°C
	±0.1	±0.1	% FSR max	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[2]	2	2	ppm FSR/°C typ	
DC Crosstalk	1	1	LSB max	
REFERENCE INPUT/OUTPUT				
Reference Input[2]				
Reference Input Voltage	1.25	1.25	V	±1% for specified performance
DC Input Impedance	1	1	MΩ min	Typically 100 MΩ
Input Current	±1	±1	µA max	Typically ±30 nA
Reference Range	1 V to AV_{DD}/2	1 V to AV_{DD}/2	V min/max	
Reference Output[3]				Enabled via internal/external bit in control register; REF select bit in control register selects the reference voltage
Output Voltage	1.245/1.255	1.245/1.255	V min/max	At ambient, optimized for 1.25 V operation
	2.47/2.53	2.47/2.53	V min/max	At ambient when 2.5 V reference is selected
Reference TC	±10	±10	ppm max	Temperature range: 25°C to 85°C
	±15	±15	ppm max	Temperature range: −40°C to +85°C
Output Impedance	800	800	Ω typ	
OUTPUT CHARACTERISTICS[2]				
Output Voltage Range[4]	0/AV_{DD}	0/AV_{DD}	V min/max	
Short-Circuit Current	40	40	mA max	
Load Current	±1	±1	mA max	
Capacitive Load Stability				
R_L = ∞	200	200	pF max	
R_L = 5 kΩ	1000	1000	pF max	
DC Output Impedance	0.6	0.6	Ω max	
MONITOR OUTPUT PIN[2]				
Output Impedance	1000	1000	Ω typ	
Three-State Leakage Current	100	100	nA typ	
LOGIC INPUTS[2]				DV_{DD} = 2.7 V to 5.5 V
V_{IH}, Input High Voltage	2	2	V min	
V_{IL}, Input Low Voltage				
DVDD > 3.6 V	0.8	0.8	V max	
DVDD ≤ 3.6 V	0.6	0.6	V max	
Input Current	±1	±1	µA max	Total for all pins. $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance	10	10	pF max	

Parameter	AD5390-3[1] AD5392-3[1]	AD5391-3[1]	Unit	Test Conditions/Comments
Logic Inputs (SCL, SDA Only)				
V_{IH}, Input High Voltage	0.7 × DV_{DD}	0.7 × DV_{DD}	V min	SMBus-compatible at DV_{DD} < 3.6 V
V_{IL}, Input Low Voltage	0.3 × DV_{DD}	0.3 × DV_{DD}	V max	SMBus-compatible at DV_{DD} < 3.6 V
I_{IN}, Input Leakage Current	±1	±1	µA max	
V_{HYST}, Input Hysteresis	0.05 × DV_{DD}	0.05 × DV_{DD}	V min	
Glitch Rejection	50	50	ns max	Input filtering suppresses noise spikes <50 ns
Logic Outputs ($\overline{BUSY}$, SDO)[2]				
Output Low Voltage	0.4	0.4	V max	DV_{DD} = 2.7 V to 5.5 V, sinking 200 µA
Output High Voltage	DV_{DD} − 0.5	DV_{DD} − 0.5	V min	DV_{DD} = 2.7 V to 3.6 V, SDO only, sourcing 200 µA
	DV_{DD} − 0.1	DV_{DD} − 0.1	V min	DV_{DD} = 4.5 V to 5.5 V, SDO only, sourcing 200 µA
High Impedance Leakage Current	±1	±1	µA max	
High Impedance Output Capacitance	5	5	pF typ	
Logic Output (SDA)[2]				
V_{OL}, Output Low Voltage	0.4	0.4	V max	I_{SINK} = 3 mA
	0.6	0.6	V max	I_{SINK} = 6 mA
Three-State Leakage Current	±1	±1	µA max	
Three-State Output Capacitance	8	8	pF typ	
POWER REQUIREMENTS				
AV_{DD}	2.7/3.6	2.7/3.6	V min/max	
DV_{DD}	2.7/5.5	2.7/5.5	V min/max	
Power Supply Sensitivity[2]				
ΔMidscale/ΔAV_{DD}	−85	−85	dB typ	
AI_{DD}	0.375	0.375	mA/channel max	Outputs unloaded, boost off, 0.25 mA/channel typ
AI_{DD}	0.475	0.475	mA/channel max	Outputs unloaded, boost on, 0.325 mA/channel typ
DI_{DD}	1	1	mA max	V_{IH} = DV_{DD}, V_{IL} = DGND
AI_{DD} (Power-Down)	20	20	µA max	Typically 100 nA
DI_{DD} (Power-Down)	20	20	µA max	Typically 1 µA
Power Dissipation	21	21	mW max	AD5390/AD5391 with outputs unloaded, AV_{DD} = DV_{DD} = 3 V, boost off
	12	12	mW max	AD5392 with outputs unloaded, AV_{DD} = DV_{DD} = 3 V, boost off

[1] The AD5390-3/AD5391-3/AD5392-3 are calibrated with a 1.25 V reference. Temperature range for all versions: −40°C to +85°C.
[2] Guaranteed by characterization, not production tested.
[3] Programmable either to 1.25 V typical or 2.5 V typical via the AD5390/AD5391/AD5392 control register. Operating the AD5390-3/AD5391-3/AD5392-3 with a reference of 2.5 V leads to a degradation in performance accuracy.
[4] Accuracy guaranteed from VOUT = 39 mV to AV_{DD} − 50 mV.

AD5390-3/AD5391-3/AD5392-3 AC CHARACTERISTICS

AV_{DD} = 2.7 V to 3.6 V; DV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V; C_L = 200 pF to AGND.

Table 4.

Parameter	All[1]	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Voltage Settling Time			¼ scale to ¾ scale change settling to ±1 LSB
AD5390/AD5392	3	µs typ	Boost mode off, CR11 = 0
	8	µs max	Boost mode off, CR11 = 0
AD5391	3	µs typ	Boost mode off, CR11 = 0
	8	µs max	Boost mode on, CR11 = 1
Slew Rate[2]	2.5	V/µs typ	Boost mode on
	1.5	V/µs typ	Boost mode off, CR11 = 0
Digital-to-Analog Glitch Energy	12	nV-s typ	
Glitch Impulse Peak Amplitude	15	mV typ	
Channel-to-Channel Isolation	100	dB typ	See the Terminology section
DAC-to-DAC Crosstalk	1	nV-s typ	See the Terminology section
Digital Crosstalk	0.8	nV-s typ	
Digital Feedthrough	0.1	nV-s typ	Effect of input bus activity on DAC output under test
OUTPUT NOISE (0.1 Hz to 10 Hz)	15	µV p-p typ	External reference midscale loaded to DAC
	40	µV p-p typ	Internal reference midscale loaded to DAC
Output Noise Spectral Density			
@ 1 kHz	150	nV/(Hz)$^{1/2}$ typ	
@ 10 kHz	100	nV/(Hz)$^{1/2}$ typ	

[1] Guaranteed by design and characterization, not production tested.
[2] The slew rate can be programmed via the current boost control bit in the AD5390/AD5391/AD5392 control registers.

TIMING CHARACTERISTICS

SERIAL SPI-, QSPI-, MICROWIRE-, AND DSP-COMPATIBLE INTERFACE

DV_{DD} = 2 V to 5.5 V; AV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 5. 3-Wire Serial Interface[1]

Parameter[2, 3]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[4]	13	ns min	24th SCLK falling edge to $\overline{SYNC}$ falling edge
t_6[4]	33	ns min	Minimum $\overline{SYNC}$ low time
t_7	10	ns min	Minimum $\overline{SYNC}$ high time
t_7	140	ns min	Minimum $\overline{SYNC}$ high time in readback mode
t_8	5	ns min	Data setup time
t_9	4.5	ns min	Data hold time
t_{10}[4]	36	ns max	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{11}	670	ns max	$\overline{BUSY}$ pulse width low (single channel update)
t_{12}[4]	20	ns min	24th SCLK falling edge to $\overline{LDAC}$ falling edge
t_{13}	20	ns min	$\overline{LDAC}$ pulse width low
t_{14}	100/2000	ns min/max	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0	ns min	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	100	ns min	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}	3	µs typ	DAC output settling time, AD5390/AD5391/AD5392; boost mode off
t_{18}	20	ns min	$\overline{CLR}$ pulse width low
t_{19}	40	µs max	$\overline{CLR}$ pulse activation time
t_{20}[5]	20	ns max	SCLK rising edge to SDO valid
t_{21}[4]	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{22}[4]	8	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{23}[4]	20	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge

[1] Guaranteed by design and characterization, not production tested.
[2] All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.2 V.
[3] See Figure 2, Figure 3, Figure 4, and Figure 5.
[4] Standalone mode only.
[5] Daisy-chain mode only.

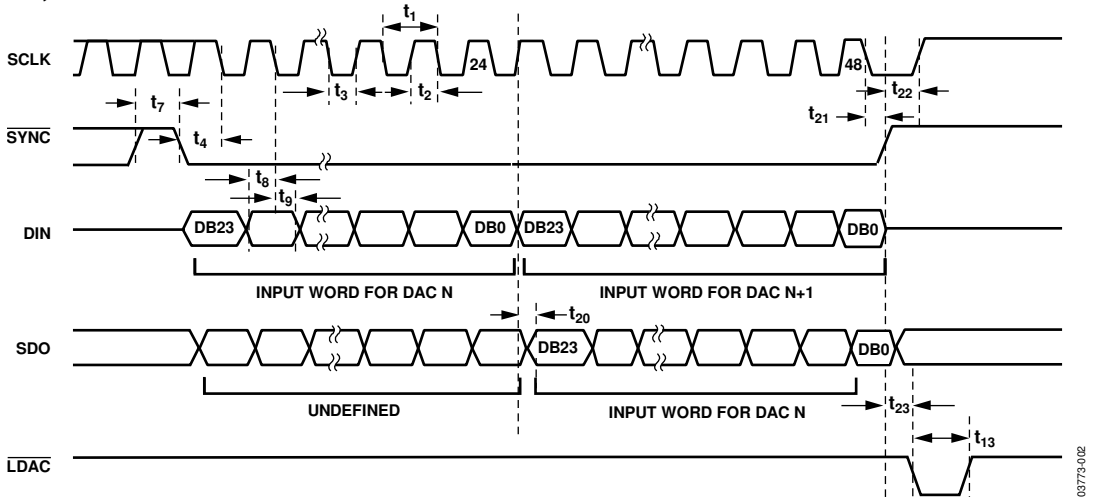


Figure 2. Serial Interface Timing Diagram (Daisy-Chain Mode)

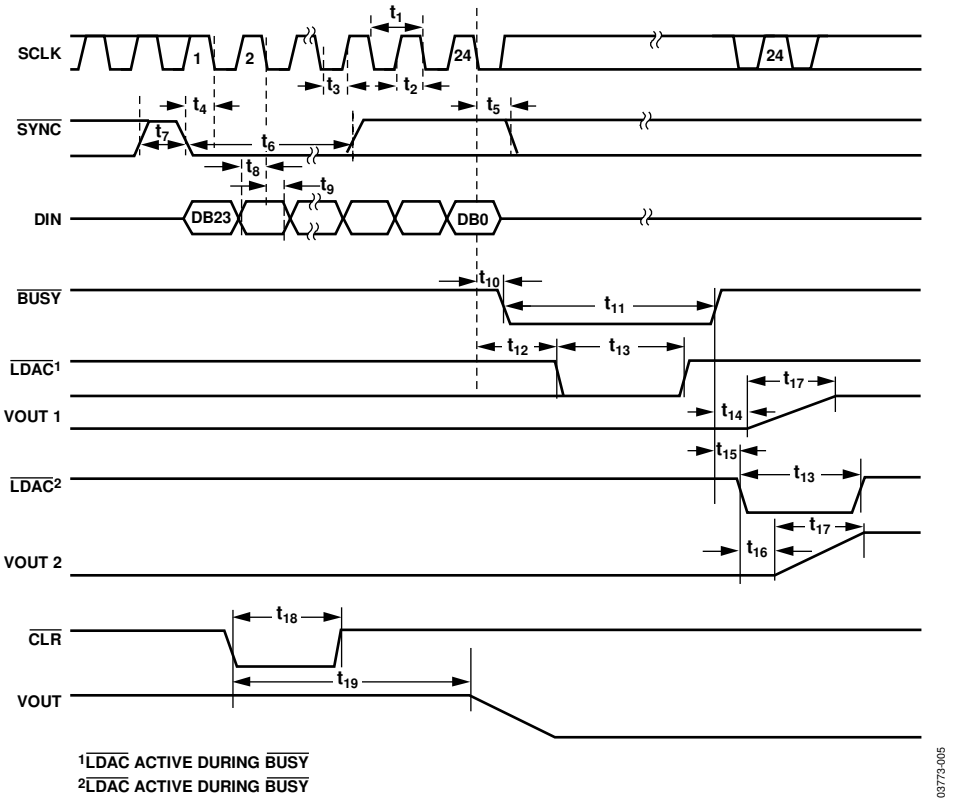


Figure 3. Serial Interface Timing Diagram (Standalone Mode)

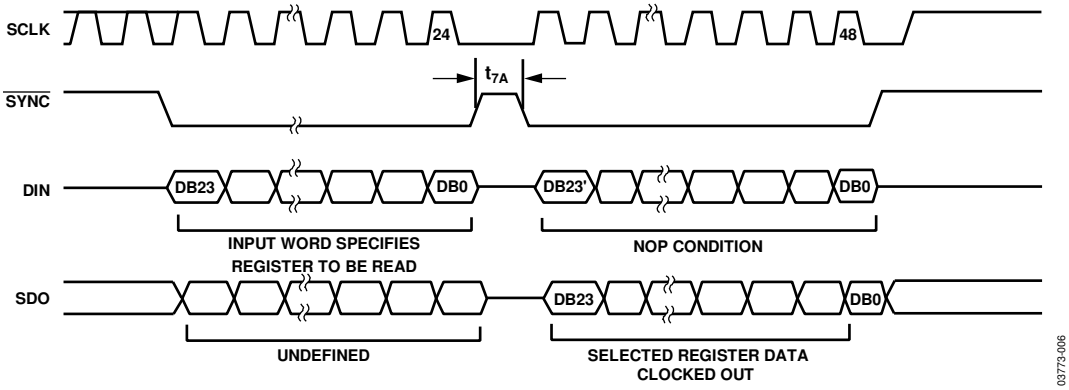


Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

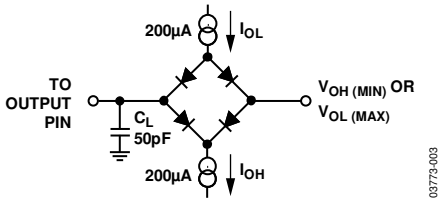


Figure 5. Load Circuit for Digital Output Timing

I²C SERIAL INTERFACE

DV_{DD} = 2.7 V to 5.5 V; AV_{DD} = 2.7 V to 5.5 V; AGND = DGND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 6. I²C Serial Interface[1]

Parameter[2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
F_{SCL}	400	kHz max	SCL clock frequency
t_1	2.5	µs min	SCL cycle time
t_2	0.6	µs min	t_{HIGH}, SCL high time
t_3	1.3	µs min	t_{LOW}, SCL low time
t_4	0.6	µs min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100	ns min	$t_{SU, DAT}$, data setup time
t_6[3]	0.9	µs max	$t_{HD, DAT}$ data hold time
	0	µs min	$t_{HD, DAT}$ data hold time
t_7	0.6	µs min	$t_{SU, STA}$ setup time for repeated start
t_8	0.6	µs min	$t_{SU, STO}$ stop condition setup time
t_9	1.3	µs min	t_{BUF}, bus free time between a stop and a start condition
t_{10}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_R, rise time of SCL and SDA when receiving (CMOS-compatible)
t_{11}	300	ns max	t_F, fall time of SDA when transmitting
	0	ns min	t_F, fall time of SDA when receiving (CMOS-compatible)
	300	ns max	t_F, fall time of SCL and SDA when receiving
	20 + 0.1 C_B	ns min	t_F, fall time of SCL and SDA when transmitting
C_B[4]	400	pF max	Capacitive load for each bus line

[1] Guaranteed by design and characterization, not production tested.
[2] See Figure 6.
[3] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} MIN of the SCL signal) to bridge the undefined region of SCL's falling edge.
[4] C_B is the total capacitance of one bus line in pF; t_R and t_F measured between 0.3 DV_{DD} and 0.7 DV_{DD}.

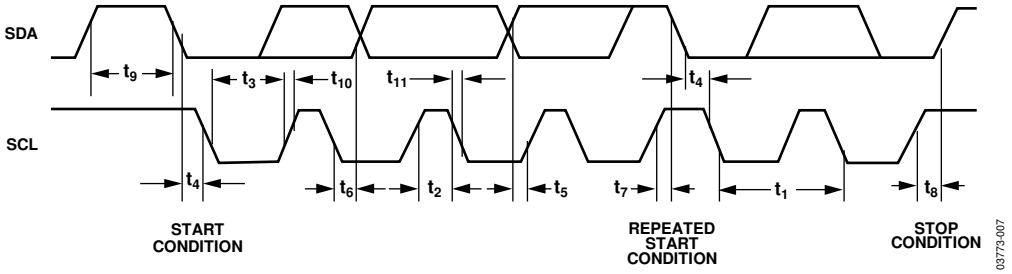


Figure 6. I²C Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Transient currents of up to 100 mA do not cause SCR latch-up.
T_A = 25°C, unless otherwise noted.

Table 7.

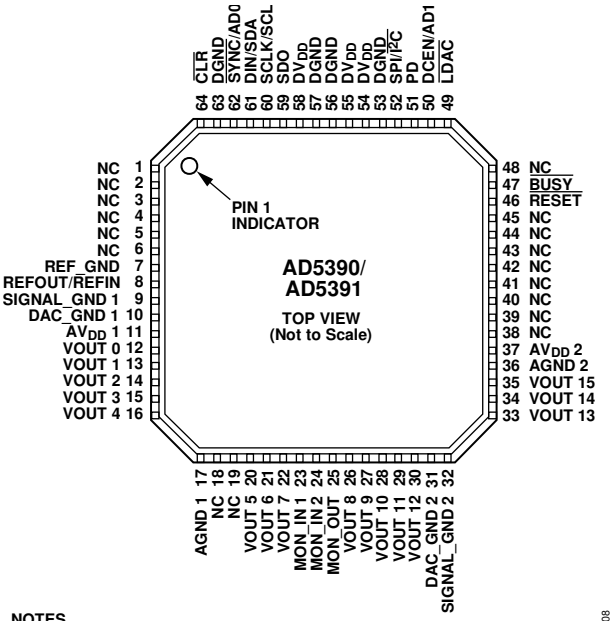
Parameter	Rating
AV_{DD} to AGND	−0.3 V to +7 V
DV_{DD} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DD} + 0.3 V
Digital Outputs to DGND	−0.3 V to DV_{DD} + 0.3 V
VREF to AGND	−0.3 V to +7 V
REFOUT to AGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
VOUTX to AGND	−0.3 V to AV_{DD} + 0.3 V
ESD	
HBM	6.5 kV
FICSM	2 kV
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
64-Lead LFCSP, θ_{JA}	22°C/W
52-Lead LQFP, θ_{JA}	38°C/W
Reflow Soldering Peak Temperature	230°C

Stresses above absolute maximum ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

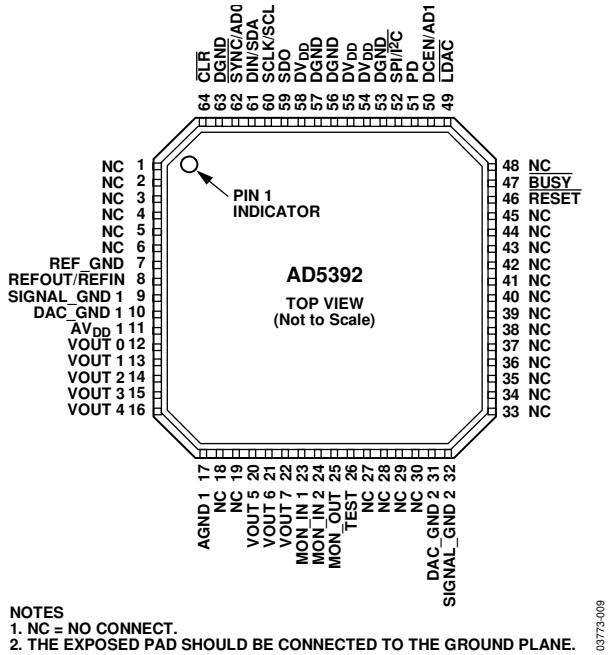
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD SHOULD BE CONNECTED TO THE GROUND PLANE.

Figure 7. AD5390/AD5391 LFCSP Pin Configuration



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED PAD SHOULD BE CONNECTED TO THE GROUND PLANE.

Figure 8. AD5392 LFCSP Pin Configuration

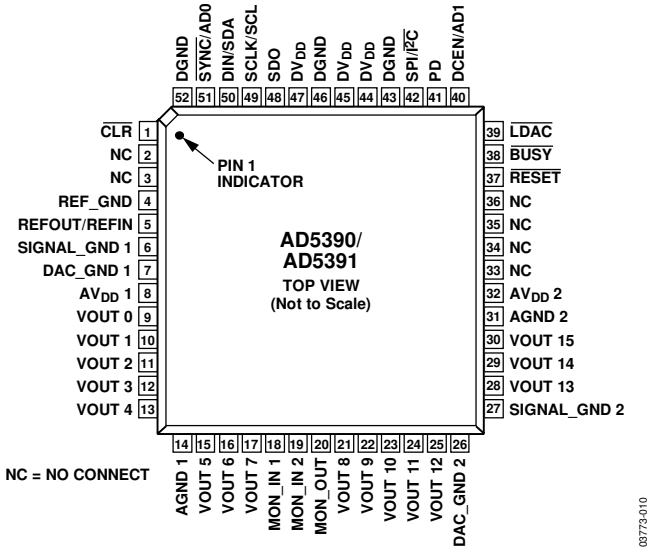


Figure 9. AD5390/AD5391 LQFP Pin Configuration

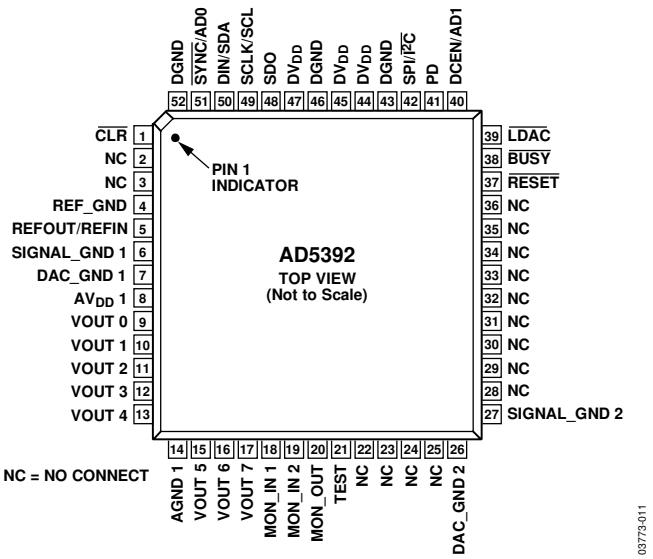


Figure 10. AD5392 LQFP Pin Configuration

Table 8. Pin Function Descriptions

Mnemonic	Function
VOUT X	Buffered Analog Outputs for Channel X. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
SIGNAL_GND 1, SIGNAL_GND 2	Analog Ground Reference Points for each group of eight output channels. All SIGNAL_GND pins are tied together internally and should be connected to the AGND plane as close as possible to the AD5390/AD5391/AD5392.
DAC_GND 1, DAC_GND 2	Each group of eight channels contains a DAC_GND pin. This is the ground reference point for the internal 14-bit DACs. These pins should be connected to the AGND plane.
AGND 1, AGND 2	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. All AGND pins should be connected externally to the AGND plane.
AV_{DD} 1, AV_{DD} 2	Analog Supply Pins. Each group of eight channels has a separate AV_{DD} pin. These pins should be decoupled with 0.1 uF ceramic capacitors and 10 µF tantalum capacitors. Operating range is 5 V ± 10%.
DGND	Ground for All Digital Circuitry.
DV_{DD}	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. Recommended that these pins be decoupled with 0.1 µF ceramic capacitors and 10 µF tantalum capacitors to DGND.
REF_GND	Ground Reference Point for the Internal Reference. Connect to AGND.
REFOUT/REFIN	The AD5390/AD5391/AD5392 contains a common REFOUT/REFIN pin. When the internal reference is selected, this pin is the reference output. If the application necessitates the use of an external reference, it can be applied to this pin and the internal reference disabled via the control register. The default for this pin is a reference input.
MON_OUT	Analog Output Pin. When the monitor function is enabled on the AD5390/AD5391, the MON_OUT acts as the output of a 16-to-1 channel multiplexer that can be programmed to multiplex any channel output to the MON_OUT pin. When the monitor function is enabled on the AD5392, the MON_OUT acts as the output of an 8-to-1 channel multiplexer that can be programmed to multiplex any channel output to the MON_OUT pin. The MON_OUT pin output impedance is typically 500 Ω and is intended to drive a high input impedance such as that exhibited by SAR ADC inputs.
MON_IN 1, MON_IN 2	Monitor Input Pins. The AD5390/AD5391/AD5392 contains two monitor input pins to which the user can connect input signals (within the maximum ratings of the device) for monitoring purposes. Any of the signals applied to the MON_IN pins along with the output channels can be switched to the MON_OUT pin via software. An external ADC, for example, can be used to monitor these signals.
$\overline{\text{SYNC}}$/AD0	Serial Interface Pin. This is the frame synchronization input signal for the serial interface. When taken low, the internal counter is enabled to count the required number of clocks before the addressed register is updated. In I^2C mode, AD0 acts as a hardware address pin.
DCEN/AD1	Interface Control Pin. Operation is determined by the interface select bit SPI/$\overline{I^2C}$. Serial Interface Mode: Daisy-Chain Select Input (level-sensitive, active high). When high, this pin enables daisy-chain operation to allow a number of devices to be cascaded together. I^2C Mode: This pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I^2C bus.
SDO	Serial Data Output. Three-state CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK and is valid on the falling edge of SCLK.
$\overline{\text{BUSY}}$	Digital CMOS Output. $\overline{\text{BUSY}}$ goes low during internal calculations of the data (x2) loaded to the DAC data register. During this time, the user can continue writing new data to further the x1, c, and m registers (these are stored in a FIFO), but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low, this event is stored. $\overline{\text{BUSY}}$ also goes low during power-on reset and when the $\overline{\text{RESET}}$ pin is low. During this time the interface is disabled and any events on $\overline{\text{LDAC}}$ are ignored. A CLR operation also brings $\overline{\text{BUSY}}$ low.
$\overline{\text{LDAC}}$	Load DAC Logic Input (active low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high), the contents of the input registers are transferred to the DAC registers and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However, any events on $\overline{\text{LDAC}}$ during power-on reset or $\overline{\text{RESET}}$ are ignored.
$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. While $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, all channels are updated with the data contained in the $\overline{\text{CLR}}$ code register. $\overline{\text{BUSY}}$ is low for a duration of 20 µs (AD5390/AD5391) and 15 µs (AD5392) while all channels are being updated with the $\overline{\text{CLR}}$ code.
$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (falling edge sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the x1, m, c, and x2 registers to their default power-on values. This sequence takes 270 µs maximum. This falling edge of $\overline{\text{RESET}}$ initiates the RESET process and $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the part resumes normal operation and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.

Mnemonic	Function
PD	Power-Down (level-sensitive, active high). Used to place the device in low power mode, in which the device consumes 1 µA analog current and 20 µA digital current. In power-down mode, all internal analog circuitry is placed in low power mode; the analog output is configured as high impedance outputs or provides a 100 kΩ load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.
SPI/$\overline{I^2C}$	Interface Select Input Pin. When this input is low, I^2C mode is selected. When this input is high, SPI mode is selected.
SCLK/SCL	Interface Clock Input Pin. In SPI-compatible serial interface mode, this pin acts as a serial clock input. It operates at clock speeds up to 50 MHz. I^2C mode: In I^2C mode, this pin performs the SCL function, clocking data into the device. Data transfer rate in I^2C mode is compatible with both 100 kHz and 400 kHz operating modes.
DIN/SDA	Interface Data Input Pin. SPI/$\overline{I^2C}$ = 1: This pin acts as the serial data input. Data must be valid on the falling edge of SCLK. SPI/$\overline{I^2C}$ = 0, I^2C mode: In I^2C mode, this pin is the serial data pin (SDA) operating as an open drain input/output.
TEST	Test pin (AD5392 only). This pin is used for production testing. For normal operation, this pin should not be connected.
NC	No Connect. These pins have no internal connection.
Exposed Pad (LFCSP only)	This pad should be connected to the ground plane.

TERMINOLOGY

Relative Accuracy or Endpoint Linearity (INL)
A measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error and is expressed in least significant bits (LSBs).

Differential Nonlinearity (DNL)
The difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
The error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and m = all 1s, c = 2^{n-1}, $VOUT_{(Zero\text{-}Scale)}$ = 0 V.

Zero-scale error is a measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV. It is mainly caused by offsets in the output amplifier.

Offset Error
A measure of the difference between VOUT (actual) and VOUT (ideal) expressed in mV in the linear region of the transfer function. Offset error is measured on the AD5390-5/AD5391-5/AD5392-5 with code 32 loaded in the DAC register and with code 64 loaded in the DAC register on the AD5390-3/AD5391-3/AD5392-3.

Gain Error
The deviation in slope of the DAC transfer characteristic from ideal and is expressed in % FSR with the DAC output unloaded. Gain error is specified in the linear region of the output range between VOUT = 10 mV and VOUT = AV_{DD} − 50 mV.

DC Crosstalk
The dc change in the output level of one DAC at midscale in response to a full-scale code (all 0s to all 1s and vice versa) and the output change of all other DACs. It is expressed in LSBs.

DC Output Impedance
The effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time
The amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change. It is measured from the rising edge of $\overline{BUSY}$.

Digital-to-Analog Glitch Energy
The amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-s. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk
The glitch impulse that appears at the output of one DAC due to both the digital change and subsequent analog output change at another DAC. The victim channel is loaded with midscale, and DAC-to-DAC crosstalk is specified in nV-s.

Digital Crosstalk
The glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter is defined as the digital crosstalk and is specified in nV-s.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device's digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
This is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/(Hz)$^{1/2}$ in a 1 Hz bandwidth at 10 kHz.

TYPICAL PERFORMANCE CHARACTERISTICS

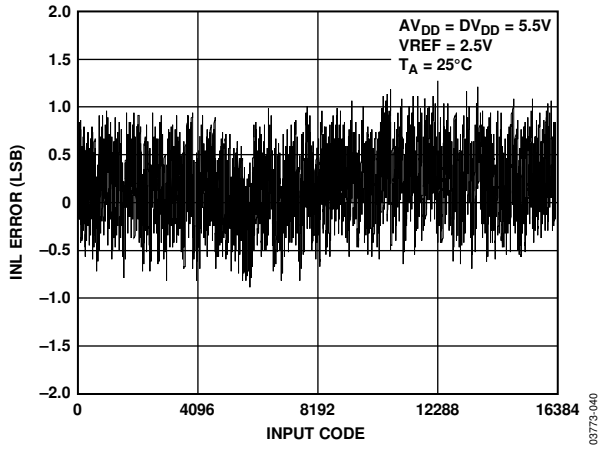


Figure 11. AD5390-5/AD5392-5 Typical INL Plot

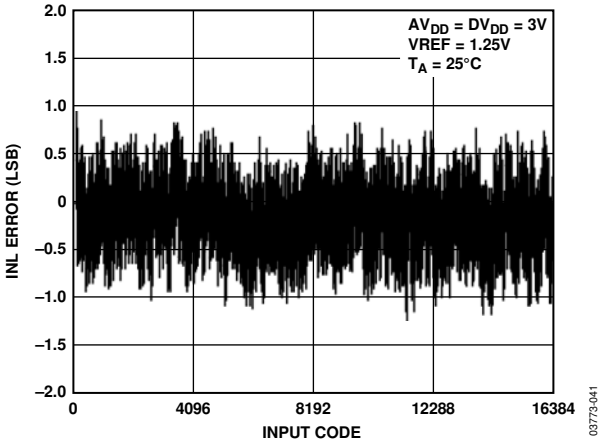


Figure 12. AD5390-3/AD5392-3 INL Plot

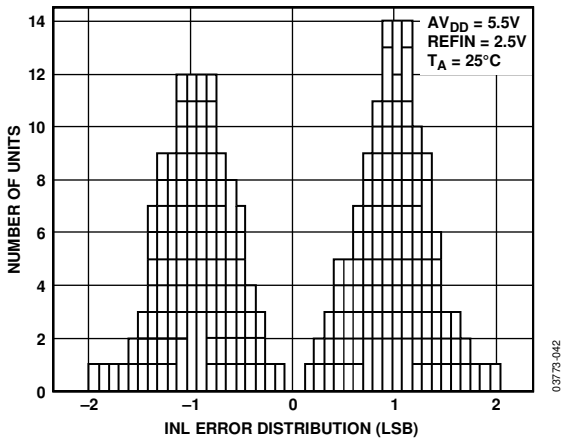


Figure 13. AD5390/AD5392 INL Histogram Plot

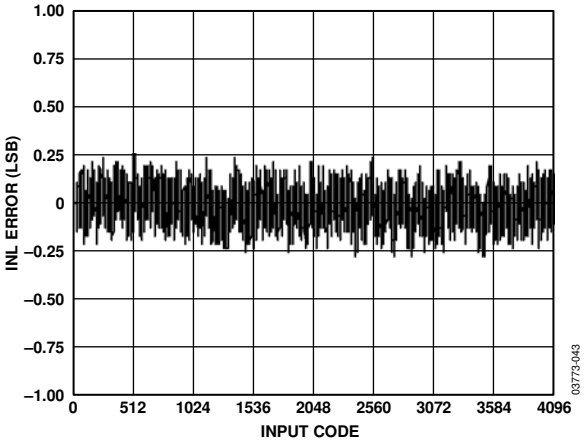


Figure 14. Typical AD5391-5 INL Plot

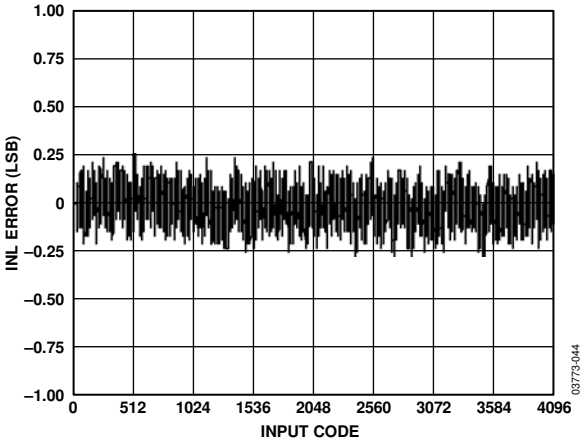


Figure 15. Typical AD5391-3 INL Plot

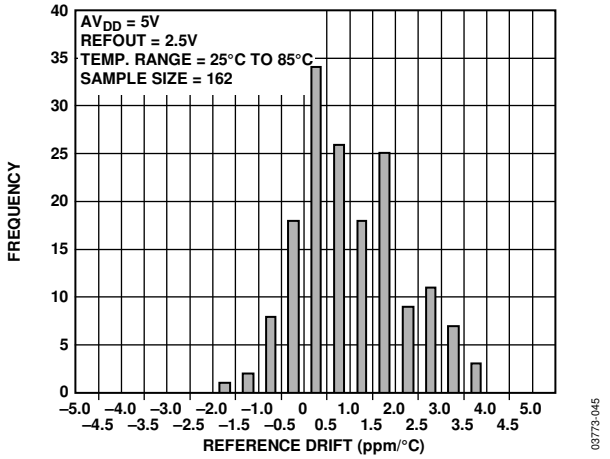


Figure 16. AD5390/AD5391/AD5392 REFOUT Temperature Coefficient

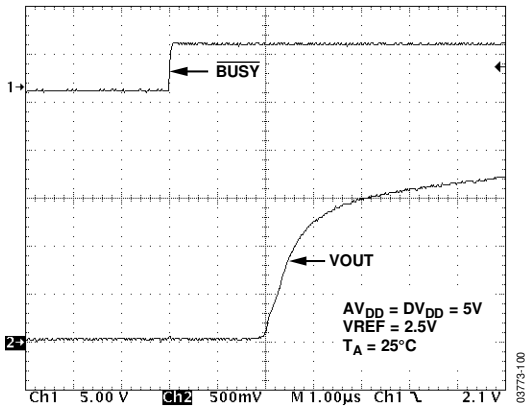


Figure 17. AD5390/AD5391/AD5392 Exiting Soft Power-Down

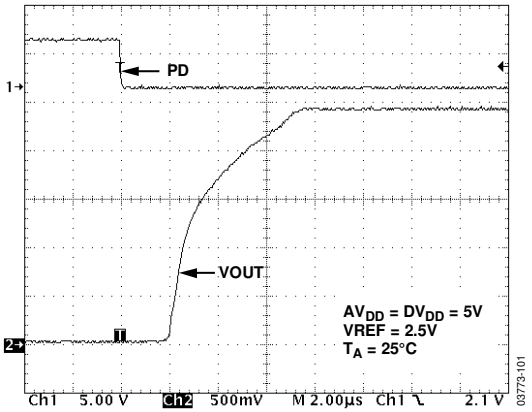


Figure 18. AD5390/AD5391/AD5392 Exiting Hardware Power-Down

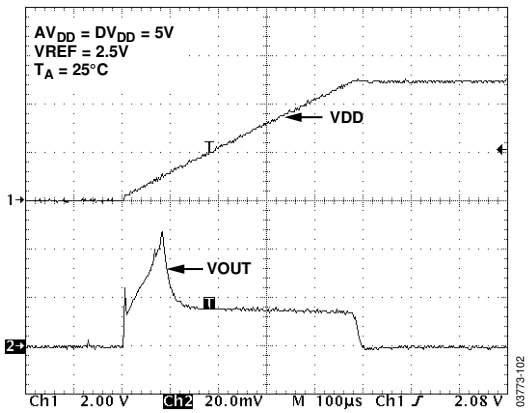


Figure 19. AD5390/AD5391/AD5392 Power-Up Transient

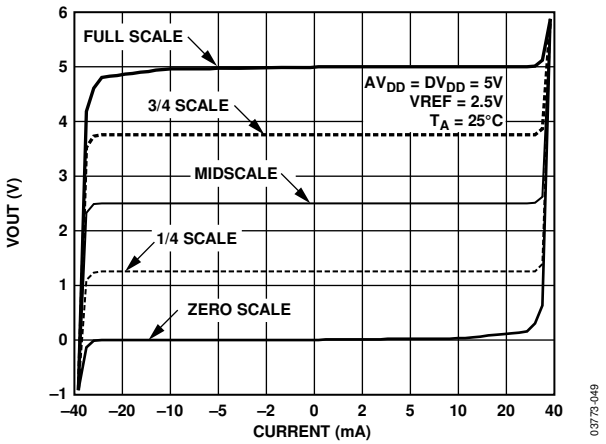


Figure 20. AD5390-5/AD5391-5/AD5392-5 Source and Sink Capability

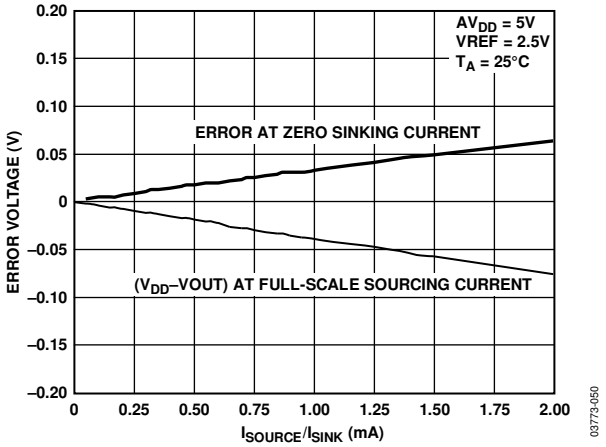


Figure 21. Headroom at Rails vs. Source/Sink Current

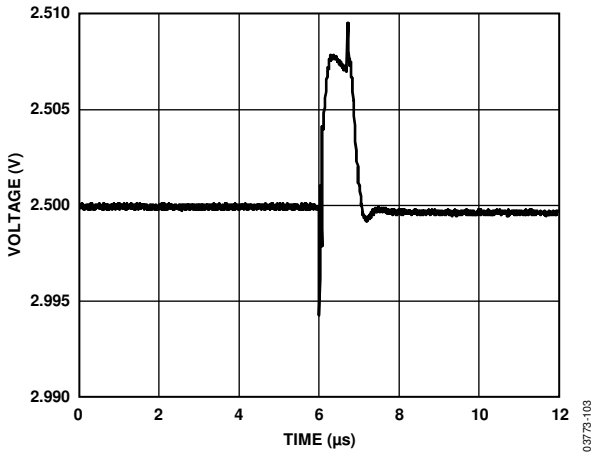


Figure 22. AD5390-5/AD5391-5/AD5392-5 Glitch Impulse Energy

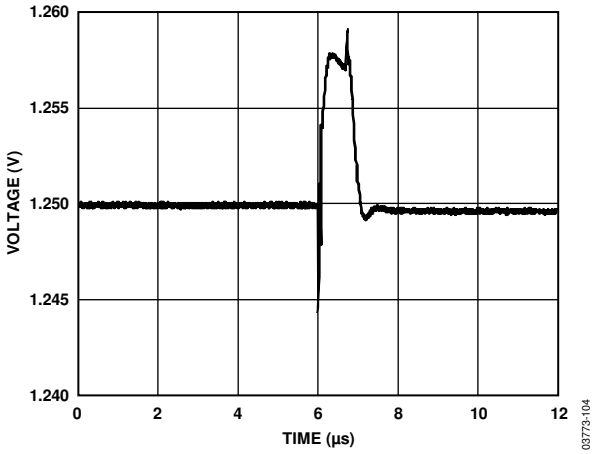


Figure 23. AD5390-3/AD5391-3/AD5392-3 Glitch Impulse

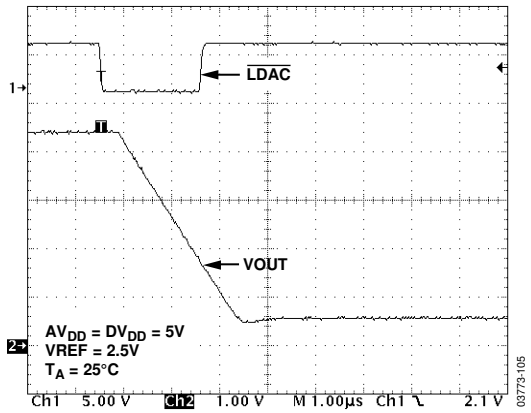


Figure 24. AD5390/AD5391/AD5392 Slew Rate Boost Off

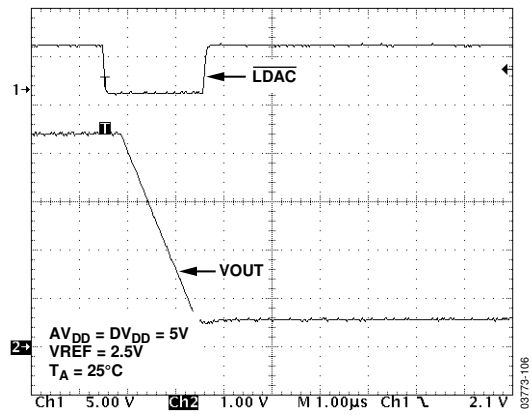


Figure 25. AD5390/AD5391/AD5392 Slew Rate Boost On

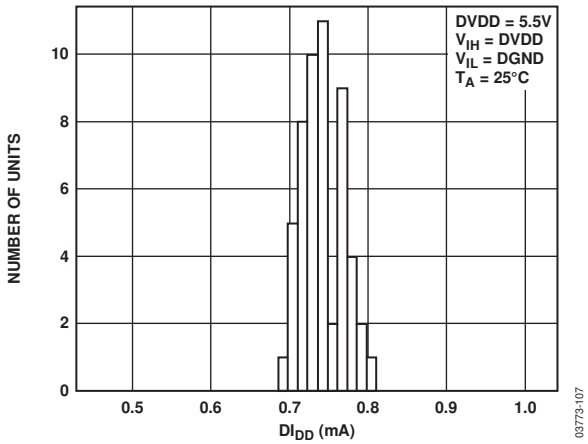


Figure 26. AD5390/AD5391/AD5392 DI_{DD} Histogram

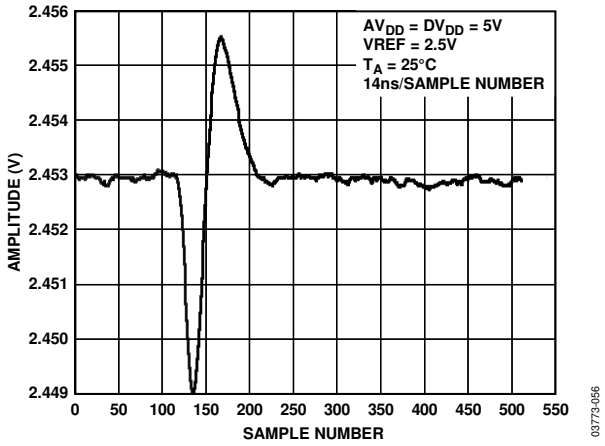


Figure 27. AD5390/AD5391/AD5392 Adjacent Channel Crosstalk

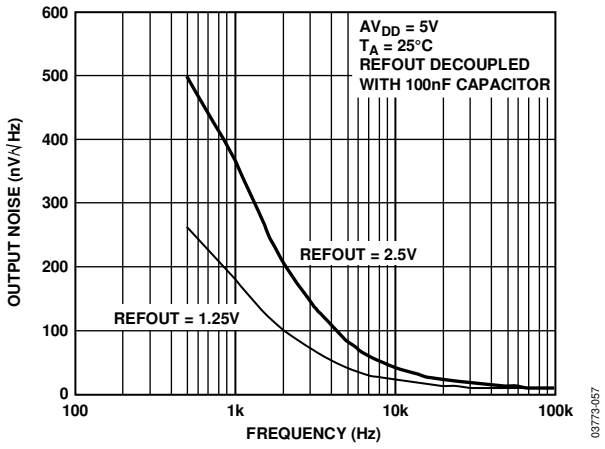


Figure 28. AD5390/AD5391/AD5392 REFOUT Noise Spectral Density

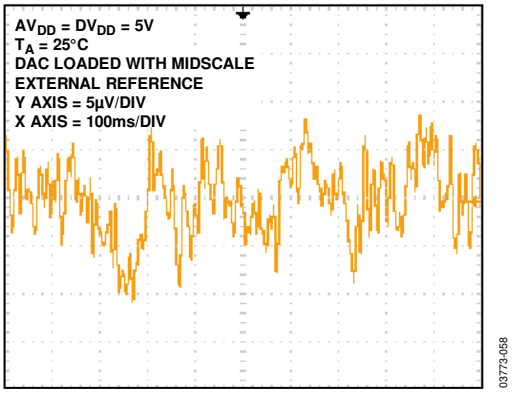


Figure 29. 0.1 Hz to 10 Hz Output Noise Plot

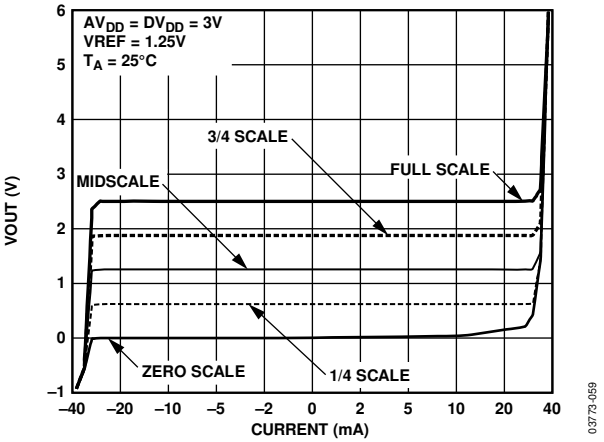


Figure 30. AD5390-3/AD5391-3/AD5392-3 Source and Sink Current Capability

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE

The AD5390/AD5391 are complete single-supply, 16-channel, voltage output DACs offering a resolution of 14 bits and 12 bits, respectively. The AD5392 is a complete single-supply, 8-channel, voltage output DAC offering 14-bit resolution. All devices are available in a 64-lead LFCSP and 52-lead LQFP, and feature serial interfaces. This family includes an internal select-able 1.25 V/2.5 V, 10 ppm/°C reference that can be used to drive the buffered reference inputs (alternatively, an external reference can be used to drive these inputs). All channels have an on-chip output amplifier with rail-to-rail output capable of driving a 5 kΩ load in parallel with a 200 pF capacitance.

The architecture of a single DAC channel consists of a 12-bit and 14-bit resistor-string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor-string architecture guarantees DAC monotonicity. The 12-bit and 14-bit binary digital code loaded to the DAC register determines at what node on the string the voltage is tapped off before being fed to the output amplifier. Each channel on these devices contains independent offset and gain control registers, allowing the user to digitally trim offset and gain.

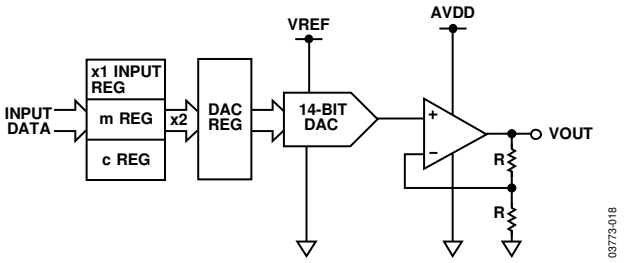


Figure 31. Single-Channel Architecture

These registers let the user calibrate out errors in the complete signal chain including the DAC using the internal m and c registers, which hold the correction factors. All channels are double-buffered, allowing synchronous updating of all channels using the $\overline{\text{LDAC}}$ pin. Figure 31 shows a block diagram of a single channel on the AD5390/AD5391/AD5392.

The digital input transfer function for each DAC can be represented as

$$x2 = \left((m+2)/2^{n}\right) \times x1 + \left(c - 2^{n-1}\right)$$

where:
$x2$ is the data-word loaded to the resistor-string DAC.
$x1$ is the 12-bit and 14-bit data-word written to the DAC input register.
m is the 12-bit and 14-bit gain coefficient (default is all 0x3FFE on the AD5390/AD5392 and 0xFFE on the AD5391). The LSB of the gain coefficient is zero.
n = DAC resolution (n = 14 for the AD5390/AD5392 and n = 12 for the AD5391).
c is the 12-bit and 14-bit offset coefficient (default is 0x2000 on the AD5390/AD5392 and 0x800 on the AD5391).

The complete transfer function for these devices can be represented as

$$VOUT = 2 \times VREF \times x2 / 2^{n}$$

where:
$x2$ is the data-word loaded to the resistor-string DAC.
V_{REF} is the reference voltage applied to the REFIN/REFOUT pin on the DAC when an external reference is used (2.5 V for specified performance on the AD5390-5/AD5391-5/AD5392-5 and 1.25 V on the AD5390-3/AD5391-3/AD5392-3).

DATA DECODING

AD5390/AD5392

The AD5390/AD5392 contain an internal 14-bit data bus. The input data is decoded depending on the data loaded to the REG1 and REG0 bits of the input serial register. This is shown in Table 9.

Data from the serial input register is loaded into the addressed DAC input register, offset (c) register, or gain (m) register. The format data, and the offset (c) and gain (m) register contents are shown in Table 10 to Table 12.

Table 9. Register Selection

REG1	REG0	Register Selected
1	1	Input data register (x1)
1	0	Offset register (c)
0	1	Gain register (m)
0	0	Special function registers (SFRs)

Table 10. AD5390/AD5392 DAC Data Format (REG1 = 1, REG0 = 1)

DB13 to DB0			DAC Output (V)
11 1111	1111	1111	$2 V_{REF} \times (16383/16384)$
11 1111	1111	1110	$2 V_{REF} \times (16382/16384)$
10 0000	0000	0001	$2 V_{REF} \times (8193/16384)$
10 0000	0000	0000	$2 V_{REF} \times (8192/16384)$
01 1111	1111	1111	$2 V_{REF} \times (8191/16384)$
00 0000	0000	0001	$2 V_{REF} \times (1/16384)$
00 0000	0000	0000	0

Table 11. AD5390/AD5392 Offset Data Format (REG1 = 1, REG0 = 0)

DB13 to DB0			Offset (LSB)
111111	1111	1111	+8191
111111	1111	1110	+8190
100000	0000	0001	+1
100000	0000	0000	+0
011111	1111	1111	–1
000000	0000	0001	–8191
000000	0000	0000	–8192

Table 12. AD5390/AD5392 Gain Data Format (REG1 = 0, REG0 = 1)

DB13 to DB0			Gain Factor
11 1111	1111	1110	1
10 1111	1111	1110	0.75
01 1111	1111	1110	0.5
00 1111	1111	1110	0.25
00 0000	0000	0000	0

AD5391

The AD5391 contains an internal 12-bit data bus. The input data is decoded depending on the value loaded to the REG1 and REG0 bits of the input serial register. The input data from the serial input register is loaded into the addressed DAC input register, offset (c) register, or gain (m) register. The format data and the offset (c) and gain (m) register contents are shown in Table 13 to Table 15.

Table 13. AD5391 DAC Data Format (REG1 = 1, REG0 = 1)

DB11 to DB0			DAC Output (V)
1111	1111	1111	$2 V_{REF} \times (4095/4096)$
1111	1111	1110	$2 V_{REF} \times (4094/4096)$
1000	0000	0001	$2 V_{REF} \times (2049/4096)$
1000	0000	0000	$2 V_{REF} \times (2048/4096)$
0111	1111	1111	$2 V_{REF} \times (2047/4096)$
0000	0000	0001	$2 V_{REF} \times (1/4096)$
0000	0000	0000	0

Table 14. AD5391 Offset Data Format (REG1 = 1, REG0 = 0)

DB11 to DB0			Offset (LSB)
1111	1111	1111	+2047
1111	1111	1110	+2046
1000	0000	0001	+1
1000	0000	0000	+0
0111	1111	1111	–1
0000	0000	0001	–2047
0000	0000	0000	–2048

Table 15. AD5391 Gain Data Format (REG1 = 0, REG0 = 1)

DB11 to DB0			Gain Factor
1111	1111	1110	1
1011	1111	1110	0.75
0111	1111	1110	0.5
0011	1111	1110	0.25
0000	0000	0000	0

INTERFACES

The AD5390/AD5391/AD5392 contain a serial interface that can be programmed to be DSP-, SPI-, and MICROWIRE-compatible, or I²C-compatible. The SPI/$\overline{I^2C}$ pin is used to select the interface mode.

To minimize both the power consumption of the device and the on-chip digital noise, the interface fully powers up only when the device is being written to, that is, on the falling edge of $\overline{SYNC}$.

DSP-, SPI-, AND MICROWIRE-COMPATIBLE SERIAL INTERFACE

The serial interface can be operated with a minimum of three wires in standalone mode or four wires in daisy-chain mode. Daisy-chaining allows many devices to be cascaded together to increase system channel count. The SPI/$\overline{I^2C}$ pin is tied to a Logic 1 pin to configure this mode of operation. The serial interface control pins are described in Table 16.

Table 16. Serial Interface Control Pins

Pin	Description
$\overline{SYNC}$, DIN, SCLK	Standard 3-wire interface pins.
DCEN	Selects standalone mode or daisy-chain mode.
SDO	Data out pin for daisy-chain mode.

Figure 2 to Figure 4 show timing diagrams for a serial write to the AD5390/AD5391/AD5392 in both standalone and daisy-chain mode. The 24-bit data-word format for the serial interface is shown in Table 17 to Table 19. Descriptions of the bits follow in Table 20.

Table 17. AD5390 16-Channel, 14-Bit DAC Serial Input Register Configuration

MSB																						LSB
$\overline{A}$/B	R/$\overline{W}$	0	0	A3	A2	A1	A0	REG1	REG0	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table 18. AD5391 16-Channel, 12-Bit DAC Serial Input Register Configuration

MSB																						LSB
$\overline{A}$/B	R/$\overline{W}$	0	0	A3	A2	A1	A0	REG1	REG0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	X	X

Table 19. AD5392 8-Channel, 14-Bit DAC Serial Input Register Configuration

MSB																						LSB
$\overline{A}$/B	R/$\overline{W}$	0	0	0	A2	A1	A0	REG1	REG0	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table 20. Serial Input Register Configuration Bit Descriptions

Bit	Description
$\overline{A}$/B	When toggle mode is enabled, this bit selects whether the data write is to the A or B register. With toggle mode disabled, this bit should be set to zero to select the A data register.
R/$\overline{W}$	The read or write control bit.
A3 to A0	Used to address the input channels.
REG1 and REG0	Select the register to which data is written, as outlined in Table 9.
DB13 to DB0	Contain the input data-word.
X	Don't care condition.