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Evaluating the AD7091R-2/AD7091R-4/AD7091R-8 12-Bit Monitor and Control System

FEATURES

- Full featured evaluation board for the AD7091R-2/AD7091R-4/AD7091R-8 family
- On-board power supplies
- Standalone capability
- System demonstration platform (SDP) compatible (EVAL-SDP-CB1Z)
- PC software for control and data analysis (download from product page)

EVALUATION KIT CONTENTS

- Evaluation board
- Screw/nut kit
- Mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

- EVAL-SDP-CB1Z (must be ordered separately) includes a USB cable
- Signal source
- PC running Windows XP SP2, Windows Vista, or Windows 7 with USB 2.0 port

EVALUATION BOARD DESCRIPTION

The EVAL-AD7091R-2SDZ, EVAL-AD7091R-4SDZ, and EVAL-AD7091R-8SDZ are full featured evaluation boards designed to allow the user to easily evaluate all features of the AD7091R-2/AD7091R-4/AD7091R-8 family of analog-to-digital converters (ADCs). The evaluation board can be controlled via the SDP connector (J13). The SDP board (EVAL-SDP-CB1Z) allows the evaluation board to be controlled through the USB port of a PC using the evaluation board software available for download from the product page.

On-board components include: the AD8031 high speed precision rail-to-rail op amp, the AD8032 high speed precision rail-to-rail dual op amp, the ADP3303 high accuracy 200 mA low dropout linear regulator, and the REF193 3.0 V precision micropower, low dropout, low voltage reference.

FUNCTIONAL BLOCK DIAGRAM

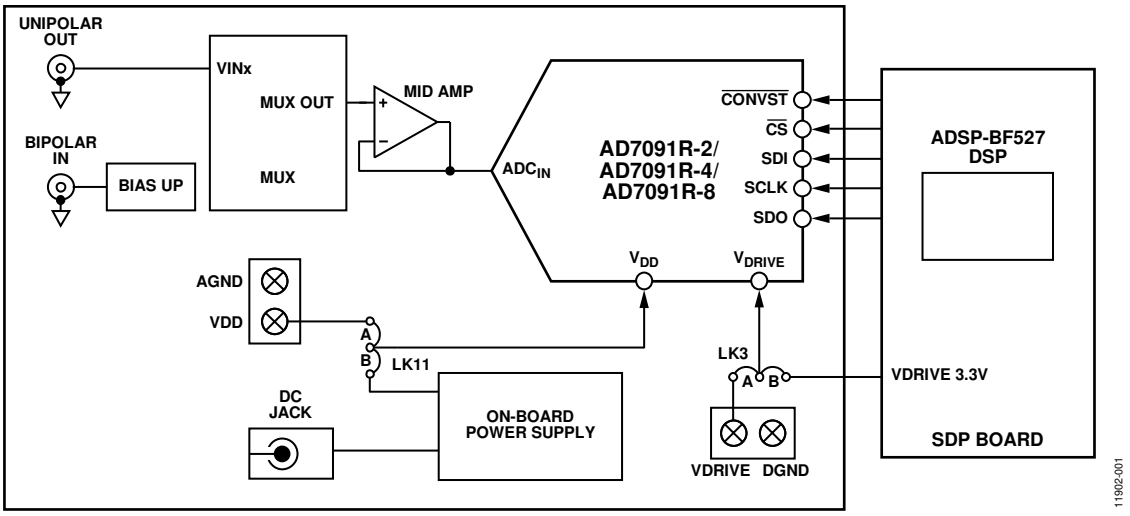

Figure 1. EVAL-AD7091R-2SDZ, EVAL-AD7091R-4SDZ, and EVAL-AD7091R-8SDZ Block Diagram

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REVISION HISTORY

6/14—Rev. 0 to Rev. A

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12/13—Revision 0: Initial Version

QUICK START GUIDE

Follow these steps to quickly evaluate the AD7091R-2/AD7091R-4/AD7091R-8 ADCs:

1. Install the evaluation software from the AD7091R-2/AD7091R-4/AD7091R-8 product page. Ensure that the EVAL-SDP-CB1Z board is disconnected from the USB port of the PC while installing the software. The PC may need to be restarted after the installation.
2. Ensure that the various link options are configured as outlined in Table 2.
3. Connect the EVAL-SDP-CB1Z board to the evaluation board as shown in Figure 2. Screw the two boards together using the enclosed nylon screw/nut set to ensure that the boards connect firmly together.
4. Connect the power supply adapter included in the kit to Connecter J1 on the evaluation board.
5. Connect the EVAL-SDP-CB1Z board to the PC via the USB cable. For Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
6. Launch the evaluation software from the **Analog Devices** subfolder in the **Programs** menu.
7. Connect an input signal via either the BIPOLAR IN/UNIPOLAR OUT connectors, J10 and J14, or any of the unipolar channel inputs, J5 to J8 and J16 to J19.

Figure 2. Evaluation Board (Left) Connected to the SDP Board (Right)

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

This user guide describes the evaluation board for the AD7091R-2/AD7091R-4/AD7091R-8 family of ADCs. All models in this family are 12-bit, ultralow power, successive approximation ADCs. These devices operate from a single 2.7 V to 5.25 V power supply and are capable of achieving a throughput rate of 1 MSPS. These ADCs also feature an on-chip conversion clock, an accurate reference, and a high speed serial interface.

The conversion process and data acquisition are controlled using a $\overline{\text{CONVST}}$ signal and an internal oscillator. The AD7091R-2/AD7091R-4/AD7091R-8 devices have a serial interface allowing data to be read after the conversion, while achieving a 1 MSPS throughput rate. This family of devices uses advanced design and process techniques to achieve ultralow power dissipation at high throughput rates. An on-chip, accurate 2.5 V reference is available.

Complete specifications for the AD7091R-2/AD7091R-4/AD7091R-8 devices are provided in the device data sheet, available from Analog Devices, Inc., which should be consulted in conjunction with this user guide when using the evaluation board. Full details on the EVAL-SDP-CB1Z are available online.

HARDWARE LINK OPTIONS

The functions of the link options are described in Table 2. The default setup is configured to operate the board with the mains power supply adapter and to interface to the EVAL-SDP-CB1Z board.

POWER SUPPLIES

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are set according to the required operating mode. See Table 2 for the complete list of link options.

This evaluation board is supplied with a wall-mountable switching power supply that provides 9 V dc output. Connect the supply to a 100 V to 240 V ac wall outlet at 50 Hz to 60 Hz. The output from the supply is provided through a 2.0 mm inner diameter jack that connects to the evaluation board at J1. The 9 V supply is connected to the on-board 5 V linear regulator that supplies the correct bias to each of the various sections on the evaluation board and on the EVAL-SDP-CB1Z board.

When using this evaluation board with the EVAL-SDP-CB1Z board, it is necessary to power the board through the J1 connector.

If the evaluation board is used without the 9 V adapter, an external power supply in the range of 2.7 V to 5.25 V must be connected to the V_{DD} input to supply the AD7091R-2/AD7091R-4/AD7091R-8 V_{DD} pin. In addition, an external supply in the range of 1.65 V to 5.25 V must be connected to the V_{DRIVE} input to supply the V_{DRIVE} pin.

Each supply is decoupled on this board using 10 µF tantalum and 100 nF multilayer ceramic capacitors.

There are two main ground planes, AGND and DGND. These are connected at one location close to the ADC.

Caution

When the EVAL-AD7091R-2SDZ/EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ is connected to the EVAL-SDP-CB1Z, care must be taken to ensure that, if an external voltage is supplied to the V_{DRIVE} input connector, J4, the voltage does not exceed 3.3 V. Otherwise, permanent damage may occur to the EVAL-SDP-CB1Z board.

Table 1. External Power Supplies Required

Power Supply	Voltage Range	Purpose
DC Jack	9 V ± 5%	Supplies power to on-board power management devices
V_{DD}	2.7 V to 5.25 V	Analog supply rail
V_{DRIVE}	1.65 V to 5.25 V	Digital supply rail without EVAL-SDP-CB1Z connected
	3.3 V ± 5%	Digital supply rail with EVAL-SDP-CB1Z connected

Table 2. Link Options

Category	Link	Default Position	Function
Power Supplies	LK1	A	This link is used to select the op amp positive supply source. In Position A, the positive supply is generated from the 9 V dc jack plug. In Position B, the positive supply is provided by the J3-3 connector.
	LK2	A	This link is used to select the op amp negative supply source. In Position A, the negative supply is generated from the 9 V dc jack plug. In Position B, the negative supply is provided by the J3-1 connector.
	LK3	A	This link is used to select the source of the V_{DRIVE} supply for the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the V_{DRIVE} supply is sourced from the on-board 5 V regulator. In Position B, the V_{DRIVE} supply is sourced externally via the J4-1 connector.
Termination	LK4	Inserted	Adds a 51 Ω termination resistor to AGND at VIN6. Inserted—51 Ω termination on the VIN6 input. Not inserted—no 51 Ω termination on the VIN6 input.
	LK5	Inserted	Adds a 51 Ω termination resistor to AGND at VIN4. Inserted—51 Ω termination on the VIN4 input. Not inserted—no 51 Ω termination on the VIN4 input.
	LK6	Inserted	Adds a 51 Ω termination resistor to AGND at VIN2. Inserted—51 Ω termination on the VIN2 input. Not inserted—no 51 Ω termination on the VIN2 input.
	LK7	Inserted	Adds a 51 Ω termination resistor to AGND at VIN0. Inserted—51 Ω termination on the VIN0 input. Not inserted—no 51 Ω termination on the VIN0 input.
Power Supplies	LK8	B	This link is used to select the source of the V_{DRIVE} supply for the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the V_{DRIVE} supply is sourced from the on-board 5 V regulator or J9-1. In Position B, the V_{DRIVE} supply is sourced from the on-board 3.3 V regulator.
	LK9	A	This link is used to select the source of the V_{DD} supply for the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the V_{DD} supply is sourced from the on-board 5 V regulator. In Position B, the V_{DD} supply is sourced externally via the J-1 connector.
Termination	LK10	Inserted	Adds a 51 Ω termination resistor to AGND at BIPOLAR IN. Inserted—51 Ω termination on the BIPOLAR IN input. Not inserted—no 51 Ω termination on the BIPOLAR IN input.

Category	Link	Default Position	Function
Power Supplies	LK11	B	This link is used to select the source of the V_{DD} supply for the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the V_{DD} supply is sourced from either the on-board 5 V regulator or J9-1. In Position B, the V_{DD} supply is sourced from the on-board 3.3 V regulator.
Reference Input	LK12	Not Inserted	This link is used to select the source of the reference input for the AD7091R-2/AD7091R-4/AD7091R-8. Inserted—reference voltage is generated by REF193. Not inserted—reference either generated internally by AD7091R-2/AD7091R-4/AD7091R-8 or provided by the J12 connector.
Analog Input	LK13	A	This link is used to select the connection option for the MUX_{OUT} pin. In Position A, the MUX_{OUT} pin is connected to Pin 3 of U16. In Position B, the MUX_{OUT} pin is connected to Pin 3 of U15 (U15 is the default, Do Not Insert). In Position C, the MUX_{OUT} pin is connected directly to LK14.
	LK14	A	This link is used to select the source of the ADC_{IN} input for the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the ADC_{IN} pin is sourced from U16. In Position B, the ADC_{IN} pin is sourced from U15 (U15 is the default, Do Not Insert). In Position C, the ADC_{IN} pin is sourced directly from position C of LK13.
Termination	LK15	Inserted	Adds a 51 Ω termination resistor to AGND at VIN7. Inserted—51 Ω termination on the VIN7 input. Not inserted—no 51 Ω termination on the VIN7 input.
	LK16	Inserted	Adds a 51 Ω termination resistor to AGND at VIN5. Inserted—51 Ω termination on the VIN5 input. Not inserted—no 51 Ω termination on the VIN5 input.
	LK17	Inserted	Adds a 51 Ω termination resistor to AGND at VIN3. Inserted—51 Ω termination on the VIN3 input. Not inserted—no 51 Ω termination on the VIN3 input.
	LK18	Inserted	Adds a 51 Ω termination resistor to AGND at VIN1. Inserted—51 Ω termination on the VIN1 input. Not inserted—no 51 Ω termination on the VIN1 input.

Category	Link	Default Position	Function
Analog Input	SL1	A	This link is used in conjunction with SL2 to select the buffering option for the VIN0 input. In Position A, the VIN0 input signal is buffered by U9-A. In Position B, the VIN0 input signal bypasses the U9-A buffer.
	SL2	A	This link is used in conjunction with SL1 to select the buffering option for the VIN0 input. In Position A, the VIN0 input signal is buffered by U9-A. In Position B, the VIN0 input signal bypasses the U9-A buffer.
	SL3	A	This link is used in conjunction with SL4 to select the buffering option for the VIN1 input. In Position A, the VIN1 input signal is buffered by U25-B. In Position B, the VIN1 input signal bypasses the U25-B buffer.
	SL4	A	This link is used in conjunction with SL3 to select the buffering option for the VIN1 input. In Position A, the VIN1 input signal is buffered by U25-B. In Position B, the VIN1 input signal bypasses the U25-B buffer.
	SL5	A	This link is used in conjunction with SL6 to select the buffering option for the VIN2 input. In Position A, the VIN2 input signal is buffered by U9-B. In Position B, the VIN2 input signal bypasses the U9-B buffer.
	SL6	A	This link is used in conjunction with SL5 to select the buffering option for the VIN2 input. In Position A, the VIN2 input signal is buffered by U9-B. In Position B, the VIN2 input signal bypasses the U9-B buffer.
	SL7	A	This link is used in conjunction with SL8 to select the buffering option for the VIN3 input. In Position A, the VIN3 input signal is buffered by U25-A. In Position B, the VIN3 input signal bypasses the U25-A buffer.
	SL8	A	This link is used in conjunction with SL7 to select the buffering option for the VIN3 input. In Position A, the VIN3 input signal is buffered by U25-A. In Position B, the VIN3 input signal bypasses the U25-A buffer.
	SL9	A	This link is used in conjunction with SL10 to select the buffering option for the VIN7 input. In Position A, the VIN7 input signal is buffered by U24-A. In Position B, the VIN7 input signal bypasses the U24-A buffer.
	SL10	A	This link is used in conjunction with SL9 to select the buffering option for the VIN7 input. In Position A, the VIN7 input signal is buffered by U24-A. In Position B, the VIN7 input signal bypasses the U24-A buffer.
	SL11	A	This link is used in conjunction with SL12 to select the buffering option for the VIN6 input. In Position A, the VIN6 input signal is buffered by U8-B. In Position B, the VIN6 input signal bypasses the U8-B buffer.
	SL12	A	This link is used in conjunction with SL11 to select the buffering option for the VIN6 input. In Position A, the VIN6 input signal is buffered by U8-B. In Position B, the VIN6 input signal bypasses the U8-B buffer.
	SL13	A	This link is used in conjunction with SL14 to select the buffering option for the VIN5 input. In Position A, the VIN5 input signal is buffered by U24-B. In Position B, the VIN5 input signal bypasses the U24-B buffer.
	SL14	A	This link is used in conjunction with SL13 to select the buffering option for the VIN5 input. In Position A, the VIN5 input signal is buffered by U24-B. In Position B, the VIN5 input signal bypasses the U24-B buffer.
	SL15	A	This link is used in conjunction with SL16 to select the buffering option for the VIN4 input. In Position A, the VIN4 input signal is buffered by U8-A. In Position B, the VIN4 input signal bypasses the U8-A buffer.
	SL16	A	This link is used in conjunction with SL15 to select the buffering option for the VIN4 input. In Position A, the VIN4 input signal is buffered by U8-A. In Position B, the VIN4 input signal bypasses the U8-A buffer.

Category	Link	Default Position	Function
Digital Input	SL17	A	This link is not connected to the circuit because of the R124 Do Not Insert instruction. Position A is the default position. Do not use in Position B.
	SL18	B	This link is not connected to the circuit because of the R125 Do Not Insert instruction. Do not use in Position A. Position B is the default position.
	SL19	A	This link is used to determine the serial clock input to the AD7091R-2/AD7091R-4/AD7091R-8. In Position A, the serial clock signal is produced by the U19 AND gate. Do not use in Position B.
	SL20	A	This link is used to determine the digital host pin that receives the ADC serial data output In Position A, the serial data output is provided to the SPORT_DR0 pin of J13. Do not use in Position B.

SOCKETS/CONNECTORS

The connectors and sockets on the EVAL-AD7091R-2SDZ/EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ are outlined in Table 3.

Table 3. On-Board Connectors

Connector	Function
J1	9 V, 2.0 mm dc jack connector
J2	External PWR_IN and GND power connector
J3	External OP_AMP_POS, OP_AMP_NEG, and GND power connector
J4	External V_{DRIVE} and GND power connector
J5	VIN6 analog input signal
J6	VIN4 analog input signal
J7	VIN2 analog input signal
J8	VIN0 analog input signal
J9	External VDD and GND power connector
J10	BIPOLAR IN analog input signal to bias up circuit
J11	MUX_{OUT} signal from output of multiplexer
J12	External reference voltage connector
J13	120-way connector for EVAL-SDP-CB1Z interface
J14	UNIPOLAR OUT analog signal from bias up circuit
J15	ADC_{IN} analog input signal
J16	VIN7 analog input signal
J17	VIN5 analog input signal
J18	VIN3 analog input signal
J19	VIN1 analog input signal

The default interface to this evaluation board is via the 120-way connector, which connects the EVAL-AD7091R-2SDZ/EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ to the EVAL-SDP-CB1Z board.

TEST POINTS

There are numerous test points on the EVAL-AD7091R-2SDZ/EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ boards. These test points provide easy access to the signals from the evaluation board for probing, evaluation, and debugging.

It is also possible to access the AD7091R-2/AD7091R-4/AD7091R-8 devices via the test points to operate the evaluation board in standalone mode without the need for the EVAL-SDP-CB1Z board.

BASIC HARDWARE SETUP

The EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ connects to the EVAL-SDP-CB1Z system demonstration platform board. The EVAL-SDP-CB1Z board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 2 shows a photograph of the connections between the EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ daughter board and the EVAL-SDP-CB1Z board.

The analog input range to the AD7091R-2/AD7091R-4/AD7091R-8 devices is 0 V to V_{REF} and should not be exceeded. When using the on-chip reference, V_{REF} is 2.5 V. An input signal in the range of 2.5 V p-p should be connected to the evaluation board via any analog input connector.

If an input signal is a bipolar input, it should be connected to BIPOLAR IN, the J10 connector. This signal is biased to $V_{REF}/2$ via the bias up circuitry on the EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ. The signal source should be a low impedance source. The signal should then be connected to any unipolar analog input by connecting UNIPOLAR OUT, the J14 connector, to any connector (J5 to J8 or J16 to J19). On-board unity gain amplifiers buffer the signal to the ADC. This is the default configuration on the evaluation board.

A unipolar input signal should be directly connected to any multiplexer input VIN0 to VIN7, the J5 to J8 and J16 to J19 connectors. On-board unity gain amplifiers buffer the signal to the AD7091R-2/AD7091R-4/AD7091R-8.

Before connecting power, connect the EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ to Connector A on the EVAL-SDP-CB1Z board. A nylon screw/nut set is included in the evaluation kit and can be used to ensure that the evaluation board and the EVAL-SDP-CB1Z boards are connected firmly together.

Ensure that the link options are in the default positions as outlined in Table 2.

After the evaluation board and the EVAL-SDP-CB1Z board are connected securely, connect the power to the evaluation board. The evaluation board requires an external power supply adapter, which is included in the evaluation board kit. Connect this power supply to Connector J1 on the evaluation board. For further details on the required power supply connections and options, see the Power Supplies section.

Before connecting the EVAL-SDP-CB1Z board to your PC, ensure that the evaluation software has been installed. The full software installation procedure is detailed in the Evaluation Board Software section.

Finally, connect the EVAL-SDP-CB1Z board to the PC via the USB cable enclosed in the EVAL-SDP-CB1Z kit. If using a Windows XP platform, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ kit includes software available for download from the product page.

1. Start the Windows operating system and download the evaluation software from the relevant product page.
2. Unzip the downloaded file.
3. Double-click the **setup.exe** file to run the install. The default location for the software is **C:\Program Files\Analog Devices\AD7091R-x**
4. Power up the evaluation board as described in the Power Supplies section.
5. Connect the evaluation board and the EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.
6. When the software detects the evaluation board, proceed through any dialog boxes that appear to finalize the installation.

There are two parts to the installation:

- EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ evaluation software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Follow Step 1 to Step 4 (see Figure 3 to Figure 6) to install the evaluation board software. Follow Step 5 to Step 8 (see Figure 7 to Figure 10) to install the EVAL-SDP-CB1Z drivers. Proceed through all of the installation steps, allowing the software and drivers to be placed in the appropriate locations. Connect the EVAL-SDP-CB1Z board to the PC only after the software and drivers have been installed.

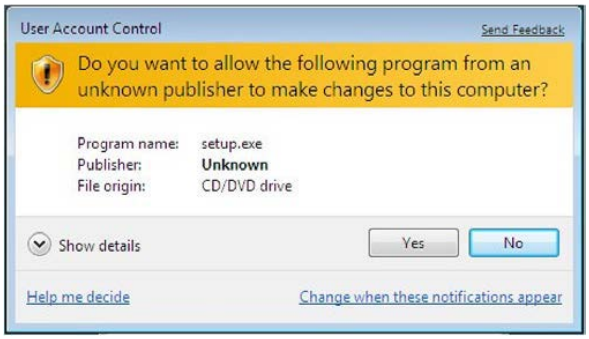

Figure 3. Evaluation Software Installation—User Account Control

1. Click **Yes** to begin the installation process.

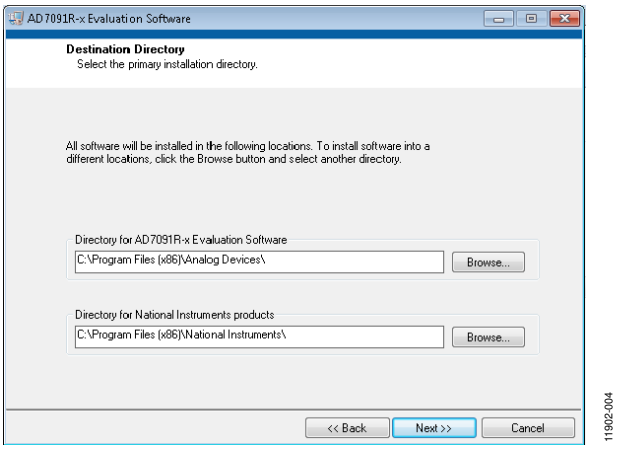

Figure 4. Evaluation Software Installation—Destination Directory

2. Select the installation directory. Click **Next**.

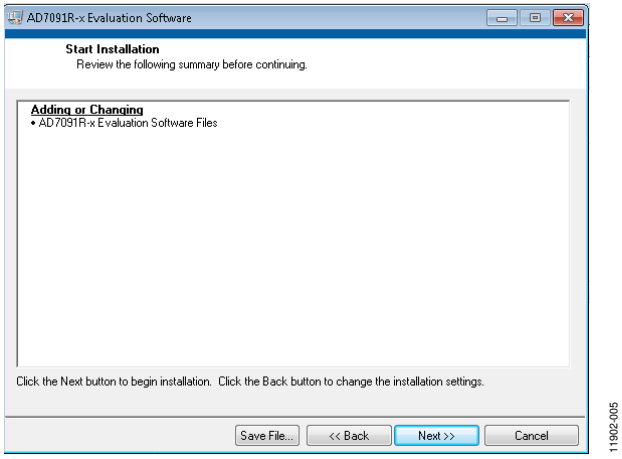

Figure 5. Evaluation Software Installation—Start Installation

3. Click **Next** to install the software.

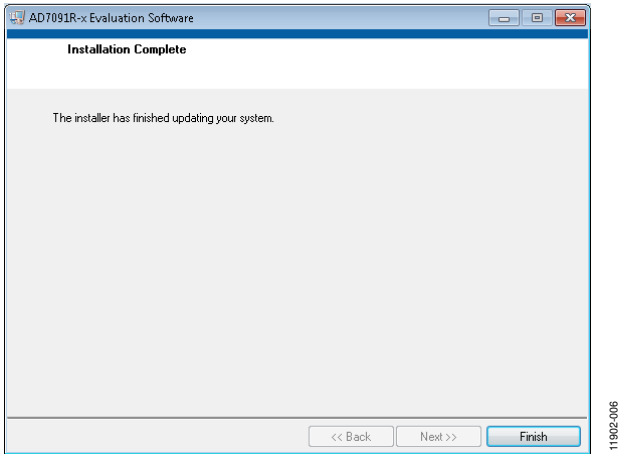

Figure 6. Evaluation Software Installation—Installation Complete

4. The installation of the evaluation software completes. Click **Finish** to proceed with the installation of the drivers.

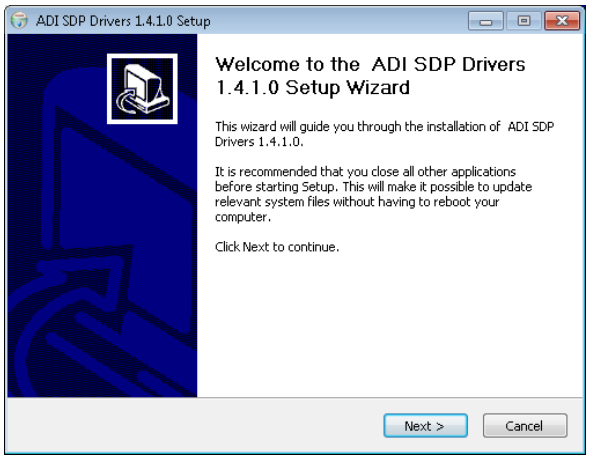

Figure 7. EVAL-SDP-CB1Z Drivers Installation—Setup Wizard

5. The setup wizard opens. Click **Next** to begin the driver installation process.

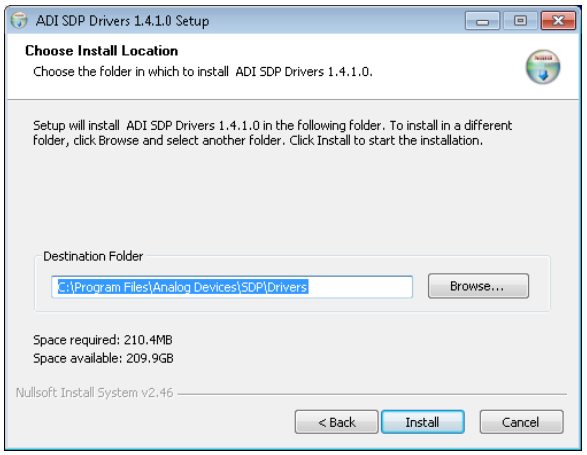

Figure 8. EVAL-SDP-CB1Z Drivers Installation—Choose Install Location

6. Select a destination folder for the SDP drivers, and click **Install**.

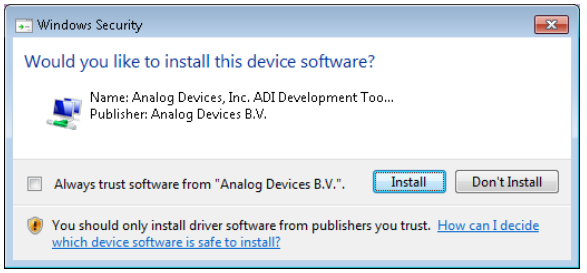

Figure 9. EVAL-SDP-CB1Z Drivers Installation—Windows Security

7. Click **Install** to proceed with the installation.

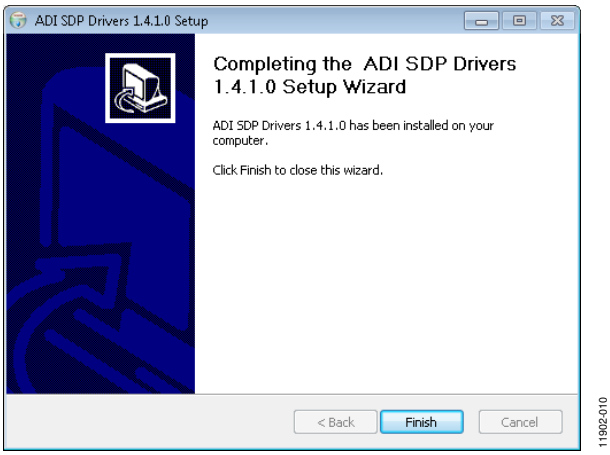

Figure 10. EVAL-SDP-CB1Z Drivers Installation—Complete

8. Click **Finish**.

After the evaluation software installation is complete, connect the EVAL-AD7091R-2SDZ/ EVAL-AD7091R-4SDZ/EVAL-AD7091R-8SDZ board to the EVAL-SDP-CB1Z board as described in the Evaluation Board Hardware section.

When you first plug in the EVAL-SDP-CB1Z board via the USB cable provided, allow the **Found Hardware Wizard** to run. After the drivers are installed, you can check that the board is connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right-clicking **My Computer**>**Manage**>**Device Manager** from the list of **System Tools** as shown in Figure 11.

The EVAL-SDP-CB1Z SDP-B board should appear under **ADI Development Tools**. This completes the installation.

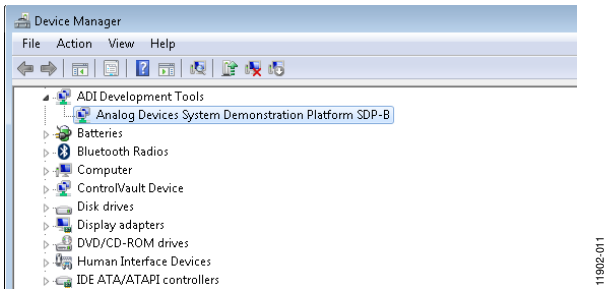

Figure 11. Device Manager

LAUNCHING THE SOFTWARE

After the evaluation board and EVAL-SDP-CB1Z board are correctly connected to your PC, the evaluation software can be launched.

From the **Start** menu, select **Programs**>**Analog Devices**> **AD7091R-x.** The main window of the software then opens (see Figure 13).

If the evaluation board is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 12). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

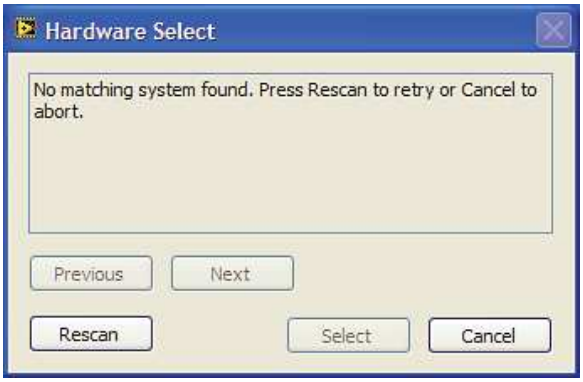

Figure 12. Connectivity Error Alert

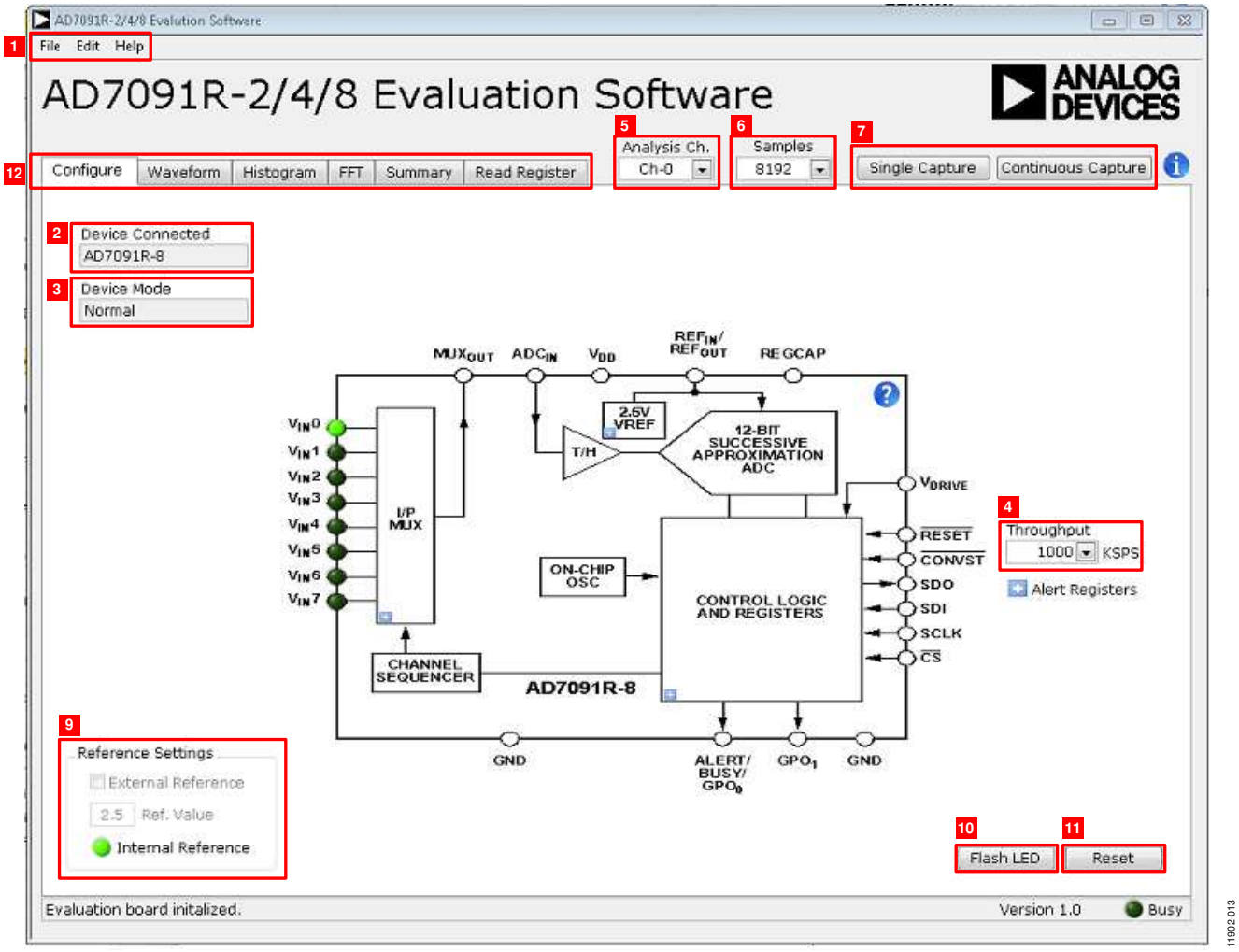

Figure 13. Evaluation Software Main Window

DESCRIPTION OF MAIN WINDOW

The following tools allow user control of the different chart displays. When the software is launched, the main software window opens (see Figure 13).

The user software panel as shown in Figure 13 has the following features:

- Menu bar
- Control buttons
- Configuration display
- Data capture display
- Register read

Menu Bar

The menu bar, labeled 1 in Figure 13, consists of the **File**, **Edit**, and **Help** menus.

File Menu

Open. Loads previously captured data in comma separated values (CSV) format for analysis.

Save Analysis Data. Saves captured data in CSV format for future analysis.

Save Picture. Saves captured data images as a JPEG file.

Save Register Configuration. Saves current device configuration for later use.

Exit. Exits the program.

Edit Menu

Reinitialize to default. Places the evaluation board in a known default state.

Help Menu

Context Help. Turns on context sensitive help.

User Guide. Open the evaluation kit user guide.

About. Provides evaluation kit information.

Control Buttons, Drop-Down Boxes, and Indicators

The evaluation software includes the following control buttons, drop-down boxes, and indicators.

Device Connected. Labeled 2 in Figure 13, this indicates which model of the AD7091R-2/AD7091R-4/AD7091R-8 has been detected.

Device Mode. Labeled 3, this indicates the operating mode of the ADC. In **Normal** mode, the ADC is ready to acquire samples. In **Sleep** mode, the device enters power-down mode with sampling disabled.

Throughput. Labeled 4 in Figure 13, this selects the sampling rate of the data acquisition.

Analysis Ch. Labeled 5, this selects which channel will be analyzed and will thus have its parametric performance data displayed in the plot analysis blocks.

Samples. Labeled 6, this selects the number of samples to be completed in a single acquisition.

Single Capture. Initiates the sampling and readback of the defined number of measurements. See Label 7 in Figure 13.

Continuous Capture. Performs a continuous capture from the ADC. Click a second time to stop sampling. See Label 7 in Figure 13.

Reference Settings. Indicates current reference setting (see Section 9 in Figure 13). If **External Reference** is selected, the user has the option to provide an off-board external reference**.** If this option is selected, the supplied reference value must be entered in **Ref. Value**.

Flash LED. Labeled 10 in Figure 13, this causes the orange **LED1A** on the SDP board to flash, which can be a useful debugging tool.

Reset. Labeled 11 in Figure 13, this resets the ADC and places the default configuration in the control register. Click a second time to release reset state.

Configuration Buttons

There are four configuration register buttons contained within the block diagram on the **Configure** tab. Selecting these blue buttons,  , produce pop-up boxes that allow the user to configure the respective section of the block diagram.

The four buttons control the enabled channels (**I/P MUX),** the source of the reference input (**2.5V VREF**), the **CONTROL LOGIC AND REGISTERS**, and the **Alert Register**. Refer to the AD7091R-2/AD7091R-4/AD7091R-8 data sheet for details on available configuration options.

Note that the light emitting diode (LED), D3, can be used to indicate an alert to the evaluation board user. Refer to the data sheet for instructions on configuring the **CONTROL LOGIC AND REGISTERS** so that a high state of the alert pin on the ADC enables the LED, D3.

Data Capture Display

There are four tabs that display the conversion data in different formats: **Waveform**, **Histogram**, **FFT**, and **Summary**. See Label 12 in Figure 13.

The tools shown in Figure 14 allow user control of the different chart displays within the four tabs.

1. USED FOR CONTROLLING THE CURSOR, IF PRESENT.
2. USED FOR ZOOMING IN AND OUT.
3. USED FOR PANNING.

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Figure 14. Chart Tools

WAVEFORM CAPTURE

Figure 15 illustrates the tab used for **Waveform** capture.

The waveform analysis reports the amplitudes recorded from the captured signal as well as the frequency of the signal tone. The analysis report is generated for the channel selected via the **Analysis Ch.** drop-down menu (see Label 1 in Figure 15).

All enabled channels can be shown in the waveform plot. It is possible to remove any undesired channel(s) from the plot by deselecting that channel within the **Plot Legend** (labeled 2). If an alert is generated, the **Alert** indicator (labeled 3) on the waveform panel illuminates.

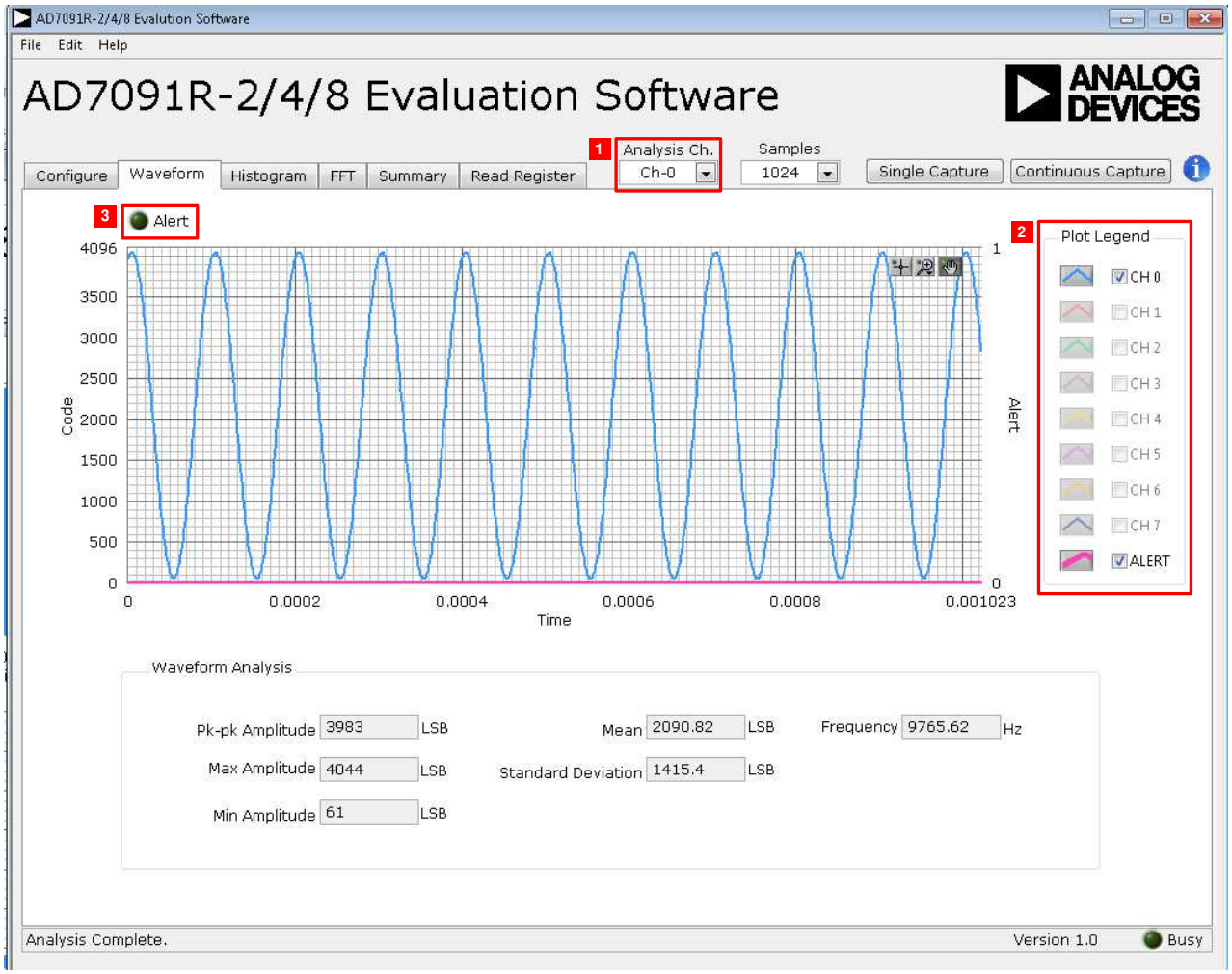

Figure 15. Waveform Capture Tab

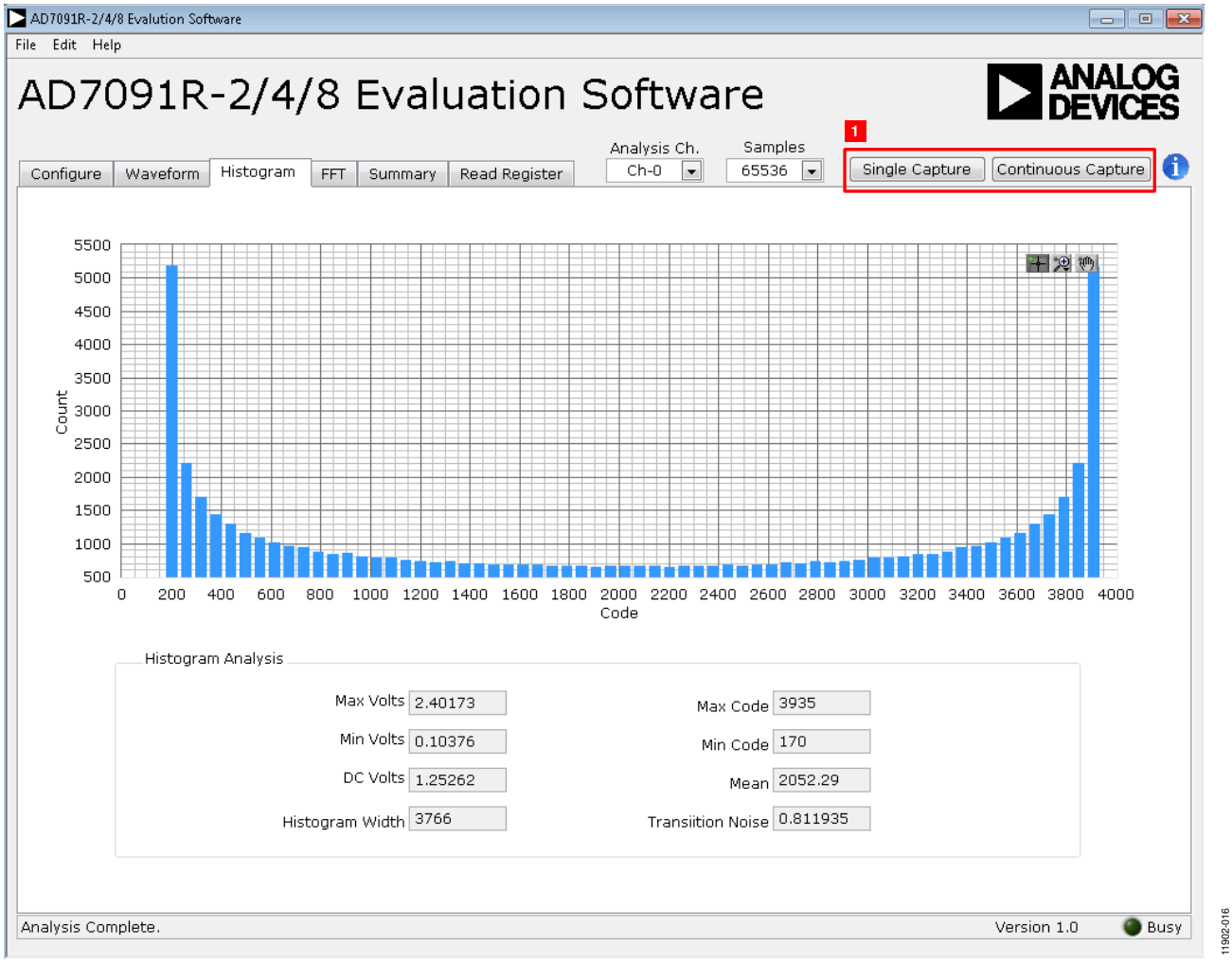

Figure 16. Histogram Capture Tab

AC TESTING—HISTOGRAM

Figure 16 shows the **Histogram** capture tab. This tests the ADC for the code distribution for the ac input and computes the mean and standard deviation, or transition noise of the converter, and displays the results.

Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab in the evaluation software main window and click the **Single Capture** or **Continuous Capture** button (labeled 1 in Figure 16).

Note that an ac histogram requires a quality signal source applied to the input BIPOLAR IN or VINx connectors.

DC TESTING—HISTOGRAM

The histogram is more commonly used for dc testing. Similar to ac testing, this tests the ADC for the code distribution for the dc input and computes the mean and standard deviation, or transition noise of the converter, and displays the results.

Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab in the evaluation software main window and click the **Single Capture** or **Continuous Capture** button (labeled 1 in Figure 16).

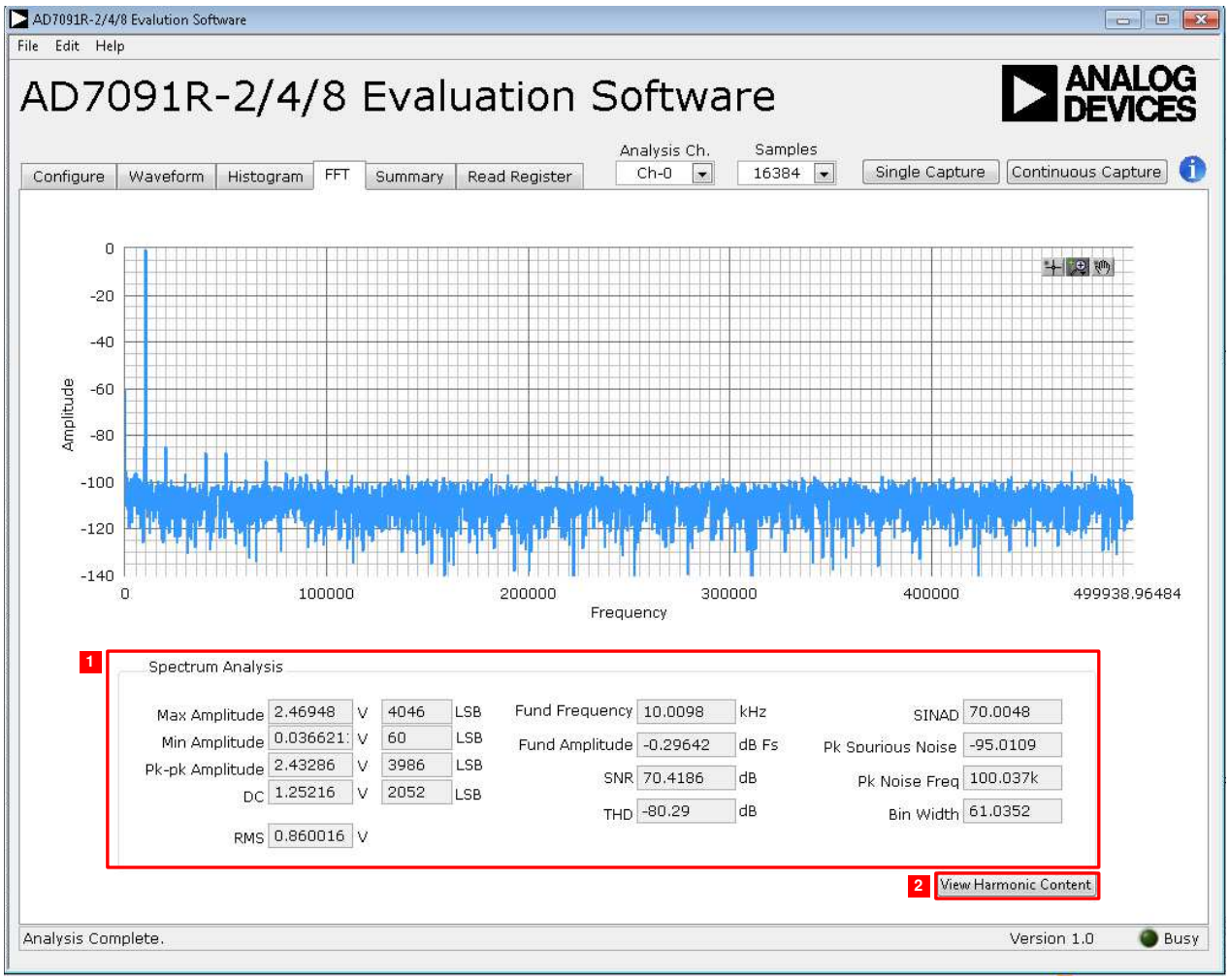

Figure 17. FFT Capture Tab

AC TESTING—FFT CAPTURE

Figure 17 shows the **FFT** capture tab. This tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed, displaying SNR, SINAD, and THD.

To perform an ac test, apply either a bipolar sinusoidal signal to the evaluation board at the BIPOLAR IN input, J10. Then, connect the UNIPOLAR OUT connector, J14, to any input multiplexer channel connector, J5 to J8 or J16 to J19, or apply a unipolar sinusoidal signal directly to any of these channel connectors. Low distortion, better than 115 dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but consideration should be taken in the choice. Furthermore, if using a low frequency band-pass filter when the full-scale input range is more than a few volts peak-to-peak, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Optional on-board anti-alias filtering can be implemented by populating RC filters connected to the noninverting inputs of channel buffers.

Figure 17 displays the spectral analysis results of the captured data.

- The plot is the FFT image of the analysis channel selected.
- The **Spectrum Analysis** panel displays the performance data: **SNR**, **THD**, **SINAD,** dynamic range, and noise performance along with the input signal characteristics. See Label 1 in Figure 17.
- Select **View Harmonic Content** to switch the panel to display the frequency and amplitude of the fundamental in addition to the 2nd to 5th harmonics. See Label 2 in Figure 17.

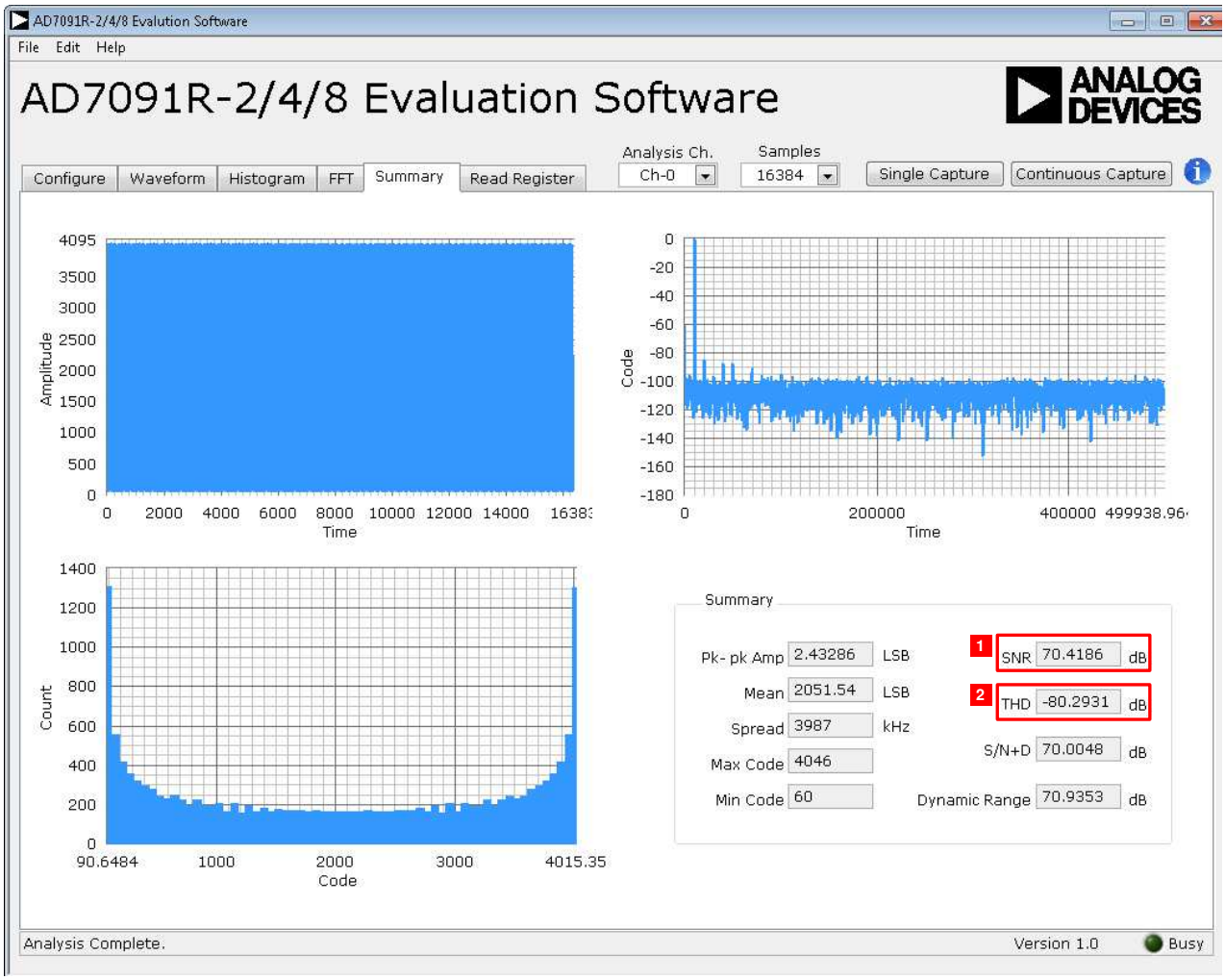

Figure 18. Summary Tab

SUMMARY TAB

Figure 18 shows the **Summary** tab. This tab captures and displays all of the information in one panel with a synopsis of the information, including key performance parameters, such as **SNR** and **THD**, labeled 1 and 2, respectively.

READ REGISTER TAB

All indicators within the **Read Register** tab are automatically updated when this tab is selected. In addition, this tab features a **Refresh Registers** button (labeled 1 in Figure 19) that is useful for monitoring the **Alert Indication** sub-tab while performing data captures and viewing the **Read Register** panel.

The **Read Register** tab as shown in Figure 19 offers the following sub-tabs:

- **Channel Register**
- **Configuration Register**
- **Alert Indication** (labeled 2 in Figure 19)
- **Alert Register**
- **All Registers**

Channel Register. Indicates the current enable/disable state of all channels available on the AD7091R-2/AD7091R-4/AD7091R-8.

Configuration Register. Indicates the configuration state of the AD7091R-2/AD7091R-4/AD7091R-8.

Alert Indication. Indicates the current high and low alert status of individual channels. This allows the user to service an alert that has been triggered.

Alert Registers. Indicates the current high, low, and hysteresis alert register values that are programmed into the AD7091R-2/AD7091R-4/AD7091R-8 control registers.

All Registers. Displays all current register values contained within the AD7091R-2/AD7091R-4/AD7091R-8.

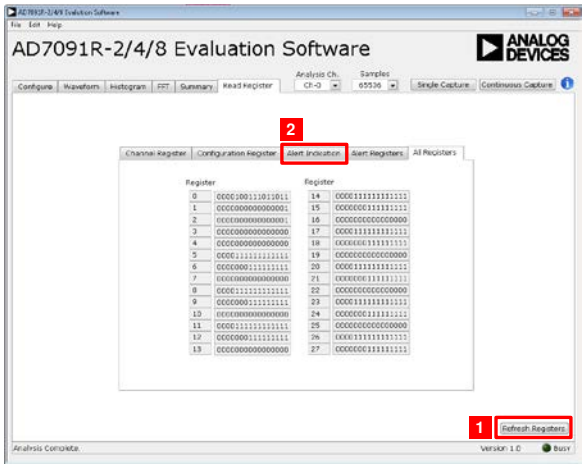

Figure 19. Read Register Tab

SAVING FILES

The software can save the current captured data for future analysis. The software has the ability to capture the current plot images and the current device configuration, as well as the raw waveform data, histogram data, and ac spectrum data.

Saving Data

To save data, go to the **File** menu, click **Save Analysis Data**, and select the desired data type to be saved.

- The **Waveform Data** saves the raw data captured as seen in the **Waveform** tab.
- The **Histogram Data** generates a file that contains two columns, one that contains the codes captured and the other containing the number of time each code was observed in the current capture.
- The **Spectrum Analysis** saves all the information that would be required for the user to recreate the spectral analysis.
- The **Save All Analysis Data** option produces a pop-up box that allows the user to save all of the analysis types to a specific folder location. For the individual saves, the save dialog box in Figure 20 opens. Save to an appropriate folder location. For the save all option, the dialog box in Figure 21 opens.

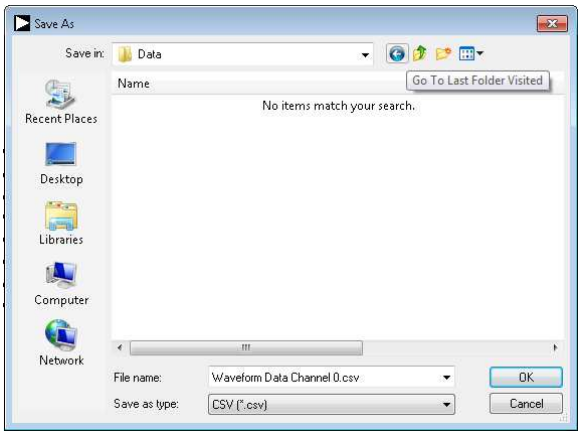

Figure 20. Save File Dialog Box

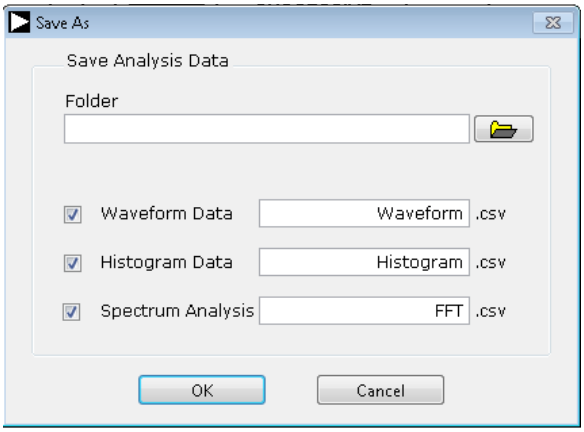

Figure 21. Save All Dialog Box

Saving Plot Images

To save plot images, go to the **File** menu, click **Save Picture** and select the desired plot image to be saved.

The **Waveform** option saves the image from the waveform panel.

The **Histogram** options save the image from the histogram panel.

The **FFT** option saves the image from the FFT panel.

The images are saved in JPEG format and do not contain any raw data information. Saved plots cannot be loaded back into the evaluation environment. To save images, the **Save As** dialog box in Figure 22 opens. Save the images to an appropriate location.

Saving Device Configurations

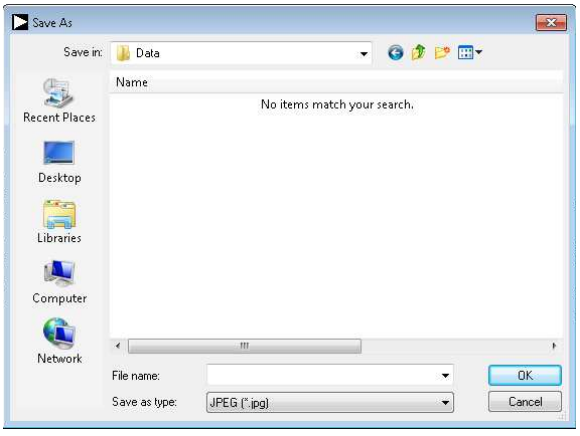

Figure 22. Save Image Dialog Box

To save the current device configuration in XML format, go to the **File** menu and click **Save Register Configuration**.

To save the current device configuration, the **Save As** dialog box in Figure 23 opens. Save to an appropriate location.

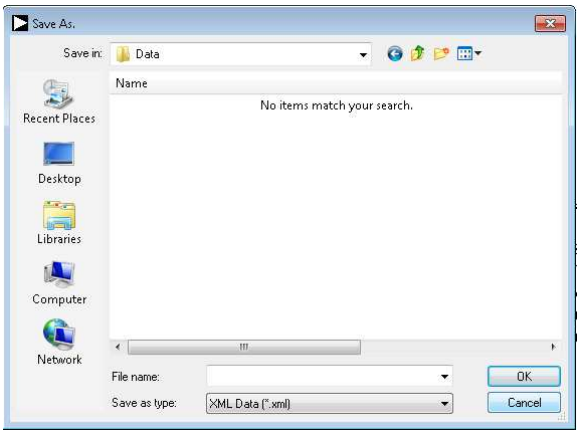

Figure 23. Save Register Configuration Dialog Box

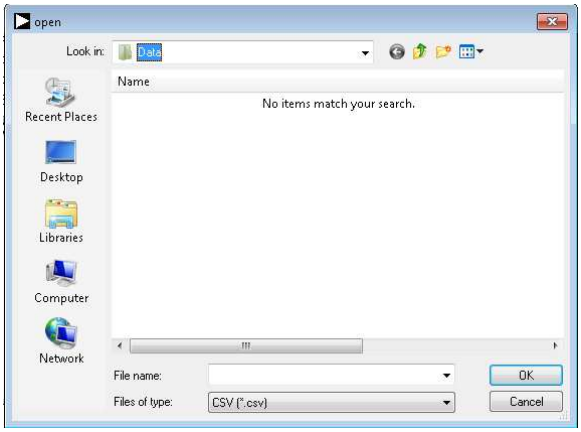

Figure 24. Open File Dialog Box

OPENING FILES

Loading Captured Data

The software can load previously captured data for analysis.

Go to the **File** menu, click **Open**, and select **Waveform Data**. Only the previously captured waveform data can be opened, not a histogram or spectral analysis file. The waveform data is a raw data capture that rebuilds the histogram and ac spectrum analyses upon being loaded into the evaluation platform.

When **Waveform Data** is selected, the **Open** file dialog box in Figure 24 opens for loading an appropriate file. The evaluation software expects that a previously generated waveform file is in .CSV format.

Loading Device Configurations

The software can load a previously utilized device configuration.

Go to the **File** menu, click **Open**, and select **Register Configuration**. The software loads all previously used device settings to the ADC and updates the evaluation platform appropriately. When **Register Configuration** is selected, the **Open** file dialog box in Figure 25 opens. Load an appropriate .XML file.

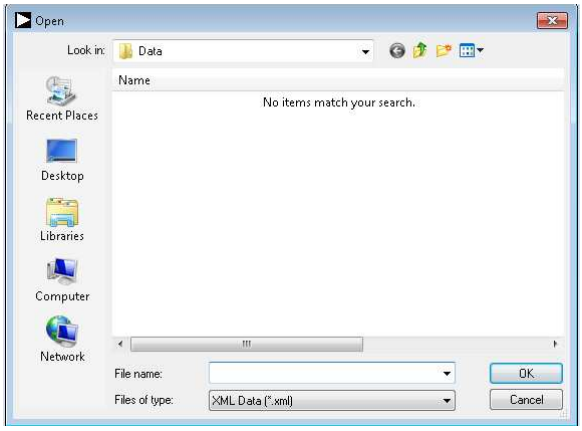

Figure 25. Open Configuration Dialog Box

EVALUATION BOARD SCHEMATICS AND ARTWORK

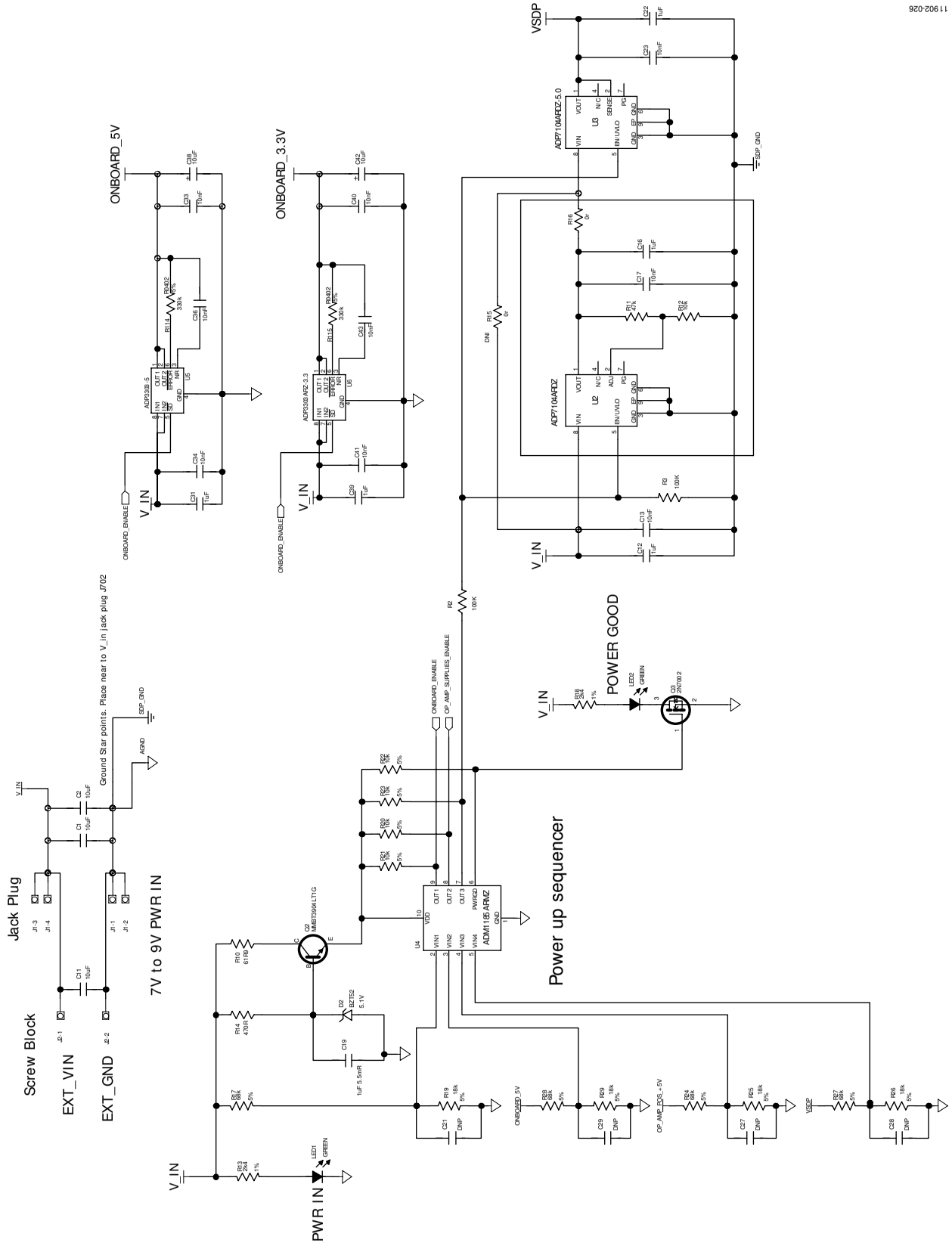

Figure 26. Schematic Page 1

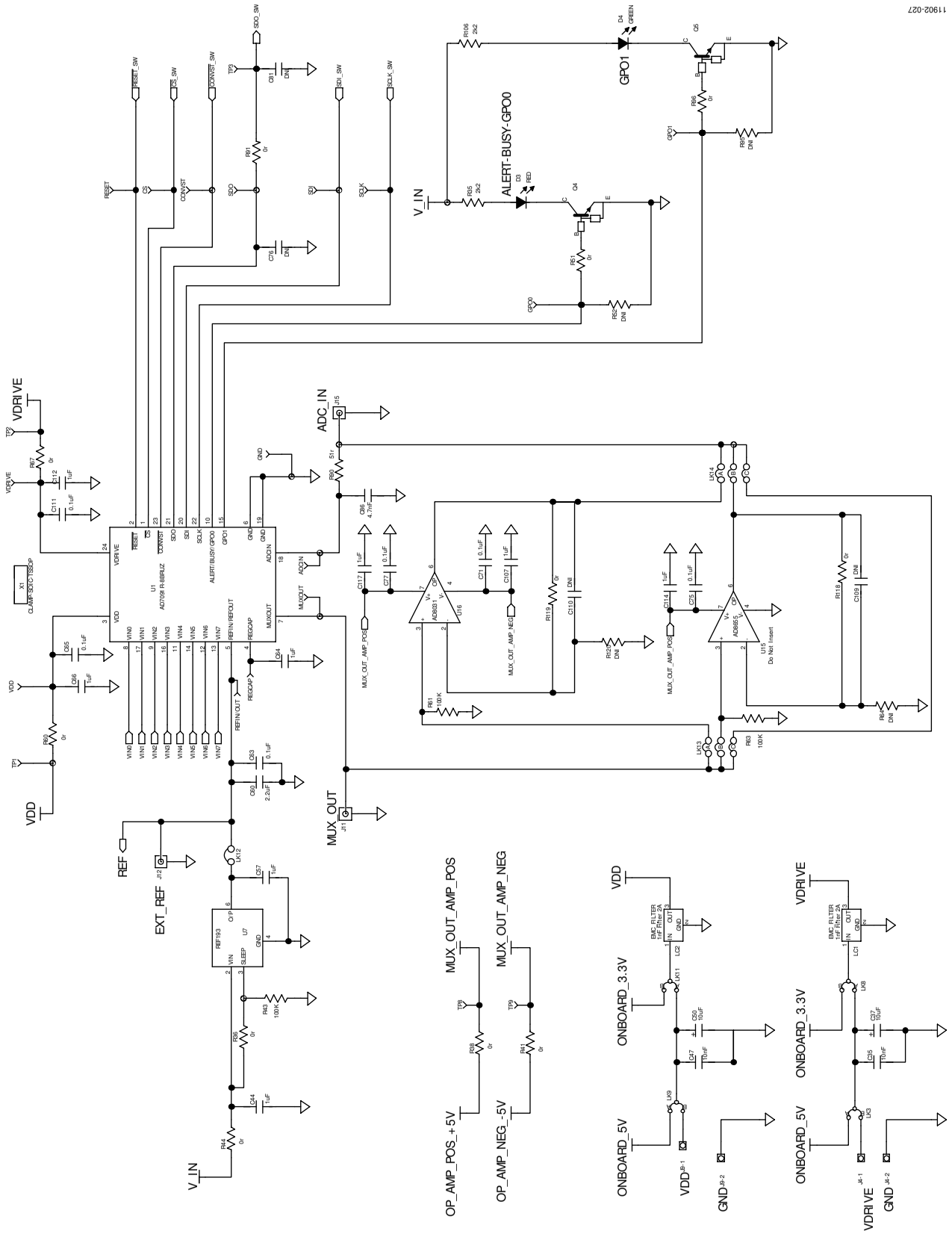

Figure 27. Schematic Page 2

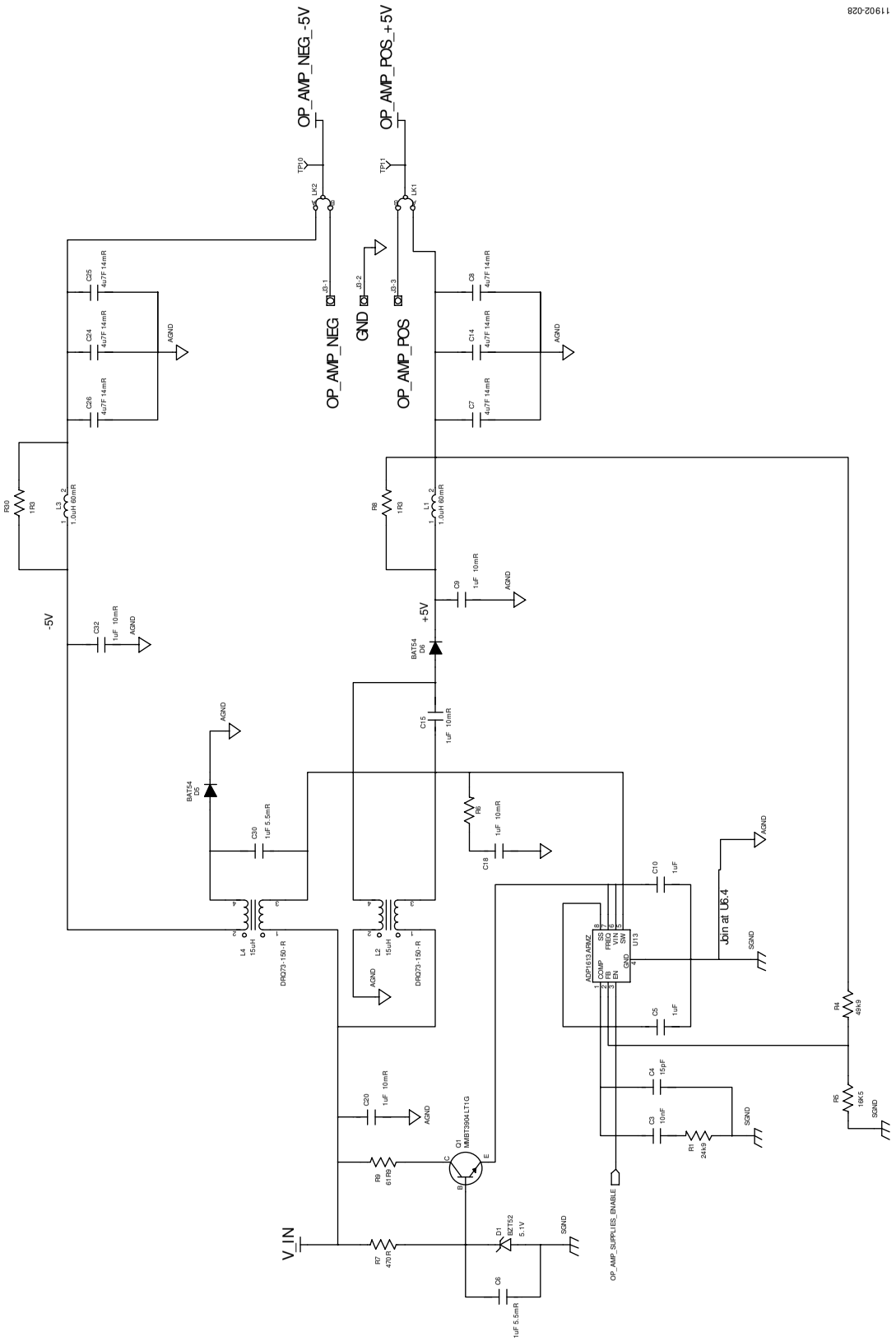

Figure 28. Schematic Page 3

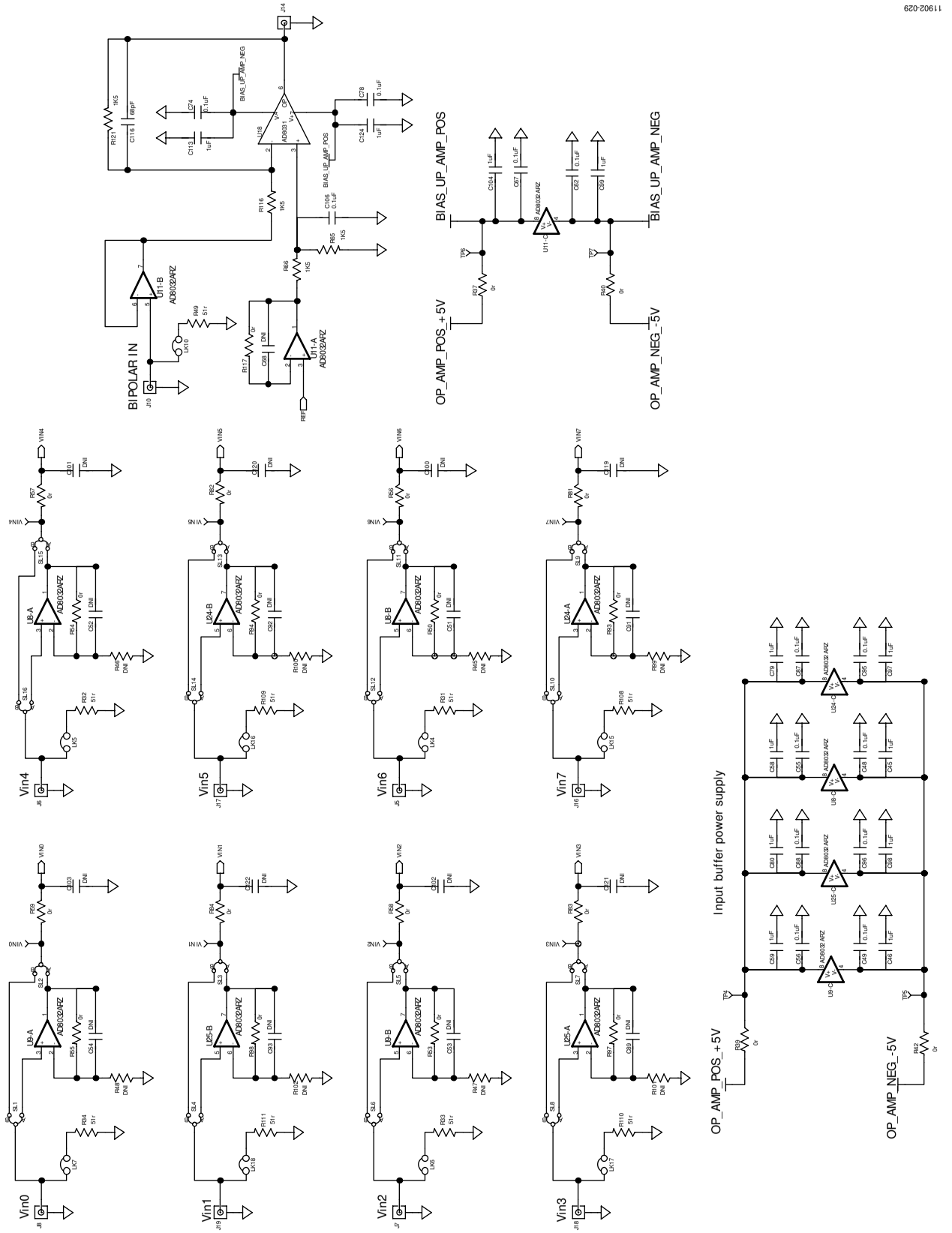

Figure 29. Schematic Page 4

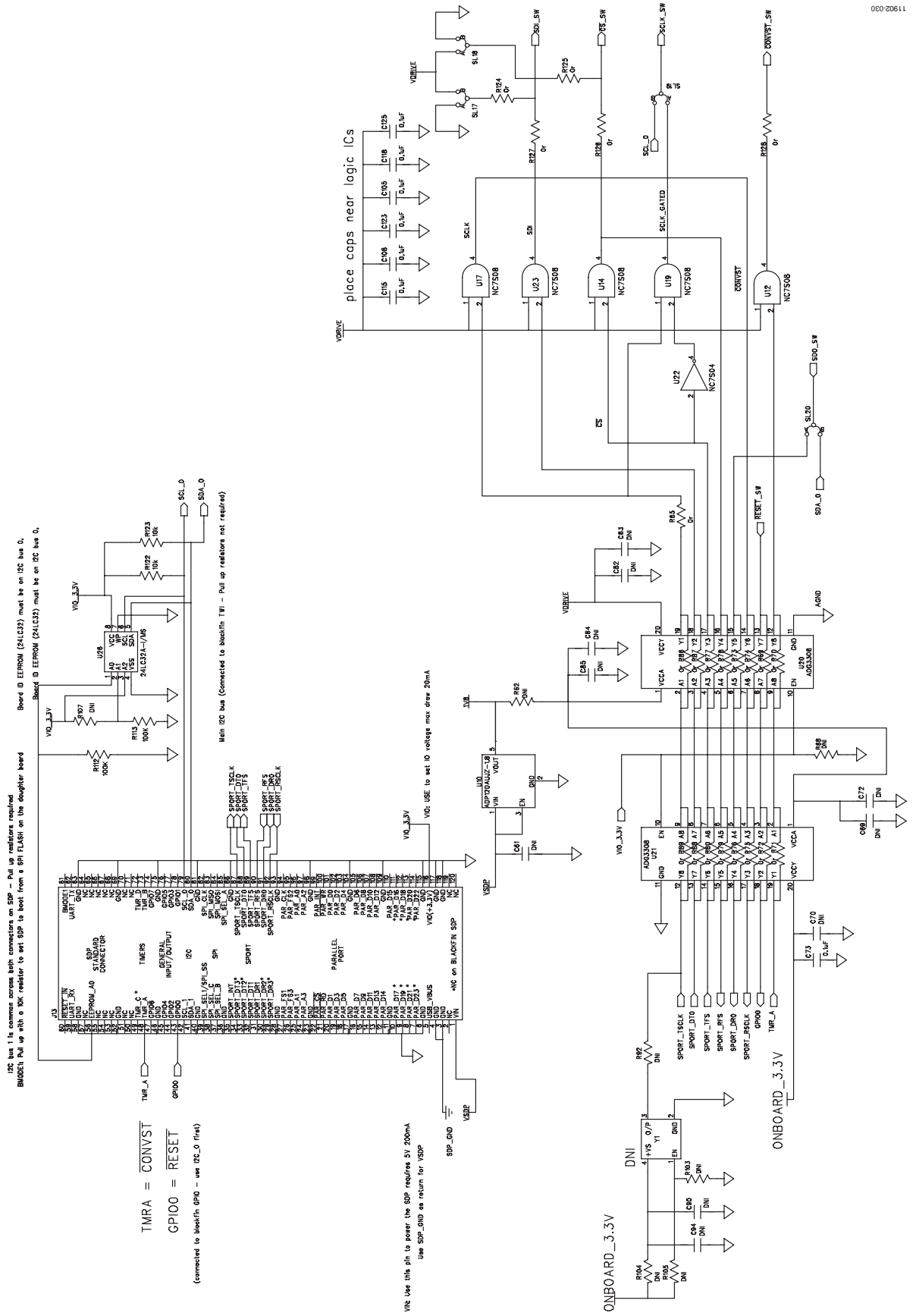

Figure 30. Schematic Page 5