Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 •
www.analog.com

Evaluation Board for the AD7124-8—
8-Channel, Low Noise, Low Power, 24-bit S-D ADC with In- Amp and Reference

FEATURES

Full featured evaluation board for the AD7124-8
PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time domain)
Standalone capability

ONLINE RESOURCES

Evaluation Kit Contents
EVAL-AD7124-8SDZ evaluation board
Evaluation software CD for the AD7124-8
Documents Needed
AD7124-8 data sheet
AD7124-8 user guide
Required Software
EVAL-AD7124-8SDZ evaluation software

EQUIPMENT NEEDED

EVAL-AD7124-8SDZ evaluation board
EVAL-SDP-CB1Z system demonstration platform
DC signal source
USB cable
PC running Windows with USB 2.0 port

GENERAL DESCRIPTION

The EVAL-AD7124-8SDZ evaluation kit features the AD7124-8 24-bit, low power, low noise analog-to-digital converter (ADC).

A 7 V to 9 V external supply is regulated to 3.3 V to supply the AD7124-8 and support all necessary components. The EVAL-AD7124-8SDZ board connects to the USB port of the PC by connection to the EVAL-SDP-CB1Z motherboard.

The EVAL-AD7124-8SDZ software fully configures the AD7124-8 device register functionality and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EVAL-AD7124-8SDZ is an evaluation board that is designed to allow the user to evaluate the features of the ADC. The user PC software executable controls the AD7124-8 over the USB through the system demonstration platform board (EVAL-SDP-CB1Z).

FUNCTIONAL BLOCK DIAGRAM

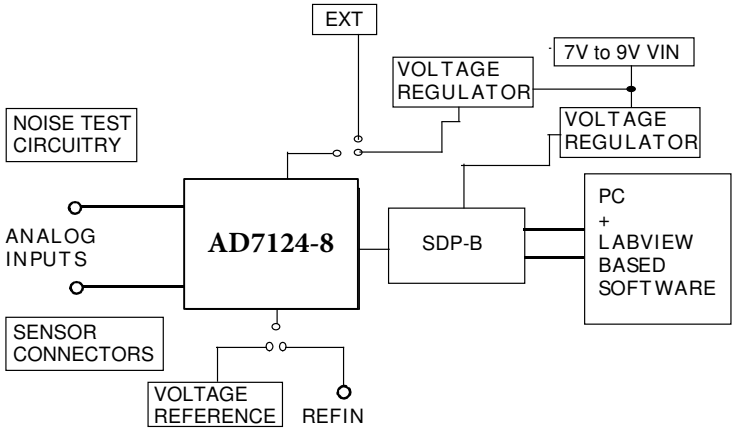

Figure 1. EVAL-AD7124-8SDZ Block Diagram

TABLE OF CONTENTS

REVISION HISTORY

1/15—Revision PrA: Initial Version

EVAL-AD7124-8SDZ QUICK START GUIDE

To begin using the evaluation board, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7124-8 evaluation board software from the CD included in the evaluation board kit. The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7124-8SDZ board.
    a. Screw the two boards together using the plastic screw-washer set included in the evaluation board kit to ensure that the boards are connected firmly together.
3. Apply an external voltage in the range of 7 V to 9 V to the J3 or J5 connecter of the EVAL-AD7124-8SDZ board. This provides the power supply for the board.
4. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. If you are using Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.
5. Launch the EVAL-AD7124-8SDZ software from the **Analog Devices** subfolder in the **Programs** menu.

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7124-8 is a low power, low noise, complete analog front end for high precision measurement applications. It contains a low noise, 24-bit Σ-Δ ADC. It can be configured to have four differential inputs or seven single-ended or pseudo-differential inputs. The on-chip low noise instrumentation amplifier means that signals of small amplitude can be interfaced directly to the ADC. Other on-chip features include a low drift 2.5 V reference, excitation currents, reference buffers, multiple filter options and many diagnostic features.

Complete specifications for the AD7124-8 are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details about the EVAL-SDP-CB1Z are available on the Analog Devices, Inc., website.

HARDWARE LINK OPTIONS

The default link options are listed in Table 1. By default, the board is configured to operate from a wall wart (dc plug) power supply via Connector J5. The supply required for the AD7124-8 comes from the on-board ADP1720 LDOs, which generate their input voltage from J5.

Table 1. Default Link and Solder Link Options

Link No.	Default Option	Description
LK1	A	Connects the AVDD voltage to the power supply sequencer, ADM1185. When AVDD equals 3.3 V, LK1 must be in Position A. When AVDD equals 1.8 V, LK1 must be in Position B.
LK2	B	Selects the connector for the external 7 V to 9 V power supply. In Position A, this link selects the external 7 V to 9 V power supply to come from Connector J3. In Position B, this link selects the external 7 V to 9 V power supply to come from Connector J5.
LK3	Inserted	Inserting this link connects REFIN(-) to AVSS.
LK4	2.5 V	Selects the reference source for the ADC. In position 2.5V, REFIN1(+) is connected to the external 2.5 V reference (ADR4525). In position INT REF, REFIN1(+) is connected to the REFOUT pin of the AD7124-8. The AD7124-8's internal reference can be enabled and applied to the AD7124-8 external to the ADC.
LK5	Inserted	This link shorts AIN0 to AIN1. This is useful to perform noise tests on the AD7124-8. The internal bias can be enabled on AIN0 or AIN1 so that AIN0 and AIN1 are at an appropriate voltage for the noise test.
LK6	Inserted	Headers J13 and J14 can be used to connect channels AIN4 and AIN5 to external components such as an external amplifier. Both links at LK6 should be opened to include the external component on the front-end.
SL2	A	Sets the voltage applied to the AVDD pin. In Position A, this link sets the voltage applied to the AVDD pin to be a 3.3 V supply from the ADP1720-3.3 (U7) regulator or a 2.5 V supply from the ADP1720 (U4) regulator. In Position B, this link sets the voltage applied to the AVDD pin to be supplied from an external voltage source via Connector J9.
SL3, SL7	A, A	With SL3 and SL7 in Position A, AVDD is supplied with 3.3 V from ADP1720-3.3 (U7) regulator. With SL3 and SL7 in Position B, AVDD is supplied with 1.8 V from the ADP1720 (U4) regulator.
SL5	B	With this link in Position A, the IOVDD supply is provided from an external source via Connector J9. With this link in Position B, the 3.3 V supply is generated by the ADP1720-3.3 (U10) regulator. The evaluation system operates with 3.3 V logic.
AVSS to AGND	R49, R50, R51, R52	When these links are inserted, AVSS is tied to AGND. When AVSS is set to −1.8 V, these links must be removed.

On-Board Connectors

Table 2 provides information about the external connectors on the EVAL-AD7124-8SDZ.

Table 2. On-Board Connectors

Connector	Function
J1	A 120-pin connector that mates with the EVAL-SDP-CB1Z (black colored controller board).
J2	Straight PCB Mount SMB/SMA Jack for master clock (not inserted). The EVAL-AD7124-8SDZ has the footprint to include an SMA/SMB connector, if an external clock source is being used to provide the master clock to the ADC.
J3	Bench top power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.
J5	Wall wart (dc plug) power supply voltage input. Apply 7 V to 9 V and GND (0 V) to this connector to power the evaluation board.
J6	Analog input connector. Connections to AIN0 to AIN5 are available along with REFIN1(±) connections. This connector can be used to connect an RTD to the AD7124-8.
J9	Optional external connector, allowing external bench top or alternative supply for AVDD and IOVDD. When split supplies are used, AVSS is supplied externally via J9.
J11	Analog input connector. Connections to AIN6 to AIN7 are available along with REFIN1(±) and analog power supply connections. This connector can be used to connect a loadcell to the AD7124-8.
J12	6-pin connector. Provides an I2C interface to allow the SDP to interface to a digital temperature sensor. This is required if a thermocouple is interfaced to the AD7124-8 using connector A2.
J13	7-pin connector which can be used to connect an external amplifier to channel AIN4/AIN5.
J14	7-pin connector which allows connection to pins AIN4 and AIN5.
A0	Straight PCB Mount SMB/SMA Jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to analog input AIN4.
A1	Straight PCB Mount SMB/SMA Jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal to analog input AIN5.
A2	Thermocouple connector. This connector is required useful if a thermocouple is being interfaced to the evaluation board.
A5	Straight PCB Mount SMB/SMA Jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal REFIN1(+).
A6	Straight PCB Mount SMB/SMA Jack. The footprint for an SMA/SMB connector is included on the evaluation board to provide the signal REFIN1(-).

POWER SUPPLIES

The evaluation board requires that an external power supply—either a bench top supply or a wall wart (dc plug) supply—be applied to J3 or J5 (see Table 3 for more information). Linear regulators generate the required power supply levels from the applied V_{IN} rail. The regulators used are the ADP1720-3.3 (U7) and the ADP1720 (U4), which supply 3.3 V and 1.8 V, respectively, to AVDD of the ADC. The 3.3 V ADP1720 (U10) delivers 3.3 V to the IOVDD pin of the AD7124.4.

When a split power supply is used, the AVSS voltage must be applied from an external source via Connector J9. AVDD and IOVDD can also be provided via Connector J9. However, the 7 V to 9 V supply is still required because the on-board reference (ADR4525) is supplied from this power supply.

Each supply is decoupled at the point where it enters the board and again at the point where it connects to each device (see the schematics shown in **Error! Reference source not found.** to **Error! Reference source not found.** to identify decoupling points).

SERIAL INTERFACE

The AD7124-8 evaluation board connects via the SPI to the Blackfin® ADSP-BF527 on the EVAL-SDP-CB1Z. There are four primary signals: CS, SCLK, DIN, and DOUT/$\overline{\text{RDY}}$ (all are inputs, except for DOUT/$\overline{\text{RDY}}$, which is an output.)

If you wish to operate the EVAL-AD7124-8SDZ in standalone mode, the AD7124-8 serial interface lines can be disconnected from the 120-pin header by removing the 0 Ω links, R9 through R13. The test points can then be used to fly-wire the signals to an alternative digital capture setup.

ANALOG INPUTS

The EVAL-AD7124-8SDZ primary analog inputs can be applied in two ways:

- Using J6 and J11, the green screw in terminal connectors
- Using the A0 and A1 SMB/SMA footprints on the evaluation board which connect to analog inputs AIN4and AIN5.

The EVAL-AD7124-8SDZ software is set up to analyze dc inputs to the ADC.

Table 3. Required External Power Supply[1]

Power Supply (V_{IN}) Applied To	Voltage Range	Function
J3	7 V to 9 V	Bench top supply to the evaluation board. Supplies LDOs that create 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Ensure that LK2 is set to Position A when the external power supply is applied to this connector.
J5	7 V to 9 V	Wall wart (dc plug) supply to the evaluation board. Supplies LDOs that create 3.3 V and 1.8 V rails. It also supplies the ADR4525 external reference. Ensure that LK2 is set to Position B when the external power supply is applied to this connector.

[1] Only a single supply is required, either J3 or J5. This can be selected using LK2.

REFERENCE OPTIONS

The EVAL-AD7124-8SDZ includes an external 2.5 V reference (the ADR4525) and an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 2.5 V ADR4525 on the evaluation board.

The reference used for a conversion is selected by choosing the reference in the Configx registers associated with Setup 0 to Setup 15.

Switch between using the internal reference and external reference by accessing the AD7124-8 register map via the evaluation software. Figure 2 shows how to select the reference source for Setup 0 to Setup 15. Figure 3 shows the ADC_Control register setting that enables the internal reference.

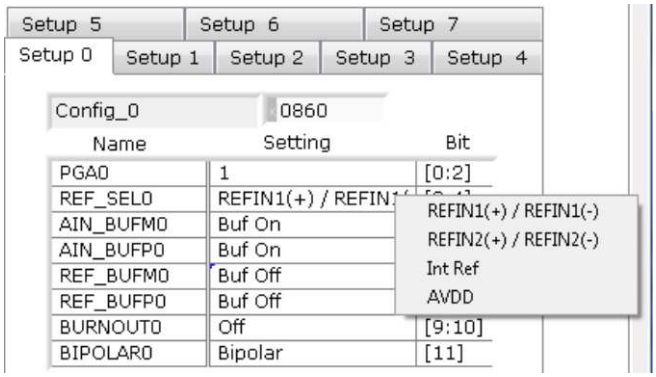

Figure 2. Selecting the Reference Source

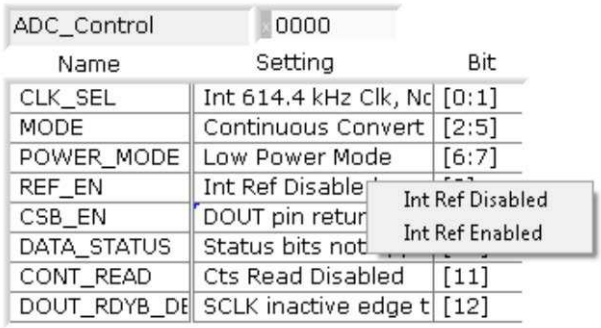

Figure 3. Turning On the Internal 2.5 V Reference

EVALUATION BOARD SETUP PROCEDURES

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-SDP-CB1Z board to Connector A or Connector B on the EVAL-AD7176-2SDZ board. Screw the two boards together using the plastic screw-washer set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect the power supplies to the EVAL-AD7124-8SDZ board. The EVAL-AD7124-8SDZ board, by default, uses the wall wart (dc plug) supply that accompanies the evaluation kit. Connect this supply to J5 on the EVAL-AD7124-8SDZ board. (For more information about the required connections and available options, refer to the Power Supplies section.)
3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7124-8SDZ evaluation kit includes a CD containing software to be installed on your PC before you begin using the evaluation board.

There are two parts to the installation:

- AD7124-8 evaluation board software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the AD7124-8 Evaluation Board Software

To install the AD7124-8 evaluation board software,

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7124-8**.
3. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.

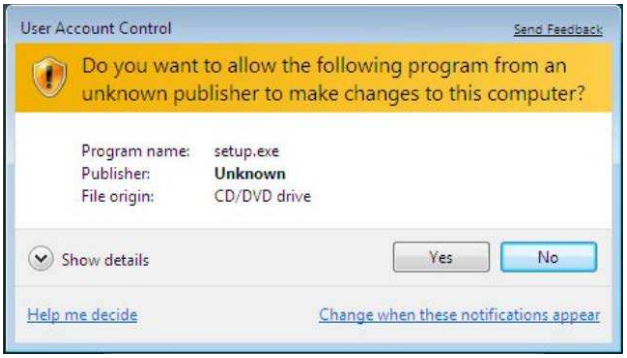

Figure 4. AD7124-8 Evaluation Software Installation: Granting Permission for the Program to Make Changes to Your Computer

4. Select the location to install the software, and then click **Next**. (Figure 5 shows the default locations, which are displayed when the window opens, but you can select another location by clicking **Browse**.)

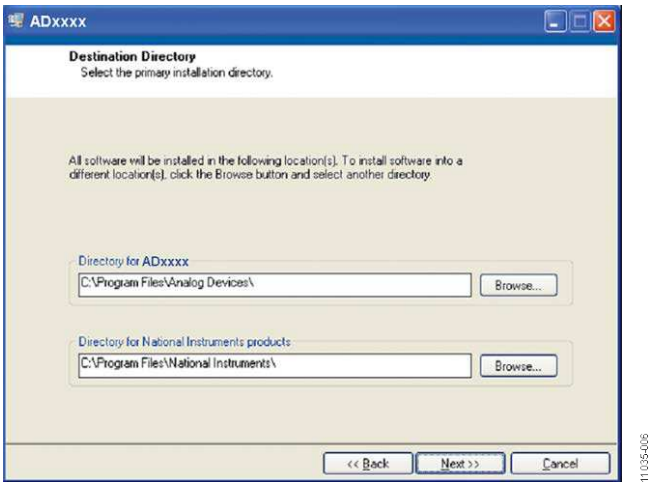

Figure 5. AD7124-8 Evaluation Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next**.

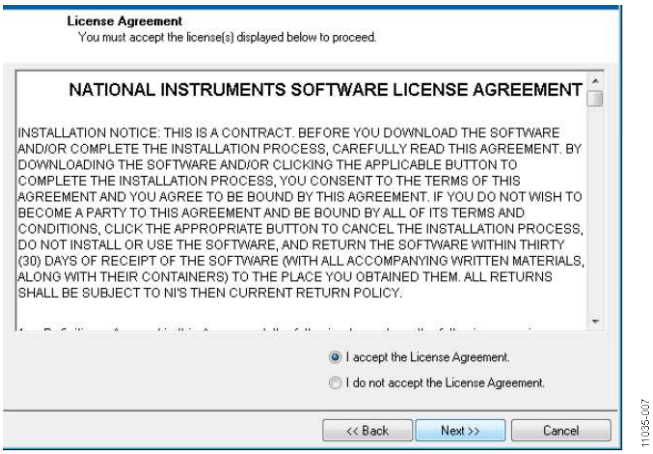

Figure 6. AD7124-8 Evaluation Software Installation: Accepting the License Agreement

6. A summary of the installation is displayed. Click **Next** to continue.

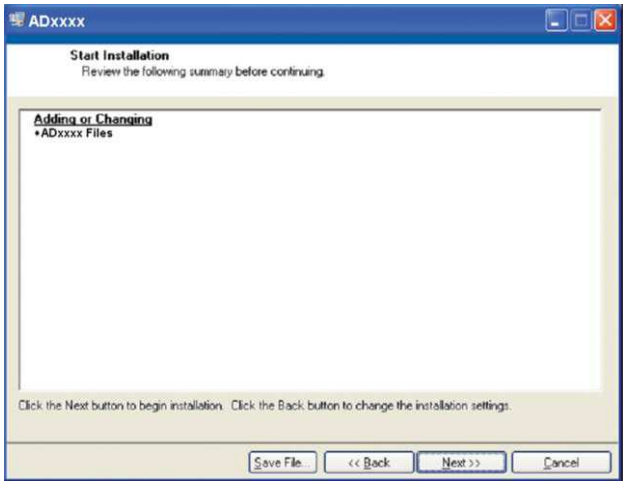

Figure 7. AD7124-8 Evaluation Software Installation: Reviewing a Summary of the Installation

7. A dialog box informs you when the installation is complete. Click **Next**.

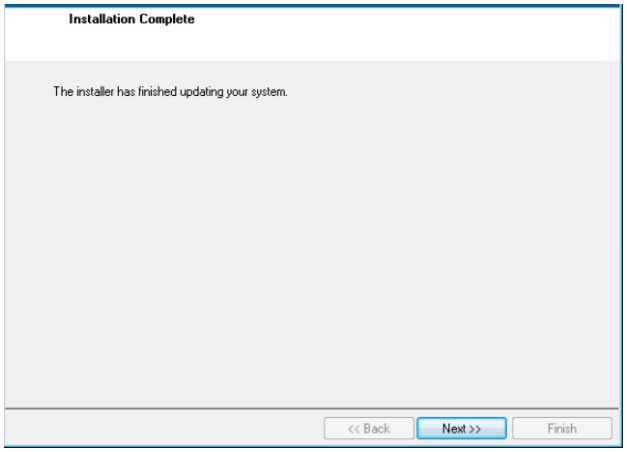

Figure 8. AD7124-8 Evaluation Software Installation: Indicating When the Installation Is Complete

Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers

After the installation of the evaluation software is complete, a welcome window is displayed for the installation of the EVAL-SDP-CB1Z system demonstration platform board drivers.

1. With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.

Figure 9. EVAL-SDP-CB1Z Drivers Setup: Beginning the Drivers Installation

2. Select the location to install the drivers, and then click **Next**.

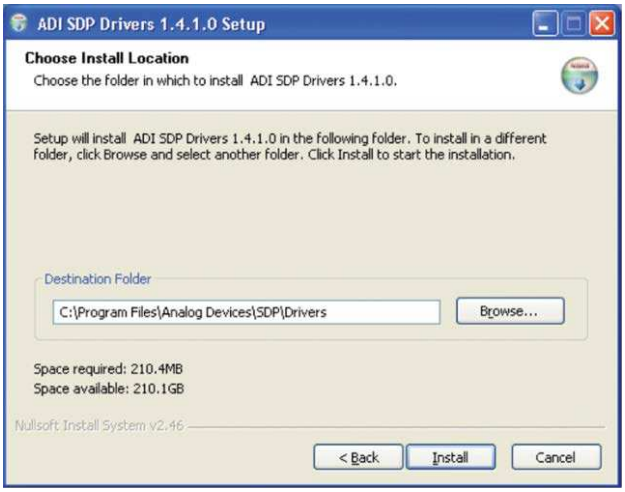

Figure 10. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

3. Click **Install** to confirm that you would like to install the drivers.

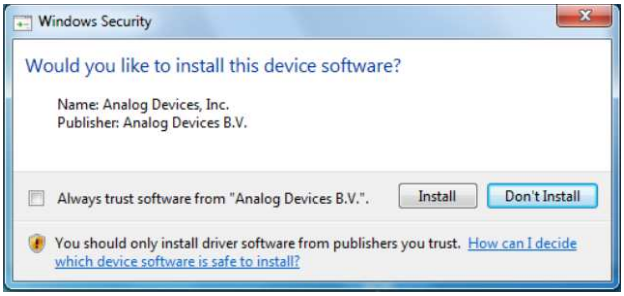

Figure 11. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers

4. To complete the drivers installation, click **Finish**, which closes the installation wizard.

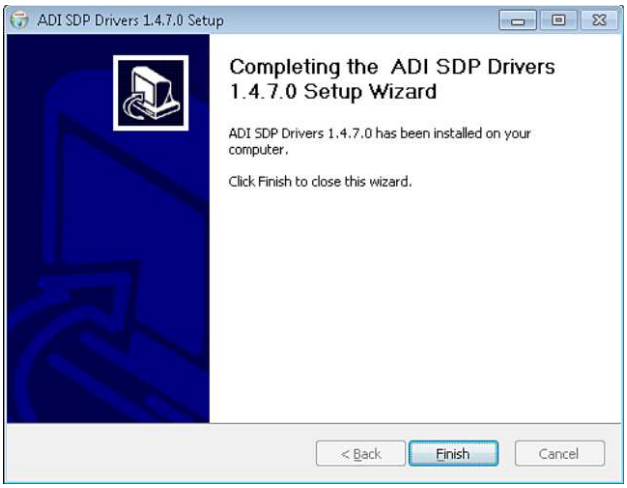

Figure 12. EVAL-SDP-CB1Z Drivers Setup: Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart the computer.

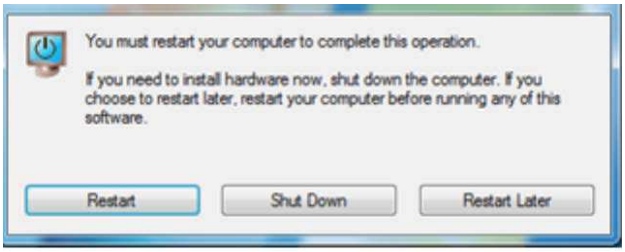

Figure 13. EVAL-SDP-CB1Z Drivers Setup: Restarting the Computer

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Hardware sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the EVAL-SDP-CB1Z board is plugged into your PC. (If you are using Windows XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
2. Check that the board is connecting to the PC correctly using the **Device Manager** of the PC.
   a. Access the **Device Manager** as follows:
      i. Right-click **My Computer** and then click **Manage**.
      ii. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.
      iii. The **Computer Management** box appears. Click **Device Manager** from the list of **System Tools** (see Figure 14).
   b. The EVAL-SDP-CB1Z board should appear under **ADI Development Tools**. This indicates that the driver software is installed and that the board is connecting to the PC correctly.

Figure 14. Device Manager: Checking That the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7124-8 software as follows:

1. From the **Start** menu, select **Programs** > **Analog Devices** > **AD7124-8** > **AD7124-8 Evaluation Board Software**. The main window of the software then displays.
2. If the AD7124-8 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 15). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and then follow the on-screen instructions.

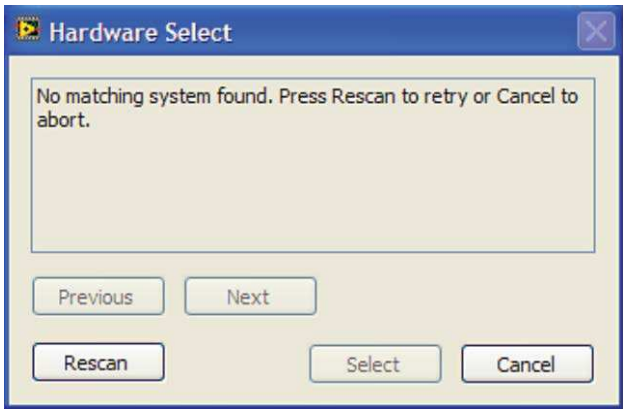

Figure 15. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the generic SDP attached to the PC is detected, and then the main window appears (see Figure 16).

SOFTWARE OPERATION

Overview of the Main Window

The main window of the software (see Figure 16) contains three tabs: Configure, Waveform and Histogram. Above the tabs, there are buttons that are used in all three tabs.

The **Configure** tab allows the user to setup the ADC, reset the ADC and read the diagnostics.

The **Waveform** tab graphs the conversions gathered and processes the data, calculating the p-p noise, rms noise and resolution.

The **Histogram** tab generates a histogram using the gathered samples and processes the data, calculating the p-p noise, rms noise and resolution.

Start Sampling Button

Clicking **Start Sampling**, located near the top right hand corner of the main window (see Figure 16), starts ADC sampling; results are reported in the graphs of the **Waveform** and **Histogram** sections. The software captures a specified number of samples, the sample size being set via the **Samples** box. The software can also continuously convert if the **Capture Defined Sample Set** is set to **Continuous.**

Delete Data/Clear Graphs

Clicking **Delete Data/Clear Graphs** clears the waveform graph and histogram and clears any conversion data gathered.

File

This allows you to write the current set of data to a file for later use, log data as it is gathered, and exit the program.

Help

This details the revision of the software.

Exiting the Software

To exit the software, click the red X at the top right hand corner of the main window. The software can also be exited using **File**.

Configure

ADC Setup Button

Clicking **ADC Setup** opens the **AD7124-8 Register Interface** window.

ADC Reset Button

Clicking **ADC Reset** resets the AD7124-8 so the registers are at their default (power-on reset) values.

Check Diagnostics Button

Clicking **Check Diagnostics** displays the current settings of the error bits in the Error register.

External Reference

This box displays the value of the external reference. It defaults to 2.5V since the AD4525 is a 2.5V reference. If a reference of a different value is used, update this box so that the software can correctly calculate the noise and resolution.

CRC Error Indicator

When the CRC is enabled, the software generates the CRC word for every write operation and checks the CRC value returned with any conversions or register values read. If a CRC error is detected in the communications between the software and the AD7124-8, the CRC Error LED becomes visible at the bottom of the window and is lit. The CRC functionality on the AD7124-8 is disabled by default.

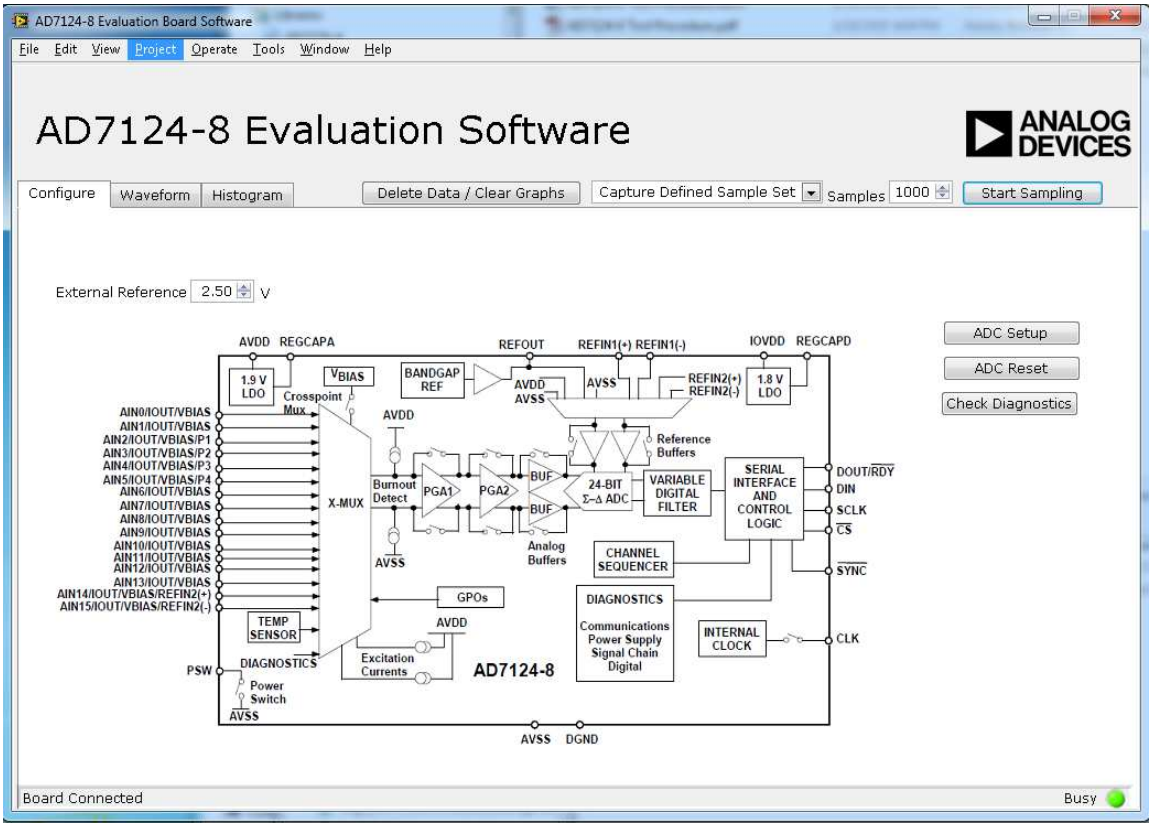

Figure 16. Main Window

Noise Test—Quick Start Demonstration

To perform a noise test using the AD7124-8 evaluation board, LK5 should be inserted so that AIN0 and AIN1 are connected together.

1. Click **ADC Setup** to open the **AD7124-8 Register Interface** window. The AD7124-8 should be configured as follows:
   a. In the ADC_Control register, select the full power mode.
   b. Provide a bias voltage to the analog input by enabling the VBIAS0 in the IO_Control_2 register.
   c. In the Channel 0 register, AIN0 is connected to the positive input, AIN1 is connected to the negative input of the ADC for this channel, and Setup 0 is selected. Therefore, the AIN0 to AIN1 conversion is mapped using the Setup 0 configuration.
   d. Setup 0 is configured with the following register settings:
      i. In the Config_0 register, the external reference is selected as the reference source for the ADC conversion.
      ii. In the Filter_0 register, FS0 is set to 2047 and the sinc4 filter is selected. This sets the output data rate to 9.38 sps.
      iii. In the Offset_0 register, the default offset register value is selected.
      iv. In the Gain_0 register, the factory trimmed gain error value is selected.
2. Figure 17 shows the contents of the **AD7124-8 Register Interface** and the state of the AD7124-8 registers. Click **OK** to return to the main window. Figure 18 shows an example of the main window after running a noise test.
3. Set the number of samples to be collected in each batch in the **Samples** box, which is located just to the left of **Start Sampling**, near the top right hand corner of the main window.
4. Click **Start Sampling** to acquire samples from the ADC.

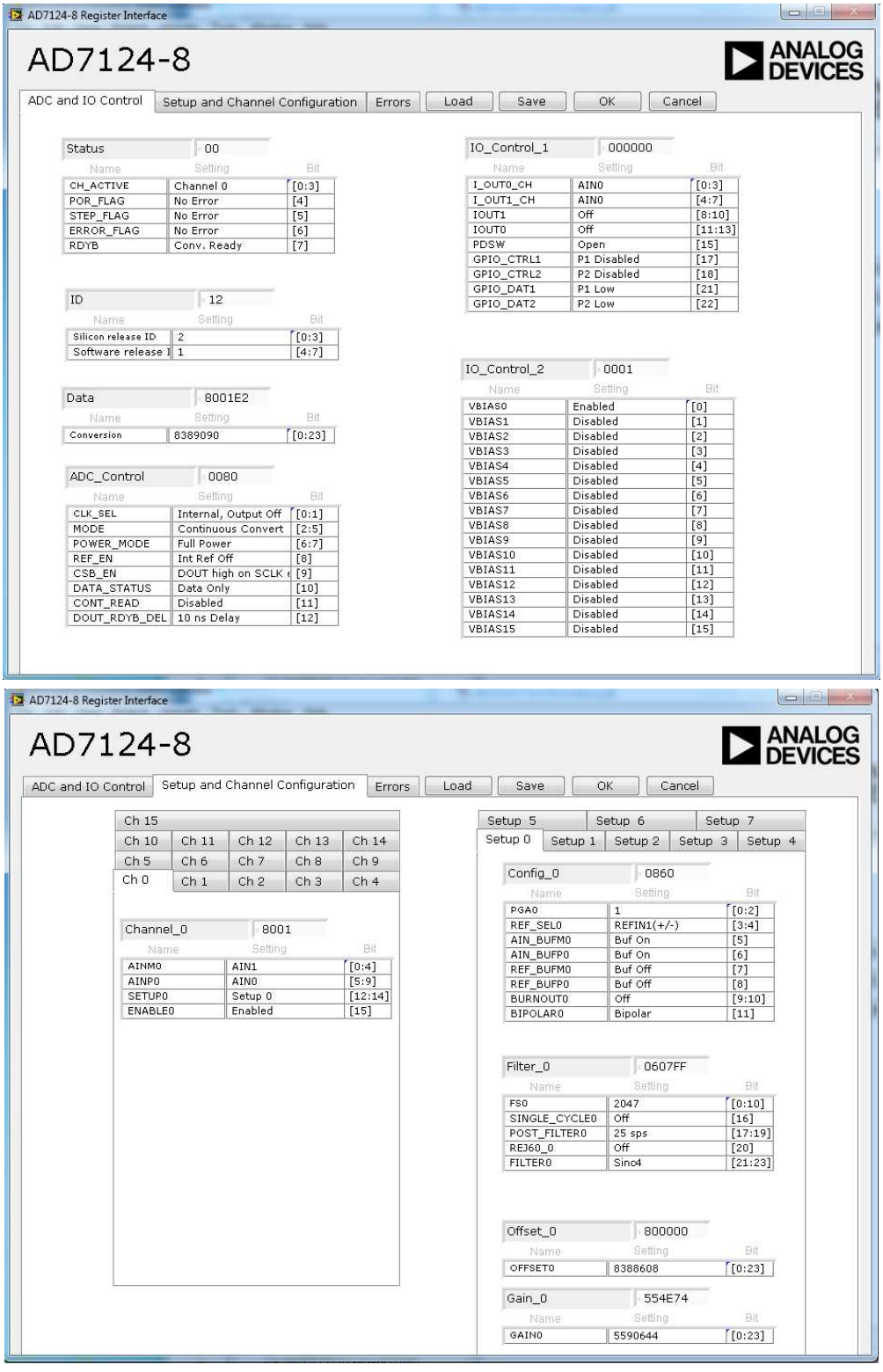

Figure 17. Configuration for Noise Test

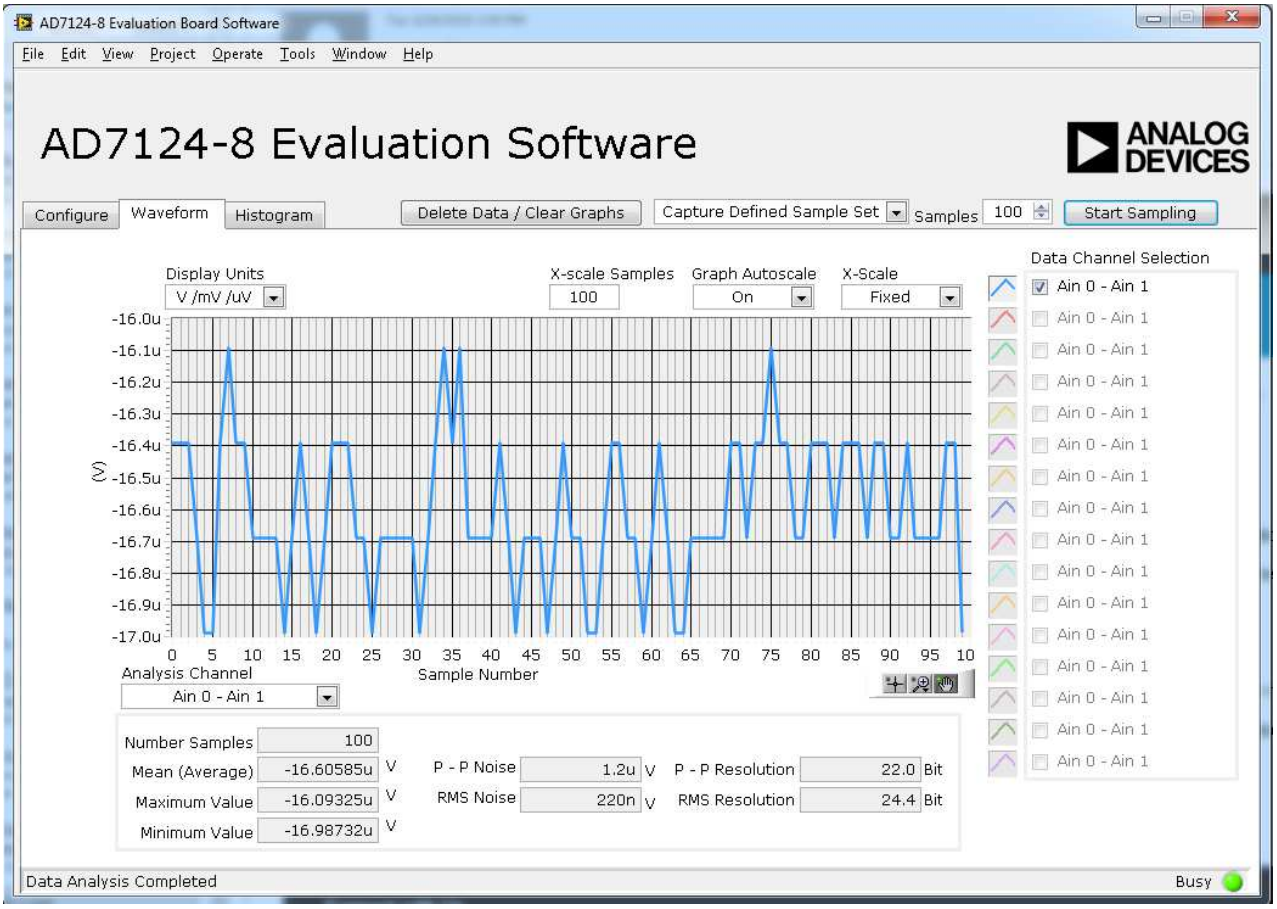

Figure 18. Example of the Main Window After Running a Noise Test

Reading Samples from the ADC

The evaluation board is set up to use the external 2.5 V on-board reference (ADR4525). To read samples from the ADC,

1. The value in the **Vref** box is set to 2.5 V by default to use the external 2.5 V on-board reference (ADR4525). If a different reference is used, such as the 2.5 V internal reference, set the value in the **Vref** box accordingly. (The analysis results are based on the value set in this box.)
2. Select the number of samples to analyze in the **Samples** box. (Note that when performing a continuous capture, this number is limited to 65,536 samples.)
3. When **Sampling** is set to **Capture**, a batch of samples is read when **Start Sampling** is clicked, with the batch size being set by the value in the **Samples** box. When **Sampling** is set to **Continuous**, the software performs a continuous capture from the ADC when **Start Sampling** is clicked.
4. Click **Stop** to stop streaming data.
5. Use the navigation tools within each graph to control the cursor, zooming, and panning.
6. If desired, save the current captured data for later analysis (see the **WaveformError! Reference source not found.** and the **Histogram** section).

Waveform

The waveforms resulting from the gathered samples are shown in the tab. The waveform graph shows each successive sample of the ADC output (input referred). The indicators beside this graph show the channels being converted. Navigation tools are provided to allow you to control the cursor, zooming, and panning. The conversions can be displayed as codes or as volts.

Parameters such as peak-to-peak noise and rms noise are displayed below the graph in the **Analysis** section for the current batch of samples. If several analog input channels are enabled, each enabled channel can be selected and the conversions on that channel analysed using **Analysis Channel**.

The conversion data can be saved in a text file using **File** at the top of the window. To save the data into an Excel file. right-click on the waveform graph and select **Export Data** from the drop-down menu that appears. A **Save** dialog box is displayed, prompting you to save the data to an appropriate folder location.

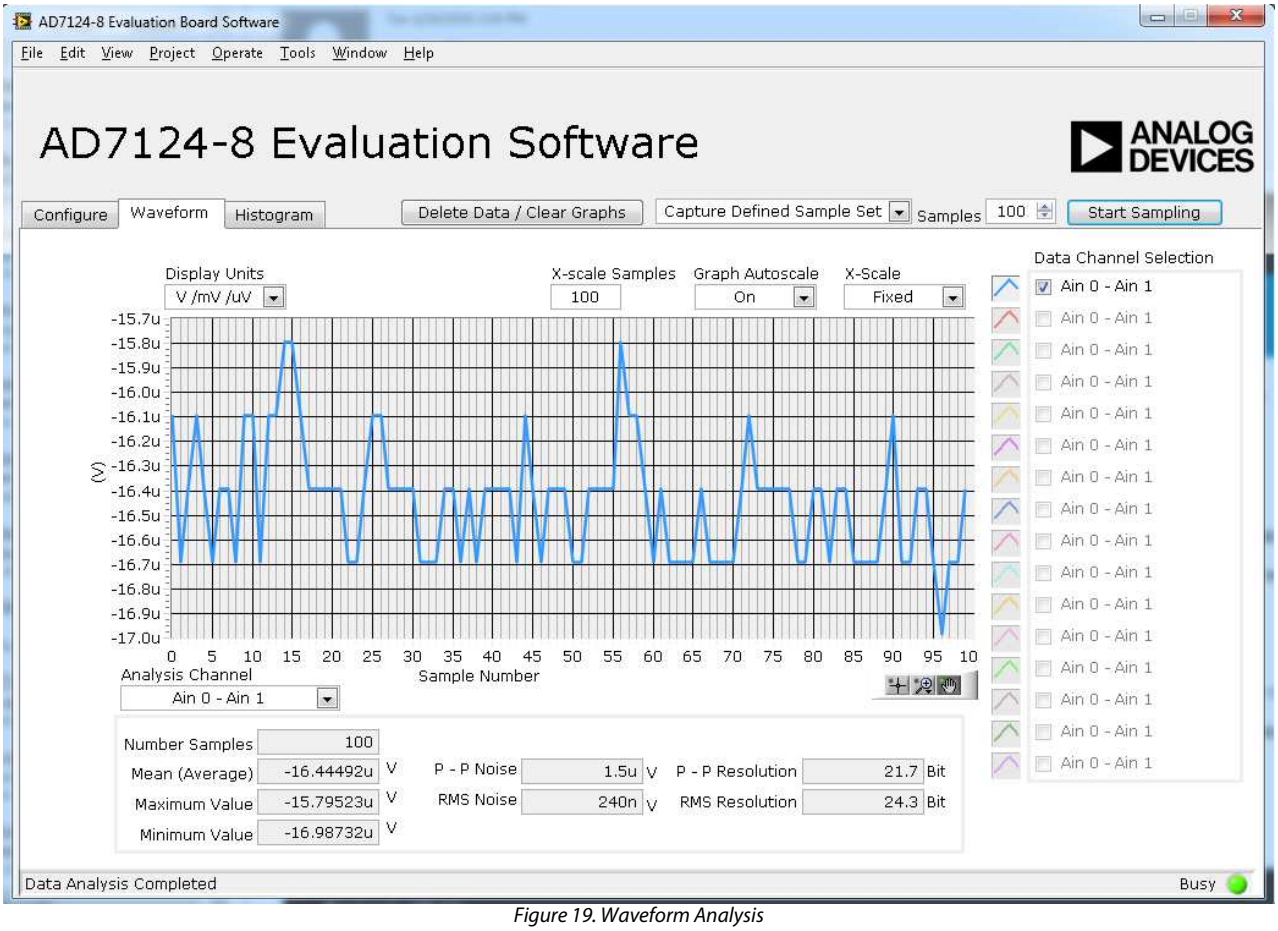

Figure 19. Waveform Analysis

Histogram

This tab shows the histogram analysis. The indicators beside this graph show the channels being converted. Navigation tools are provided to allow you to control the cursor, zooming, and panning. The conversions can be displayed as codes or as volts.

Parameters such as peak-to-peak noise and rms noise are displayed to the right of the graph in the **Analysis Results** section for the current batch of samples.

The conversion data can be saved in a text file using **File** at the top of the window. To save the data into an Excel file. right-click on the histogram graph and select **Export Data** from the drop-down menu that appears. A **Save** dialog box is displayed, prompting you to save the data to an appropriate folder location.

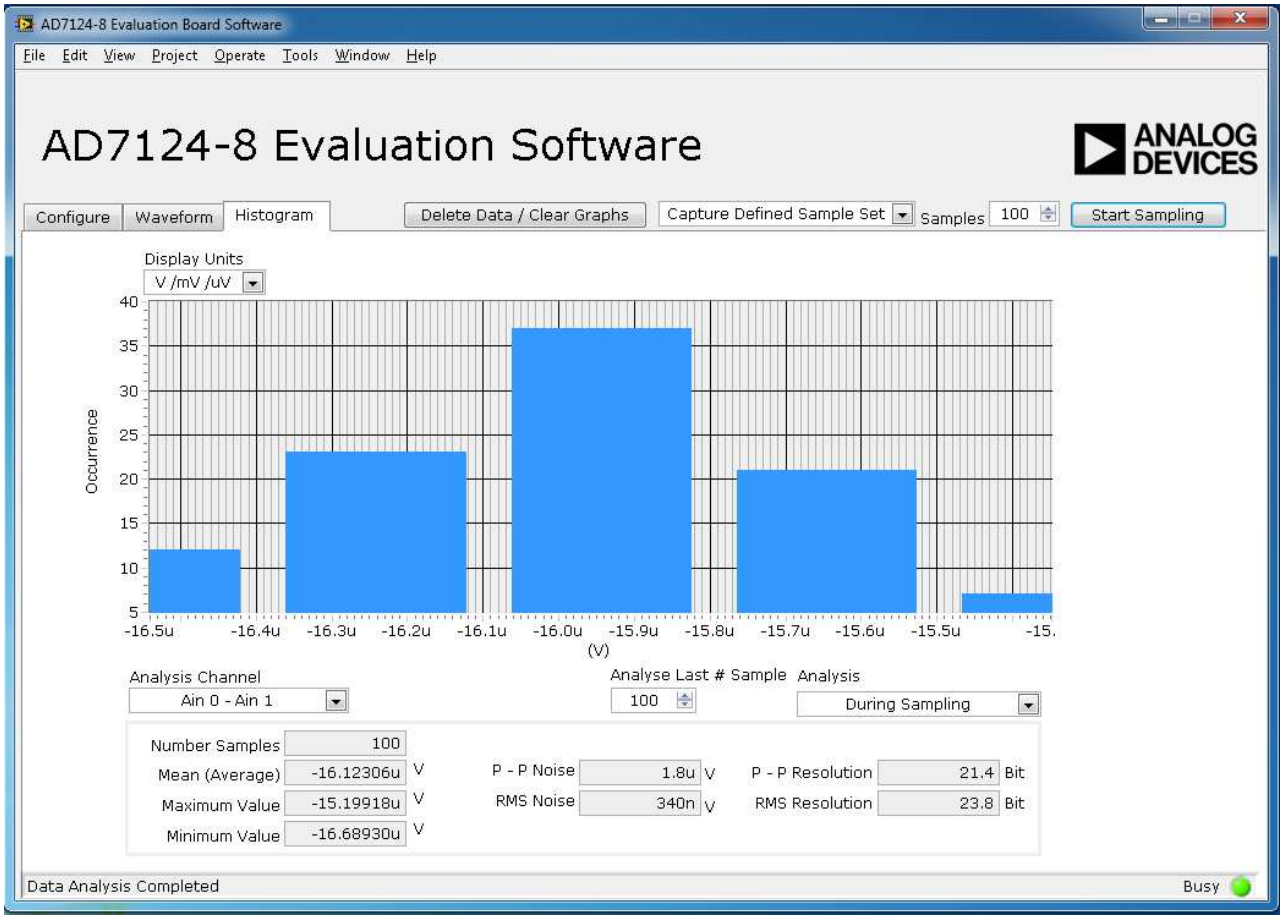

Figure 20. Histogram Analysis

EVALUATION BOARD SCHEMATICS AND ARTWORK

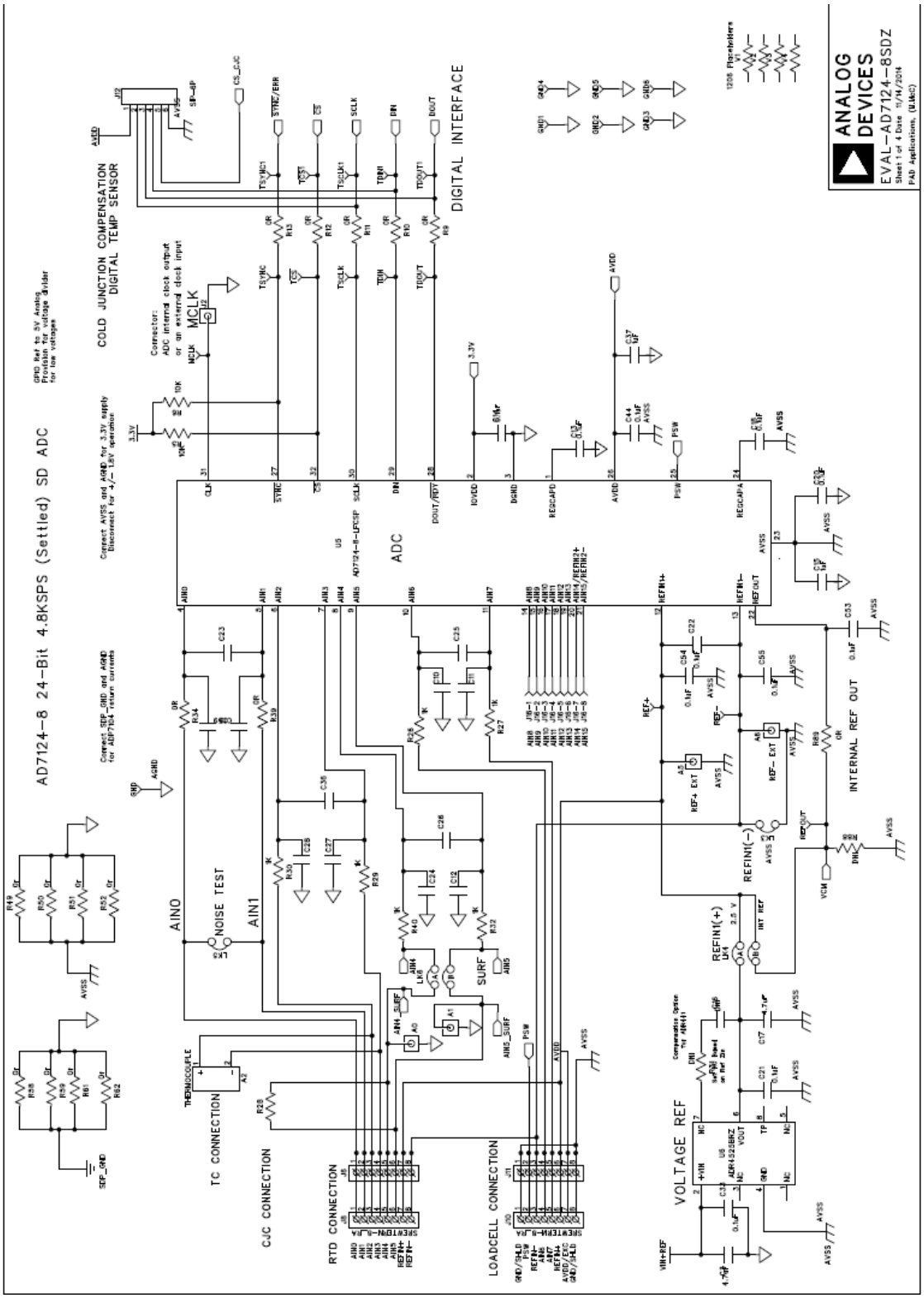

Figure 21. Schematic

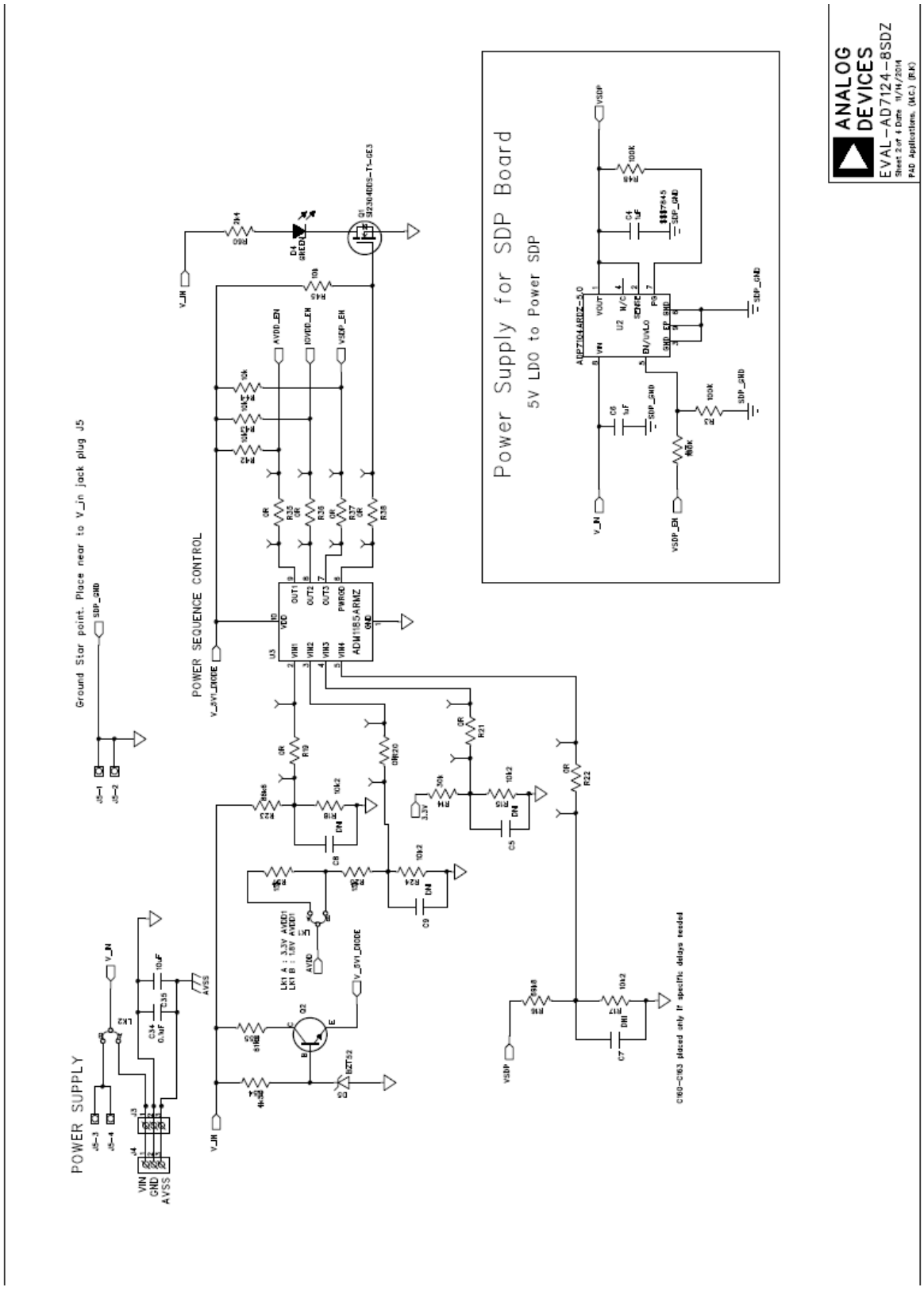

Figure 22. Schematic – Power Supply

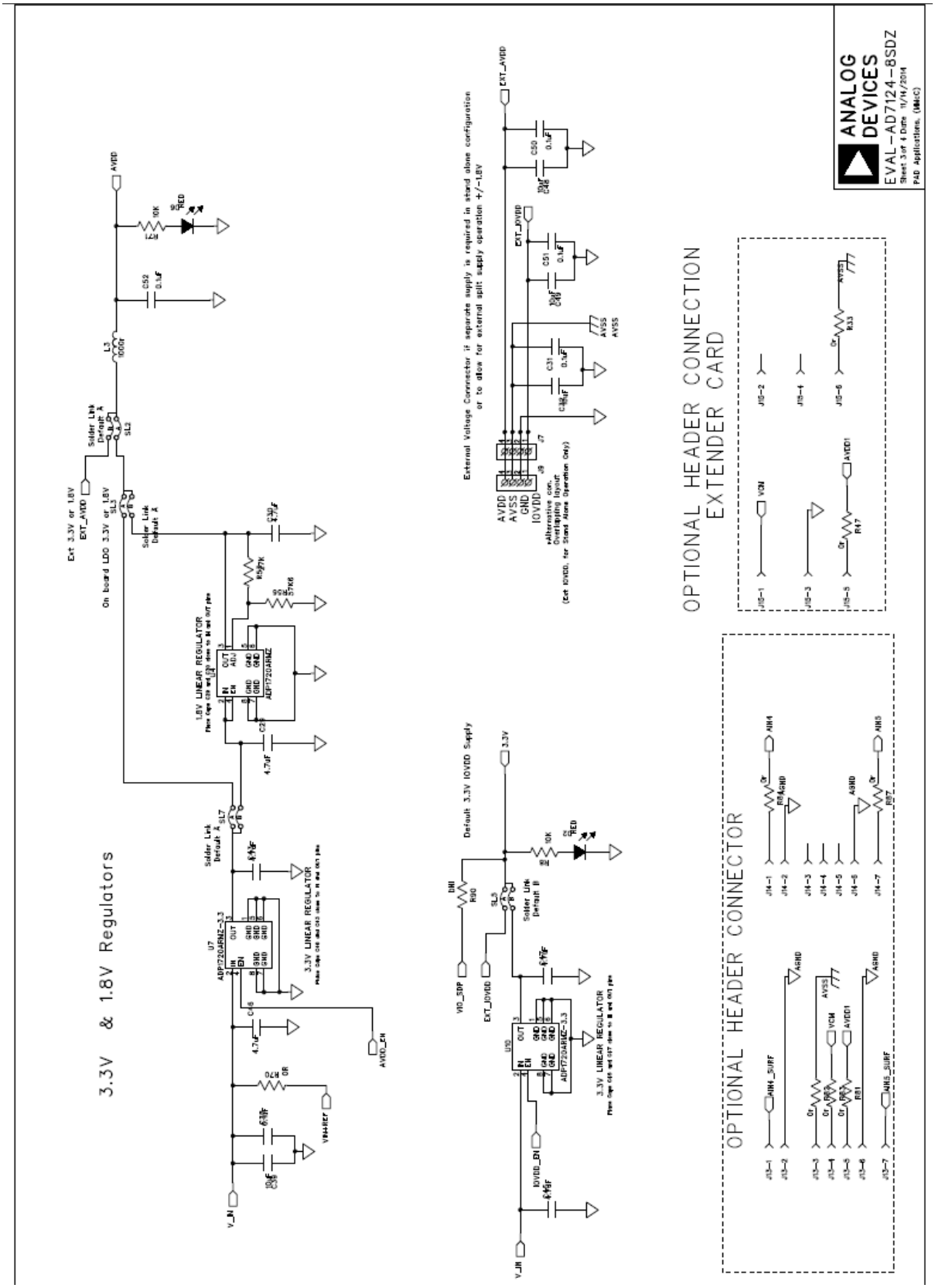

Figure 23. Schematic – Regulators

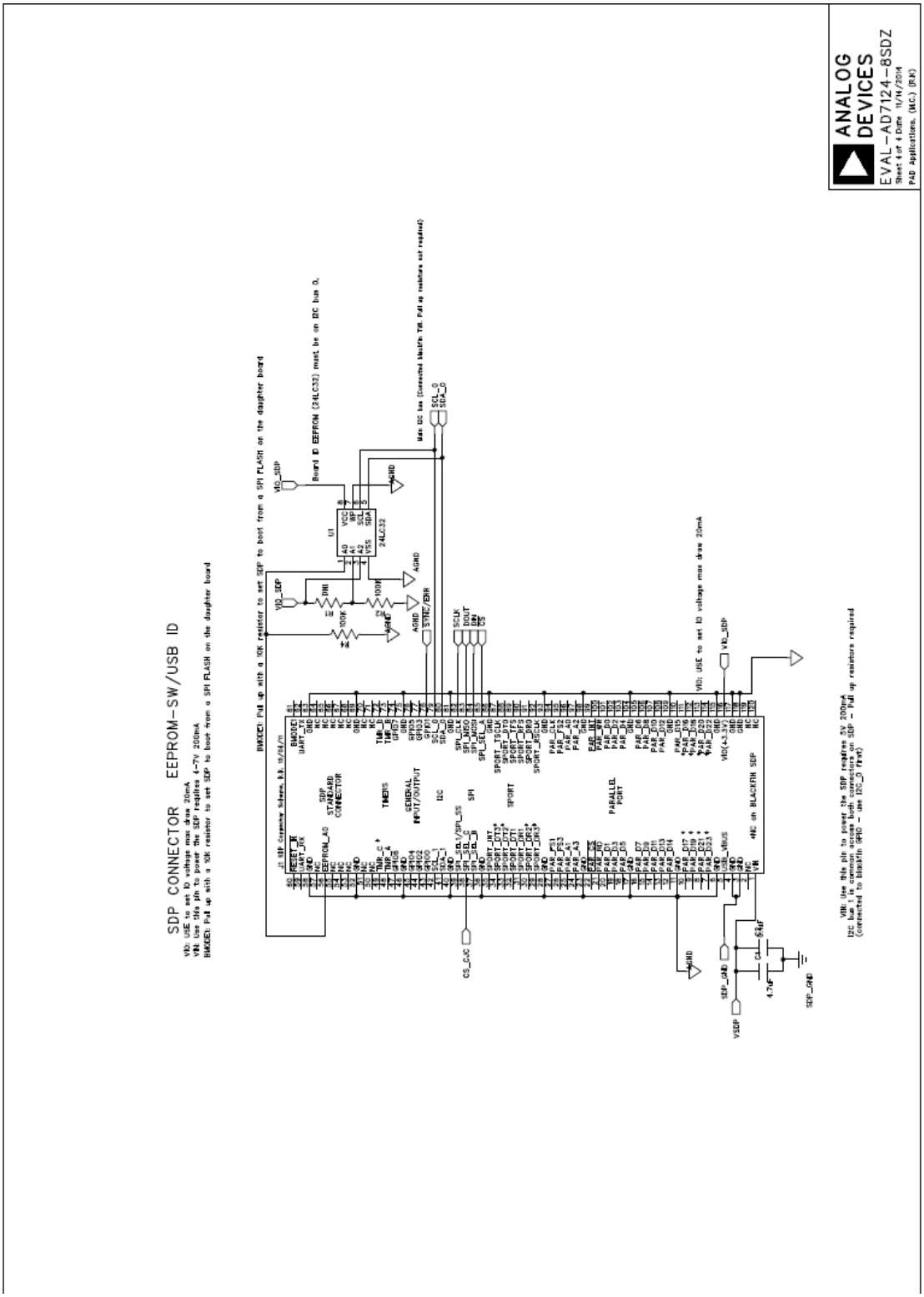

Figure 24. Schematic - SDP

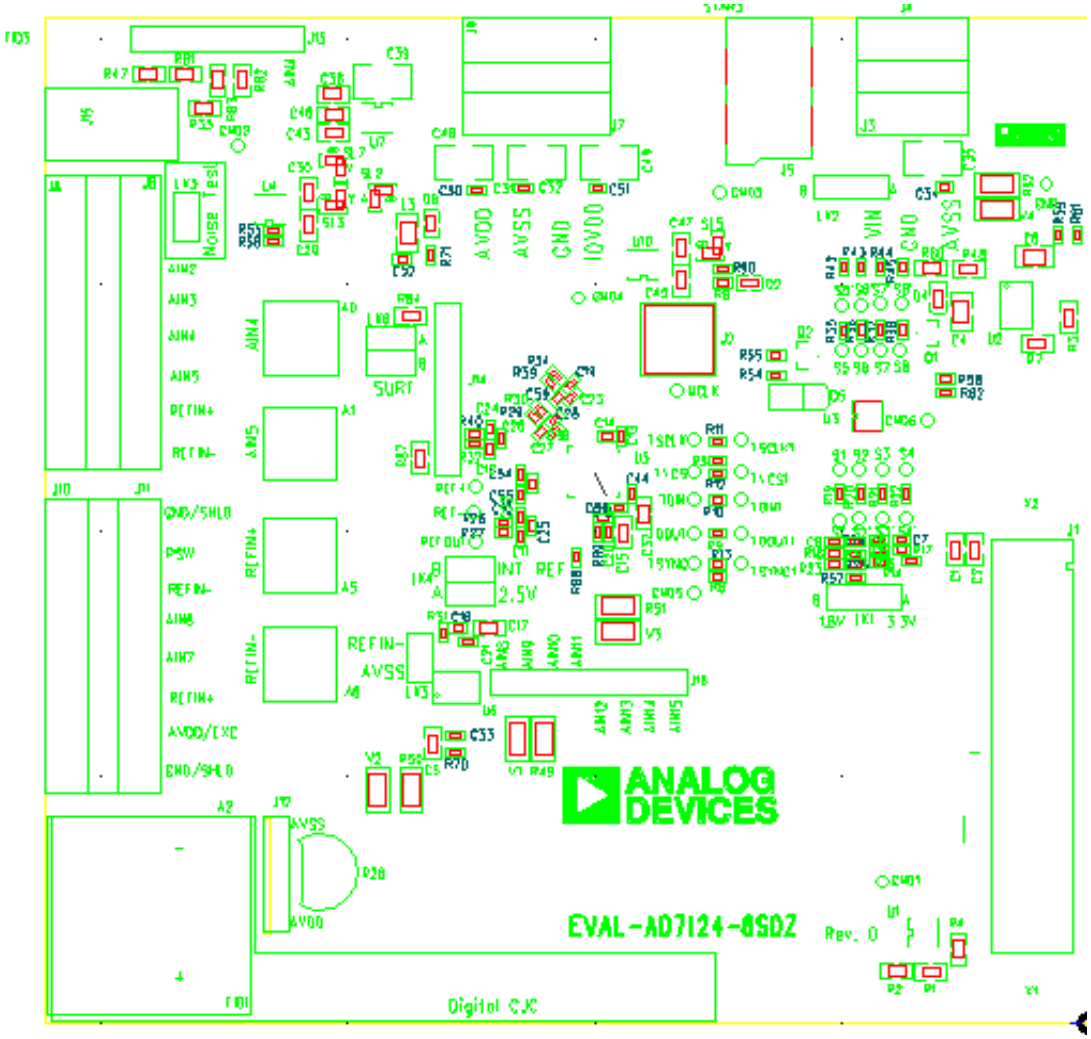

Figure 25. Top Printed Circuit Board (PCB) Silkscreen

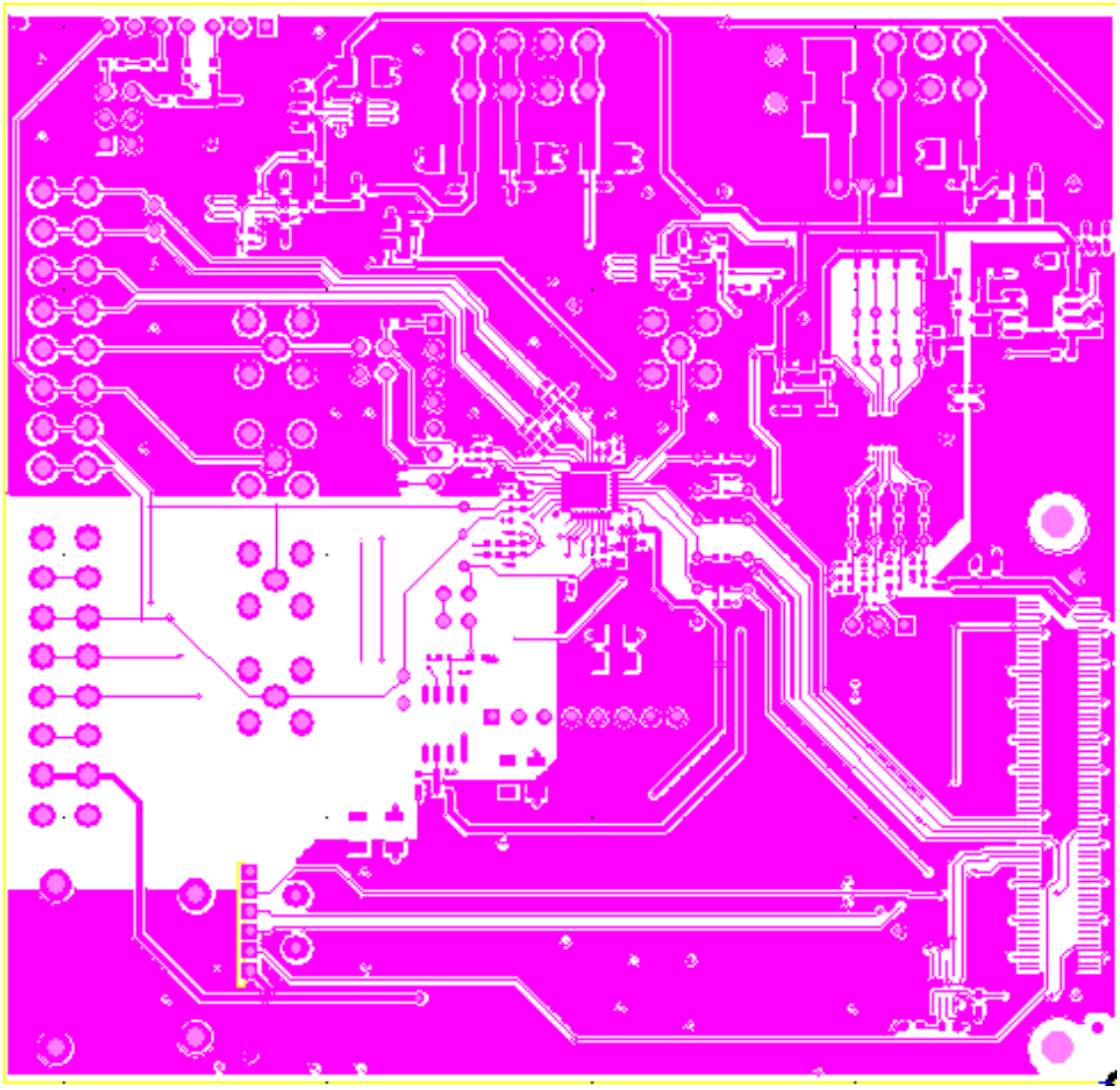

Figure 26. Layer 1 Component Side

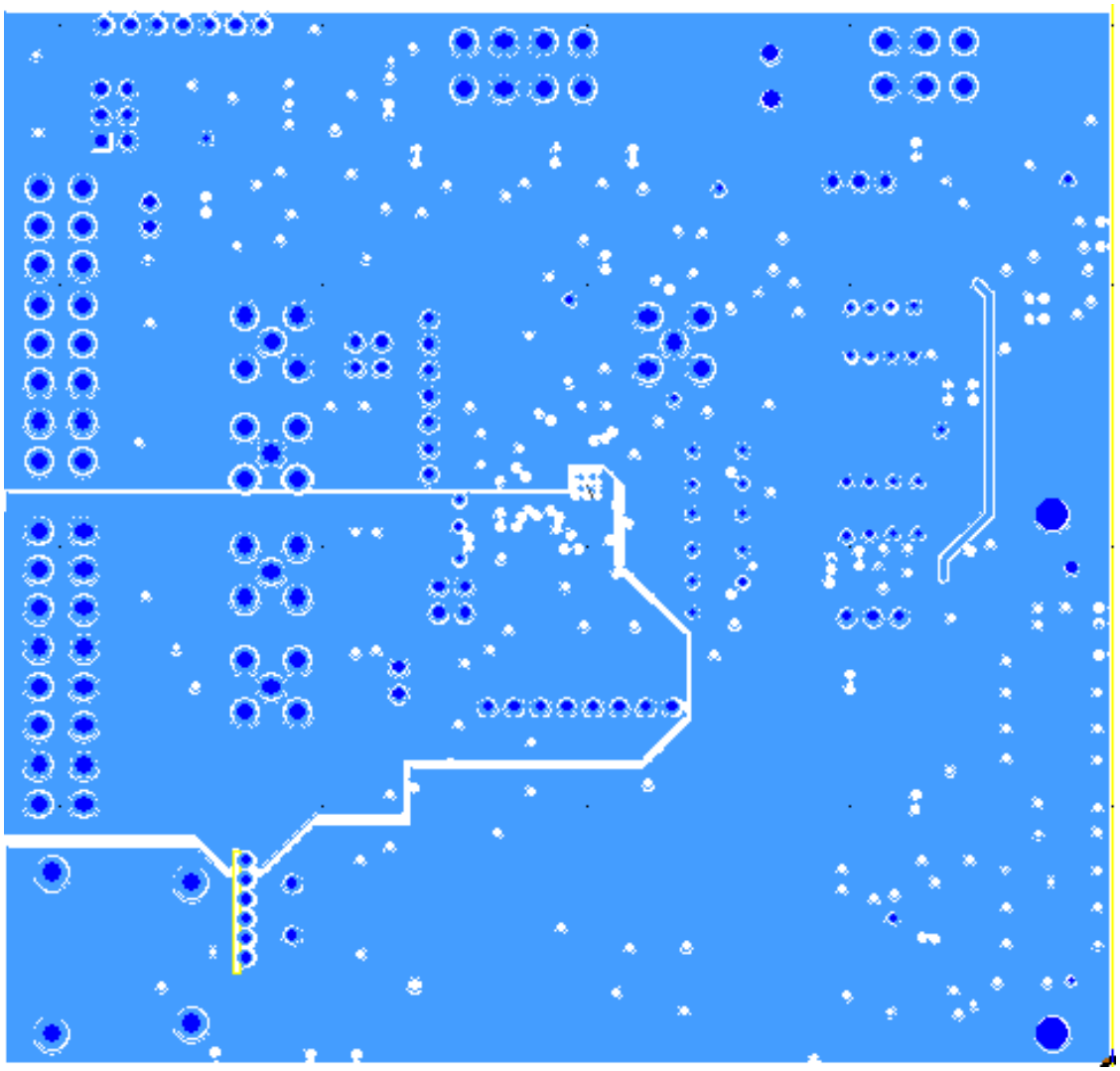

Figure 27. Layer 2 Ground Plane

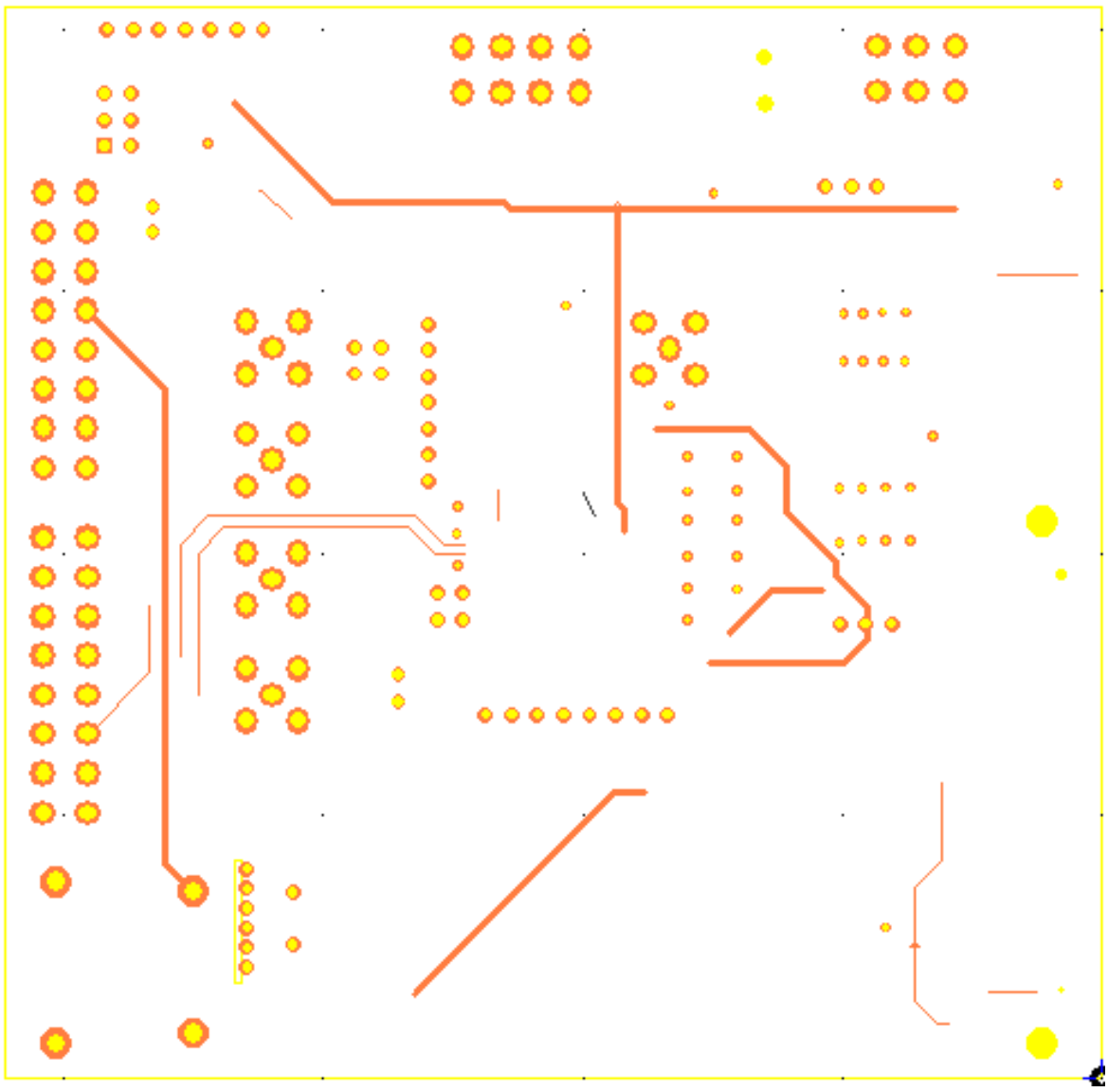

Figure 28. Layer 3 Power/Ground Plane