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Evaluating the **AD7175-8** 24-Bit, 250 kSPS, Sigma-Delta ADC with 20 μ s Settling and Integrated Analog Input Buffers

FEATURES

Full featured evaluation board for the **AD7175-8**
 PC control in conjunction with the Analog Devices, Inc.,
 SDP-B board (**EVAL-SDP-CB1Z**)
 PC software for control and data analysis (time domain)
 Standalone capability

EVALUATION KIT CONTENTS

EVAL-AD7175-8SDZ evaluation board
 Evaluation software CD
 7 V to 9 V ac-to-dc adapter

ADDITIONAL EQUIPMENT NEEDED

DC signal source

GENERAL DESCRIPTION

The **EVAL-AD7175-8SDZ** evaluation board features the **AD7175-8**, a 24-bit, 250 kSPS analog-to-digital converter (ADC) with integrated analog input buffers, on-board power supply regulation, and an external amplifier section for amplifier evaluation. A 7 V to 9 V ac-to-dc adapter is regulated to 5 V and 3.3 V; this supplies the **AD7175-8** and support components. The evaluation board connects to a USB port via the SDP-B system demonstration platform controller board (**EVAL-SDP-CB1Z**).

The **AD7175-8** evaluation software fully configures the **AD7175-8** device functionality via a user accessible register interface and provides dc time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

Full specifications on the **AD7175-8** are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board. Full details for the SDP-B controller board are available on the Analog Devices website.

FUNCTIONAL BLOCK DIAGRAM

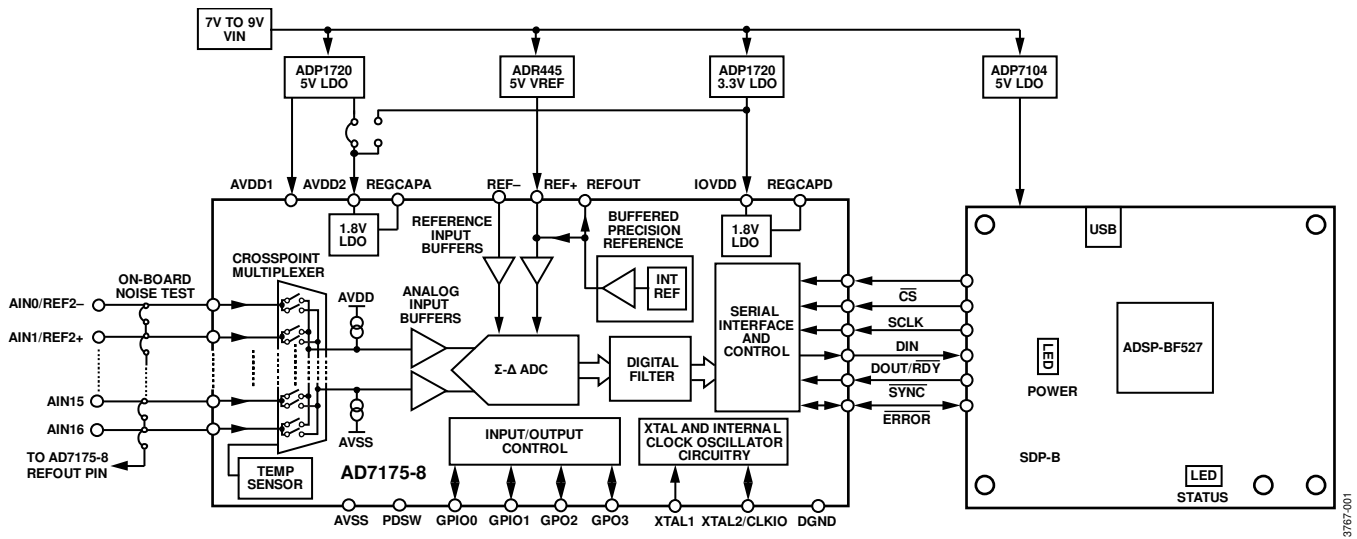


Figure 1. EVAL-AD7175-8SDZ Block Diagram

TABLE OF CONTENTS

Features	1	Power Supply Configurations.....	6
Evaluation Kit Contents.....	1	Analog Inputs.....	6
Additional Equipment Needed.....	1	Reference Options	6
General Description	1	Evaluation Board Software.....	7
Functional Block Diagram	1	Software Installation	7
Revision History	2	Launching the Software.....	7
EVAL-AD7175-8SDZ Quick Start Guide.....	3	Software Operation	8
Recommended Quick Start Guide	3	Overview of the Main Window.....	8
Quick Start Noise Test	3	Control Toolbar	8
Evaluation Board Hardware	4	Data Section	9
Device Description.....	4	Analysis Section.....	9
Hardware Link Options.....	4	Status	9
Sockets and Connectors	5	Exiting the Software.....	9
Serial Interface	5	Saving Results	9
Power Supplies	5		

REVISION HISTORY

11/15—Revision 0: Initial Version

EVAL-AD7175-8SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

Follow these steps to set up the board:

1. Disconnect the SDP-B board from the USB port of the PC. Install the [AD7175-8](#) software from the enclosed CD. Restart the PC after installation.
2. Connect the SDP-B board to the [EVAL-AD7175-8SDZ](#) evaluation board, as shown in Figure 2.
3. Fasten the two boards together with the enclosed plastic screw washer set.
4. Connect the external 9 V power supply to Connector J4 of the evaluation board, as shown in Figure 2. Set LK2 to Position B.
5. Connect the SDP-B board to the PC via the USB cable. For Windows® XP, you may need to search for the SDP drivers. Choose to automatically search for the drivers for the SDP-B board if prompted by the operating system.
6. From the **Analog Devices** subfolder in the **Programs** menu, launch the [AD7175-8](#) software.

QUICK START NOISE TEST

Use the following procedure to quickly test the noise performance:

1. Insert Link LK5 to Link LK20 to initiate the noise performance test mode. In this mode, analog input channels short to the REFOUT pin via SL11.
2. In the evaluation software, click **Start Sampling** to acquire samples from the ADC (see Figure 7).

The **Samples** numeric control in the top right corner of the main window sets the number of samples collected in each batch.

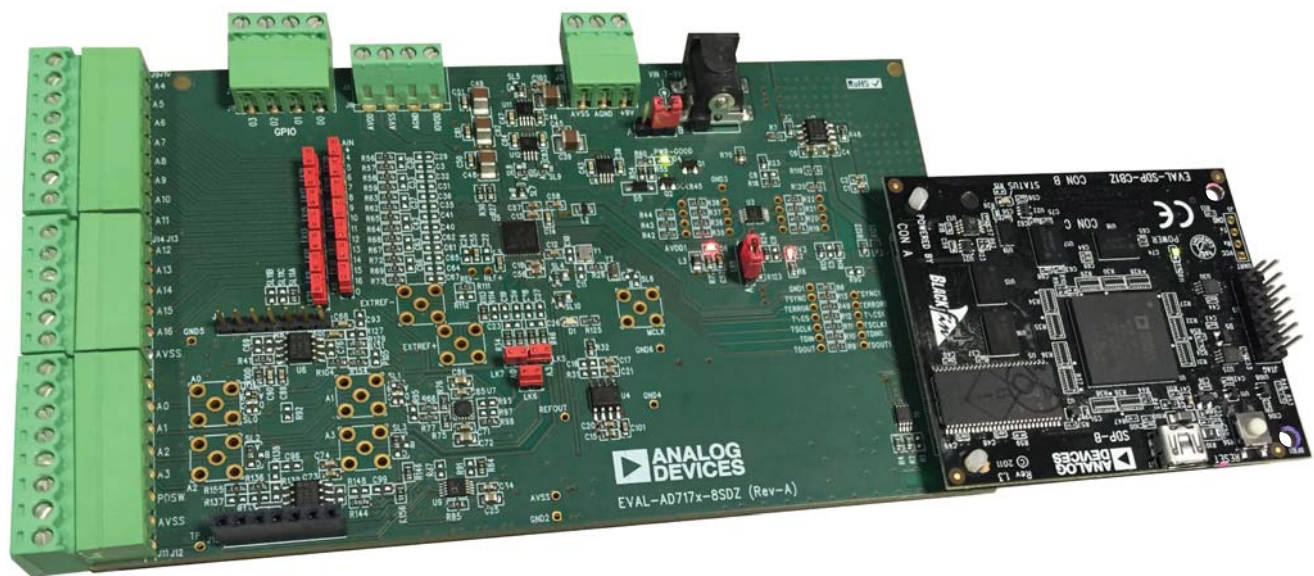


Figure 2. Hardware Configuration, Setting Up the [EVAL-AD7175-8SDZ](#)

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The [AD7175-8](#) is a highly accurate, high resolution, multiplexed, 8-/16-channel (full/pseudo differential) Σ - Δ ADC. The [AD7175-8](#) has a maximum channel-to-channel scan rate of 50 kSPS (20 μ s) for fully settled data. The output data rates range from 5 SPS to 250 kSPS. The device includes integrated analog input and reference buffers, an integrated precision 2.5 V reference, and an integrated oscillator.

HARDWARE LINK OPTIONS

See Table 1 for the default link options. By default, the board is configured to operate from the supplied 9 V ac-to-dc adapter connected to Connector J4. The 5 V supply required for the [AD7175-8](#) comes from the on-board low dropout regulator (LDO). The [ADP1720](#), with a 5 V fixed output voltage, receives its input voltage from J2 or J4 (depending on the position of LK2) and generates a 5 V output.

Table 1. Default Link and Solder Link Options

Link	Default Option	Description
LK1	A	Selects the voltage applied to the power supply sequencer circuit (U3); dependent on AVDD1. Place this link in Position A if using 5 V AVDD1, or Position B if using 2.5 V AVDD1.
LK2	B	Selects the external power supply from Connector J3 (Position A), or J4 (Position B).
LK5 to LK20	Inserted	Inserting these links sets up the on-board noise test. In this mode, all inputs short to the common voltage via SL11.
SL0	A	Routes A0 to one of the following: Position A: AIN0/REF2– pin on the AD7175-8 Position B: Buffer U6 Position C: U7 for use with a single-ended to differential driver circuit Position D: J15-1
SL1	A	Routes A1 to one of the following: Position A: AIN1/REF2+ pin on the AD7175-8 Position B: Buffer U6 Position C: U7 for use with a single-ended to differential driver circuit Position D: J15-7
SL2	A	Routes A2 to one of the following: Position A: AIN2 pin on the AD7175-8 Position B: Buffer U10 Position C: U9 for use with a single-ended to differential driver circuit
SL3	A	Routes A3 to one of the following: Position A: AIN3 pin on the AD7175-8 Position B: Buffer U10 Position C: U9 for use with a single-ended to differential driver circuit
SL4	A	Sets the voltage applied to the AVDD2 pin. Operates using the AVDD1 supply (default). Position B sets the AVDD2 voltage to the 3.3 V supply from the ADP1720 3.3 V regulator (U11).
SL5	B	Selects between an external or on-board IOVDD source. Supplies IOVDD from the ADP1720 3.3 V regulator (U11) (default). The evaluation board operates with a 3.3 V logic.
SL6	Removed	Position A connects Crystal Y1 as an external MCLK clock source. Position B connects the MCLK SMA/SMB connector for use as a clock input or an ADC internal clock output.
SL7	A	Selects between an external or on-board AVDD1 source. Supplies AVDD1 from the ADP1720 5 V regulator (U8) (default).
SL8 to SL9	A	Selects between a 5 V and 2.5 V LDO supply for AVDD1. Supplies AVDD1 with 5 V (default).
SL10	A	Selects the voltage applied to the AVDD1 pin. Operates using the supply set up by Link SL8 to Link SL9 (default). When inserted in Position B, sets the AVDD1 voltage to the 3.3 V supply from the ADP1720 3.3 V regulator.
SL11	A	Selects the voltage applied to analog input during on-board noise test (LK5 to LK20 inserted). Position A connects to the AD7175-8 REFOUT pin. Position B connects to GND. Position C connects to AVSS.
SL12 to SL15	Inserted	Connects AVSS and AGND for single-supply operation. To operate in split supply mode, remove these links.

SOCKETS AND CONNECTORS

Table 2. Connector Details

Connector	Function	Connector Type	Manufacturer	Manufacturer Number	Order Code ¹
J1	Connector to the EVAL-SDP-CB1Z	120-way connector, 0.6 mm pitch	Hirose	FX8-120S-SV(21)	FEC1324660
A0 to A3	Analog inputs to the ADC	Straight PCB mount SMB/SMA jack	Tyco	1-1337482-0	Not applicable
J3	External bench top voltage supply for the EVAL-AD7175-8SDZ	Power socket block, 3-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 3-G-3,81	FEC3704757
J4	External ac-to-dc adapter input for the EVAL-AD7175-8SDZ , 7 V to 9 V	DC power connectors, 2 mm SMT power jack	Kycon	KLDX-SMT2-0202-A	MOUSER 806-KLDX-SMT20202A
J5	External bench top voltage supply option for AVDD1/AVDD2 and IOVDD inputs on the AD7175-8	Screw terminal block, 3.81 mm pitch	Phoenix Contact	MKDS 1/4-3.81	FEC3704592
J8	GPIO terminal	Power socket block, 4-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 4-G-3,81	FEC3704749
J10 and J12	Analog input terminal block; wired connection to external source or sensor	Power socket block, 8-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 8-G-3,81	FEC3704774
J14	Analog input terminal block; wired connection to external source or sensor	Power socket block, 6-pin, 3.81 mm pitch	Phoenix Contact	MC 1,5/ 6-G-3,81	FEC3704762
J15	Optional header	7-way, 2.54 mm pin header	Samtec	SSW-107-01-T-S	FEC1803478
J16	Optional header	7-way, 2.54 mm socket	Samtec	TLW-107-05-G-S	FEC1668499

¹ Order codes starting with FEC are for Farnell.

SERIAL INTERFACE

The [EVAL-AD7175-8SDZ](#) evaluation board connects to the Blackfin® [ADSP-BF527](#) on the SDP-B controller board via the serial peripheral interface (SPI). There are four primary signals, CS, SCLK, and DIN (all inputs), and one output from the ADC, DOUT/RDY.

To operate the evaluation board in standalone mode, disconnect the [AD7175-8](#) serial interface lines from the 120-pin header by removing the 0 Ω, R9 through R13 links. Use the test points to connect the signals to an alternative digital capture setup.

POWER SUPPLIES

Power the evaluation board from the ac-to-dc adapter connected to J4, or from an external bench top supply applied to J3 or J5. Linear LDOs generate the required voltages from the applied input voltage (V_{IN}) rail when using J3 or J4. Use J5 to bypass the on-board regulators. The regulators used are the 5 V fixed output voltage and 2.5 V adjustable output voltage [ADP1720](#) devices, which supply the AVDD1 and AVDD2 rails to the ADC; the [ADP1720](#) (3.3 V) supplies the IOVDD rail. Use the [ADP7104](#) (5 V) to supply 5 V for the SDP-B controller board. Each supply is decoupled where it enters the board and again at each device. Table 3 shows the various power supply configurations available, including split supply operation.

Table 3. Power Supply Configurations¹

Configuration	Input Voltage Range	Description
Single Supply (Regulated)	7 V to 9 V	The 7 V to 9 V input is regulated to 5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. This supply also powers the external 5 V reference. See the Single Supply (Regulated) section.
Single Supply (Unregulated)	7 V to 9 V, 5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Single Supply (Unregulated) section.
Split Supply (Regulated)	7 V to 9 V and -2.5 V	The 7 V to 9 V input is regulated to 2.5 V for AVDD1/AVDD2 and 3.3 V for IOVDD. The 7 V to 9 V input powers the external 5 V reference, and the -2.5 V input is connected to AVSS directly (unregulated). See the Split Supply (Regulated) section.
Split Supply (Unregulated)	7 V to 9 V, ±2.5 V, and 3.3 V	The input is unregulated and connects directly to AVDD1/AVDD2 and IOVDD from J5. The 7 V to 9 V input powers the external 5 V reference. See the Split Supply (Unregulated) section.

¹ Only one configuration can be used at a time.

POWER SUPPLY CONFIGURATIONS

Single Supply (Regulated)

There are two available power supply options for the single-supply (regulated) configuration.

- An ac-to-dc adapter (included) connected to J4. Set LK2 to Position B.
- A bench top power supply connected to J3. Set LK2 to Position A and ensure that AVSS = AGND = 0 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Single Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL5 to Position A and SL7 to Position B.
2. Connect the two terminals of J5 labeled AGND and AVSS.
3. Connect 0 V (GND) to J5 at the terminal labeled AGND.
4. Connect 5 V to J5 at the terminal labeled AVDD.
5. Connect 3.3 V to J5 at the terminal labeled IOVDD.
6. Connect the 7 V to 9 V input to either J3 or J4.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Regulated)

To set up the board, use the following procedure:

1. Remove SL12 to SL15. These links connect AVSS to AGND.
2. Connect a bench top power supply to J3 and set LK2 to Position A. Make sure that AVSS = -2.5 V in this case.
3. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links to the default settings as outlined in Table 1.

Split Supply (Unregulated)

To set up the board, use the following procedure:

1. Move SL5 to Position A and move SL7 to Position B.
2. Remove SL12 to SL15.
3. Connect 0 V (GND) to J5 at the terminal labeled AGND.
4. Connect 2.5 V to J5 at the terminal labeled AVDD.
5. Connect -2.5 V to J5 at the terminal labeled AVSS.
6. Connect 3.3 V to J5 at the terminal labeled IOVDD.
7. Connect 7 V to 9 V to either J3 or J4. Connect or disconnect the AVSS terminal of J3 to the AVSS terminal of J5.
8. Set LK1 to Position B. This sets the input to the power monitor circuitry to work with the lower AVDD1 supply of 2.5 V.

Set all other links and solder links set to the default settings as outlined in Table 1.

ANALOG INPUTS

The [EVAL-AD7175-8SDZ](#) primary analog inputs can be applied in two separate ways:

- J10, J12, and J14 connectors on the left side of the board
- A0 to A3 SMB/SMA footprints on the evaluation board

The analog inputs route directly to the associated analog input pins on the [AD7175-8](#), provided that the LK5 to LK20 links (on-board noise test) are removed. The [AD7175-8](#) evaluation software is set up to analyze dc inputs to the ADC. The [AD7175-8](#) input buffers work for dc input signals.

REFERENCE OPTIONS

The [EVAL-AD7175-8SDZ](#) includes an external 5 V reference, the [ADR445](#). The [AD7175-8](#) includes an internal 2.5 V reference. The default operation is to use the external reference input, which is set to accept the 5 V [ADR445](#) on the evaluation board.

Choose the reference in the SETUPCONx registers associated with Setup 0 to Setup 7 to select the reference used for conversions by the [AD7175-8](#).

Change between the internal and external references by accessing the [AD7175-8](#) register map in the evaluation software (click [ADC Setup](#)).

EVALUATION BOARD SOFTWARE SOFTWARE INSTALLATION

The [EVAL-AD7175-8SDZ](#) evaluation kit includes software on a CD. Double-click the **setup.exe** file from the CD to run the installer. The default installation location for the software is **C:\Program Files\Analog Devices\EVAL-AD7175-8SDZ**.

Install the evaluation software before connecting the evaluation board and SDP-B controller board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the installation:

- [AD7175-8](#) evaluation board software installation
- [EVAL-SDP-CB1Z](#) SDP-B board drivers installation

Place the software and drivers in the appropriate locations by proceeding through all of the installation steps. Connect the SDP-B board to the PC only after the software and drivers are installed. The installer may prompt for permission to allow the program to make changes to the computer. Click **Yes** to proceed (see Figure 3).

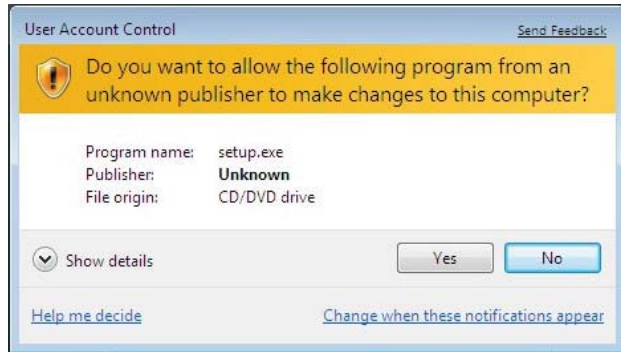


Figure 3. User Account Control Permission Dialog Box

A security warning may appear as part of the SDP-B controller board driver installation. Click **Install** to proceed with the installation of the driver (see Figure 4). Without this confirmation, the software cannot operate correctly.



Figure 4. SDP-B Drivers Installation Confirmation Dialog Box

After installation is complete, connect the [EVAL-AD7175-8SDZ](#) evaluation board to the [EVAL-SDP-CB1Z](#) SDP-B board, as shown in Figure 2. Connect the SDP-B board via the USB cable to the computer.

Take the following steps to verify that the SDP-B controller board driver is installed and working correctly:

1. Allow the **Found New Hardware Wizard** to run.
2. After the drivers are installed, check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer**, selecting **Manage**, and then **Device Manager** from the list of **System Tools** (see Figure 5).
3. The SDP-B board appears under **ADI Development Tools** as **Analog Devices System Development Platform** or similar. The installation is complete.

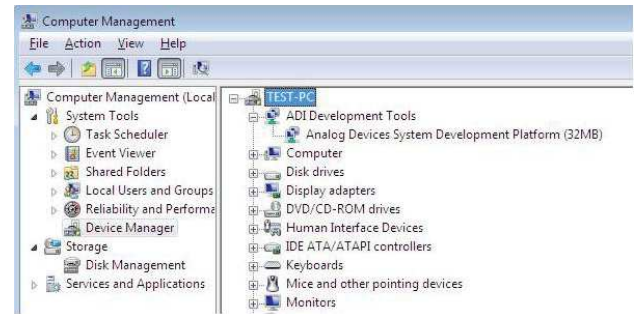


Figure 5. Device Manager

LAUNCHING THE SOFTWARE

The [AD7175-8](#) software can be launched when the [EVAL-AD7175-8SDZ](#) evaluation board and the [EVAL-SDP-CB1Z](#) SDP-B controller board are correctly connected to the PC.

To launch the software, do the following:

1. From the **Start** menu, click **Programs**, **Analog Devices**, and then **EVAL-AD7175-8SDZ**. The main window of the software then displays (see Figure 7).
2. If the [AD7175-8](#) evaluation system is not connected to the USB port via the SDP-B board when the software is launched, a connectivity error displays (see Figure 6). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

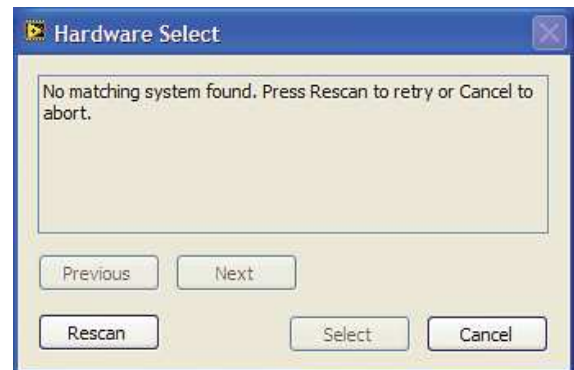


Figure 6. Connectivity Error Alert Dialog Box

SOFTWARE OPERATION

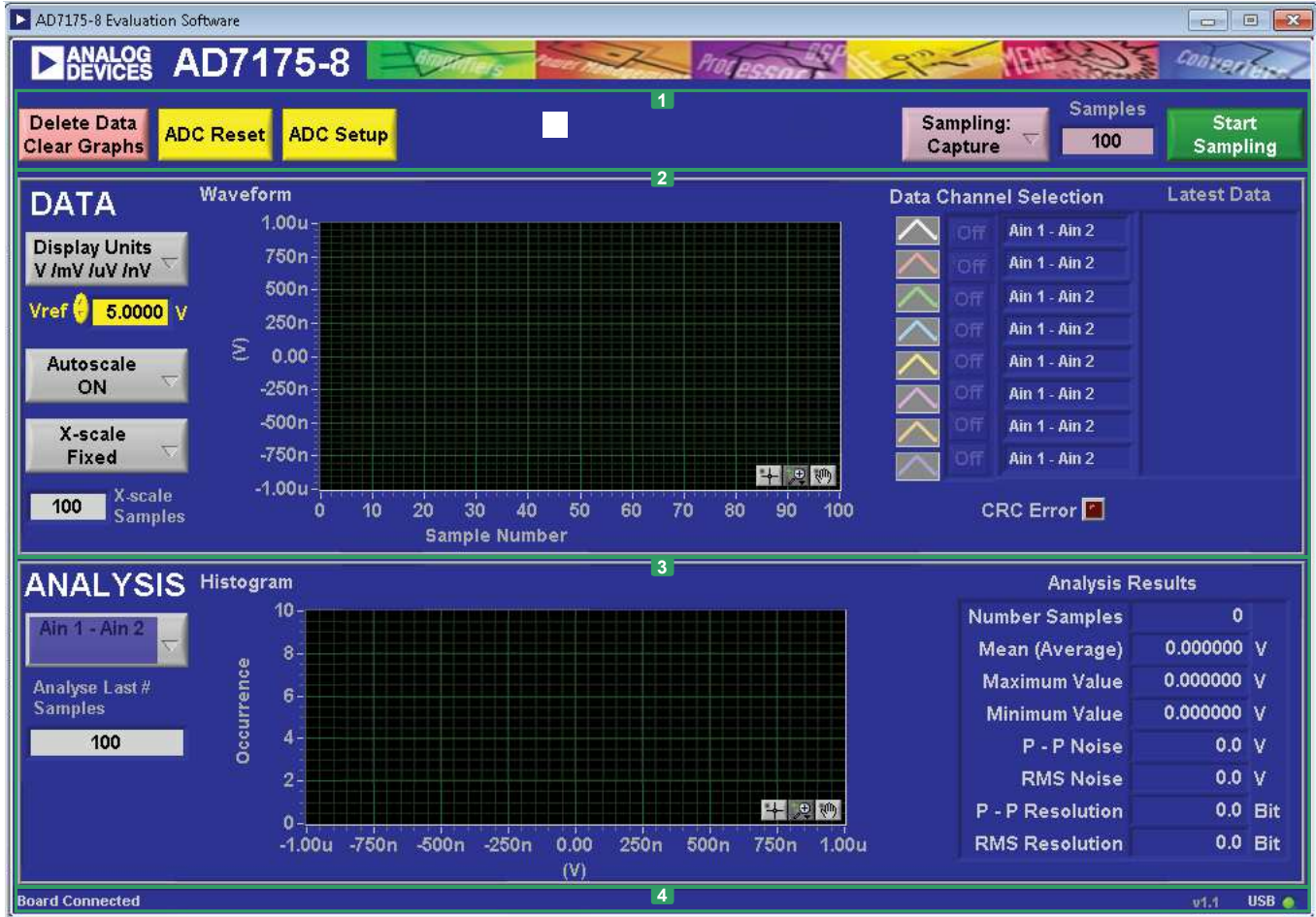


Figure 7. Main Window of the AD7175-8 Evaluation Software

OVERVIEW OF THE MAIN WINDOW

The main window of the software displays the significant control buttons and analysis indicators of the AD7175-8 evaluation software (see Figure 7). This window is divided into four sections. The green numbers shown in Figure 7 (Label 1 through Label 4) correspond to the following components of the main window:

- Control toolbar (Label 1)—control buttons
- Data section (Label 2)—waveform graph and controls
- Analysis section (Label 3)—histogram graph and controls
- Status bar (Label 4)—information

CONTROL TOOLBAR

Start Sampling and Samples

Start Sampling, located on the right of the control toolbar, gathers ADC results. Results appear in the graphs of the DATA and ANALYSIS sections of the main window. The **Samples** numeric control is the number of samples gathered per batch.

Sampling

Sampling (set to **Capture** in Figure 7) enacts the sampling mode used by the software. This is unrelated to the ADC mode. The user can capture a defined sample set or continuously gather batches of samples. In both cases, the number of samples set in the **Samples** numeric input dictates the number of samples.

ADC Setup

Click **ADC Setup** to open the ADC register map window. Use the new window to change register settings. This window allows the user to save existing register settings or load previously saved register settings.

ADC Reset

Click **ADC Reset** to perform a software reset of the AD7175-8. There is no hardware reset pin. Perform a hard reset by removing power to the board. The software reset has the same effect as a hard reset.

Delete Data Clear Graphs

Click **Delete Data Clear Graphs** to clear any existing content from the waveform and histogram graphs.

DATA SECTION

Data Waveform

The data waveform shows each successive sample of the ADC output. The toolbar in the graph allows the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

Display Units

Click **Display Units** to select whether the data graph displays in units of voltages or codes.

Vref

Vref sets the reference voltage used for calculating the results on the data graph. The user must update this value when the reference source changes, because it does not automatically update.

Autoscale

Autoscale enables and disables the y-axis autoscale control for the data graph. With this control enabled, the graph automatically sets the maximum and minimum y-axis values to fit the displayed data.

X-scale and X-scale Samples

These controls set the number of data points displayed on the x-axis. When set to fixed, the number of data points is equal to the number in the **X-scale Samples** numeric input. This control automatically updates each time **Start Sampling** is clicked. When set to dynamic, all samples are displayed, including those from previous sample batches.

Channel Selection

This control allows the user to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

Latest Data

These indicators show the value of the last sample gathered on the corresponding channel (see **Channel Selection**).

ANALYSIS SECTION

Analysis Histogram and Analysis Channel

The histogram shows the analysis of the channel selected via the analysis channel drop-down box. This graph only shows the histogram for one channel at a time.

Analysis Last # Samples

This is the number of samples used for creating the histogram analysis. This is automatically set to equal the number of samples when **Start Sampling** is clicked.

Analysis Results

This section displays the results of the histogram analysis for the selected analysis channel. This includes both noise and resolution measurements.

STATUS

The status section at the bottom of the window display status updates such as **Analysis Completed** and **Reset Completed** during software use.

EXITING THE SOFTWARE

To exit the software, click the close button at the top, right corner of the main window (see Figure 7).

SAVING RESULTS

The software can save the current captured data for later analysis.

1. Right-click the waveform graph.
2. Click **Export** in the drop-down menu.
3. Select the folder for the data to be saved into and the name of the file you want to save.
4. Click **Save**.

The data is saved in the format selected for display units via the **Display Units** option.

NOTES

**ESD Caution**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

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