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500 kSPS, 8-Channel, Software-Selectable, True Bipolar Input, 12-Bit Plus Sign ADC

Data Sheet **AD7327**

FEATURES

12-bit plus sign SAR ADC
True bipolar input ranges
Software-selectable input ranges
±10 V, ±5 V, ±2.5 V, 0 V to +10 V
500 kSPS throughput rate
8 analog input channels with channel sequencer
Single-ended, true differential, and pseudo differential analog input capability
High analog input impedance
Low power: 18 mW
Temperature indicator
Full power signal bandwidth: 22 MHz
Internal 2.5 V reference
High speed serial interface
Power-down modes
20-lead TSSOP package
***i*CMOS™ process technology**

FUNCTIONAL BLOCK DIAGRAM

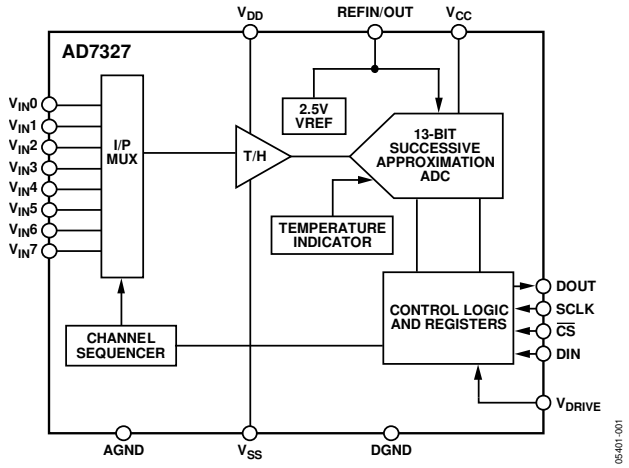

Figure 1.

GENERAL DESCRIPTION

The AD7327[1] is an 8-channel, 12-bit plus sign successive approximation ADC designed on the *i*CMOS (industrial CMOS) process. *i*CMOS is a process combining high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7327 can accept true bipolar analog input signals. The AD7327 has four software-selectable input ranges: ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7327 can be programmed to be single-ended, true differential, or pseudo differential.

The ADC contains a 2.5 V internal reference. The AD7327 also allows external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7327 can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range. The ADC has a high speed serial interface that can operate at throughput rates up to 500 kSPS.

PRODUCT HIGHLIGHTS

1. The AD7327 can accept true bipolar analog input signals, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V unipolar signals.
2. The eight analog inputs can be configured as eight single-ended inputs, four true differential inputs, four pseudo differential inputs, or seven pseudo differential inputs.
3. 500 kSPS serial interface. SPI®-/QSPI™-/DSP-/MICROWIRE™-compatible interface.
4. Low power, 18 mW, at a maximum throughput rate of 500 kSPS.
5. Channel sequencer.

Table 1. Similar Devices

Device Number	Throughput Rate	Number of bits	Number of Channels
AD7329	1000 kSPS	12-bit plus sign	8
AD7328	1000 kSPS	12-bit plus sign	8
AD7324	1000 kSPS	12-bit plus sign	4
AD7323	500 kSPS	12-bit plus sign	4
AD7322	1000 kSPS	12-bit plus sign	2
AD7321	500 kSPS	12-bit plus sign	2

[1]Protected by U.S. Patent No. 6,731,232.

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Tel: 781.329.4700
Technical Support **www.analog.com**

AD7327* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- AD7327 Evaluation Board

DOCUMENTATION

Data Sheet

- AD7327-DSCC: Military Data Sheet
- AD7327-EP: Enhanced Product Data Sheet
- AD7327: 500 kSPS, 8-Channel, Software-Selectable, True Bipolar Input, 12-Bit Plus Sign ADC Data Sheet

User Guides

- UG-419: Evaluating the AD7327/AD7328

SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7327 FMC-SDP Interposer & Evaluation Board / Xilinx KC705 Reference Design
- AD7327/AD7328 Evaluation Software
- BeMicro FPGA Project for AD7327 with Nios driver

REFERENCE MATERIALS

Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

DESIGN RESOURCES

- AD7327 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all AD7327 EngineerZone Discussions.

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Change to Endnote 1 in Table 4 ... 8
Added Power Supply Configuration Section, Figure 56, and Table 16 ... 33

1/06—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, f_{SCLK} = 10 MHz, f_S = 500 kSPS, T_A = T_{MAX} to T_{MIN}, unless otherwise noted.

Table 2.

	B Version				
Parameter[1]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DYNAMIC PERFORMANCE					F_{IN} = 50 kHz sine wave
Signal-to-Noise Ratio (SNR)[2]	76			dB	Differential mode, V_{CC} = 4.75 V to 5.25 V
	75.5			dB	Differential mode, V_{CC} < 4.75 V
	72.5			dB	Single-ended/pseudo differential mode; ±10 V, ±2.5 V and ±5 V ranges, V_{CC} = 4.75 V to 5.25 V
	72			dB	Single-ended/pseudo differential mode; 0 V to 10 V V_{CC} = 4.75 V to 5.25 V and all ranges at V_{CC} < 4.75 V
Signal-to-Noise + Distortion (SINAD)[2]	75			dB	Differential mode; ±2.5 V and ±5 V ranges
	74				Differential mode; 0 V to 10 V
		76		dB	Differential mode; ±10 V range
	72			dB	Single-ended/pseudo differential mode; ±2.5 V and ±5 V ranges
		72.5		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Total Harmonic Distortion (THD)[2]			−80	dB	Differential mode; ±2.5 V and ±5 V ranges
			−79	dB	Differential mode; 0 V to 10 V ranges
		−82		dB	Differential mode; ±10 V range
			−77	dB	Single-ended/pseudo differential mode; ±5 V range
			−79	dB	Single-ended/pseudo differential mode; ±2.5 V range
		−80		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Peak Harmonic or Spurious Noise (SFDR)[2]			−81	dB	Differential mode; ±2.5 V and ±5 V ranges
			−80	dB	Differential mode; 0 V to 10 V ranges
		−82		dB	Differential mode; ±10 V ranges
			−78	dB	Single-ended/pseudo differential mode; ±5 V range
			−80		Single-ended/pseudo differential mode; ±2.5 V range
		−79		dB	Single-ended/pseudo differential mode; 0 V to +10 V and ±10 V ranges
Intermodulation Distortion (IMD)[2]					fa = 50 kHz, fb = 30 kHz
Second-Order Terms		−88		dB	
Third-Order Terms		−90		dB	
Aperture Delay[3]		7		ns	
Aperture Jitter[3]		50		ps	
Common-Mode Rejection (CMRR)[2]		−79		dB	Up to 100 kHz ripple frequency; see Figure 17
Channel-to-Channel Isolation[2]		−72		dB	F_{IN} on unselected channels up to 100 kHz; see Figure 14
Full Power Bandwidth		22		MHz	At 3 dB
		5		MHz	At 0.1 dB

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
DC ACCURACY[4]					Single-ended/pseudo differential mode 1 LSB = FSR/4096, unless otherwise noted. Differential mode 1 LSB = FSR/8192, unless otherwise noted.
Resolution	13			Bits	
No Missing Codes	12-bit plus sign (13 bits)			Bits	Differential mode
	11-bit plus sign (12 bits)			Bits	Single-ended/pseudo differential mode
Integral Nonlinearity[2]			±1.1	LSB	Differential mode; V_{CC} = 3 V to 5.25 V, typ for V_{CC} = 2.7 V
			±1	LSB	Single-ended/pseudo differential mode, V_{CC} = 3 V to 5.25 V, typ for V_{CC} = 2.7 V
		−0.7/+1.2		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Differential Nonlinearity[2]			−0.9/+1.2	LSB	Differential mode; guaranteed no missing codes to 13 bits
			±0.9	LSB	Single-ended mode; guaranteed no missing codes to 12 bits
		−0.7/+1		LSB	Single-ended/pseudo differential mode (LSB = FSR/8192)
Offset Error[2, 5]			−4/+9	LSB	Single-ended/pseudo differential mode
			−7/+10	LSB	Differential mode
Offset Error Match[2, 5]			±0.6	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Gain Error[2, 5]			±8	LSB	Single-ended/pseudo differential mode
			±14	LSB	Differential mode
Gain Error Match[2, 5]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Positive Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±7	LSB	Differential mode
Positive Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Bipolar Zero Error[2, 6]			±8.5	LSB	Single-ended/pseudo differential mode
			±7.5	LSB	Differential mode
Bipolar Zero Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
Negative Full-Scale Error[2, 6]			±4	LSB	Single-ended/pseudo differential mode
			±6	LSB	Differential mode
Negative Full-Scale Error Match[2, 6]			±0.5	LSB	Single-ended/pseudo differential mode
			±0.5	LSB	Differential mode
ANALOG INPUT					
Input Voltage Ranges					Reference = 2.5 V; see Table 6
(Programmed via Range Registers)		±10		V	V_{DD} = +10 V min, V_{SS} = −10 V min, V_{CC} = +2.7 V to +5.25 V
		±5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		±2.5		V	V_{DD} = +5 V min, V_{SS} = −5 V min, V_{CC} = +2.7 V to +5.25 V
		0 to 10		V	V_{DD} = +10 V min, V_{SS} = AGND min, V_{CC} = +2.7 V to +5.25 V
Pseudo Differential V_{IN}(−) Input Range					V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5 V; see Figure 40 and Figure 41
		±3.5		V	Reference = 2.5 V; range = ±10 V
		±6		V	Reference = 2.5 V; range = ±5 V
		±5		V	Reference = 2.5 V; range = ±2.5 V
		+3/−5		V	Reference = 2.5 V; range = 0 V to +10 V

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
DC Leakage Current			±80	nA	$V_{IN} = V_{DD}$ or V_{SS}
		3		nA	Per input channel, $V_{IN} = V_{DD}$ or V_{SS}
Input Capacitance[3]		13.5		pF	When in track, ±10 V range
		16.5		pF	When in track, ±5 V and 0 V to +10 V ranges
		21.5		pF	When in track, ±2.5 V range
		3		pF	When in hold, all ranges
REFERENCE INPUT/OUTPUT					
Input Voltage Range	2.5		3	V	
Input DC Leakage Current			±1	µA	
Input Capacitance		10		pF	
Reference Output Voltage		2.5		V	
Reference Output Voltage Error at 25°C			±5	mV	
Reference Output Voltage T_{MIN} to T_{MAX}			±10	mV	
Reference Temperature Coefficient			25	ppm/°C	
		3		ppm/°C	
Reference Output Impedance		7		Ω	
LOGIC INPUTS					
Input High Voltage, V_{INH}	2.4			V	
Input Low Voltage, V_{INL}			0.8	V	V_{CC} = 4.75 V to 5.25 V
			0.4	V	V_{CC} = 2.7 to 3.6 V
Input Current, I_{IN}			±1	µA	V_{IN} = 0 V or V_{DRIVE}
Input Capacitance, C_{IN}[3]		10		pF	
LOGIC OUTPUTS					
Output High Voltage, V_{OH}	V_{DRIVE} – 0.2 V			V	I_{SOURCE} = 200 µA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 µA
Floating-State Leakage Current			±1	µA	
Floating-State Output Capacitance[3]		5		pF	
Output Coding	Straight natural binary				Coding bit set to 1 in control register
	Twos complement				Coding bit set to 0 in control register
CONVERSION RATE					
Conversion Time			1.6	µs	16 SCLK cycles with SCLK = 10 MHz
Track-and-Hold Acquisition Time[2, 3]			305	ns	Full-scale step input; see the Terminology section
Throughput Rate			500	kSPS	See the Serial Interface section
POWER REQUIREMENTS					Digital inputs = 0 V or V_{DRIVE}
V_{DD}	12		16.5	V	See Table 6
V_{SS}	−12		−16.5	V	See Table 6
V_{CC}	2.7		5.25	V	See Table 6
V_{DRIVE}	2.7		5.25	V	
Normal Mode (Static)		0.9		mA	V_{DD}/V_{SS} = ±16.5 V, V_{CC}/V_{DRIVE} = 5.25 V
Normal Mode (Operational)					f_{SAMPLE} = 500 kSPS
I_{DD}			180	µA	V_{DD} = 16.5 V
I_{SS}			205	µA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			2.2	mA	V_{CC}/V_{DRIVE} = 5.25 V
Autostandby Mode (Dynamic)					f_{SAMPLE} = 250 kSPS
I_{DD}			100	µA	V_{DD} = 16.5 V
I_{SS}			110	µA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			0.75	mA	V_{CC}/V_{DRIVE} = 5.25 V

Parameter[1]	B Version Min	Typ	Max	Unit	Test Conditions/Comments
Autoshutdown Mode (Static)					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V
Full Shutdown Mode					SCLK on or off
I_{DD}			1	μA	V_{DD} = 16.5 V
I_{SS}			1	μA	V_{SS} = −16.5 V
I_{CC} and I_{DRIVE}			1	μA	V_{CC}/V_{DRIVE} = 5.25 V
POWER DISSIPATION					
Normal Mode (Operational)			18	mW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V
Full Shutdown Mode			38.25	μW	V_{DD} = +16.5 V, V_{SS} = −16.5 V, V_{CC} = +5.25 V

[1] Temperature range is −40°C to +85°C.
[2] See the Terminology section.
[3] Sample tested during initial release to ensure compliance.
[4] For dc accuracy specifications, the LSB size for differential mode is FSR/8192. For single-ended mode/pseudo differential mode, the LSB size is FSR/4096, unless otherwise noted.
[5] Unipolar 0 V to 10 V range with straight binary output coding.
[6] Bipolar range with twos complement output coding.

TIMING SPECIFICATIONS

V_{DD} = 12 V to 16.5 V, V_{SS} = −12 V to −16.5 V, V_{CC} = 2.7 V to 5.25 V, V_{DRIVE} = 2.7 V to 5.25 V, V_{REF} = 2.5 V to 3.0 V internal/external, T_A = T_{MAX} to T_{MIN}. Timing specifications apply with a 32 pF load, unless otherwise noted.[1]

Table 3.

	Limit at T_{MIN}, T_{MAX}			Description
Parameter	**V_{CC} < 4.75 V**	**V_{CC} = 4.75 V to 5.25 V**	**Unit**	**$V_{DRIVE} \le V_{CC}$**
f_{SCLK}	50	50	kHz min	
	10	10	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}	16 × t_{SCLK}	ns max	$t_{SCLK} = 1/f_{SCLK}$
t_{QUIET}	75	60	ns min	Minimum time between end of serial read and next falling edge of $\overline{CS}$
t_1	12	5	ns min	Minimum $\overline{CS}$ pulse width
t_2[2]	25	20	ns min	$\overline{CS}$ to SCLK set-up time; bipolar input ranges (±10 V, ±5 V, ±2.5 V)
	45	35	ns min	Unipolar input range (0 V to 10 V)
t_3	26	14	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4	57	43	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	13	8	ns min	SCLK to data valid hold time
t_8	40	22	ns max	SCLK falling edge to DOUT high impedance
	10	9	ns min	SCLK falling edge to DOUT high impedance
t_9	4	4	ns min	DIN set-up time prior to SCLK falling edge
t_{10}	2	2	ns min	DIN hold time after SCLK falling edge
$t_{POWER-UP}$	750	750	ns max	Power-up from autostandby
	500	500	µs max	Power-up from full shutdown/autoshutdown mode, internal reference
	25	25	µs typ	Power-up from full shutdown/autoshutdown mode, external reference

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DRIVE}) and timed from a voltage level of 1.6 V.
[2] When using the 0 V to 10 V unipolar range, running at 500 kSPS throughput rate with t_2 at 20 ns, the mark space ratio needs to be limited to 50:50.

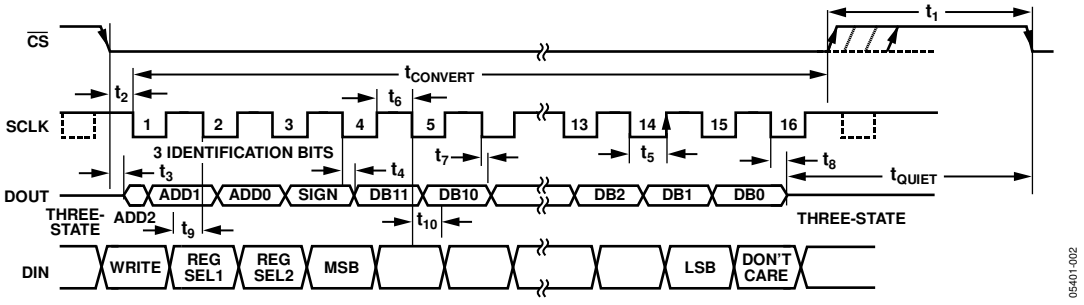

Figure 2. Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to AGND, DGND	−0.3 V to +16.5 V
V_{SS} to AGND, DGND	+0.3 V to −16.5 V
V_{DD} to V_{CC}	V_{CC} − 0.3 V to 16.5 V
V_{CC} to AGND, DGND	−0.3 V to +7 V
V_{DRIVE} to AGND, DGND	−0.3 V to +7 V
AGND to DGND	−0.3 V to +0.3 V
Analog Input Voltage to AGND[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Input Voltage to DGND	−0.3 V to +7 V
Digital Output Voltage to GND	−0.3 V to V_{DRIVE} + 0.3 V
REFIN to AGND	−0.3 V to V_{CC} + 0.3 V
Input Current to Any Pin Except Supplies[2]	±10 mA
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	143°C/W
θ_{JC} Thermal Impedance	45°C/W
Pb-Free Temperature, Soldering Reflow	260(0)°C
ESD	2.5 kV

[1] If the analog inputs are driven from alternative V_{DD} and V_{SS} supply circuitry, Schottky diodes should be placed in series with the AD7327 V_{DD} and V_{SS} supplies. See Power Supply Configuration section.

[2] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

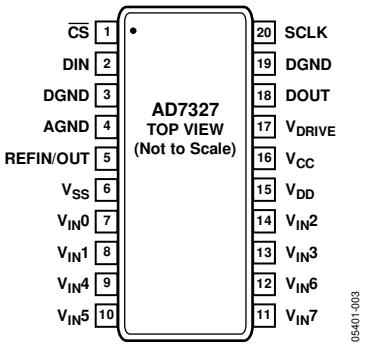

Figure 3. TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{CS}$	Chip Select. Active low logic input. This input provides the dual function of initiating conversions on the AD7327 and frames the serial data transfer.
2	DIN	Data In. Data to be written to the on-chip registers is provided on this input and is clocked into the AD7327 on the falling edge of SCLK (see the Registers section).
3, 19	DGND	Digital Ground. Ground reference point for all digital circuitry on the AD7327. The DGND and AGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
4	AGND	Analog Ground. Ground reference point for all analog circuitry on the AD7327. All analog input signals and any external reference signal should be referred to this AGND voltage. The AGND and DGND voltages ideally should be at the same potential and must not be more than 0.3 V apart, even on a transient basis.
5	REFIN/OUT	Reference Input/Reference Output. The on-chip reference is available on this pin for external use to the AD7327. The nominal internal reference voltage is 2.5 V, which appears at this pin. A 680 nF capacitor should be placed on the reference pin (see the Reference section). Alternatively, the internal reference can be disabled and an external reference applied to this input. On power-up, the external reference mode is the default condition.
6	V_{SS}	Negative Power Supply Voltage. This is the negative supply voltage for the analog input section.
7, 8, 14, 13, 9, 10, 12, 11	$V_{IN}0$ to $V_{IN}7$	Analog Input 0 to Analog Input 7. The analog inputs are multiplexed into the on-chip track-and-hold. The analog input channel for conversion is selected by programming the channel address Bit ADD2 through Bit ADD0 in the control register. The inputs can be configured as eight single-ended inputs, four true differential input pairs, four pseudo differential inputs, or seven pseudo differential inputs. The configuration of the analog inputs is selected by programming the mode bits, Bit Mode 1 and Bit Mode 0, in the control register. The input range on each input channel is controlled by programming the range registers. Input ranges of ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V can be selected on each analog input channel when a +2.5 V reference voltage is used (see the Registers section).
15	V_{DD}	Positive Power Supply Voltage. This is the positive supply voltage for the analog input section.
16	V_{CC}	Analog Supply Voltage, 2.7 V to 5.25 V. This is the supply voltage for the ADC core on the AD7327. This supply should be decoupled to AGND.
17	V_{DRIVE}	Logic Power Supply Input. The voltage supplied at this pin determines at what voltage the interface operates. This pin should be decoupled to DGND. The voltage at this pin may be different to that at V_{CC}, but it should not exceed V_{CC} by more than 0.3 V.
18	DOUT	Serial Data Output. The conversion output data is supplied to this pin as a serial data stream. The bits are clocked out on the falling edge of the SCLK input, and 16 SCLKs are required to access the data. The data stream consists of three channel identification bits, the sign bit, and 12 bits of conversion data. The data is provided MSB first (see the Serial Interface section).
20	SCLK	Serial Clock, Logic Input. A serial clock input provides the SCLK used for accessing the data from the AD7327. This clock is also used as the clock source for the conversion process.

TYPICAL PERFORMANCE CHARACTERISTICS

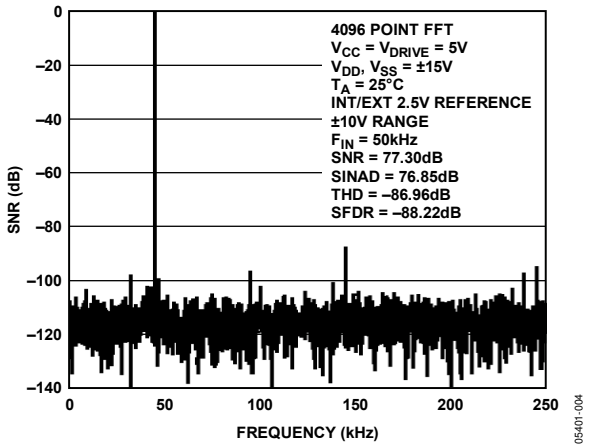

Figure 4. FFT True Differential Mode

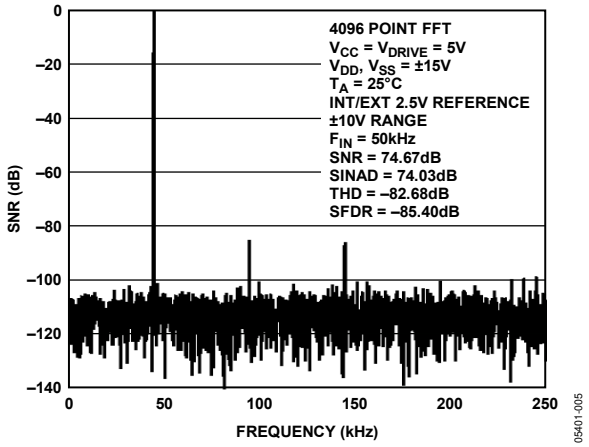

Figure 5. FFT Single-Ended Mode

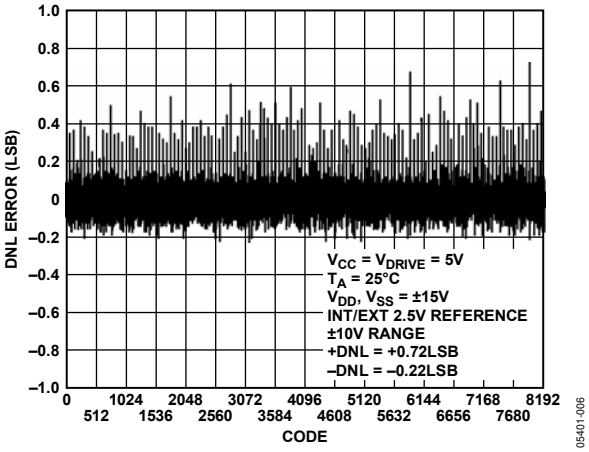

Figure 6. Typical DNL True Differential Mode

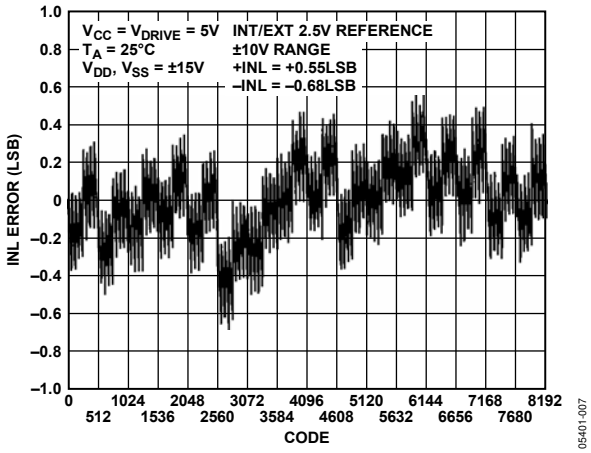

Figure 7. Typical INL True Differential Mode

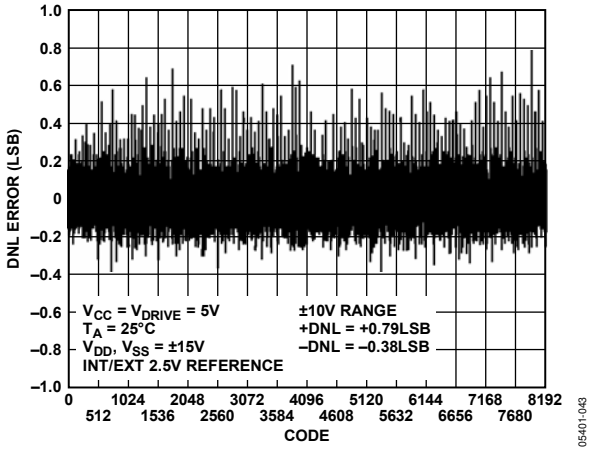

Figure 8. Typical DNL Single-Ended Mode

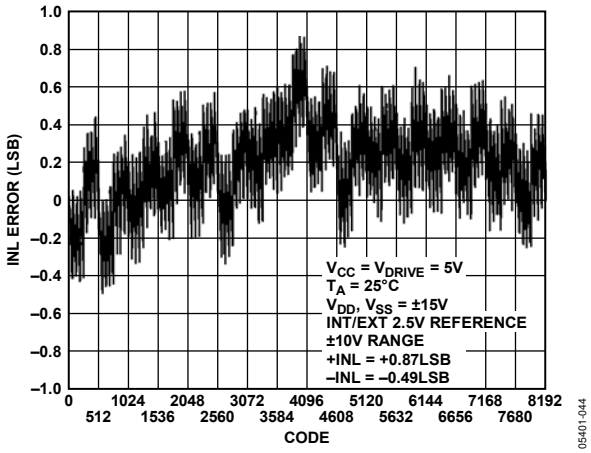

Figure 9. Typical INL Single-Ended Mode

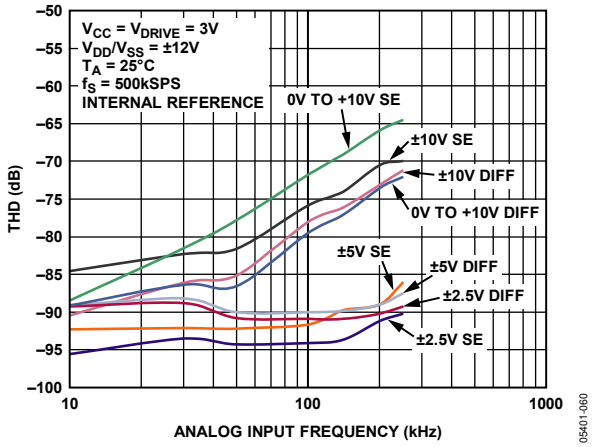

Figure 10. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 3 V V_{CC}

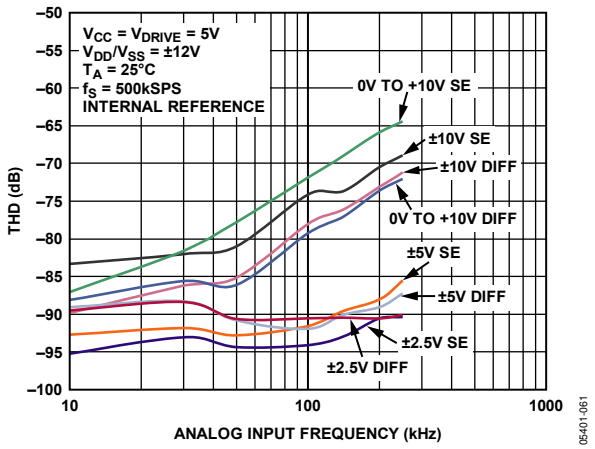

Figure 11. THD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 5 V V_{CC}

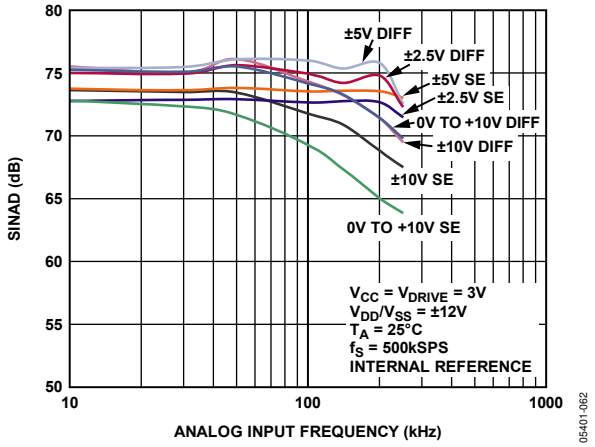

Figure 12. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 3 V V_{CC}

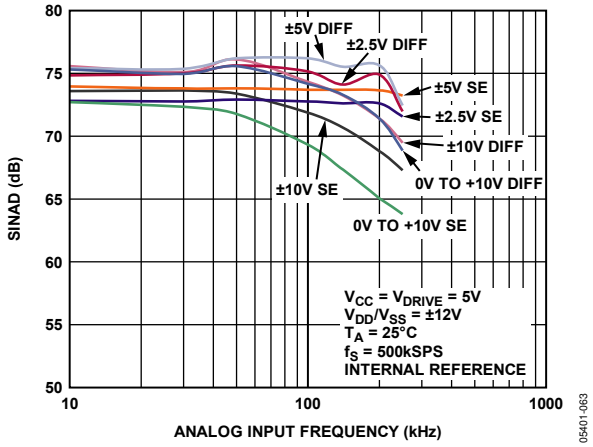

Figure 13. SINAD vs. Analog Input Frequency for Single-Ended (SE) and True Differential Mode (Diff) at 5 V V_{CC}

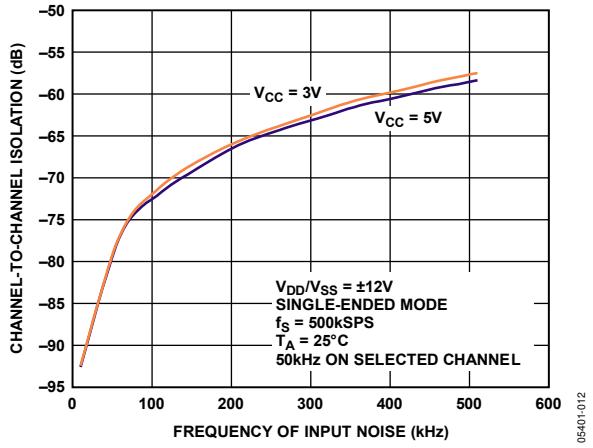

Figure 14. Channel-to-Channel Isolation

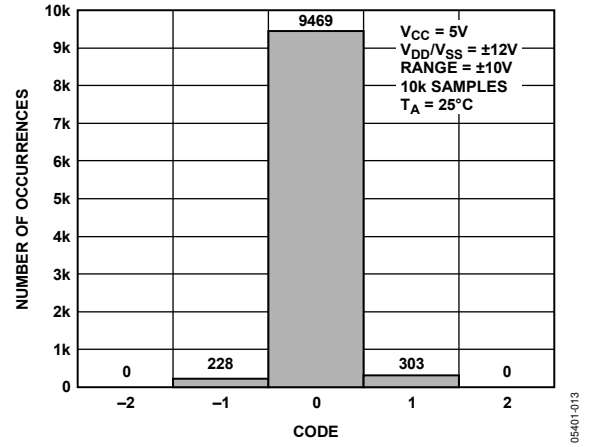

Figure 15. Histogram of Codes, True Differential Mode

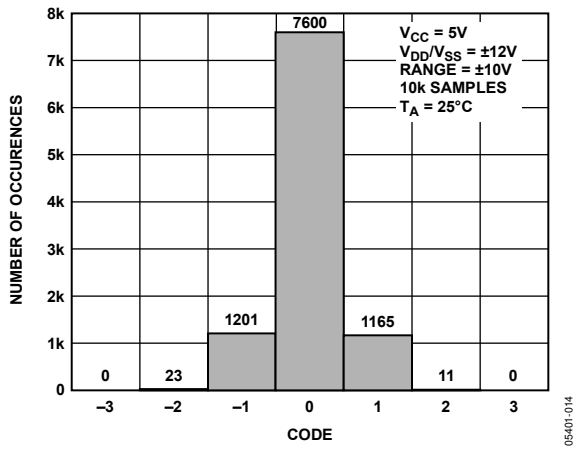

Figure 16. Histogram of Codes, Single-Ended Mode

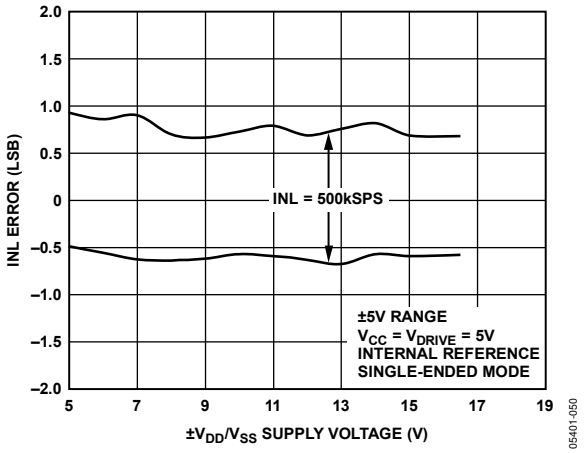

Figure 19. INL Error vs. Supply Voltage at 500 kSPS

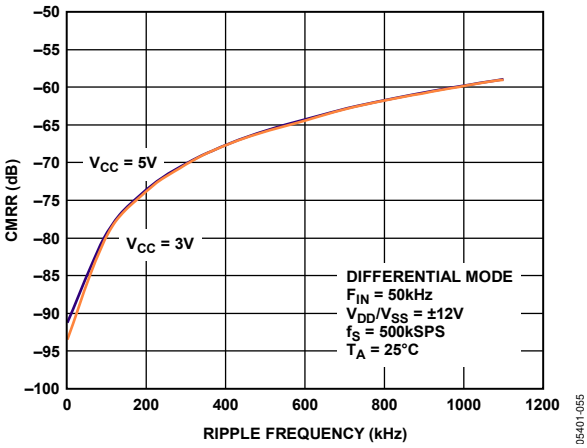

Figure 17. CMRR vs. Common-Mode Ripple Frequency

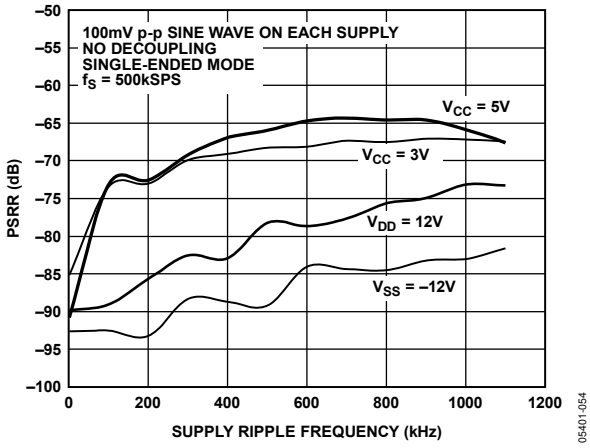

Figure 20. PSRR vs. Supply Ripple Frequency Without Supply Decoupling

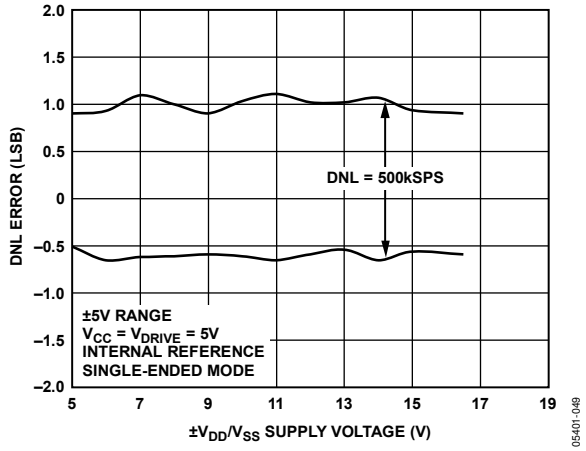

Figure 18. DNL Error vs. Supply Voltage at 500 kSPS

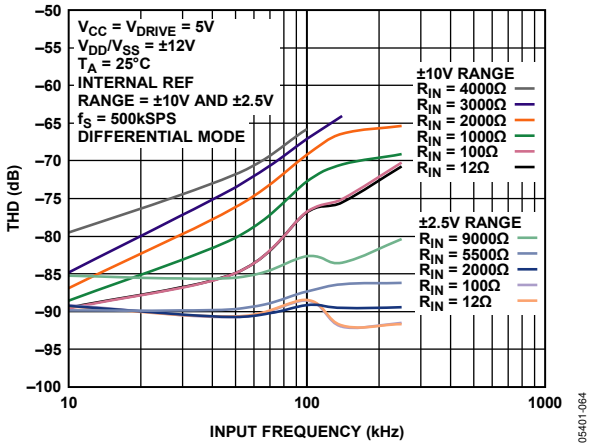

Figure 21. THD vs. Analog Input Frequency for Various Source Impedances, True Differential Mode

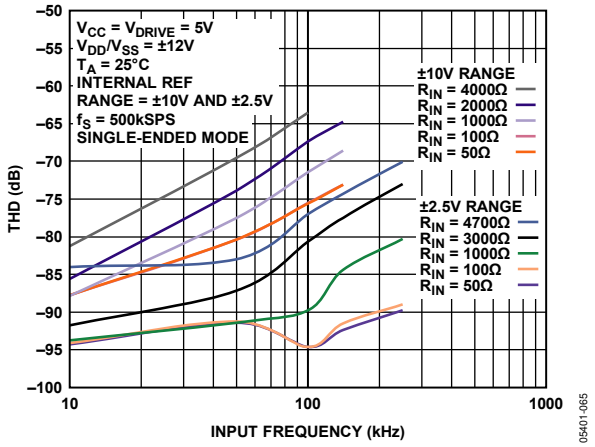

Figure 22. THD vs. Analog Input Frequency for Various Source Impedances, Single-Ended Mode

TERMINOLOGY

Differential Nonlinearity
This is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Integral Nonlinearity
This is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale (a point 1 LSB below the first code transition) and full scale (a point 1 LSB above the last code transition).

Offset Code Error
This applies to straight binary output coding. It is the deviation of the first code transition (00 ... 000) to (00 ... 001) from the ideal, that is, AGND + 1 LSB.

Offset Error Match
This is the difference in offset error between any two input channels.

Gain Error
This applies to straight binary output coding. It is the deviation of the last code transition (111 ... 110) to (111 ... 111) from the ideal (that is, $4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the offset error.

Gain Error Match
This is the difference in gain error between any two input channels.

Bipolar Zero Code Error
This applies when using twos complement output coding and a bipolar analog input. It is the deviation of the midscale transition (all 1s to all 0s) from the ideal input voltage, that is, AGND − 1 LSB.

Bipolar Zero Code Error Match
This refers to the difference in bipolar zero code error between any two input channels.

Positive Full-Scale Error
This applies when using twos complement output coding and any of the bipolar analog input ranges. It is the deviation of the last code transition (011…110) to (011…111) from the ideal ($4 \times V_{REF} - 1$ LSB, $2 \times V_{REF} - 1$ LSB, $V_{REF} - 1$ LSB) after adjusting for the bipolar zero code error.

Positive Full-Scale Error Match
This is the difference in positive full-scale error between any two input channels.

Negative Full-Scale Error
This applies when using twos complement output coding and any of the bipolar analog input ranges. This is the deviation of the first code transition (10 ... 000) to (10 ... 001) from the ideal (that is, $-4 \times V_{REF} + 1$ LSB, $-2 \times V_{REF} + 1$ LSB, $-V_{REF} + 1$ LSB) after adjusting for the bipolar zero code error.

Negative Full-Scale Error Match
This is the difference in negative full-scale error between any two input channels.

Track-and-Hold Acquisition Time
The track-and-hold amplifier returns into track mode after the 14th SCLK rising edge. Track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±½ LSB, after the end of a conversion. For the ±2.5 V range, the specified acquisition time is the time required for the track-and-hold amplifier to settle to within ±1 LSB.

Signal to (Noise + Distortion) Ratio
This is the measured ratio of signal to (noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all non-fundamental signals up to half the sampling frequency ($f_S/2$), excluding dc. The ratio is dependent on the number of quantization levels in the digitization process. The more levels, the smaller the quantization noise. Theoretically, the signal to (noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$Signal\ to\ (Noise + Distortion) = (6.02\ N + 1.76)\ \text{dB}$$

For a 13-bit converter, this is 80.02 dB.

Total Harmonic Distortion
Total harmonic distortion (THD) is the ratio of the rms sum of harmonics to the fundamental. For the AD7327, it is defined as

$$THD(\text{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where V_1 is the rms amplitude of the fundamental, and V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second through the sixth harmonics.

Peak Harmonic or Spurious Noise
Peak harmonic or spurious noise is defined as the ratio of the rms value of the next largest component in the ADC output spectrum (up to $f_S/2$, excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, the largest harmonic could be a noise peak.

Channel-to-Channel Isolation
Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 100 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 50 kHz signal. Figure 14 shows the worst-case across all eight channels for the AD7327. The analog input range is programmed to be the same on all channels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), whereas the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7327 is tested using the CCIF standard where two input frequencies near the top end of the input bandwidth are used. In this case, the second-order terms are usually distanced in frequency from the original sine waves, whereas the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

PSR (Power Supply Rejection)
Variations in power supply affect the full-scale transition but not the linearity of the converter. Power supply rejection is the maximum change in the full-scale transition point due to a change in power supply voltage from the nominal value (see the Typical Performance Characteristics section).

CMRR (Common-Mode Rejection Ratio)
CMRR is defined as the ratio of the power in the ADC output at full-scale frequency, f, to the power of a 100 mV sine wave applied to the common-mode voltage of the $V_{IN}+$ and $V_{IN}-$ frequency, f_S, as

$$CMRR\ (\text{dB}) = 10 \log (Pf/Pf_S)$$

where Pf is the power at frequency f in the ADC output, and Pf_S is the power at frequency f_S in the ADC output (see Figure 17).

THEORY OF OPERATION

CIRCUIT INFORMATION

The AD7327 is a fast, 8-channel, 12-bit plus sign, bipolar input, serial ADC. The AD7327 can accept bipolar input ranges that include ±10 V, ±5 V, and ±2.5 V; it can also accept a 0 V to +10 V unipolar input range. A different analog input range can be programmed on each analog input channel via the on-chip registers. The AD7327 has a high speed serial interface that can operate at throughput rates up to 500 kSPS.

The AD7327 requires V_{DD} and V_{SS} dual supplies for the high voltage analog input structures. These supplies must be equal to or greater than the analog input range. See Table 6 for the requirements of these supplies for each analog input range. The AD7327 requires a low voltage 2.7 V to 5.25 V V_{CC} supply to power the ADC core.

Table 6. Reference and Supply Requirements for Each Analog Input Range

Selected Analog Input Range (V)	Reference Voltage (V)	Full-Scale Input Range (V)	AV_{CC} (V)	Minimum V_{DD}/V_{SS} (V)[1]
±10	2.5	±10	3/5	±10
	3.0	±12	3/5	±12
± 5	2.5	±5	3/5	±5
	3.0	±6	3/5	±6
±2.5	2.5	±2.5	3/5	±5
	3.0	±3	3/5	±5
0 to +10	2.5	0 to +10	3/5	+10/AGND
	3.0	0 to +12	3/5	+12/AGND

[1] Guaranteed performance for V_{DD} = 12 V to 16.5 V and V_{SS} = −12 V to −16.5 V.

The performance specifications are guaranteed for V_{DD} = 12 V to 16.5 V and V_{SS} = −12 V to −16.5 V. With V_{DD} and V_{SS} supplies outside this range, the AD7327 is fully functional but performance is not guaranteed. It may be necessary to decrease the throughput rate when the AD7327 is configured with the minimum V_{DD} and V_{SS} supplies to meet the performance specifications (see the Typical Performance Characteristics section). Figure 31 shows the change in THD as the V_{DD} and V_{SS} supplies are reduced. For ac performance at the maximum throughput rate, the THD degrades slightly as V_{DD} and V_{SS} are reduced. It might, therefore, be necessary to reduce the throughput rate when using minimum V_{DD} and V_{SS} supplies so that there is less degradation of THD and the specified performance can be maintained. The degradation is due to an increase in the on resistance of the input multiplexer when the V_{DD} and V_{SS} supplies are reduced. Figure 18 and Figure 19 show the change in INL and DNL as the V_{DD} and V_{SS} voltages are varied. For dc performance when operating at the maximum throughput rate, as the V_{DD} and V_{SS} supply voltages are reduced, the typical INL and DNL error remains constant.

The analog inputs can be configured as eight single-ended inputs, four true differential inputs, four pseudo differential inputs, or seven pseudo differential inputs. Selection can be made by programming the mode bits, Mode 0 and Mode 1, in the control register.

The serial clock input accesses data from the part and provides the clock source for the successive approximation ADC. The AD7327 has an on-chip 2.5 V reference; however, the AD7327 can also work with an external reference. On power-up, the external reference operation is the default option. If the internal reference is the preferred option, the user must write to the reference bit in the control register to select the internal reference operation.

The AD7327 also features power-down options to allow power savings between conversions. The power-down modes are selected by programming the on-chip control register, as described in the Modes of Operation section.

CONVERTER OPERATION

The AD7327 is a successive approximation ADC built around two capacitive DACs. Figure 23 and Figure 24 show simplified schematics of the ADC in single-ended mode during the acquisition and conversion phases, respectively. Figure 25 and Figure 26 show simplified schematics of the ADC in differential mode during acquisition and conversion phases, respectively. The ADC is composed of control logic, a SAR, and capacitive DACs. In Figure 23 (the acquisition phase), SW2 is closed and SW1 is in Position A, the comparator is held in a balanced condition, and the sampling capacitor array acquires the signal on the input.

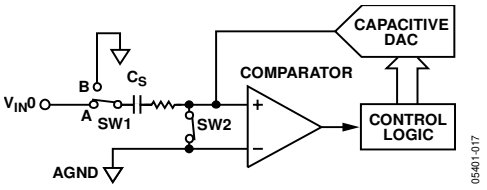

Figure 23. ADC Acquisition Phase (Single-Ended)

When the ADC starts a conversion (Figure 24), SW2 opens and SW1 moves to Position B, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the capacitive DAC to bring the comparator back into a balanced condition. When the comparator is rebalanced, the conversion is complete. The control logic generates the ADC output code.

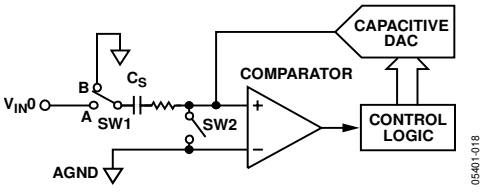

Figure 24. ADC Conversion Phase (Single-Ended)

Figure 25 shows the differential configuration during the acquisition phase. For the conversion phase, SW3 opens and SW1 and SW2 move to Position B (see Figure 26). The output impedances of the source driving the $V_{IN}+$ and $V_{IN}-$ pins must match; otherwise, the two inputs have different settling times, resulting in errors.

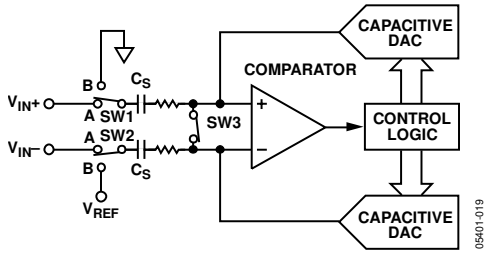

Figure 25. ADC Differential Configuration During Acquisition Phase

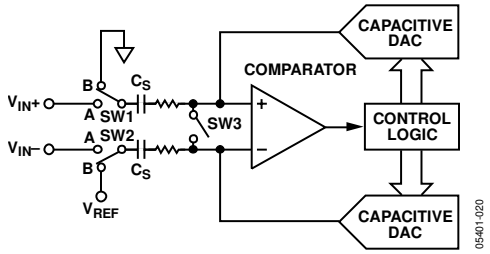

Figure 26. ADC Differential Configuration During Conversion Phase

Output Coding

The AD7327 default output coding is set to twos complement. The output coding is controlled by the coding bit in the control register. To change the output coding to straight binary coding, the coding bit in the control register must be set. When operating in sequence mode, the output coding for each channel in the sequence is the value written to the coding bit during the last write to the control register.

Transfer Functions

The designed code transitions occur at successive integer LSB values (that is, 1 LSB, 2 LSB, and so on). The LSB size is dependent on the analog input range selected.

Table 7. LSB Sizes for Each Analog Input Range

Input Range	Full-Scale Range/8192 Codes	LSB Size
±10 V	20 V	2.441 mV
±5 V	10 V	1.22 mV
±2.5 V	5 V	0.61 mV
0 V to +10 V	10 V	1.22 mV

The ideal transfer characteristic for the AD7327 when twos complement coding is selected is shown in Figure 27. The ideal transfer characteristic for the AD7327 when straight binary coding is selected is shown in Figure 28.

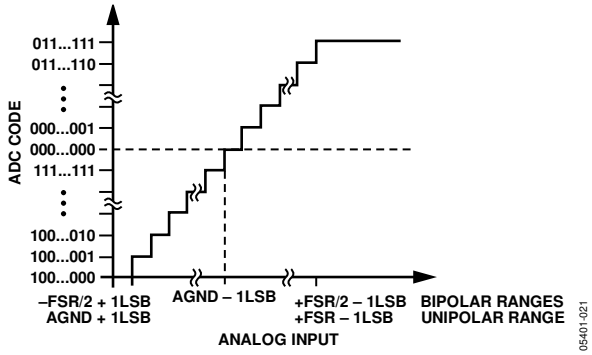

Figure 27. Twos Complement Transfer Characteristic

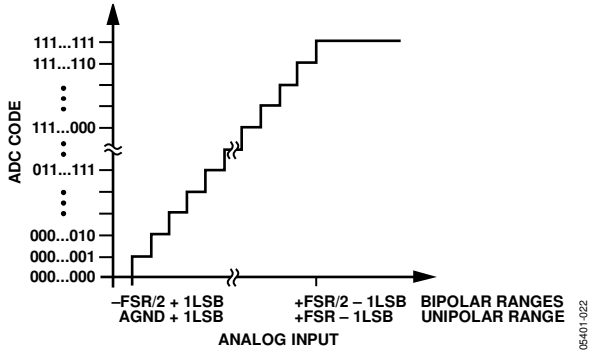

Figure 28. Straight Binary Transfer Characteristic

ANALOG INPUT STRUCTURE

The analog inputs of the AD7327 can be configured as single-ended, true differential, or pseudo differential via the control register mode bits (see Table 9). The AD7327 can accept true bipolar input signals. On power-up, the analog inputs operate as eight single-ended analog input channels. If true differential or pseudo differential is required, a write to the control register is necessary after power-up to change this configuration.

Figure 29 shows the equivalent analog input circuit of the AD7327 in single-ended mode. Figure 30 shows the equivalent analog input structure in differential mode. The two diodes provide ESD protection for the analog inputs.

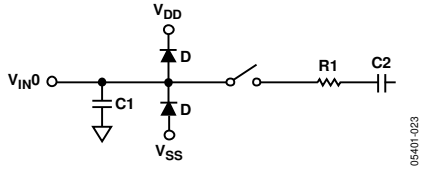

Figure 29. Equivalent Analog Input Circuit (Single-Ended)

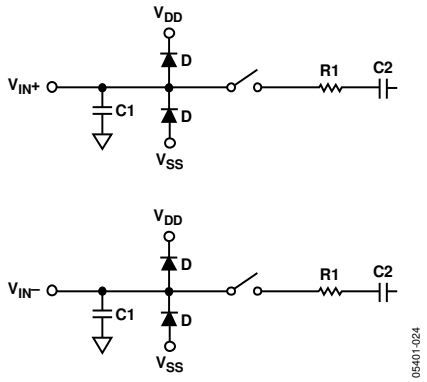

Figure 30. Equivalent Analog Input Circuit (Differential)

Care should be taken to ensure that the analog input does not exceed the V_{DD} and V_{SS} supply rails by more than 300 mV. Exceeding this value causes the diodes to become forward biased and to start conducting into either the V_{DD} supply rail or V_{SS} supply rail. These diodes can conduct up to 10 mA without causing irreversible damage to the part.

In Figure 29 and Figure 30, Capacitor C1 is typically 4 pF and can primarily be attributed to pin capacitance. Resistor R1 is a lumped component made up of the on resistance of the input multiplexer and the track-and-hold switch. Capacitor C2 is the sampling capacitor; its capacitance varies depending on the analog input range selected (see the Specifications section).

Track-and-Hold Section

The track-and-hold on the analog input of the AD7327 allows the ADC to accurately convert an input sine wave of full-scale amplitude to 13-bit accuracy. The input bandwidth of the track-and-hold is greater than the Nyquist rate of the ADC. The AD7327 can handle frequencies up to 22 MHz.

The track-and-hold enters its tracking mode on the 14th SCLK rising edge after the $\overline{CS}$ falling edge. The time required to acquire an input signal depends on how quickly the sampling capacitor is charged. With 0 source impedance, 305 ns is sufficient to acquire the signal to the 13-bit level. The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 10 \times ((R_{SOURCE} + R) \times C)$$

where C is the sampling capacitance, and R is the resistance seen by the track-and-hold amplifier looking back on the input.

For the AD7327, the value of R includes the on resistance of the input multiplexer and is typically 300 Ω. R_{SOURCE} should include any extra source impedance on the analog input.

The AD7327 enters track on the 14th SCLK rising edge. When running the AD7327 at a throughput rate of 500 kSPS with a 10 MHz SCLK signal, the ADC has approximately

$$1.5 \text{ SCLK} + t_8 + t_{QUIET}$$

to acquire the analog input signal. The ADC goes back into hold mode on the $\overline{CS}$ falling edge.

As the V_{DD}/V_{SS} supply voltage is reduced, the on resistance of the input multiplexer increases. Therefore, based on the equation for t_{ACQ}, it is necessary to increase the amount of acquisition time provided to the AD7327, and, therefore, decrease the overall throughput rate. Figure 31 shows that as the V_{DD} and V_{SS} supplies are reduced, the specified THD performance degrades slightly. If the throughput rate is reduced when operating with the minimum V_{DD} and V_{SS} supplies, the specified THD performance is maintained.

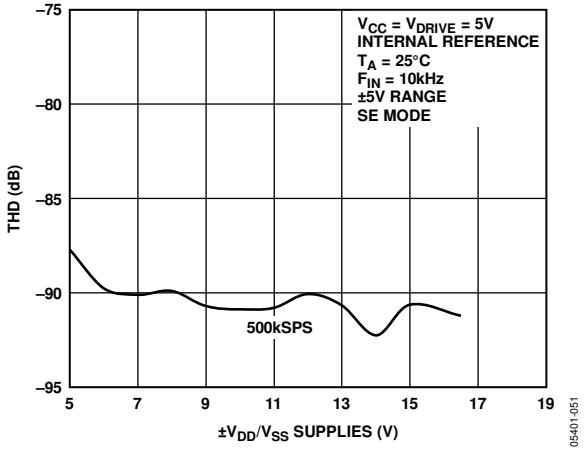

Figure 31. THD vs. ±V_{DD}/V_{SS} Supply Voltage at 500 kSPS

Unlike other bipolar ADCs, the AD7327 does not have a resistive analog input structure. On the AD7327, the bipolar analog signal is sampled directly onto the sampling capacitor. This gives the AD7327 high analog input impedance. An approximation for the analog input impedance can be calculated from the following formula:

$$Z = 1/(f_S \times C_S)$$

where f_S is the sampling frequency, and C_S is the sampling capacitor value.

C_S depends on the analog input range chosen (see the Specifications section). When operating at 500 kSPS, the analog input impedance is typically 145 kΩ for the ±10 V range. As the sampling frequency is reduced, the analog input impedance further increases. As the analog input impedance increases, the current required to drive the analog input, therefore, decreases.

TYPICAL CONNECTION DIAGRAM

Figure 32 shows a typical connection diagram for the AD7327. In this configuration, the AGND pin is connected to the analog ground plane of the system, and the DGND pin is connected to the digital ground plane of the system. The analog inputs on the AD7327 can be configured to operate in single-ended, true differential, or pseudo differential mode. The AD7327 can operate with either an internal or external reference. In Figure 32, the AD7327 is configured to operate with the internal 2.5 V reference. A 680 nF decoupling capacitor is required when operating with the internal reference.

The V_{CC} pin can be connected to either a 3 V supply voltage or a 5 V supply voltage. The V_{DD} and V_{SS} are the dual supplies for the high voltage analog input structures. The voltage on these pins must be equal to or greater than the highest analog input range selected on the analog input channels (see Table 6). The V_{DRIVE} pin is connected to the supply voltage of the microprocessor. The voltage applied to the V_{DRIVE} input controls the voltage of the serial interface. V_{DRIVE} can be set to 3 V or 5 V.

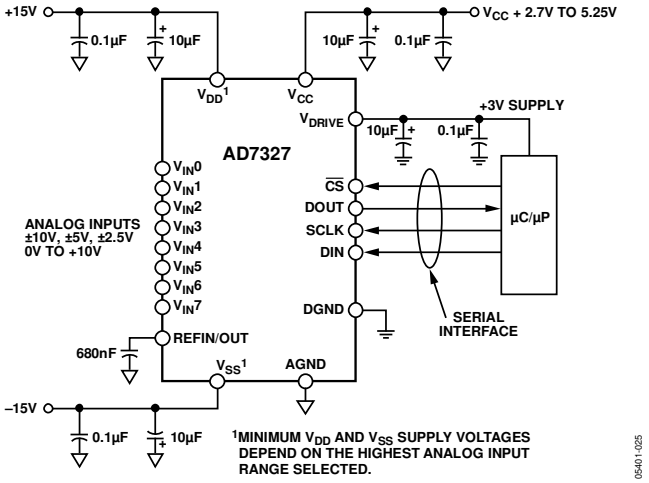

Figure 32. Typical Connection Diagram

ANALOG INPUT

Single-Ended Inputs

The AD7327 has a total of eight analog inputs when operating the AD7327 in single-ended mode. Each analog input can be independently programmed to one of the four analog input ranges. In applications where the signal source is high impedance, it is recommended to buffer the signal before applying it to the ADC analog inputs. Figure 33 shows the configuration of the AD7327 in single-ended mode.

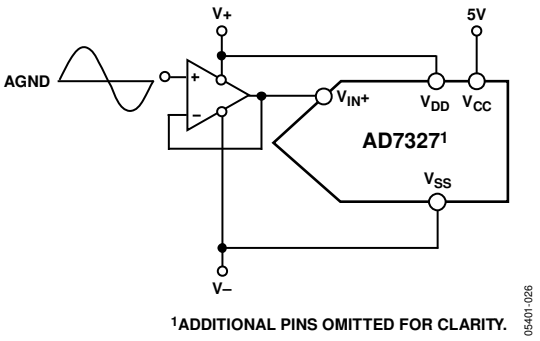

Figure 33. Single-Ended Mode Typical Connection Diagram

True Differential Mode

The AD7327 can have a total of four true differential analog input pairs. Differential signals have some benefits over single-ended signals, including better noise immunity based on the common-mode rejection of the device and improvements in distortion performance. Figure 34 defines the configuration of the true differential analog inputs of the AD7327.

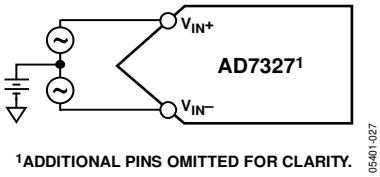

Figure 34. True Differential Inputs

The amplitude of the differential signal is the difference between the signals applied to the $V_{IN}+$ and $V_{IN}-$ pins in each differential pair ($V_{IN}+ - V_{IN}-$). $V_{IN}+$ and $V_{IN}-$ should be simultaneously driven by two signals each of amplitude $\pm 4 \times V_{REF}$ (depending on the input range selected) that are 180° out of phase. Assuming the $\pm 4 \times V_{REF}$ mode, the amplitude of the differential signal is −20 V to +20 V p-p ($2 \times 4 \times V_{REF}$), regardless of the common mode.

The common mode is the average of the two signals

$$(V_{IN}+ + V_{IN}-)/2$$

and is, therefore, the voltage on which the two input signals are centered.

This voltage is set up externally, and its range varies with reference voltage. As the reference voltage increases, the common-mode range decreases. When driving the differential inputs with an amplifier, the actual common-mode range is determined by the output swing of the amplifier. If the differential inputs are not driven from an amplifier, the common-mode range is determined by the supply voltage on the V_{DD} and the V_{SS} supply pins.

When a conversion takes place, the common mode is rejected, resulting in a noise-free signal of amplitude $-2 \times (4 \times V_{REF})$ to $+2 \times (4 \times V_{REF})$ corresponding to digital Code −4096 to Code +4095.

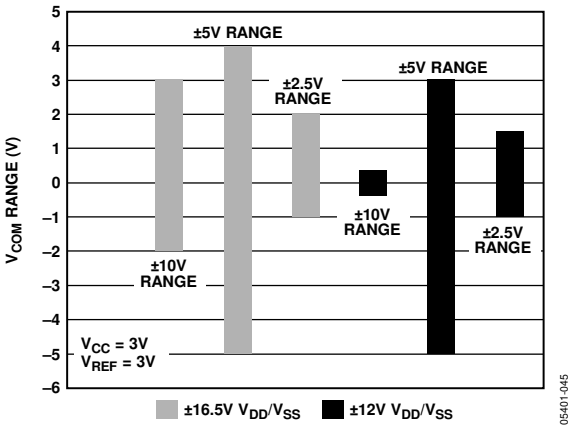

Figure 35. Common-Mode Range for V_{CC} = 3 V and REFIN/OUT = 3 V

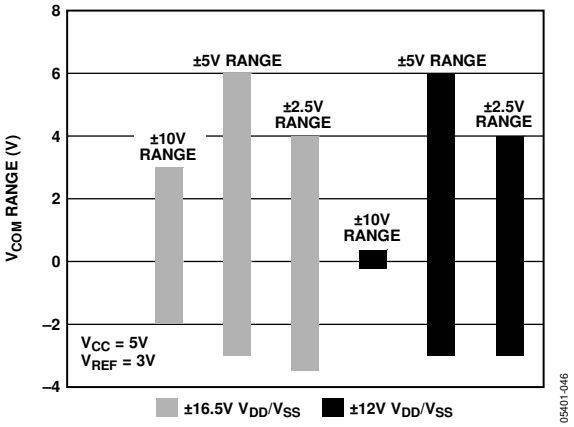

Figure 36. Common-Mode Range for V_{CC} = 5 V and REFIN/OUT = 3 V

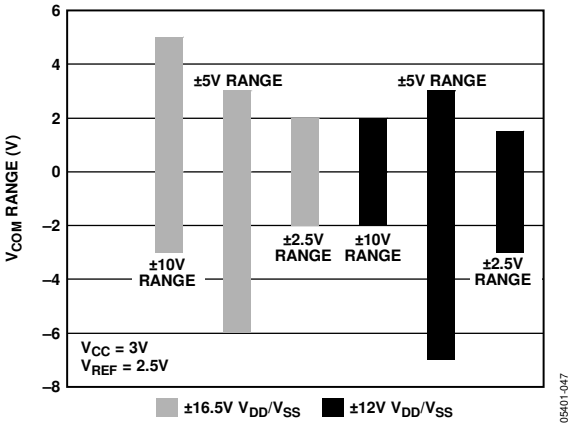

Figure 37. Common-Mode Range for V_{CC} = 3 V and REFIN/OUT = 2.5 V

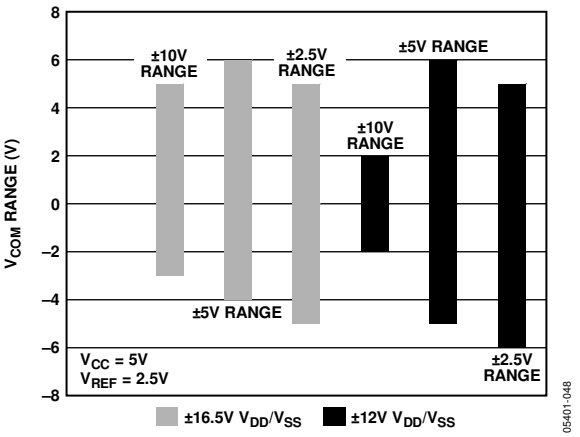

Figure 38. Common-Mode Range for V_{CC} = 5 V and REFIN/OUT = 2.5 V

Pseudo Differential Inputs

The AD7327 can have four pseudo differential pairs or seven pseudo differential inputs referenced to a common $V_{IN}-$ pin. The $V_{IN}+$ inputs are coupled to the signal source and must have an amplitude within the selected range for that channel as programmed in the range registers. A dc input is applied to the $V_{IN}-$ pin. The voltage applied to this input provides an offset for the $V_{IN}+$ input from ground or a pseudo ground. Pseudo differential inputs separate the analog input signal ground from the ADC ground, allowing cancellation of dc common mode voltages.

When a conversion takes place, the pseudo ground corresponds to Code −4096 and the maximum amplitude corresponds to Code +4095.

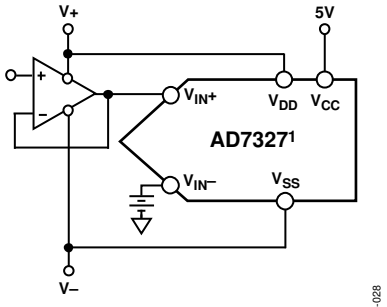

Figure 39. Pseudo Differential Inputs

Figure 40 and Figure 41 show the typical voltage range on the $V_{IN}-$ pin for the different analog input ranges when configured in the pseudo differential mode.

For example, when the AD7327 is configured to operate in pseudo differential mode and the ±5 V range is selected, with ±16.5 V V_{DD}/V_{SS} supplies and 5 V V_{CC}, the voltage on the $V_{IN}-$ pin can vary from −6.5 V to +6.5 V.

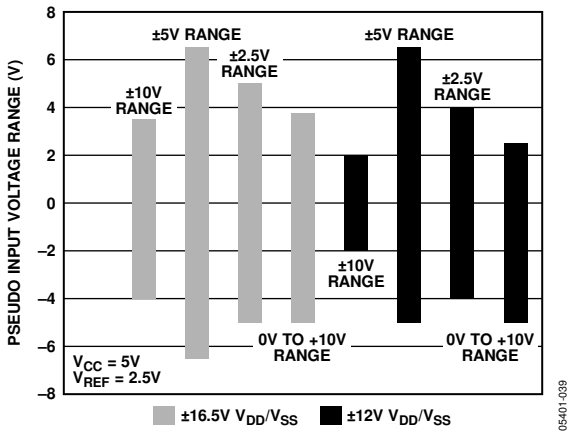

Figure 40. Pseudo Input Range with V_{CC} = 5 V

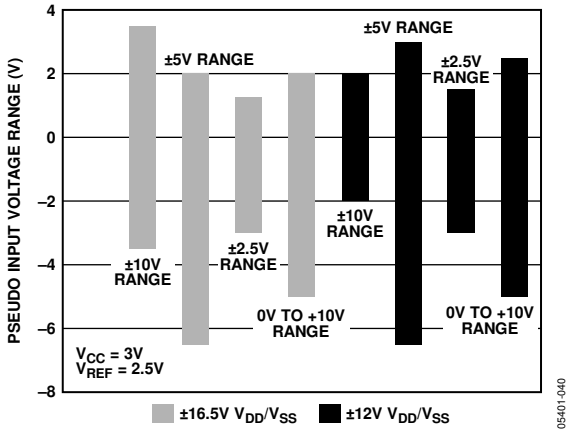

Figure 41. Pseudo Input Range with V_{CC} = 3 V

DRIVER AMPLIFIER CHOICE

In applications where the harmonic distortion and signal-to-noise ratio are critical specifications, the analog input of the AD7327 should be driven from a low impedance source. Large source impedances significantly affect the ac performance of the ADC and can necessitate the use of an input buffer amplifier.

When no amplifier is used to drive the analog input, the source impedance should be limited to low values. The maximum source impedance depends on the amount of THD that can be tolerated in the application. The THD increases as the source impedance increases and performance degrades. Figure 21 and Figure 22 show graphs of the THD vs. the analog input frequency for various source impedances. Depending on the input range and analog input configuration selected, the AD7327 can handle source impedances of up to 5.5 kΩ before the THD starts to degrade.

Due to the programmable nature of the analog inputs on the AD7327, the choice of op amp used to drive the inputs is a function of the particular application and depends on the input configuration and the analog input voltage ranges selected.

The driver amplifier must be able to settle for a full-scale step to a 13-bit level, 0.0122%, in less than the specified acquisition time of the AD7327. An op amp such as the AD8021 meets this requirement when operating in single-ended mode. The AD8021 needs an external compensating NPO type of capacitor. The AD8022 can also be used in high frequency applications where a dual version is required. For lower frequency applications, op amps such as the AD797, AD845, and AD8610 can be used with the AD7327 in single-ended mode configuration.

Differential operation requires that V_{IN}+ and V_{IN}− be simultaneously driven with two signals of equal amplitude that are 180° out of phase. The common mode must be set up externally to the AD7327. The common-mode range is determined by the REFIN/OUT voltage, the V_{CC} supply voltage, and the particular amplifier used to drive the analog inputs. Differential mode with either an ac input or a dc input provides the best THD performance over a wide frequency range. Because not all applications have a signal preconditioned for differential operation, there is often a need to perform the single-ended-to-differential conversion.

This single-ended-to-differential conversion can be performed using an op amp pair. Typical connection diagrams for an op amp pair are shown in Figure 42 and Figure 43. In Figure 42, the common-mode signal is applied to the noninverting input of the second amplifier.

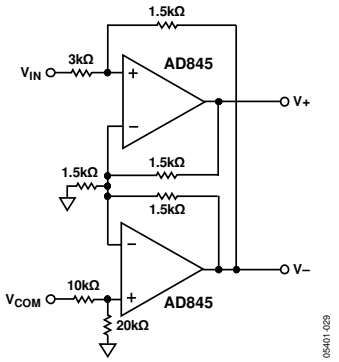

Figure 42. Single-Ended-to-Differential Configuration with the AD845

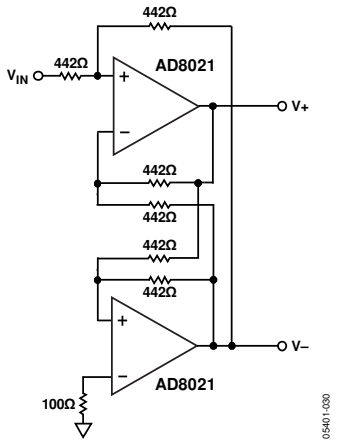

Figure 43. Single-Ended-to-Differential Configuration with the AD8021

REGISTERS

The AD7327 has four programmable registers: the control register, sequence register, Range Register 1, and Range Register 2. These registers are write-only registers.

ADDRESSING REGISTERS

A serial transfer on the AD7327 consists of 16 SCLK cycles. The three MSBs on the DIN line during the 16 SCLK transfer are decoded to determine which register is addressed. The three MSBs consist of the write bit, the Register Select 1 bit, and the Register Select 2 bit. The register select bits are used to determine which of the four on-board registers is selected. The write bit determines if the data on the DIN line following the register select bits loads into the addressed register. If the write bit is 1, the bits load into the register addressed by the register select bits. If the write bit is 0, the data on the DIN line does not load into any register.

Combinations of the write bit, the Register Select 1 bit, and the Register Select 2 bit other than those specified in Table 8 access registers for Analog Devices internal use only. Do not access these registers, as doing so may lead to unspecified operation of the device.

Table 8. Decoding Register Select Bits and Write Bit

Write	Register Select 1	Register Select 2	Description
0	0	0	Data on the DIN line during this serial transfer is ignored.
1	0	0	This combination selects the control register. The subsequent 12 bits are loaded into the control register.
1	0	1	This combination selects Range Register 1. The subsequent 8 bits are loaded into Range Register 1.
1	1	0	This combination selects Range Register 2. The subsequent 8 bits are loaded into Range Register 2.
1	1	1	This combination selects the sequence register. The subsequent 8 bits are loaded into the sequence register.

CONTROL REGISTER

The control register is used to select the analog input channel, analog input configuration, reference, coding, and power mode. The control register is a write-only, 12-bit register. Data loaded on the DIN line corresponds to the AD7327 configuration for the next conversion. If the sequence register is being used, data should be loaded into the control register after the range registers and the sequence register have been initialized. The bit functions of the control register are shown in Table 9 (the power-up status of all bits is 0).

MSB **LSB**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write	Register Select 1	Register Select 2	ADD2	ADD1	ADD0	Mode 1	Mode 0	PM1	PM0	Coding	Ref	Seq1	Seq2	ZERO	0

Table 9. Control Register Details

Bit	Mnemonic	Description
12, 11, 10	ADD2, ADD1, ADD0	These three channel address bits are used to select the analog input channel for the next conversion if the sequencer is not being used. If the sequencer is being used, the three channel address bits are used to select the final channel in a consecutive sequence.
9, 8	Mode 1, Mode 0	These two mode bits are used to select the configuration of the eight analog input pins, $V_{IN}0$ to $V_{IN}7$. These pins are used in conjunction with the channel address bits. On the AD7327, the analog inputs can be configured as eight single-ended inputs, four fully differential inputs, four pseudo differential inputs, or seven pseudo differential inputs (see Table 10).
7, 6	PM1, PM0	The power management bits are used to select different power mode options on the AD7327 (see Table 11).
5	Coding	This bit is used to select the type of output coding the AD7327 uses for the next conversion result. If coding = 0, the output coding is twos complement. If coding = 1, the output coding is straight binary. When operating in sequence mode, the output coding for each channel is the value written to the coding bit during the last write to the control register.
4	Ref	The reference bit is used to enable or disable the internal reference. If Ref = 0, the external reference is enabled and used for the next conversion and the internal reference is disabled. If Ref = 1, the internal reference is used for the next conversion. When operating in sequence mode, the reference used for each channel is the value written to the Ref bit during the last write to the control register.
3, 2	Seq1, Seq2	The Sequence 1 and Sequence 2 bits are used to control the operation of the sequencer (see Table 12).
1	ZERO	A 0 should be written to this bit at all times.

The eight analog input channels can be configured as seven pseudo differential analog inputs, four pseudo differential inputs, four true differential inputs, or eight single-ended analog inputs.

Table 10. Analog Input Configuration Selection

Channel Address Bits			Mode 1 = 1, Mode 0 = 1		Mode 1 = 1, Mode 0 = 0		Mode 1 = 0, Mode 0 =1		Mode 1 = 0, Mode 0 = 0	
			7 Pseudo Differential Inputs		4 Fully Differential Inputs		4 Pseudo Differential Inputs		8 Single-Ended Inputs	
ADD2	ADD1	ADD0	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$	$V_{IN}+$	$V_{IN}-$
0	0	0	$V_{IN}0$	$V_{IN}7$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	AGND
0	0	1	$V_{IN}1$	$V_{IN}7$	$V_{IN}0$	$V_{IN}1$	$V_{IN}0$	$V_{IN}1$	$V_{IN}1$	AGND
0	1	0	$V_{IN}2$	$V_{IN}7$	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	AGND
0	1	1	$V_{IN}3$	$V_{IN}7$	$V_{IN}2$	$V_{IN}3$	$V_{IN}2$	$V_{IN}3$	$V_{IN}3$	AGND
1	0	0	$V_{IN}4$	$V_{IN}7$	$V_{IN}4$	$V_{IN}5$	$V_{IN}4$	$V_{IN}5$	$V_{IN}4$	AGND
1	0	1	$V_{IN}5$	$V_{IN}7$	$V_{IN}4$	$V_{IN}5$	$V_{IN}4$	$V_{IN}5$	$V_{IN}5$	AGND
1	1	0	$V_{IN}6$	$V_{IN}7$	$V_{IN}6$	$V_{IN}7$	$V_{IN}6$	$V_{IN}7$	$V_{IN}6$	AGND
1	1	1	Temperature indicator		$V_{IN}6$	$V_{IN}7$	$V_{IN}6$	$V_{IN}7$	$V_{IN}7$	AGND

Table 11. Power Mode Selection

PM1	PM0	Description
1	1	Full Shutdown Mode. In this mode, all internal circuitry on the AD7327 is powered down. Information in the control register is retained when the AD7327 is in full shutdown mode.
1	0	Autoshutdown Mode. The AD7327 enters autoshutdown on the 15th SCLK rising edge when the control register is updated. All internal circuitry is powered down in autoshutdown.
0	1	Autostandby Mode. In this mode, all internal circuitry is powered down, excluding the internal reference. The AD7327 enters autostandby mode on the 15th SCLK rising edge after the control register is updated.
0	0	Normal Mode. All internal circuitry is powered up at all times.

Table 12. Sequencer Selection

Seq1	Seq2	Description
0	0	The channel sequencer is not used. The analog input channel, selected by programming the ADD2 bit to ADD0 bit in the control register, selects the next channel for conversion.
0	1	Uses the sequence of channels previously programmed into the sequence register for conversion. The AD7327 starts converting on the lowest channel in the sequence. The channels are converted in ascending order. If uninterrupted, the AD7327 keeps converting the sequence. The range for each channel defaults to the range previously written into the corresponding range register.
1	0	Used in conjunction with the channel address bits in the control register. This allows continuous conversions on a consecutive sequence of channels, from Channel 0 up to and including a final channel selected by the channel address bits in the control register. The range for each channel defaults to the range previously written into the corresponding range register.
1	1	The channel sequencer is not used. The analog channel, selected by programming the ADD2 bit to ADD0 bit in the control register, selects the next channel for conversion.

SEQUENCE REGISTER

The sequence register on the AD7327 is an 8-bit, write-only register. Each of the eight analog input channels has one corresponding bit in the sequence register. To select an analog input channel for inclusion in the sequence, set the corresponding channel bit to 1 in the sequence register.

MSB															LSB
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	$V_{IN}0$	$V_{IN}1$	$V_{IN}2$	$V_{IN}3$	$V_{IN}4$	$V_{IN}5$	$V_{IN}6$	$V_{IN}7$	0	0	0	0	0

RANGE REGISTERS

The range registers are used to select one analog input range per analog input channel. Range Register 1 is used to set the ranges for Channel 0 to Channel 3. It is an 8-bit, write-only register with two dedicated range bits for each of the analog input channels from Channel 0 to Channel 3. There are four analog input ranges, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. A write to Range Register 1 is selected by setting the write bit to 1 and the register select bits to 0 and 1. After the initial write to Range Register 1 occurs, each time an analog input is selected, the AD7327 automatically configures the analog input to the appropriate range, as indicated by Range Register 1. The ±10 V input range is selected by default on each analog input channel (see Table 13).

MSB **LSB**

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	$V_{IN}0A$	$V_{IN}0B$	$V_{IN}1A$	$V_{IN}1B$	$V_{IN}2A$	$V_{IN}2B$	$V_{IN}3A$	$V_{IN}3B$	0	0	0	0	0

Range Register 2 is used to set the ranges for Channel 4 to Channel 7. It is an 8-bit, write-only register with two dedicated range bits for each of the analog input channels from Channel 4 to Channel 7. There are four analog input ranges, ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. After the initial write to Range Register 2 occurs, each time an analog input is selected, the AD7327 automatically configures the analog input to the appropriate range, as indicated by Range Register 2. The ±10 V input range is selected by default on each analog input channel (see Table 13).

MSB **LSB**

16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Write	Register Select 1	Register Select 2	$V_{IN}4A$	$V_{IN}4B$	$V_{IN}5A$	$V_{IN}5B$	$V_{IN}6A$	$V_{IN}6B$	$V_{IN}7A$	$V_{IN}7B$	0	0	0	0	0

Table 13. Range Selection

V_{IN}xA	V_{IN}xB	Description
0	0	This combination selects the ±10 V input range on V_{IN}x.
0	1	This combination selects the ±5 V input range on V_{IN}x.
1	0	This combination selects the ±2.5 V input range on V_{IN}x.
1	1	This combination selects the 0 V to +10 V input range on V_{IN}x.