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AD7327/AD7328 Evaluation Board User Guide

UG-419

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Evaluating the AD7327/AD7328

FEATURES

Full-featured evaluation board for the AD7327/AD7328
PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
PC software for control and data analysis (time and frequency domain)
Standalone capability

EVAL-AD7327SDZ/EVAL-AD7328SDZ KIT CONTENTS

EVAL-AD7327SDZ/EVAL-AD7328SDZ evaluation board
Evaluation software CD for the AD7327/AD7328
9 V mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

System demonstration platform (EVAL-SDP-CB1Z)
Precision analog signal source
SMB cables
USB cables

EVALUATION BOARD DESCRIPTION

The EVAL-AD7327SDZ/EVAL-AD7328SDZ is a full-featured evaluation board, designed to allow the user to easily evaluate all features of the AD7327/AD7328. The evaluation board can be controlled via the SDP connector (J2). The EVAL-SDP-CB1Z board allows the evaluation board to be controlled via the USB port of a PC using the AD7327/AD7328 evaluation software.

The EVAL-AD7327SDZ/EVAL-AD7328SDZ generates all required power supplies on-board and supplies power to the EVAL-SDP-CB1Z controller board.

On-board components include the following:

- AD8597: ultralow noise op amp
- ADP1613: step-up PWM dc-to-dc switching converter
- ADP3303-5: high accuracy anyCAP® 200 mA low dropout linear regulator
- ADP2301: 1.2 A, 20 V, 1.4 MHz nonsynchronous step-down switching regulator
- ADM1185: quad voltage monitor and sequencer
- ADP190: logic controlled, high-side power switch
- ADG3308: low voltage, 1.15 V to 5.5 V, 8-channel bidirectional logic level translator
- AD780: 5 V/3.0 V ultrahigh precision band gap voltage reference

Various link options are described in the Evaluation Board Hardware section.

TABLE OF CONTENTS

REVISION HISTORY

10/12—Revision 0: Initial Version

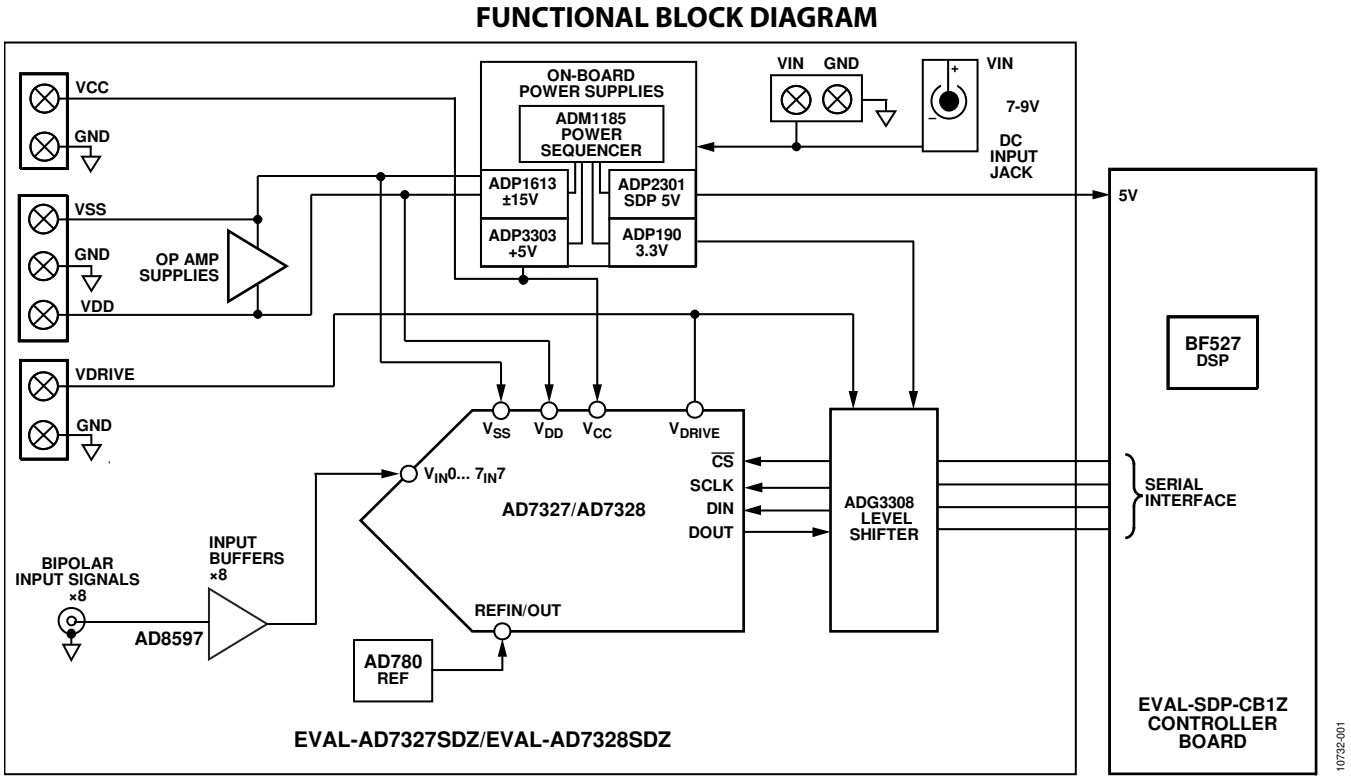
FUNCTIONAL BLOCK DIAGRAM
VCC
GND
VSS
GND
VDD
OP AMP SUPPLIES
VDRIVE
GND
ON-BOARD POWER SUPPLIES
ADM1185 POWER SEQUENCER
ADP1613 ±15V
ADP2301 SDP 5V
ADP3303 +5V
ADP190 3.3V
VIN GND
VIN
7-9V
DC INPUT JACK
5V
BF527 DSP
VSS VDD VCC VDRIVE
VIN0... 7IN7
AD7327/AD7328
CS
SCLK
DIN
DOUT
ADG3308 LEVEL SHIFTER
SERIAL INTERFACE
BIPOLAR INPUT SIGNALS ×8
INPUT BUFFERS ×8
AD8597
REFIN/OUT
AD780 REF
EVAL-AD7327SDZ/EVAL-AD7328SDZ
EVAL-SDP-CB1Z CONTROLLER BOARD
10732-001

Figure 1.

EVAL-AD7327SDZ/EVAL-AD7328SDZ QUICK START GUIDE

RECOMMENDED QUICK START GUIDE

To install the software, do the following:

1. Install the AD7327/AD7328 software from the enclosed CD. When installing the software, ensure that the EVAL-SDP-CB1Z board is disconnected from the USB port of the PC. After installation, restart the PC.
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7327SDZ/EVAL-AD7328SDZ board, as shown in Figure 2.
3. Screw the EVAL-SDP-CB1Z board to the EVAL-AD7327SDZ/EVAL-AD7328SDZ board together with the enclosed nylon screw-nut set to ensure that the boards connect firmly together.
4. Connect the 9 V power supply adapter included in the kit to the J702 connecter on the EVAL-AD7327SDZ/EVAL-AD7328SDZ board.
5. Connect the EVAL-SDP-CB1Z board to the PC via the USB cable. For Windows® XP, searching for the EVAL-SDP-CB1Z drivers may be needed. If prompted by the operating system, choose to automatically search for the drivers for the EVAL-SDP-CB1Z board.
6. Launch the AD7327/AD7328 software from the Analog Devices, Inc., subfolder in the **All Programs** menu.

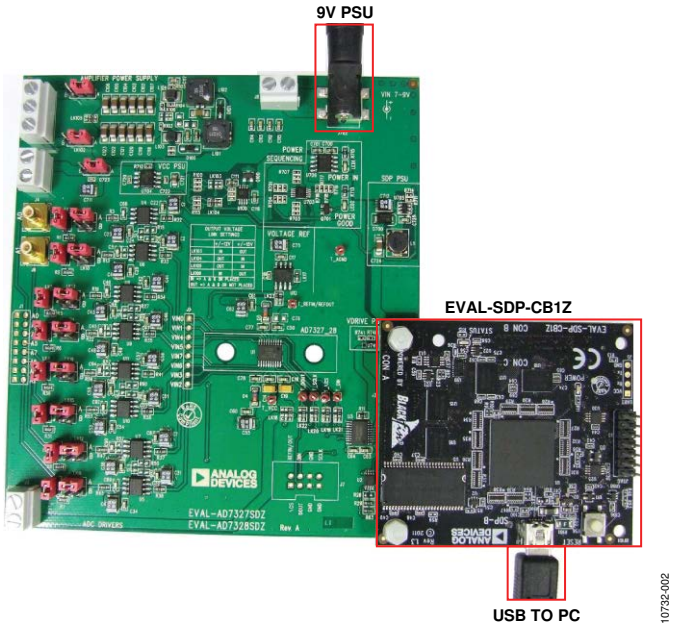

Figure 2. Setting Up the EVAL-AD7327SDZ/EVAL-AD7328SDZ

EVALUATION BOARD HARDWARE

AD7327 DEVICE DESCRIPTION

The AD7327 is an 8-channel, 12-bit plus sign, successive approximation analog-to-digital converter (ADC) designed on the industrial CMOS (*i*CMOS) process. *i*CMOS is a process that combines high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7327 can accept true bipolar analog input signals. The AD7327 has four software-selectable input ranges: ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7327 can be programmed to be single-ended, true differential, or pseudo differential.

The ADC contains a 2.5 V internal reference. The AD7327 also allows external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7327 can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range. The ADC has a high speed serial interface that can operate at throughput rates up to 500 kSPS.

AD7328 DEVICE DESCRIPTION

The AD7328 is an 8-channel, 12-bit plus sign, successive approximation ADC designed on the industrial CMOS (*i*CMOS) process. *i*CMOS is a process that combines high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can accept bipolar input signals while providing increased performance, dramatically reduced power consumption, and reduced package size.

The AD7328 can accept true bipolar analog input signals. The AD7328 has four software-selectable input ranges: ±10 V, ±5 V, ±2.5 V, and 0 V to +10 V. Each analog input channel can be independently programmed to one of the four input ranges. The analog input channels on the AD7328 can be programmed to be single-ended, true differential, or pseudo differential.

The ADC contains a 2.5 V internal reference. The AD7328 also allows for external reference operation. If a 3 V reference is applied to the REFIN/OUT pin, the AD7328 can accept a true bipolar ±12 V analog input. Minimum ±12 V V_{DD} and V_{SS} supplies are required for the ±12 V input range. The ADC has a high speed serial interface that can operate at throughput rates up to 1 MSPS.

Complete specifications for the AD7327/AD7328 are provided in the AD7327/AD7328 data sheet, available from Analog Devices, which should be consulted in conjunction with this user guide when using the EVAL-AD7327SDZ/EVAL-AD7328SDZ evaluation board.

HARDWARE LINK OPTIONS

Before using the evaluation board, the required operating setup has 23 link options that must be set. The functions of these options are outlined in Table 1. Table 1 lists the position in which all the links are set when the evaluation board is packaged. Before using the evaluation board, set the jumper and solder link (LKx) options correctly to select the appropriate operating setup. The default link positions are listed in Table 2, and the functions of these options are outlined in Table 1.

Table 1. Link Options

Link No.	Function
LK1	Sets Input A0 load to 51 Ω when inserted
LK2	Sets Input A1 load to 51 Ω when inserted
LK3	Sets Input A2 load to 51 Ω when inserted
LK4	Sets Input A3 load to 51 Ω when inserted
LK5	Sets Input A4 load to 51 Ω when inserted
LK6	Sets Input A5 load to 51 Ω when inserted
LK7	Sets Input A6 load to 51 Ω when inserted
LK8	Sets Input A7 load to 51 Ω when inserted
LK9	A0 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK10	A1 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers

Link No.	Function
LK11	A2 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK12	A3 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK13	A4 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK14	A5 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK15	A6 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK16	A7 signal selection Position A: input signal passed to input buffer amplifiers Position B: 0 V passed to input buffer amplifiers
LK17	VREF voltage selection (0 Ω) Inserted: VREF = 3.0 V Removed: VREF = 2.5 V
LK18	VDRIVE selection Position A: VDRIVE = 3.3 V Position B: VDRIVE = VCC Position C: VDRIVE set externally via Socket J3, Pin 2
LK19	$\overline{CS}$ selection Position A: $\overline{CS}$ sourced from the EVAL-SDP-CB1Z Position B: $\overline{CS}$ sourced externally via J7, Pin 1
LK20	SCLK selection Position A: SCLK sourced from the EVAL-SDP-CB1Z Position B: SCLK sourced externally via J7, Pin 8
LK21	DIN selection Position A: DIN sourced from the EVAL-SDP-CB1Z Position B: DIN sourced externally via J7, Pin 4
LK22	DOUT Selection Position A: DOUT sourced from the EVAL-SDP-CB1Z Position B: DOUT sourced externally via J7, Pin 3
LK23	REFIN/REFOUT selection Position A: REFIN/REFOUT supplied from the on-board precision reference AD780 Position B: REFIN/REFOUT supplied externally via J7, Pin 2 Open: internal reference used; must be enabled over SPORT
LK101[1]	VSS selection Position A: VSS supplied from on-board supply Position B: VSS supplied from external source via J100 Terminal 1
LK102[1]	VDD selection Position A: VDD supplied from on-board supply Position B: VDD supplied from external source via J100 Terminal 3

Link No.	Function		
LK103, LK104, LK105, LK106	Sets the VDD and VSS levels when using the on-board supplies		
	Link	**±12V**	**±15V**
	LK103	POP (place both 0 Ω resistors)	NOPOP (neither 0 Ω resistor is placed)
	LK104	NOPOP (neither 0 Ω resistor is placed)	POP (place both 0 Ω resistors)
	LK105	NOPOP(neither 0 Ω resistor is placed)	POP (place both 0 Ω resistors)
	LK106	POP (place both 0 Ω resistors)	NOPOP (neither 0 Ω resistor is placed)
LK701	VCC selection Position A: VCC supplied from on-board 5 V supply Position B: VDD supplied from external source via J703 Terminal 1		
SL1 to SL4	Not used		

[1] Both LK101 and LK102 should always be in matching positions.

Table 2. Link Options—Setup Conditions

Link No.	Position	Function
LK1 to LK8	Inserted	Signal inputs, A0 to A7, set to 51 Ω
LK9 to LK16	A	Input signals passed to input buffer amplifiers
LK17	A	Output from AD780 set to 3.0 V
LK18	A	VDRIVE pin on AD7327/AD7328 set to 3.3 V
LK19	A	$\overline{CS}$ pin on the AD7327/AD7328 is connected to the EVAL-SDP-CB1Z board
LK20	A	SCLK pin on the AD7327/AD7328 is connected to the EVAL-SDP-CB1Z board
LK21	A	DIN pin on the AD7327/AD7328 is connected to the EVAL-SDP-CB1Z board
LK22	A	DOUT pin on the AD7327/AD7328 is connected to the EVAL-SDP-CB1Z board
LK23	A	VREF is supplied from the AD780 precision voltage reference
LK101	A	VSS supplied from on-board supply
LK102	A	VDD supplied from on-board supply
LK103	POP	Both 0 Ω resistors placed VDD = 15 V; VSS = −15 V
LK104	NOPOP	Neither 0 Ω resistors placed VDD = 15 V; VSS = −15 V
LK105	NOPOP	Neither 0 Ω resistors placed VDD = 15 V; VSS = −15 V
LK106	POP	Both 0 Ω resistors placed VDD = 15 V; VSS = −15 V
LK701	A	VCC supplied from on-board 5 V supply

POWER SUPPLIES

Take care before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode.

When using the EVAL-AD7327SDZ/EVAL-AD7328SDZ in conjunction with the EVAL-SDP-CB1Z board, connect the ac transformer to the J702 connector. VCC, VDD, VSS, and VDRIVE are generated on board.

Each supply is decoupled on the EVAL-AD7327SDZ/EVAL-AD7328SDZ using the 10 µF and 0.1 µF capacitors. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 3. External Power Supply Required

Power Supply	Voltage Range (V)	Purpose
VIN[1], J8 or J702	+7 to +9	Supplies all on-board power supplies that generate all the required voltages to run the evaluation board
VDD, J100	+12 to +16.5	Amplifier +VDD
VSS, J100	−12 to −16.5	Amplifier −VSS
VCC, J703	+2.7 to +5.25	ADC supply
VDRIVE, J3	+2.7 to +5.25	Supply voltage for the digital interface circuitry

[1] When this is supplied, all other power supplies are available on-board. If this supply is not used, all other supplies must be sourced from an external source.

SERIAL INTERFACE

The AD7327/AD7328 uses a high speed serial interface that allows sampling rates up to 500 kSPS for the AD7327 and 1 MSPS for the AD7328. For details on the operation of the serial bus, refer to the AD7327 data sheet and the AD7328 data sheet.

The EVAL-AD7327SDZ/EVAL-AD7328SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3 V logic level. The level shifters allow the VDRIVE voltages to exceed 3.3 V and be used without damaging the SDP interface.

Details of the serial interface can be found in the AD7327 data sheet and the AD7328 data sheet.

ANALOG INPUTS

The analog inputs on the EVAL-AD7327SDZ/EVAL-AD7328SDZ are filtered and buffered by the AD8597 ultralow distortion, ultra-low noise op amp. The EVAL-AD7327SDZ/EVAL-AD7328SDZ is configured for single-ended input mode.

The A0 and A1 inputs allow a signal to be connected to the board via the SMB connectors. Alternatively, all signals can be connected via Header J1.

For performance evaluation, using the SMB connections is recommended for the best signal quality on the A0 and A1 inputs.

Each analog input to the EVAL-AD7327SDZ/EVAL-AD7328SDZ allows a 51 Ω load to be placed on the input, if required. LK1 to LK8 are placed to connect the inputs to the 51 Ω loads.

REFERENCE OPTIONS

The reference source can be from the AD7327/AD7328 REFIN/OUT pin or from an AD780, 5 V/3.0 V, ultrahigh, precision band gap, voltage reference (U12). An external reference voltage may also be applied to Pin 2 of J7.

SOCKETS/CONNECTORS

Table 4. Socket Connection Functions

Socket	Function
J1	A0 to A7 inputs with ground pins adjacent to each signal pin
J2	SDP1Z socket for evaluation control board
J3	External screw connection for VDRIVE
J4	Analog A0 input; buffered to VIN0, AD7327/AD7328
J5	Test point access to VIN0 to VIN7 signals
J6	Analog A1 input; buffered to VIN0, AD7327/AD7328
J7	External connection for serial interface and reference voltage
J8	7 V to 9 V bench supply screw terminal connector
J100	VSS and VDD screw terminal connectors
J702	7 V to 9 V dc transformer power connector
J703	AVCC screw terminal connector

EVAL-AD7327SDZ/EVAL-AD7328SDZ BASIC HARDWARE SETUP

The AD7327/AD7328 evaluation board connects to the SDP board (EVAL-SDP-CB1Z). The EVAL-SDP-CB1Z board is the controller board, which is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7327/AD7328 daughter board and the EVAL-SDP-CB1Z board.

Before connecting power, connect the EVAL-AD7327SDZ/EVAL-AD7328SDZ board to Connector A or Connector B on the EVAL-SDP-CB1Z board. Use the nylon screws included in the EVAL-AD7327SDZ/EVAL-AD7328SDZ evaluation kit and to ensure the EVAL-AD7327SDZ/EVAL-AD7328SDZ board and the EVAL-SDP-CB1Z board are connected firmly together.

When the EVAL-AD7327SDZ/EVAL-AD7328SDZ board and the EVAL-SDP-CB1Z board are connected securely, connect the power supplies on the EVAL-AD7327SDZ/EVAL-AD7328SDZ board. The EVAL-AD7327SDZ/EVAL-AD7328SDZ requires an external power supply, which is included in the evaluation board kit. Connect this power supply to the J702 connector on the EVAL-AD7327SDZ/EVAL-AD7328SDZ board. Alternatively, a bench power supply can be used to power the EVAL-AD7327SDZ/EVAL-AD7328SDZ via J8. Further details on the required power supplies connections and options are detailed in Table 4.

Before connecting the EVAL-SDP-CB1Z board to a PC, ensure that the AD7327/AD7328 software has been installed from the enclosed CD. The full software installation procedure is detailed in the Evaluation Board Software section.

Finally, connect the EVAL-SDP-CB1Z board to the PC via the USB cable enclosed in the EVAL-SDP-CB1Z kit. If using the Windows XP® platform, the EVAL-SDP-CB1Z drivers may need to be searched for. If prompted by the operating system, choose to automatically search for the drivers for the EVAL-SDP-CB1Z board.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7327SDZ/EVAL-AD7328SDZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the install. The default location for the software is the following: **C:\Program Files\Analog Devices\AD7327_28**.

Install the evaluation software before connecting the evaluation board and the EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts to the installation

- AD7327/AD7328 evaluation board software install
- EVAL-SDP-CB1Z SDP board drivers install

Figure 3 to Figure 7 show the separate stages of the AD7327/AD7328 evaluation software. Figure 8 to Figure 12 show the separate steps to install the EVAL-SDP-CB1Z drivers. Proceed through all of the installation steps allowing the software and drivers to be placed in the appropriate locations. Only after the software and drivers have been installed should the EVAL-SDP-CB1Z board be connected to the PC.

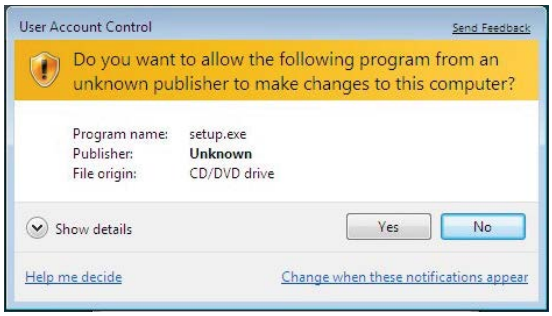

Figure 3. AD7327/AD7328 Install Window 1

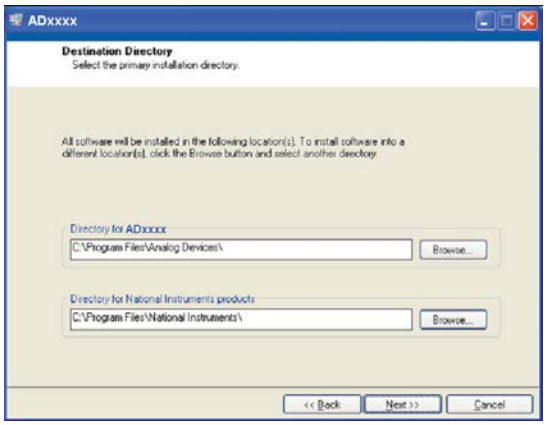

Figure 4. AD7327/AD7328 Install Window 2

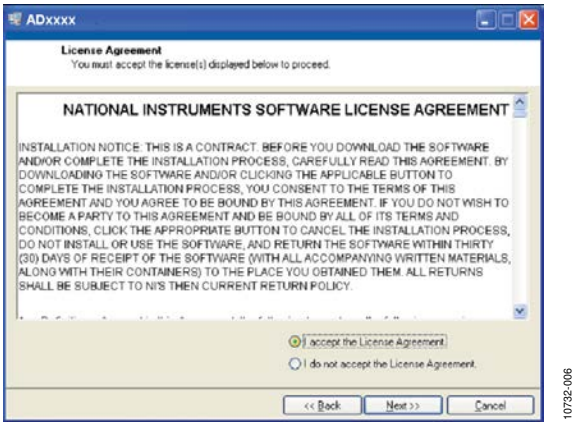

Figure 5. Install Window 3

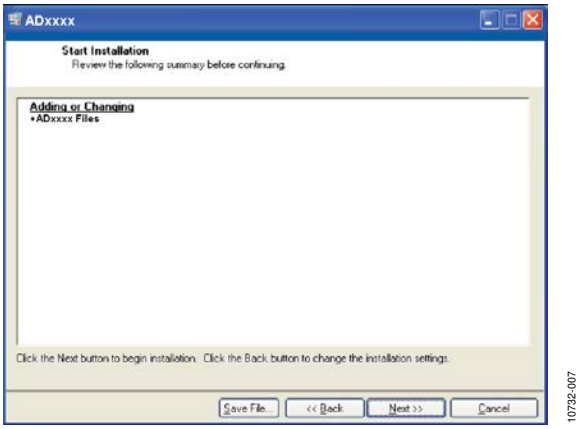

Figure 6. AD7327/AD7328 Install Window 4

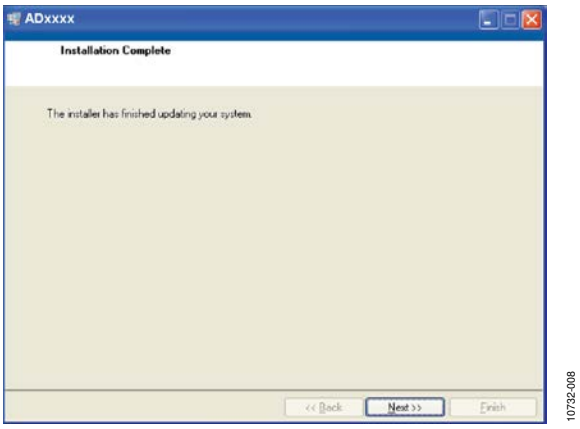

Figure 7. AD7327/AD7328 Install Window 5

Figure 8. EVAL-SDP-CB1Z Drivers Setup Window 1

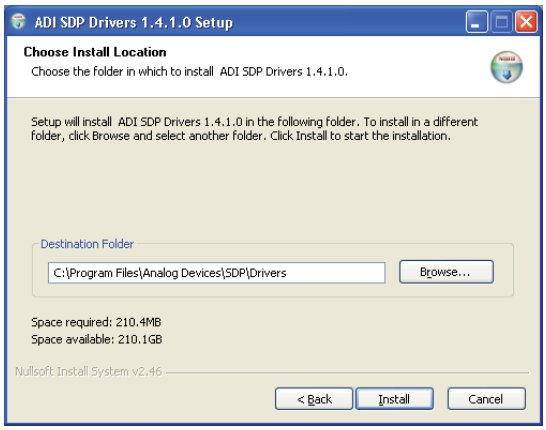

Figure 9. EVAL-SDP-CB1Z Drivers Setup Window 2

Figure 10. EVAL-SDP-CB1Z Drivers Setup Window 3

Figure 11. EVAL-SDP-CB1Z Drivers Setup Window 4

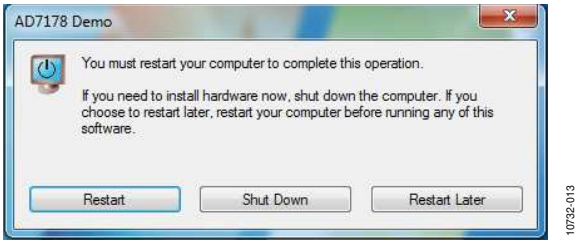

Figure 12. EVAL-SDP-CB1Z Drivers Setup Window 5

After installation from the CD is complete, connect the EVAL-AD7327SDZ/EVAL-AD7328SDZ board to the EVAL-SDP-CB1Z board as described in the Evaluation Board Hardware section.

When the EVAL-SDP-CB1Z board is first plugged in via the USB cable provided, allow the **Found New Hardware Wizard** to run. Once the drivers are installed, ensure that the board has connected correctly by looking at the **Device Manager** of the PC. When the EVAL-SDP-CB1Z board appears under **ADI Development Tools**, the installation is completed.

Figure 13. Device Manager

LAUNCHING THE SOFTWARE

When the EVAL-AD7327SDZ/EVAL-AD7328SDZ and EVAL-SDP-CB1Z are correctly connected to the PC, the AD7327/AD7328 software can be launched.

To launch the software, complete the following steps:

1. From the **Start** menu, select **Programs**/**Analog Devices**/**AD7327**/**AD7328**. The main window of the software then displays.
2. If the AD7327/AD7328 evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation board to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the instructions.

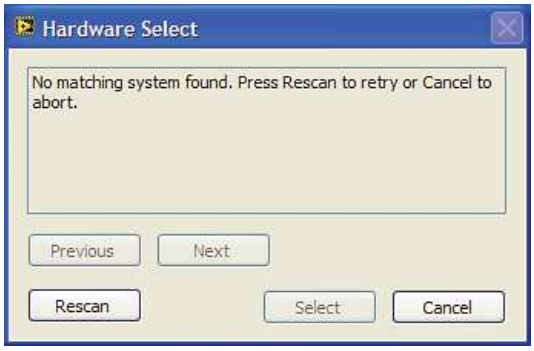

Figure 14. Connectivity Error Alert

SOFTWARE OPERATION

When the software is launched, the panel opens and the software looks for hardware connected to the PC. The software detects the generic attached to the PC and returns this in a user dialog box. The user software panel then launches as shown in Figure 15.

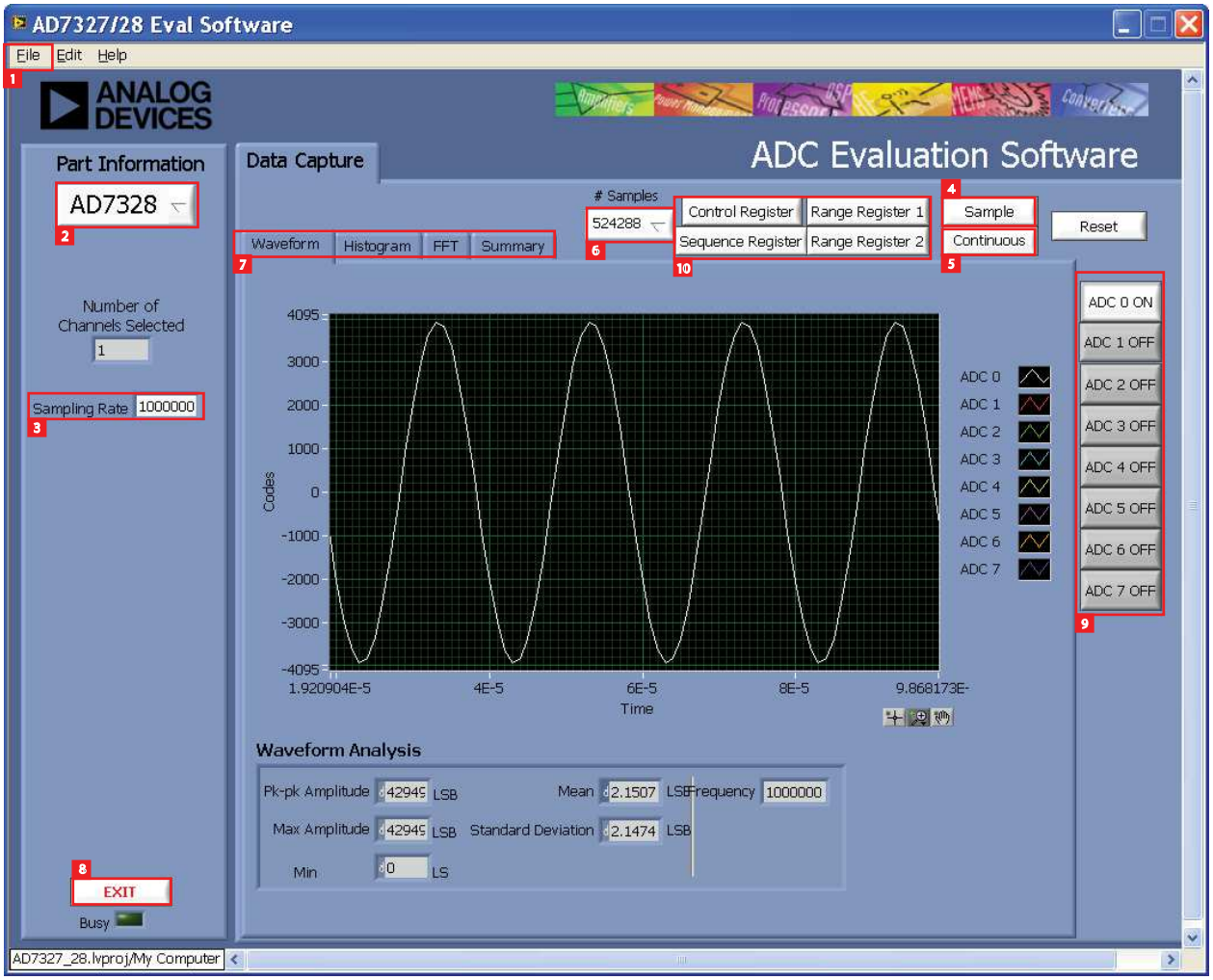

Figure 15. User Software Panel, Setup Screen

DESCRIPTION OF USER SOFTWARE PANEL

The user software panel, as shown in Figure 15, has the following features:

1. **File** menu with the choice of the following:
   a. **Load data**: load previously captured data in .tsv (tab separated values) format for analysis
   b. **Save Data as .tsv**: save captured data in .tsv) format for future analysis
   c. **Print Front Panel Picture**: use to print the front panel to the default printer.
   d. **Save Picture**: use to save the current screen capture
   e. **EXIT**
2. Use this drop-down menu to select the generic, AD7327 or AD7328.
3. **Sampling Rate**: The default sampling frequency matches the maximum sample rate of the ADC selected from the drop-down menu. User can adjust the sampling frequency; however, there are limitations around the sample frequency, where unusable sample frequencies are input, and the software automatically adjusts the sample frequency accordingly. Units can be entered such as 10k for 10,000 Hz. As the maximum sample frequency possible is device dependent, with some of the ADCs capable of operating up to 250 kSPS, while others can run to 1.3 MSPS, the software matches the particular ADC ability. If the user enters a value larger than the ability of the existing device, the software indicates this and reverts to the maximum sample frequency.
4. **Sample**: to perform a single capture.
5. **Continuous**: to perform a continuous capture from the ADC. Press a second time to stop sampling.
6. Select the number of samples (**# Samples**) to analyze.
7. There are four tabs available displaying the data in different formats, these are listed here and described in more detail in the Data Capture/WaveForm Tab, AC Testing—Data Capture/Histogram Tab, DC Testing—Data Capture/Histogram Tab, AC Testing—Data Capture/FFT Tab, and Data Capture/Summary Tab sections.
   a. **Waveform**
   b. **Histogram**
   c. **FFT**
   d. **Summary**

8. **EXIT** button. Use this button to exit the software. Alternatively, go to **File**/**Exit**.
9. Channel display buttons. Use these to display multiple channel reads on the display. For FFT analysis, select only one channel.
10. Registers (**Control Register**, **Sequence Register**, **Range Register 1**, and **Range Register 2**). Use these buttons to access the register settings dialog boxes. See the Register Controls section for more details.

Within any of the chart panels, the following tools allow user control of the different chart displays.

 is used for controlling the cursor. if present.

 is used for zooming in and out.

 is used for panning.

Click **Save Plot** to save plots.

REGISTER CONTROLS

There are four registers used to control the operations of the AD7327/AD7328. For detailed settings of these registers, refer to the relevant data sheet.

*Figure 16. **Control Register** Dialog Box*

The **Control Register** sets up the addressing, modes, and power management, as well as setting the sequence, coding, and reference source (see Figure 16).

Figure 17. Sequence Register Dialog Box

The **Sequence Register** selects which channels are included in the channel sequencing (see Figure 17).

Figure 18. Range Register1 Dialog Box

Figure 19. Range Register2 Dialog Box

Range Register 1 and **Range Register 2** allow the range of each channel to be individually selected (Figure 18 and Figure 19).

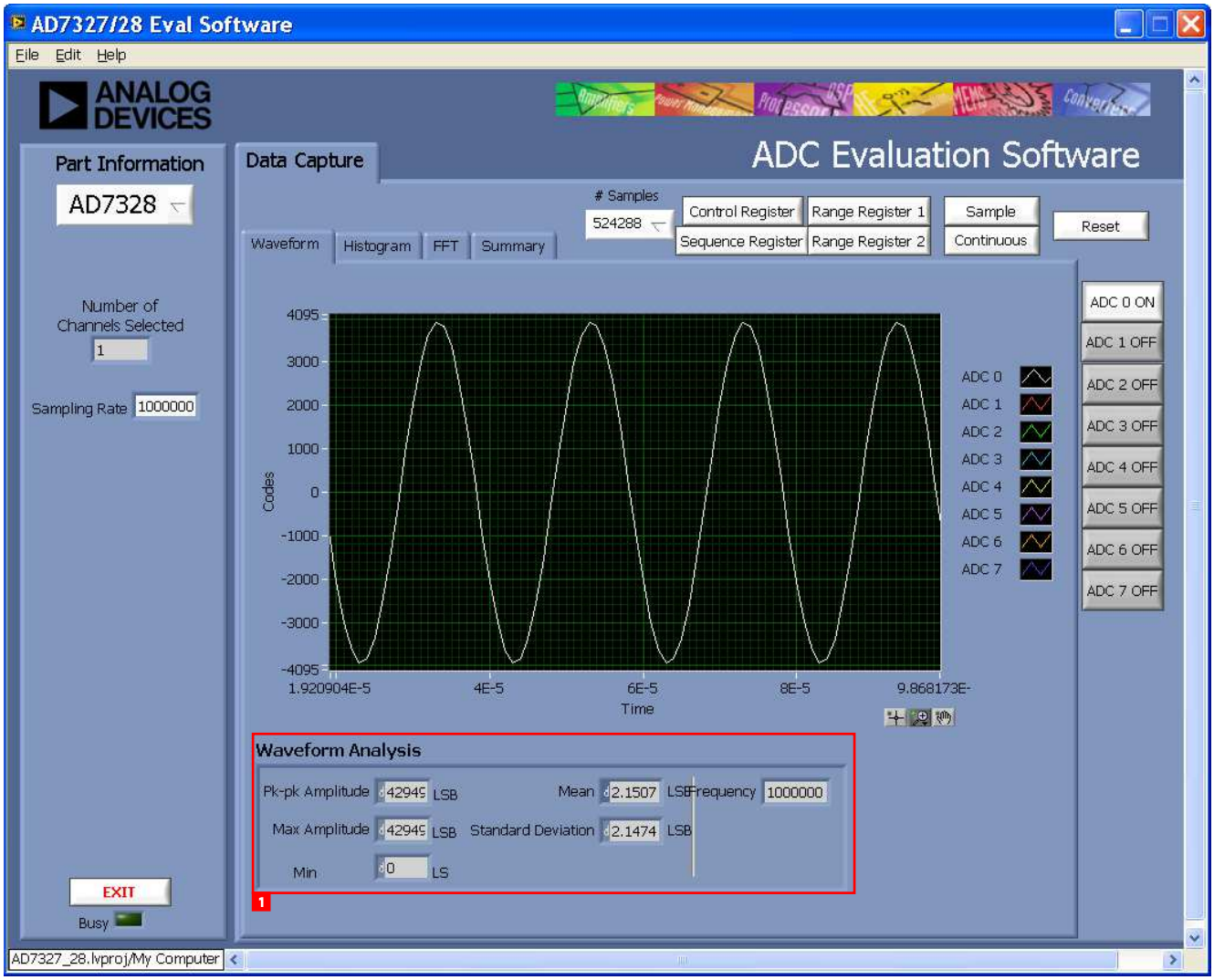

*Figure 20. **Data Capture/Waveform** Tab*

DATA CAPTURE/WAVEFORM TAB

Figure 20 illustrates the **Data Capture/Waveform** tab. The input signal here is a 50 kHz sine wave.

Number 1 in Figure 20 shows that the waveform analysis reports back the amplitudes recorded from the captured signal in addition to the frequency of the signal tone (see Figure 20).

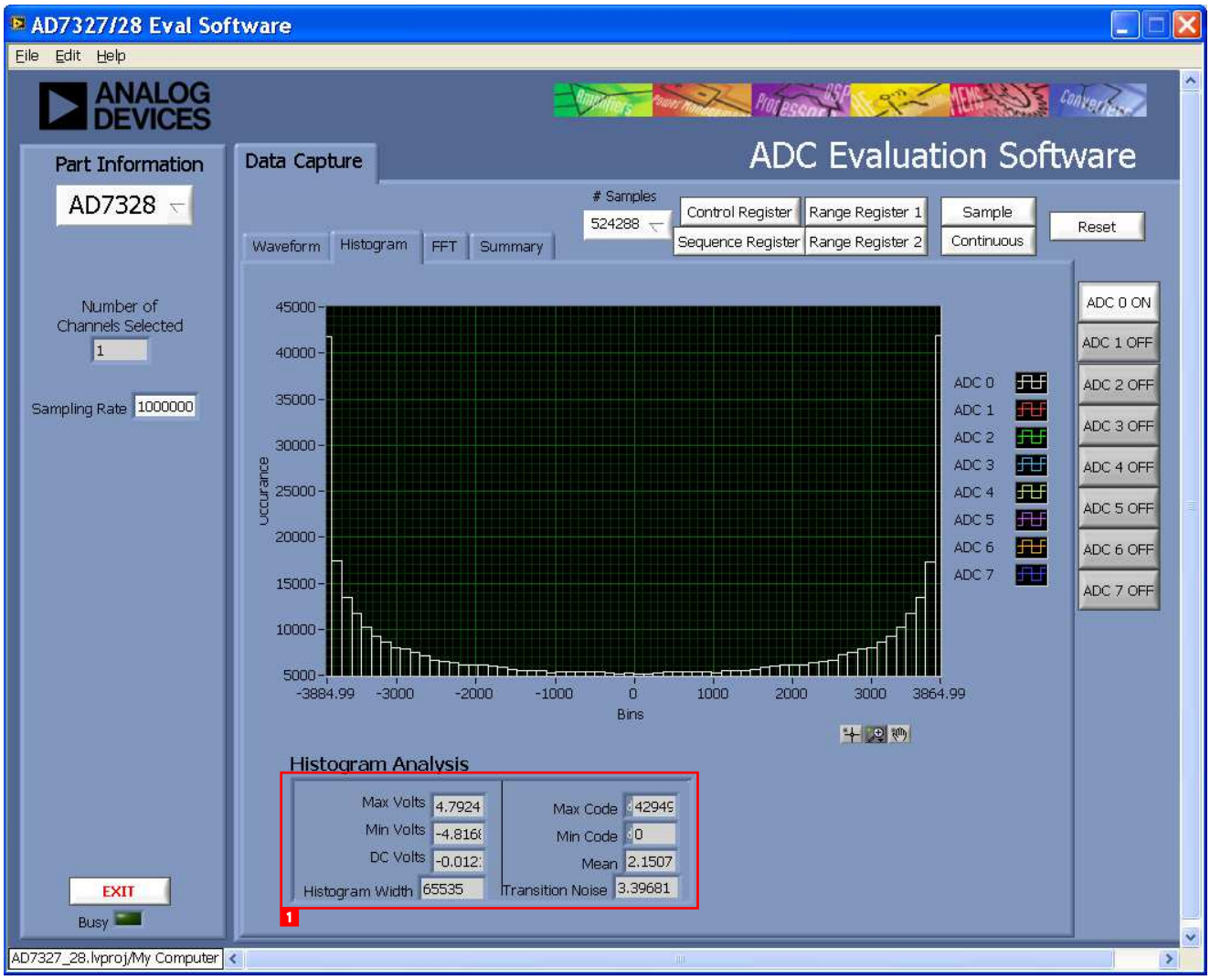

*Figure 21. **Data Capture/Histogram** Tab*

AC TESTING—DATA CAPTURE/HISTOGRAM TAB

Figure 21 shows the **Data Capture/Histogram** tab. This tab allows the user to test the ADC for the code distribution for ac input and computes the mean and standard deviation, or transition noise of the converter, and displays the results.

Raw data is captured and then passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab and click **Sample**.

An ac histogram needs a quality signal source applied to the input of the SK1/SK3 connectors. Figure 21 shows the histogram for a 50 kHz sine wave applied to the ADC input and the results calculated.

Number 1 in Figure 21 illustrates the different measured values for the data captured.

DC TESTING—DATA CAPTURE/HISTOGRAM TAB

More commonly, the histogram is used for dc testing, where the ADC is tested for the code distribution for dc input and computes the mean and standard deviation, or transition noise of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations. To perform a histogram test, select the **Histogram** tab click **Sample**.

A histogram test can be performed without an external source because the evaluation board has a buffered $V_{REF}/2$ source at the ADC input. To test other dc values, apply a source to the J3 and J4 inputs. To make the dc source noise compatible with that of the ADC, it may be required to filter the signal.

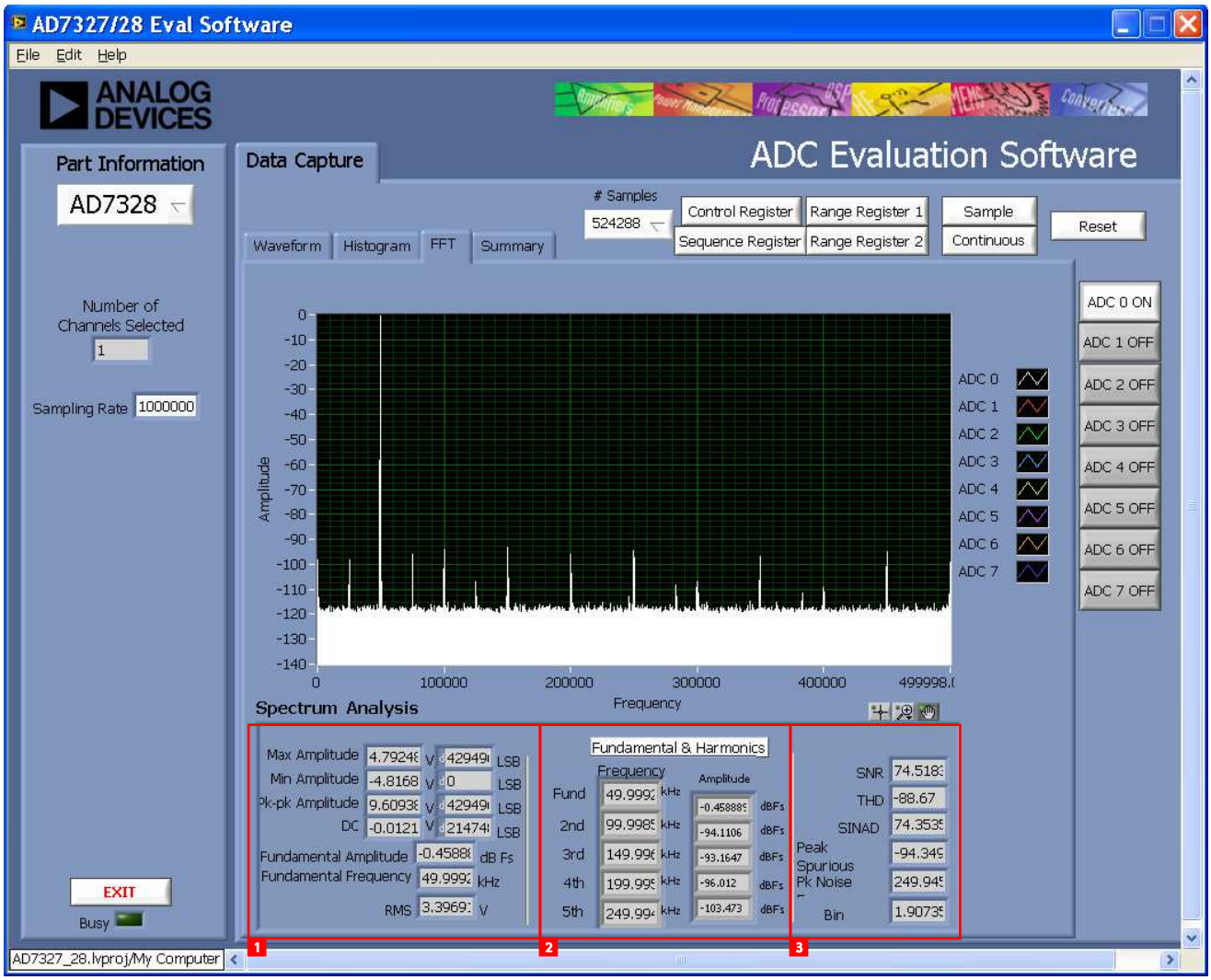

*Figure 22. **Data Capture/FFT** Tab*

AC TESTING—DATA CAPTURE/FFT TAB

Figure 22 shows the **Data Capture/FFT** tab This tests the traditional ac characteristics of the converter and displays a Fast Fourier Transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC, where the FFT is performed displaying the signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), total harmonic distortion (THD), and spurious-free dynamic range (SFDR). To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMB inputs, J4 and J6. Low distortion, better than 115 dB, is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter; however, take consideration in the choice. Furthermore, if using a low frequency, band-pass filter when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 22 displays the results of the captured data.

1. Shows the input signal information
2. Displays the fundamental frequency (**Fund**) and amplitude in addition to the second (**2nd**) to fifth (**5th**) harmonics.
3. Displays the performance data: **SNR**, **THD**, **SINAD**, **Peak Spurious**, **Pk Noise Freq**, and **Bin**.

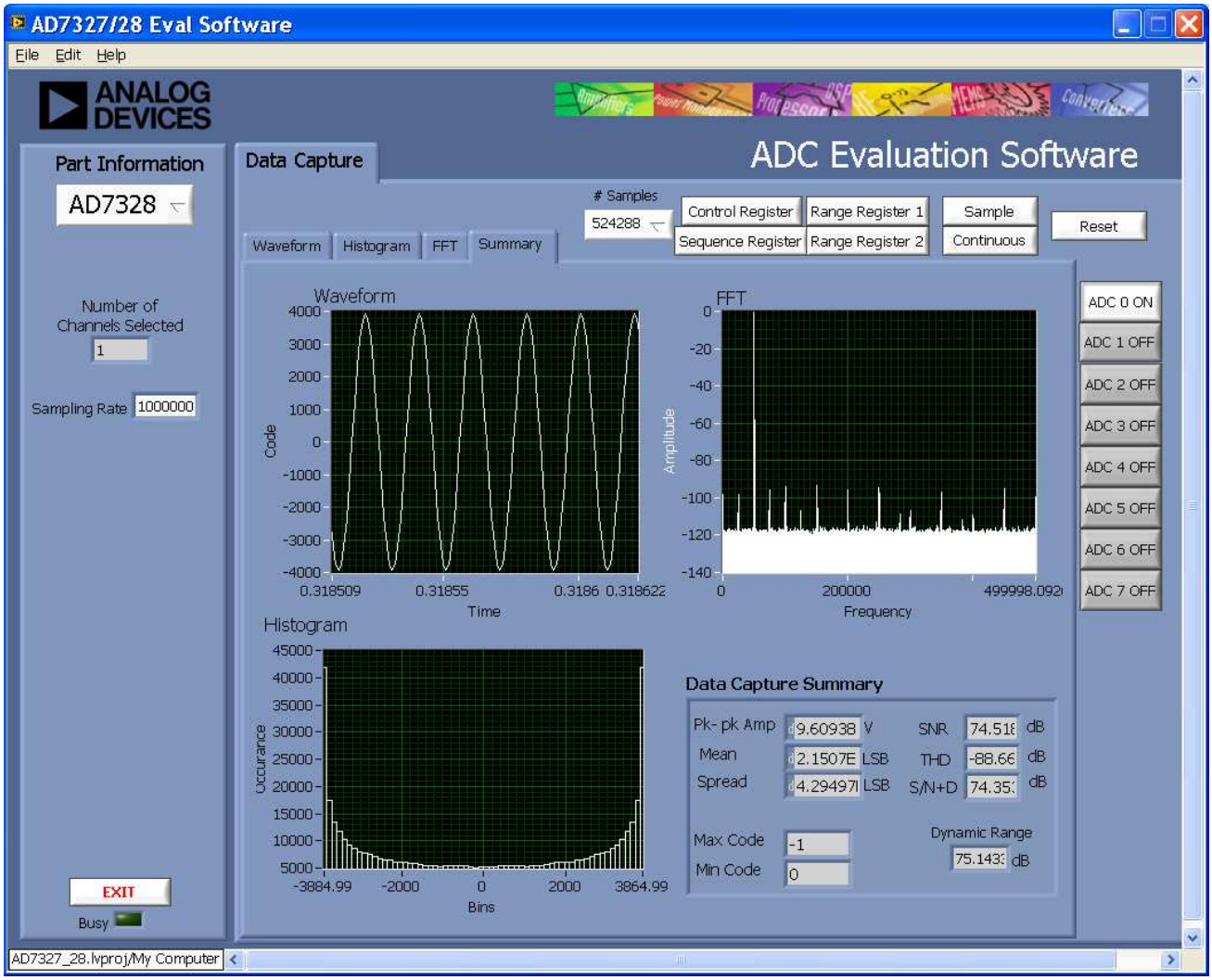

*Figure 23. **Data Capture/Summary** Tab*

DATA CAPTURE/SUMMARY TAB

Figure 23 shows the **Data Capture/Summary** tab. It captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters, such as SNR and THD.

SAVE FILE

The software can save the current captured data for later analysis to a .tsv file (see Figure 24). Window users are prompted to save to an appropriate folder location.

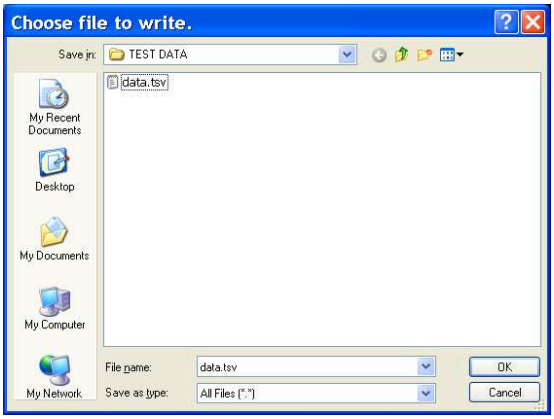

*Figure 24. Save File Dialog Box (**Choose file to write.**)*

LOAD FILE

In the **Choose file to read.** window, users are prompted to load the file (see Figure 25). User may have to navigate to find these example files. The default location for the example files is: **C:\Program Files\Analog Devices\AD7327_28\examples**.

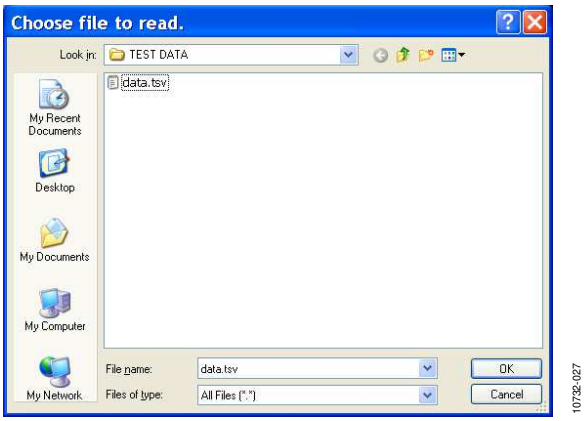

*Figure 25. Load File Dialog Box (**Choose file to read.**)*

EVALUATION BOARD SCHEMATICS AND ARTWORK

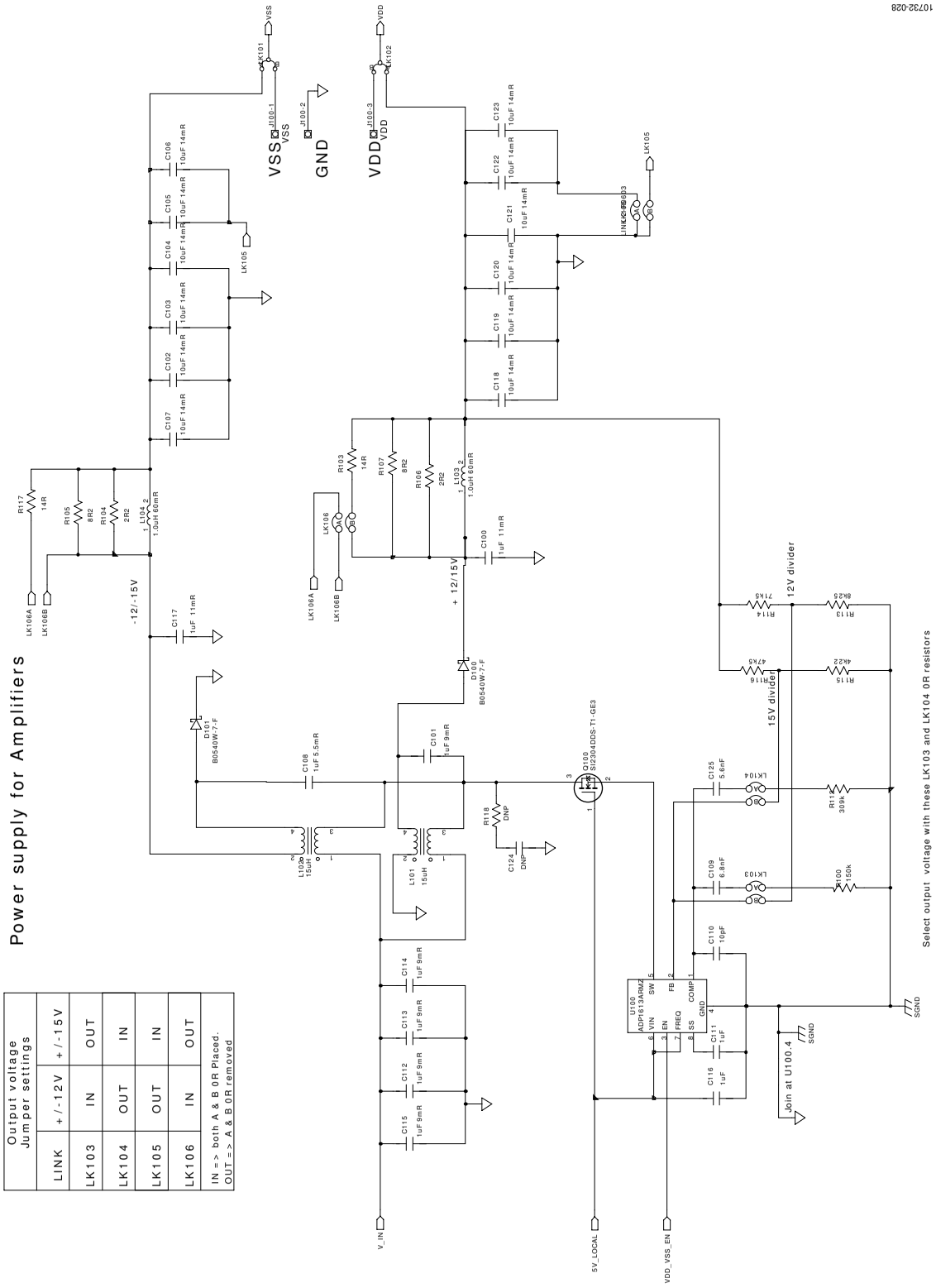

Figure 26. Schematic Page 1

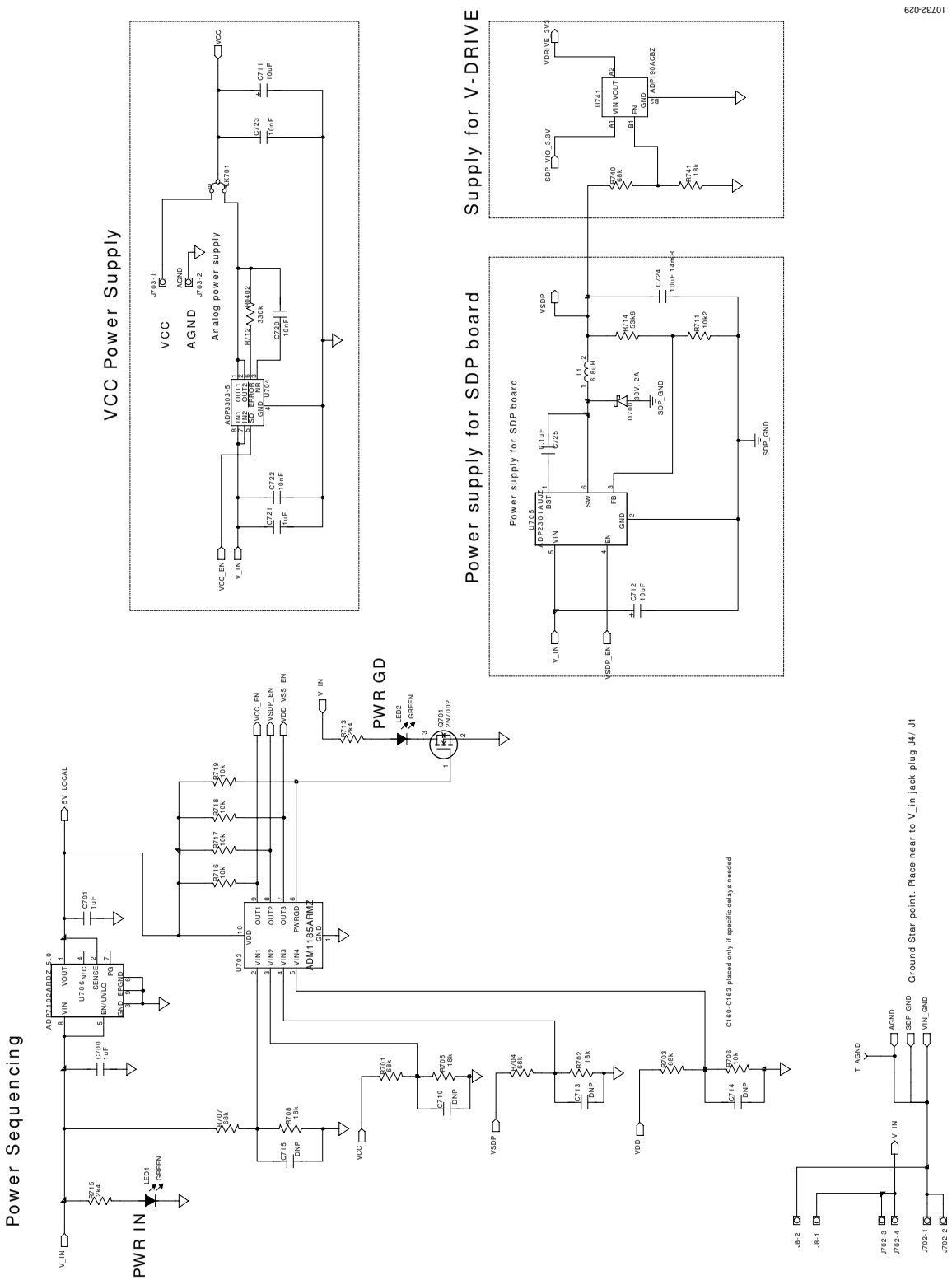

Figure 27. Schematic Page 2

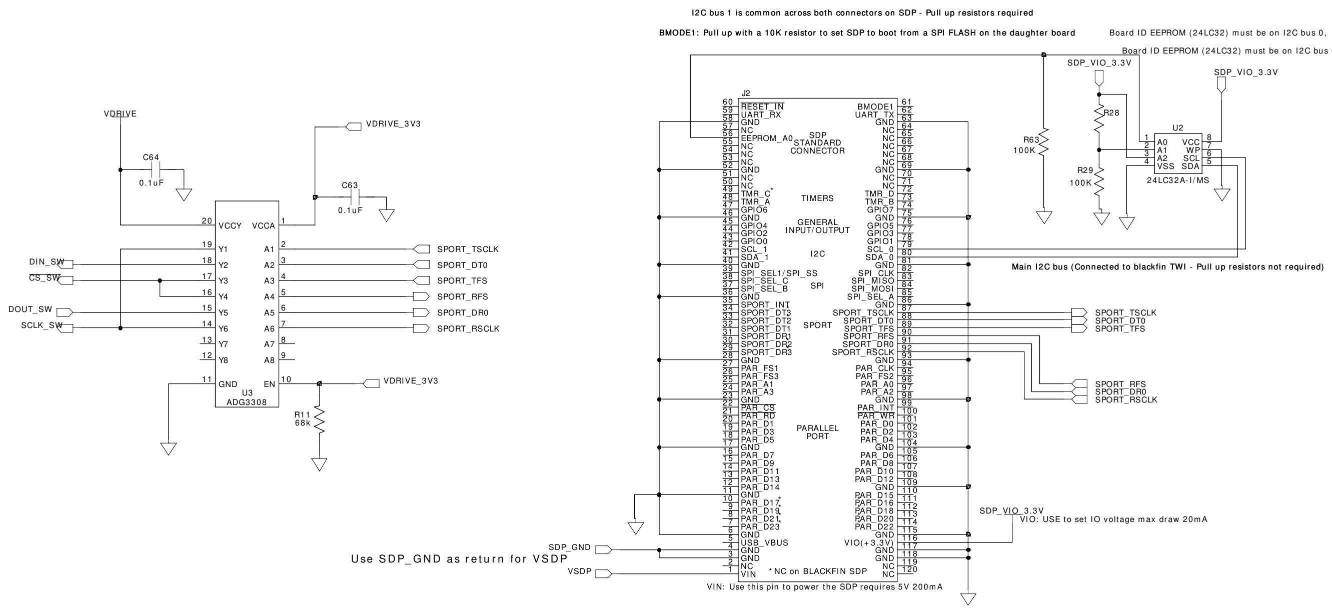

Figure 28. Schematic Page 3

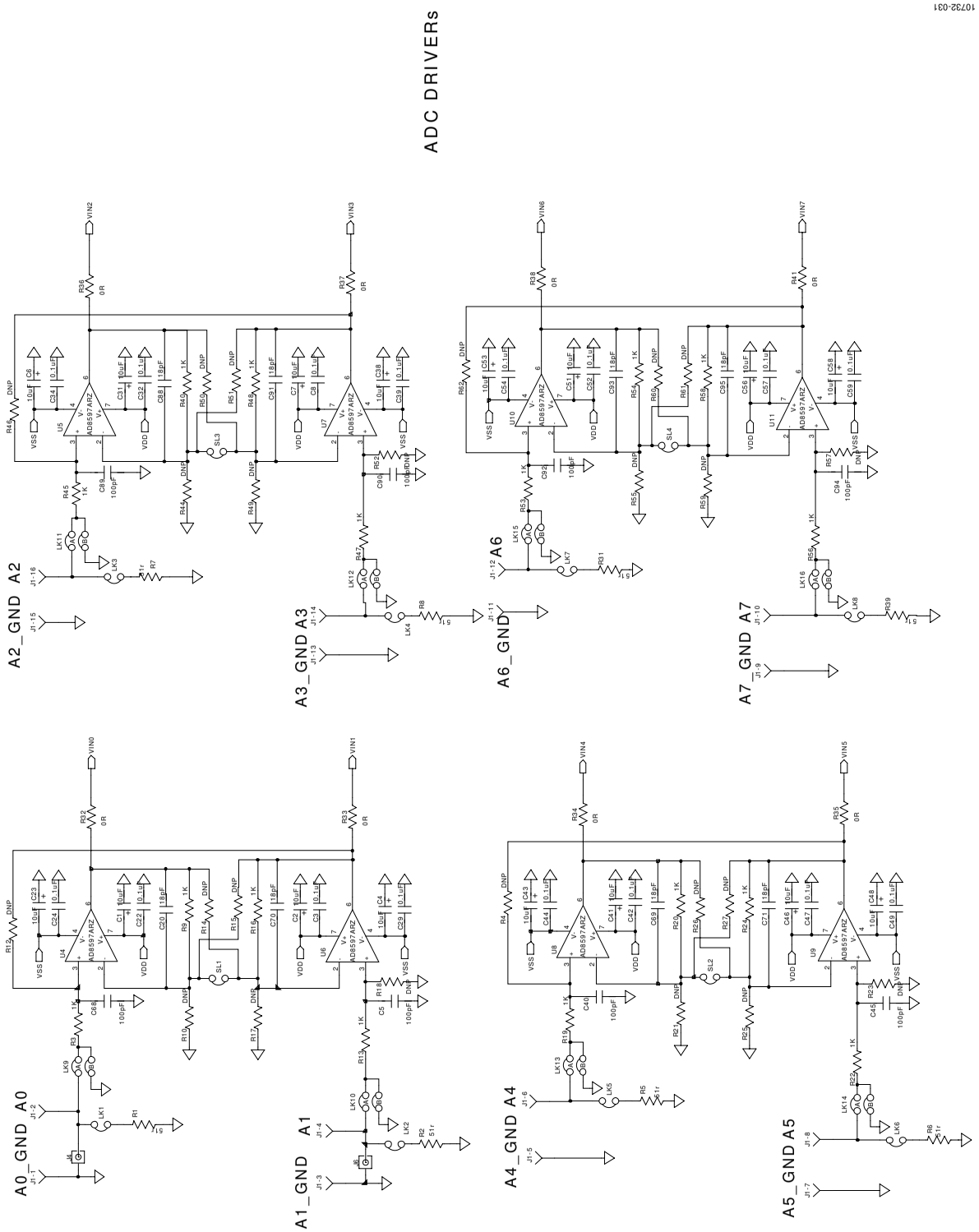

Figure 29. Schematic Page 4

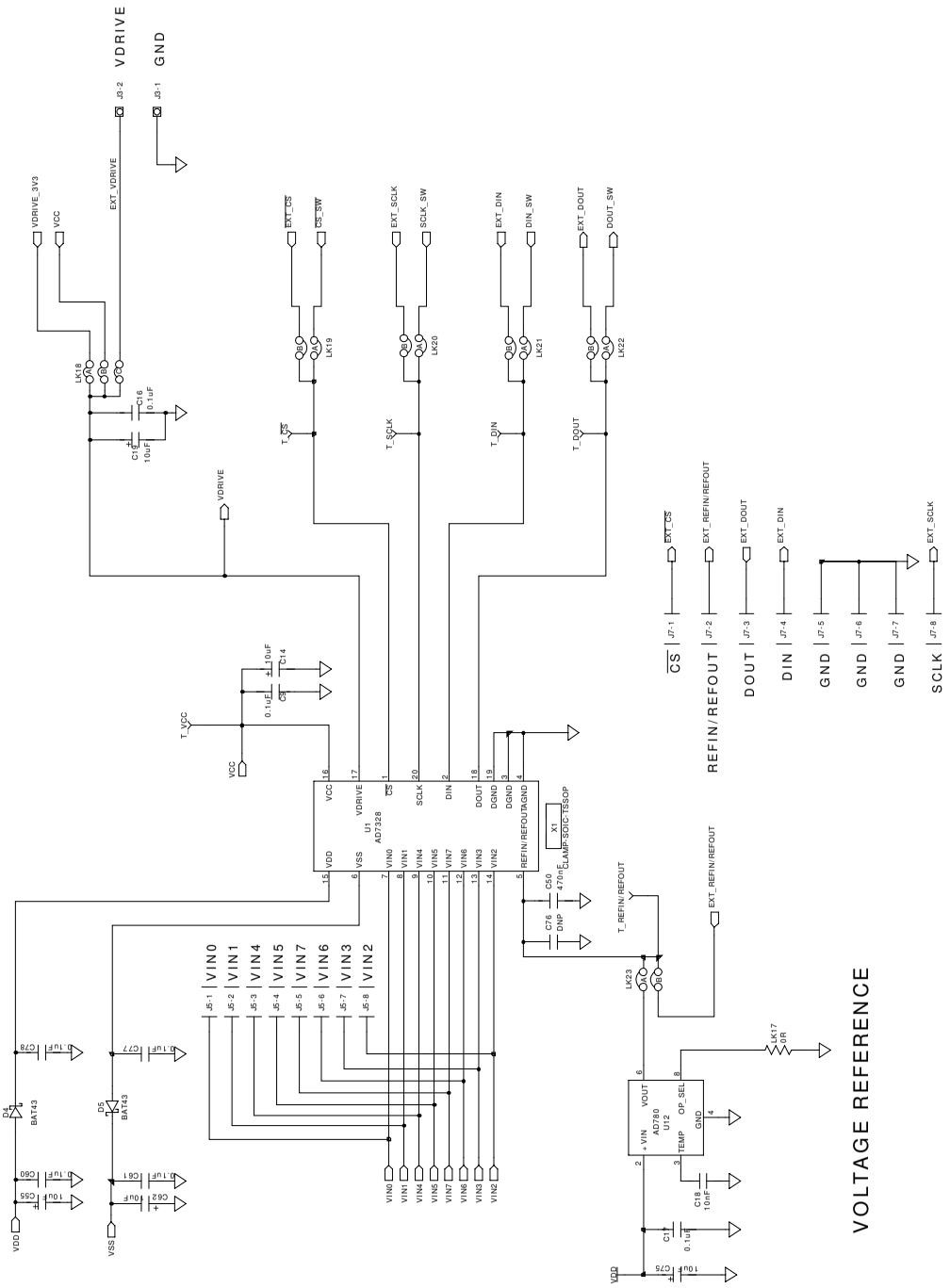

Figure 30. Schematic Page 5

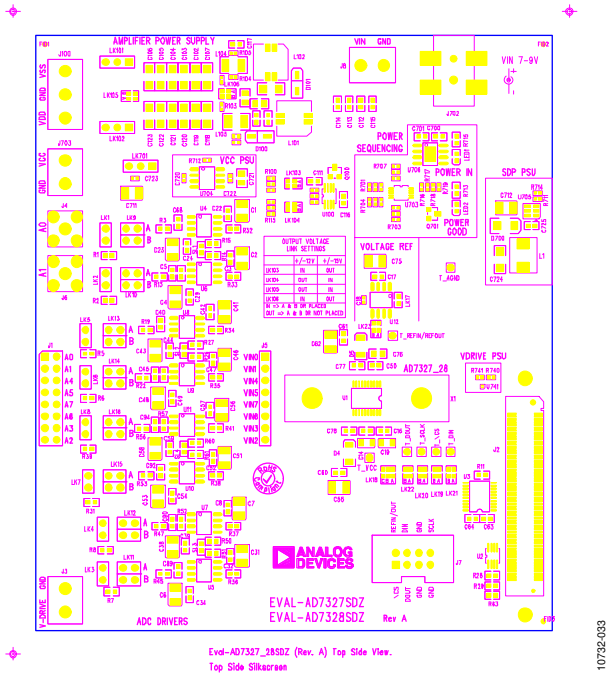

Figure 31. Top Printed Circuit Board (PCB) Silkscreen

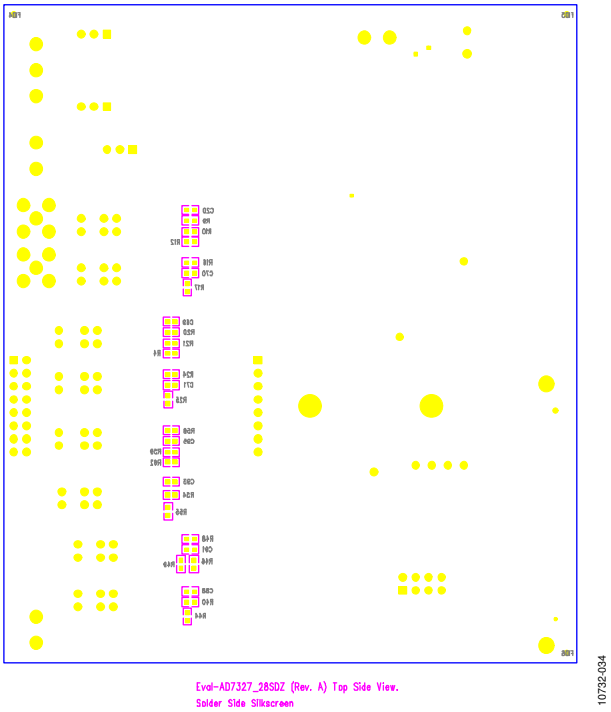

Figure 32. Bottom Printed Circuit Board (PCB) Silkscreen

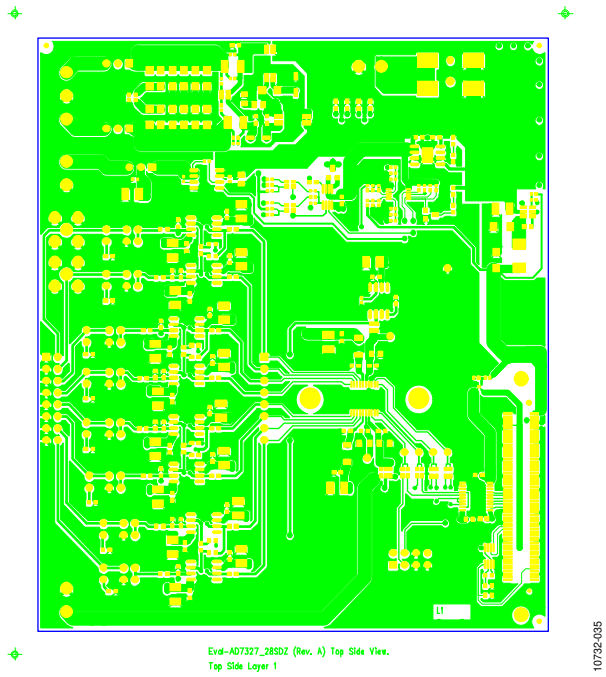

Figure 33. Layer 1 Component Side View

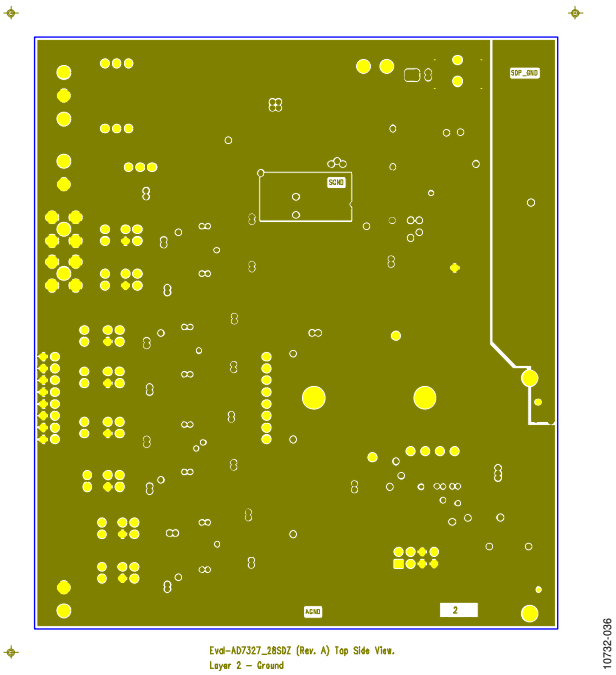

Figure 34. Layer 2 Component Side View