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### FEATURES

- 8 simultaneously sampled inputs
- True differential inputs
- True bipolar analog input ranges:  $\pm 10\text{ V}$ ,  $\pm 5\text{ V}$
- Single 5 V analog supply and 2.3 V to 5.25 V  $V_{\text{DRIVE}}$
- Fully integrated data acquisition solution
  - Analog input clamp protection
  - Input buffer with 1 M $\Omega$  analog input impedance
  - Second-order antialiasing analog filter
  - On-chip accurate reference and reference buffer
  - 18-bit ADC with 200 kSPS on all channels
  - Oversampling capability with digital filter
- Flexible parallel/serial interface
- SPI/QSPI™/MICROWIRE™/DSP compatible
- Performance
  - 7 kV ESD rating on analog input channels
  - 98 dB SNR, -107 dB THD
  - Dynamic range: up to 105 dB typical
  - Low power: 100 mW
  - Standby mode: 25 mW
- 64-lead LQFP package

### APPLICATIONS

- Power line monitoring and protection systems
- Multiphase motor control
- Instrumentation and control systems
- Multiaxis positioning systems
- Data acquisition systems (DAS)

### COMPANION PRODUCTS

- External References: [ADR421](#), [ADR431](#)
- Digital Isolators: [ADuM1402](#), [ADuM5000](#), [ADuM5402](#)
- Power: [ADIsimPower](#), [Supervisor Parametric Search](#)
- Additional companion products on the [AD7609 product page](#)*

Table 1. High Resolution, Bipolar Input, Simultaneous Sampling DAS Solutions

Resolution	Single-Ended Inputs	True Differential Inputs	Number of Simultaneous Sampling Channels
18 Bits	<a href="#">AD7608</a>	<a href="#">AD7609</a> <sup>1</sup>	8
16 Bits	<a href="#">AD7606</a> <a href="#">AD7606-6</a> <a href="#">AD7606-4</a>		8 6 4
14 Bits	<a href="#">AD7607</a>		8

<sup>1</sup> Protected by U.S. Patent Number 8,072,360 B2.

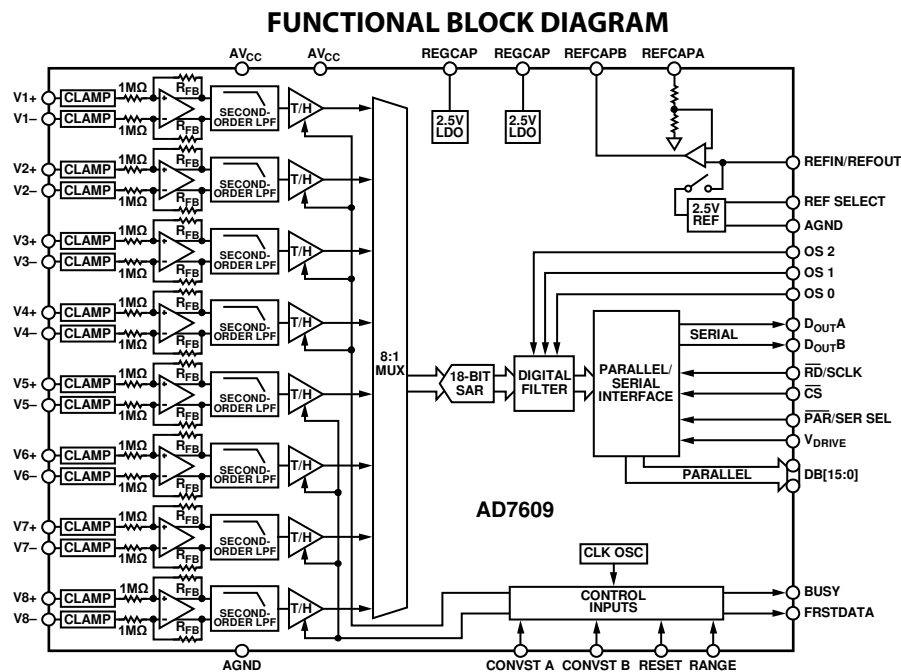


Figure 1.

### Rev. B

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# AD7609\* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## EVALUATION KITS

- AD7609 Evaluation Board

## DOCUMENTATION

### Data Sheet

- AD7609: 8-Channel Differential DAS with 18-Bit, Bipolar, Simultaneous Sampling ADC Data Sheet

## SOFTWARE AND SYSTEMS REQUIREMENTS

- AD7609 Evaluation Software

## TOOLS AND SIMULATIONS

- AD7609 Filter Model

## REFERENCE MATERIALS

### Technical Articles

- MS-2210: Designing Power Supplies for High Speed ADC

## DESIGN RESOURCES

- AD7609 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

## DISCUSSIONS

View all AD7609 EngineerZone Discussions.

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## TABLE OF CONTENTS

Features .....	1	Converter Details .....	21
Applications.....	1	Analog Input .....	21
Companion Products.....	1	ADC Transfer Function.....	22
Functional Block Diagram .....	1	Internal/External Reference.....	23
Revision History .....	2	Typical Connection Diagram .....	24
General Description .....	3	Power-Down Modes .....	24
Specifications.....	4	Conversion Control .....	25
Timing Specifications .....	7	Digital Interface .....	26
Absolute Maximum Ratings.....	11	Parallel Interface ( $\overline{\text{PAR}}/\text{SER SEL} = 0$ ).....	26
Thermal Resistance .....	11	Serial Interface ( $\overline{\text{PAR}}/\text{SER SEL} = 1$ ).....	26
ESD Caution.....	11	Reading During Conversion.....	27
Pin Configuration and Function Descriptions.....	12	Digital Filter .....	28
Typical Performance Characteristics .....	15	Layout Guidelines.....	32
Terminology .....	19	Outline Dimensions .....	34
Theory of Operation .....	21	Ordering Guide .....	34

## REVISION HISTORY

### 5/14—Rev. A to Rev. B

Changes to Patent Footnote .....	1
Changes to Figure 37.....	22
Changes to Figure 39 and Figure 40.....	23

### 2/12—Rev. 0 to Rev. A

Changes to Analog Input Ranges Section .....	21
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### 7/11—Revision 0: Initial Version

## GENERAL DESCRIPTION

The [AD7609](#) is an 18-bit, 8-channel, true differential, simultaneous sampling analog-to-digital data acquisition system (DAS). The part contains analog input clamp protection, a second-order antialiasing filter, a track-and-hold amplifier, an 18-bit charge redistribution successive approximation analog-to-digital converter (ADC), a flexible digital filter, a 2.5 V reference and reference buffer, and high speed serial and parallel interfaces.

The [AD7609](#) operates from a single 5 V supply and can accommodate  $\pm 10$  V and  $\pm 5$  V true bipolar differential input signals while sampling at throughput rates up to 200 kSPS for all channels. The input clamp protection circuitry can tolerate voltages up to  $\pm 16.5$  V. The [AD7609](#) has 1 M $\Omega$  analog input impedance regardless of sampling frequency. The single supply operation, on-chip filtering, and high input impedance eliminate the need for driver op amps and external bipolar supplies. The [AD7609](#) antialiasing filter has a  $-3$  dB cutoff frequency of 32 kHz and provides 40 dB antialias rejection when sampling at 200 kSPS. The flexible digital filter is pin driven, yields improvements in SNR, and reduces the  $-3$  dB bandwidth.

## SPECIFICATIONS

$V_{REF} = 2.5$  V external/internal,  $AV_{CC} = 4.75$  V to  $5.25$  V,  $V_{DRIVE} = 2.3$  V to  $5.25$  V;  $f_{SAMPLE} = 200$  kSPS,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>DYNAMIC PERFORMANCE</b>					
Signal-to-Noise Ratio (SNR) <sup>2,3</sup>	$f_{IN} = 1$ kHz sine wave unless otherwise noted				
	Oversampling by 16; $\pm 10$ V range; $f_{IN} = 160$ Hz	98	101		dB
	Oversampling by 16; $\pm 5$ V range; $f_{IN} = 160$ Hz		100		dB
	No oversampling; $\pm 10$ V range	90	91		dB
	No oversampling; $\pm 5$ V range	89.5	90.5		dB
Signal-to-(Noise + Distortion) (SINAD) <sup>2</sup>	No oversampling; $\pm 10$ V range	89.5	91		dB
	No oversampling; $\pm 5$ V range	89	90		dB
Dynamic Range	No oversampling; $\pm 10$ V range		91.5		dB
	No oversampling; $\pm 5$ V range		90.5		dB
Total Harmonic Distortion (THD) <sup>2,3</sup>	No oversampling; $\pm 10$ V range		-107	-97	dB
	No oversampling; $\pm 5$ V range		-110	-96	dB
Peak Harmonic or Spurious Noise (SFDR) <sup>2</sup>			-108		dB
Intermodulation Distortion (IMD) <sup>2</sup>	$f_a = 1$ kHz, $f_b = 1.1$ kHz				
Second-Order Terms			-110		dB
Third-Order Terms			-106		dB
Channel-to-Channel Isolation <sup>2</sup>	$f_{IN}$ on unselected channels up to 160 kHz		-95		dB
<b>ANALOG INPUT FILTER</b>					
Full Power Bandwidth	-3 dB, $\pm 10$ V range		32		kHz
	-3 dB, $\pm 5$ V range		23		kHz
	-0.1 dB, $\pm 10$ V range		13		kHz
	-0.1 dB, $\pm 5$ V range		10		kHz
$t_{GROUP DELAY}$	$\pm 10$ V range		7.1		$\mu s$
	$\pm 5$ V range		10.2		$\mu s$
<b>DC ACCURACY</b>					
Resolution	No missing codes	18			Bits
Differential Nonlinearity <sup>2</sup>			$\pm 0.75$	-0.99/+2	LSB <sup>4</sup>
Integral Nonlinearity <sup>2</sup>			$\pm 3$	$\pm 7.5$	LSB
Total Unadjusted Error (TUE)	$\pm 10$ V range		$\pm 10$		LSB
	$\pm 5$ V range		$\pm 90$		LSB
Positive Full-Scale Error <sup>2,5</sup>	External reference		$\pm 8$	$\pm 140$	LSB
	Internal reference		$\pm 40$		LSB
Positive Full-Scale Error Drift	External reference		$\pm 2$		ppm/ $^{\circ}C$
	Internal reference		$\pm 7$		ppm/ $^{\circ}C$
Positive Full-Scale Error Matching <sup>2</sup>	$\pm 10$ V range		12	80	LSB
	$\pm 5$ V range		40	100	LSB
Bipolar Zero Code Error <sup>2,6</sup>	$\pm 10$ V range		$\pm 3$	$\pm 24$	LSB
	$\pm 5$ V range		$\pm 3$	$\pm 48$	LSB
Bipolar Zero Code Error Drift	$\pm 10$ V range		10		$\mu V/^{\circ}C$
	$\pm 5$ V range		5		$\mu V/^{\circ}C$
Bipolar Zero Code Error Matching <sup>2</sup>	$\pm 10$ V range		2.7	30	LSB
	$\pm 5$ V range		13	65	LSB
Negative Full-Scale Error <sup>2,5</sup>	External reference		$\pm 8$	$\pm 140$	LSB
	Internal reference		$\pm 40$		LSB
Negative Full-Scale Error Drift	External reference		$\pm 4$		ppm/ $^{\circ}C$
	Internal reference		$\pm 8$		ppm/ $^{\circ}C$
Negative Full-Scale Error Matching <sup>2</sup>	$\pm 10$ V range		12	80	LSB
	$\pm 5$ V range		40	100	LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
<b>ANALOG INPUT</b>					
Differential Input Voltage Ranges	$V_{IN} = V_{x+} - (V_{x-})$ RANGE = 1; $\pm 10\text{ V}$ RANGE = 0; $\pm 5\text{ V}$	-20		+20	V
Absolute Voltage Input	$\pm 10\text{ V}$ range, see the Analog Input Clamp Protection section $\pm 5\text{ V}$ range, see the Analog Input Clamp Protection section	-10		+10	V
Common-Mode Input Range		-4	$\pm 5$	+4	V
CMRR			-70		dB
Analog Input Current	10 V, see Figure 28 5 V, see Figure 28		5.4		$\mu\text{A}$
Input Capacitance <sup>7</sup>			2.5		$\mu\text{A}$
Input Impedance			5		pF
			1		M $\Omega$
<b>REFERENCE INPUT/OUTPUT</b>					
Reference Input Voltage Range		2.475	2.5	2.525	V
DC Leakage Current				$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>7</sup>	REF SELECT = 1		7.5		pF
Reference Output Voltage	REFIN/REFOUT		2.49/ 2.505		V
Reference Temperature Coefficient			$\pm 10$		ppm/ $^{\circ}\text{C}$
<b>LOGIC INPUTS</b>					
Input High Voltage ( $V_{INH}$ )		$0.7 \times V_{DRIVE}$			V
Input Low Voltage ( $V_{INL}$ )				$0.3 \times V_{DRIVE}$	V
Input Current ( $I_{IN}$ )				$\pm 2$	$\mu\text{A}$
Input Capacitance ( $C_{IN}$ ) <sup>7</sup>			5		pF
<b>LOGIC OUTPUTS</b>					
Output High Voltage ( $V_{OH}$ )	$I_{SOURCE} = 100\ \mu\text{A}$	$V_{DRIVE} - 0.2$			V
Output Low Voltage ( $V_{OL}$ )	$I_{SINK} = 100\ \mu\text{A}$			0.2	V
Floating-State Leakage Current			$\pm 1$	$\pm 20$	$\mu\text{A}$
Floating-State Output Capacitance <sup>7</sup>			5		pF
Output Coding	Twos complement				
<b>CONVERSION RATE</b>					
Conversion Time	All eight channels included		4		$\mu\text{s}$
Track-and-Hold Acquisition Time			1		$\mu\text{s}$
Throughput Rate	Per channel, all eight channels included			200	kSPS
<b>POWER REQUIREMENTS</b>					
$A_{VCC}$		4.75		5.25	V
$V_{DRIVE}$		2.3		5.25	V
$I_{TOTAL}$	Digital inputs = 0 V or $V_{DRIVE}$				
Normal Mode (Static)			16	22	mA
Normal Mode (Operational) <sup>8</sup>	$f_{SAMPLE} = 200\text{ kSPS}$		20	28.5	mA
Standby Mode			5	8	mA
Shutdown Mode			2	11	$\mu\text{A}$

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Power Dissipation					
Normal Mode (Static)			80	115.5	mW
Normal Mode (Operational) <sup>8</sup>	$f_{\text{SAMPLE}} = 200 \text{ kSPS}$		100	157	mW
Standby Mode			25	42	mW
Shutdown Mode			10	60.5	$\mu\text{W}$

<sup>1</sup> Temperature range for B version is  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

<sup>2</sup> See the Terminology section.

<sup>3</sup> This specification applies when reading during a conversion or after a conversion. If reading during a conversion in parallel and serial modes with  $V_{\text{DRIVE}} = 5 \text{ V}$ , SNR typically reduces by 1.5 dB and THD by 3 dB.

<sup>4</sup> LSB means least significant bit. With  $\pm 5 \text{ V}$  input range,  $1 \text{ LSB} = 76.29 \mu\text{V}$ . With  $\pm 10 \text{ V}$  input range,  $1 \text{ LSB} = 152.58 \mu\text{V}$ .

<sup>5</sup> These specifications include the full temperature range variation and contribution from the internal reference buffer but do not include the error contribution from the external reference.

<sup>6</sup> Bipolar zero code error is calculated with respect to the analog input voltage. See the Analog Input Clamp Protection section.

<sup>7</sup> Sample tested during initial release to ensure compliance.

<sup>8</sup> Operational power/current figure includes contribution when running in oversampling mode.



## TIMING SPECIFICATIONS

$V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ,  $V_{DRIVE} = 2.3\text{ V to }5.25\text{ V}$ ,  $V_{REF} = 2.5\text{ V}$  external reference/ internal reference,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.<sup>1</sup>

Table 3.

Parameter	Limit at $T_{MIN}, T_{MAX}$			Unit	Description
	Min	Typ	Max		
PARALLEL/SERIAL/BYTE MODE					
$t_{CYCLE}$			5	$\mu\text{s}$	1/throughput rate
			5	$\mu\text{s}$	Parallel mode, reading during; or after conversion $V_{DRIVE} = 2.7\text{ V to }5.25\text{ V}$ ; or serial mode: $V_{DRIVE} = 3.3\text{ V to }5.25\text{ V}$ , reading during a conversion using $D_{OUTA}$ and $D_{OUTB}$ lines
			10.1	$\mu\text{s}$	Parallel mode reading after conversion $V_{DRIVE} = 2.3\text{ V}$
			11.5	$\mu\text{s}$	Serial mode reading after conversion; $V_{DRIVE} = 2.7\text{ V}$ , $D_{OUTA}$ and $D_{OUTB}$ lines
$t_{CONV}$					Serial mode reading after a conversion; $V_{DRIVE} = 2.3\text{ V}$ , $D_{OUTA}$ and $D_{OUTB}$ lines
					Conversion time
	3.45	4	4.15	$\mu\text{s}$	Oversampling off
	7.87		9.1	$\mu\text{s}$	Oversampling by 2
	16.05		18.8	$\mu\text{s}$	Oversampling by 4
	33		39	$\mu\text{s}$	Oversampling by 8
	66		78	$\mu\text{s}$	Oversampling by 16
	133		158	$\mu\text{s}$	Oversampling by 32
	257		315	$\mu\text{s}$	Oversampling by 64
$t_{WAKE-UP\ STANDBY}$			100	$\mu\text{s}$	$\overline{STBY}$ rising edge to $CONVST$ x rising edge; power-up time from standby mode
$t_{WAKE-UP\ SHUTDOWN}$					
Internal Reference			30	ms	$\overline{STBY}$ rising edge to $CONVST$ x rising edge; power-up time from shutdown mode
External Reference			13	ms	$\overline{STBY}$ rising edge to $CONVST$ x rising edge; power-up time from shutdown mode
$t_{RESET}$	50			ns	RESET high pulse width
$t_{OS\_SETUP}$	20			ns	BUSY to OS x pin setup time
$t_{OS\_HOLD}$	20			ns	BUSY to OS x pin hold time
$t_1$			45	ns	$CONVST$ x high to BUSY high
$t_2$	25			ns	Minimum $CONVST$ x low pulse
$t_3$	25			ns	Minimum $CONVST$ x high pulse
$t_4$	0			ns	BUSY falling edge to $\overline{CS}$ falling edge setup time
$t_5^2$			0.5	ms	Maximum delay allowed between $CONVST$ A, $CONVST$ B rising edges
$t_6$			25	ns	Maximum time between last $\overline{CS}$ rising edge and BUSY falling edge
$t_7$	25			ns	Minimum delay between RESET low to $CONVST$ x high
PARALLEL READ OPERATION					
$t_8$	0			ns	$\overline{CS}$ to $\overline{RD}$ setup time
$t_9$	0			ns	$\overline{CS}$ to $\overline{RD}$ hold time
$t_{10}$					$\overline{RD}$ low pulse width
	19			ns	$V_{DRIVE}$ above 4.75 V
	24			ns	$V_{DRIVE}$ above 3.3 V
	30			ns	$V_{DRIVE}$ above 2.7 V
	37			ns	$V_{DRIVE}$ above 2.3 V
$t_{11}$	15			ns	$\overline{RD}$ high pulse width
$t_{12}$	22			ns	$\overline{CS}$ high pulse width (see Figure 5); $\overline{CS}$ and $\overline{RD}$ linked

Parameter	Limit at T <sub>MIN</sub> , T <sub>MAX</sub>			Unit	Description
	Min	Typ	Max		
t <sub>13</sub>			19	ns	Delay from $\overline{CS}$ until DB[15:0] three-state disabled
			24	ns	V <sub>DRIVE</sub> above 4.75 V
			30	ns	V <sub>DRIVE</sub> above 3.3 V
			37	ns	V <sub>DRIVE</sub> above 2.7 V
t <sub>14</sub> <sup>3</sup>			37	ns	V <sub>DRIVE</sub> above 2.3 V
			19	ns	Data access time after $\overline{RD}$ falling edge
			24	ns	V <sub>DRIVE</sub> above 4.75 V
			30	ns	V <sub>DRIVE</sub> above 3.3 V
t <sub>15</sub>	6			ns	V <sub>DRIVE</sub> above 2.7 V
t <sub>16</sub>	6			ns	V <sub>DRIVE</sub> above 2.3 V
t <sub>17</sub>			22	ns	Delay from $\overline{CS}$ rising edge to DB[15:0] three-state enabled
<b>SERIAL READ OPERATION</b>					
f <sub>SCLK</sub>			20	MHz	Frequency of serial read clock
			15	MHz	V <sub>DRIVE</sub> above 4.75 V
			12.5	MHz	V <sub>DRIVE</sub> above 3.3 V
			10	MHz	V <sub>DRIVE</sub> above 2.7 V
t <sub>18</sub>			18	ns	V <sub>DRIVE</sub> above 2.3 V
			23	ns	Delay from $\overline{CS}$ until D <sub>OUT</sub> A/D <sub>OUT</sub> B three-state disabled/delay from $\overline{CS}$ until MSB valid
			35	ns	V <sub>DRIVE</sub> = 2.3 V to 2.7 V
t <sub>19</sub> <sup>3</sup>			20	ns	Data access time after SCLK rising edge
			26	ns	V <sub>DRIVE</sub> above 4.75 V
			32	ns	V <sub>DRIVE</sub> above 3.3 V
			39	ns	V <sub>DRIVE</sub> above 2.7 V
t <sub>20</sub>	0.4 t <sub>SCLK</sub>			ns	V <sub>DRIVE</sub> above 2.3 V
t <sub>21</sub>	0.4 t <sub>SCLK</sub>			ns	SCLK low pulse width
t <sub>22</sub>	7			ns	SCLK high pulse width
t <sub>23</sub>			22	ns	SCLK rising edge to D <sub>OUT</sub> A/D <sub>OUT</sub> B valid hold time
					$\overline{CS}$ rising edge to D <sub>OUT</sub> A/D <sub>OUT</sub> B three-state enabled
<b>FRSTDATA OPERATION</b>					
t <sub>24</sub>			18	ns	Delay from $\overline{CS}$ falling edge until FRSTDATA three-state disabled
			23	ns	V <sub>DRIVE</sub> above 4.75 V
			30	ns	V <sub>DRIVE</sub> above 3.3 V
			35	ns	V <sub>DRIVE</sub> above 2.7 V
t <sub>25</sub>			35	ns	V <sub>DRIVE</sub> above 2.3 V
			18	ns	Delay from $\overline{CS}$ falling edge until FRSTDATA high, serial mode
			23	ns	V <sub>DRIVE</sub> above 4.75 V
			30	ns	V <sub>DRIVE</sub> above 3.3 V
t <sub>26</sub>			35	ns	V <sub>DRIVE</sub> above 2.7 V
			19	ns	V <sub>DRIVE</sub> above 2.3 V
			23	ns	Delay from $\overline{RD}$ falling edge to FRSTDATA high
			30	ns	V <sub>DRIVE</sub> above 4.75 V
		35	ns	V <sub>DRIVE</sub> above 3.3 V	
					V <sub>DRIVE</sub> above 2.7 V
					V <sub>DRIVE</sub> above 2.3 V

Parameter	Limit at $T_{MIN}, T_{MAX}$			Unit	Description
	Min	Typ	Max		
$t_{27}$			22	ns	Delay from $\overline{RD}$ falling edge to $\overline{FRSTDATA}$ low $V_{DRIVE} = 3.3\text{ V to }5.25\text{ V}$
			29	ns	$V_{DRIVE} = 2.3\text{ V to }2.7\text{ V}$
$t_{28}$			20	ns	Delay from 18 <sup>th</sup> SCLK falling edge to $\overline{FRSTDATA}$ low $V_{DRIVE} = 3.3\text{ V to }5.25\text{ V}$
			27	ns	$V_{DRIVE} = 2.3\text{ V to }2.7\text{ V}$
$t_{29}$			29	ns	Delay from $\overline{CS}$ rising edge until $\overline{FRSTDATA}$ three-state enabled

<sup>1</sup> Sample tested during initial release to ensure compliance. All input signals are specified with  $t_r = t_f = 5\text{ ns}$  (30% to 70% of  $V_{DD}$ ) and timed from a voltage level of 1.6 V.  
<sup>2</sup> The delay between the  $\overline{CONVST}$  x signals was measured as the maximum time allowed while ensuring a <40 LSB performance matching between channel sets.  
<sup>3</sup> A buffer is used on the data output pins for these measurements, which is equivalent to a load of 20 pF on the output pins.

Timing Diagrams

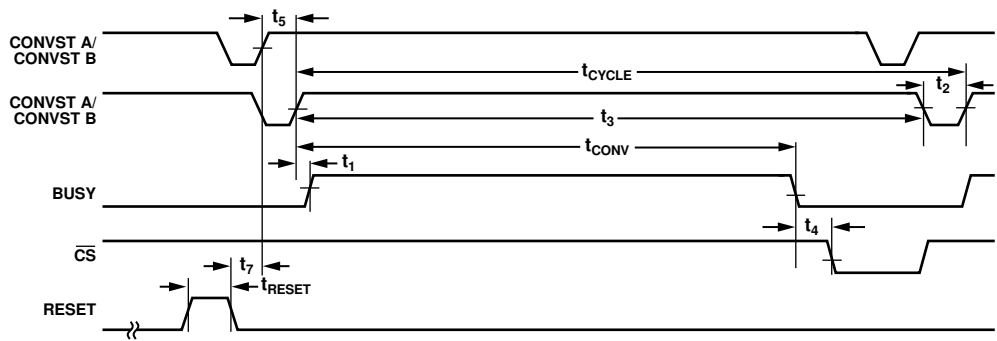


Figure 2.  $\overline{CONVST}$  x Timing—Reading After a Conversion

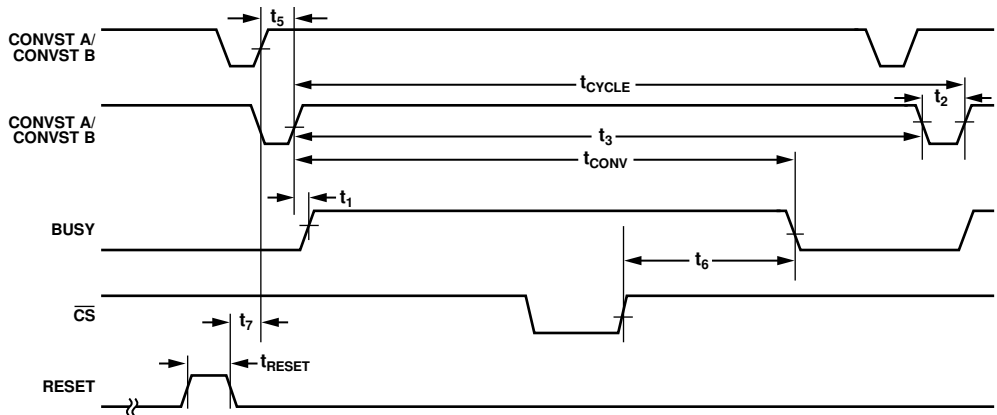


Figure 3.  $\overline{CONVST}$  x Timing—Reading During a Conversion

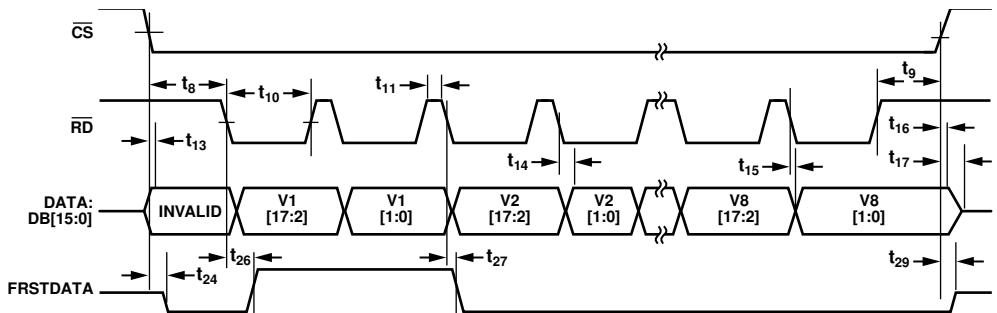


Figure 4. Parallel Mode Separate  $\overline{CS}$  and  $\overline{RD}$  Pulses

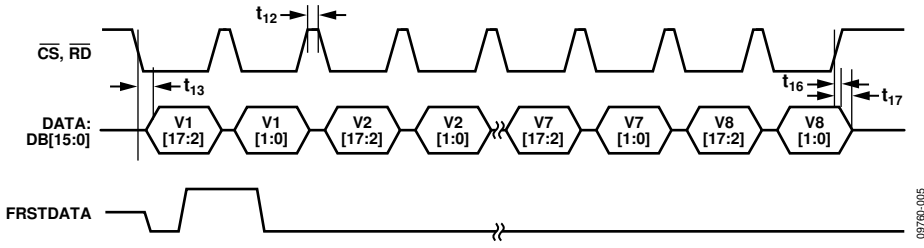


Figure 5.  $\overline{CS}$  and  $\overline{RD}$  Linked Parallel Mode

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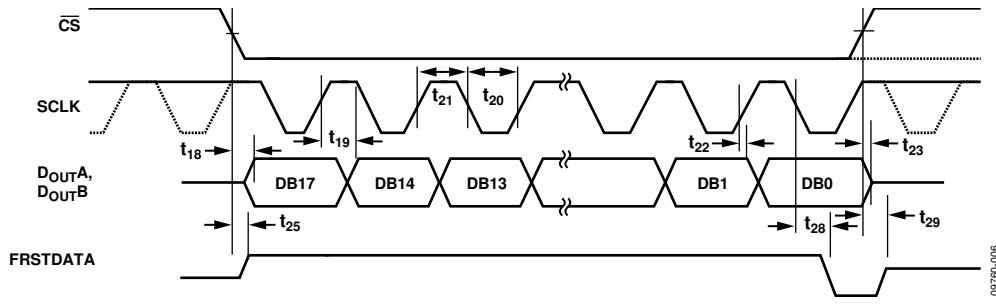


Figure 6. Serial Read Operation

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## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Rating
$AV_{CC}$ to AGND	−0.3 V to +7 V
$V_{DRIVE}$ to AGND	−0.3 V to $AV_{CC} + 0.3$ V
Analog Input Voltage to AGND <sup>1</sup>	±16.5 V
Digital Input Voltage to AGND	−0.3 V to $V_{DRIVE} + 0.3$ V
Digital Output Voltage to AGND	−0.3 V to $V_{DRIVE} + 0.3$ V
REFIN to AGND	−0.3 V to $AV_{CC} + 0.3$ V
Input Current to Any Pin Except Supplies <sup>1</sup>	±10 mA
Operating Temperature Range B Version	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Pb/SN Temperature, Soldering Reflow (10 sec to 30 sec)	240(+0)°C
Pb-Free Temperature, Soldering Reflow	260(+0)°C
ESD (All Pins Except Analog Inputs)	2 kV
ESD (Analog Input Pins Only)	7 kV

<sup>1</sup> Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. These specifications apply to a 4-layer board.

**Table 5. Thermal Resistance**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
64-Lead LQFP	45	11	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

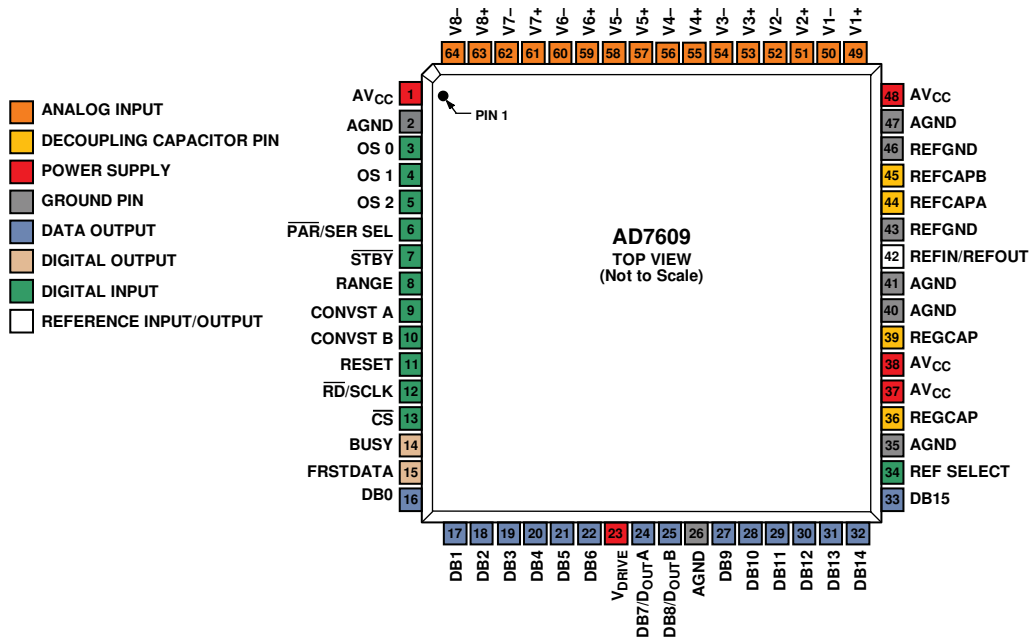


Figure 7. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Type <sup>1</sup>	Mnemonic	Description
1, 37, 38, 48	P	AV <sub>CC</sub>	Analog Supply Voltage 4.75 V to 5.25 V. This supply voltage is applied to the internal front-end amplifiers and to the ADC core. These supply pins should be decoupled to AGND.
2, 26, 35, 40, 41, 47	P	AGND	Analog Ground. This pin is the ground reference point for all analog circuitry on the AD7609. All analog input signals and external reference signals should be referred to these pins. All six of these AGND pins should connect to the AGND plane of a system.
23	P	V <sub>DRIVE</sub>	Logic Power Supply Input. The voltage (2.3 V to 5 V) supplied at this pin determines the operating voltage of the interface. This pin is nominally at the same supply as the supply of the host interface (that is, DSP, FPGA).
36, 39	P	REGCAP	Decoupling Capacitor Pins for Voltage Output from Internal Regulator. These output pins should be decoupled separately to AGND using a 1 $\mu$ F capacitor. The voltage on these output pins is in the range of 2.5 V to 2.7 V.
49, 51, 53, 55, 57, 59, 61, 63	AI+	V1+ to V8+	Analog Input V1+ to Analog Input V8+. These pins are the positive terminal of the true differential analog inputs. The analog input range of these channels is determined by the RANGE pin.
50, 52, 54, 56, 58, 60, 62, 64	AI-	V1- to V8-	Analog Input V1- to Analog Input V8-. These are the negative terminals of the true differential analog inputs. The analog input range of these channels is determined by the RANGE pin. The signal on this pin should be 180° out of phase with the corresponding Vx+ pin.
42	REF	REFIN/REFOUT	Reference Input/ Reference Output. The on-chip reference of 2.5 V is available on this pin for external use if the REF SELECT pin is set to a logic high. Alternatively, the internal reference can be disabled by setting the REF SELECT pin to a logic low and an external reference of 2.5 V can be applied to this input. See the Internal/External Reference section. Decoupling is required on this pin for both the internal or external reference options. A 10 $\mu$ F capacitor should be applied from this pin to ground close to the REFGND pins.
34	DI	REF SELECT	Internal/External Reference Selection Input. Logic input. If this pin is set to logic high, the internal reference is selected and is enabled. If this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin.
44, 45	REF	REFCAPA, REFCAPB	Reference Buffer Output Force/Sense Pins. These pins must be connected together and decoupled to AGND using a low ESR 10 $\mu$ F ceramic capacitor.
43, 46	REF	REFGND	Reference Ground Pins. These pins should be connected to AGND.

Pin No.	Type <sup>1</sup>	Mnemonic	Description
8	DI	RANGE	Analog Input Range Selection. Logic input. The polarity on this pin determines the input range of the analog input channels. If this pin is tied to a logic high, the analog input range is $\pm 10$ V for all channels. If this pin is tied to a logic low, the analog input range is $\pm 5$ V for all channels. A logic change on this pin has an immediate effect on the analog input range. Changing this pin during a conversion is not recommended. See the Analog Input section for more details.
6	DI	$\overline{\text{PAR}}$ / SER SEL	Parallel/Serial Interface Selection Input. Logic input. If this pin is tied to a logic low, the parallel interface is selected. If this pin is tied to a logic high, the serial interface is selected. In serial mode, the $\overline{\text{RD}}$ /SCLK pin functions as the serial clock input. The DB7/D <sub>OUT</sub> A and DB8/D <sub>OUT</sub> B pins function as serial data outputs. When the serial interface is selected, the DB[15:9] and DB[6:0] pins should be tied to AGND.
9, 10	DI	CONVST A, CONVST B	Conversion Start Input A, Conversion Start Input B. Logic inputs. These logic inputs are used to initiate conversions on the analog input channels. For simultaneous sampling of all input channels, CONVST A and CONVST B can be shorted together and a single conversion start signal applied. Alternatively, CONVST A can be used to initiate simultaneous sampling for V1, V2, V3, and V4, and CONVST B can be used to initiate simultaneous sampling on the other analog inputs (V5, V6, V7, and V8). This is only possible when oversampling is not switched on. When the CONVST A or CONVST B pin transitions from low to high, the front-end track-and-hold circuitry for their respective analog inputs is set to hold. This function allows a phase delay to be created inherently between the sets of analog inputs.
13	DI	$\overline{\text{CS}}$	Chip Select. This active low logic input frames the data transfer. When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus (DB[15:0]) is enabled and the conversion result is output on the parallel data bus lines. In serial mode, the $\overline{\text{CS}}$ is used to frame the serial read transfer and clocks out the MSB of the serial output data.
12	DI	$\overline{\text{RD}}$ /SCLK	Parallel Data Read Control Input When Parallel Interface is Selected ( $\overline{\text{RD}}$ )/Serial Clock Input When Serial Interface is Selected (SCLK). When both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are logic low in parallel mode, the output bus is enabled. In parallel mode, two $\overline{\text{RD}}$ pulses are required to read the full 18 bits of conversion results from each channel. The first $\overline{\text{RD}}$ pulse outputs DB[17:2], and the second $\overline{\text{RD}}$ pulses outputs DB[1:0]. In serial mode, this pin acts as the serial clock input for data transfers. The $\overline{\text{CS}}$ falling edge takes the data output lines, D <sub>OUT</sub> A and D <sub>OUT</sub> B, out of three-state and clocks out the MSB of the conversion result. The rising edge of SCLK clocks all subsequent data bits onto the serial data outputs, D <sub>OUT</sub> A and D <sub>OUT</sub> B. For further information, see the Conversion Control section.
14	DO	BUSY	Busy Output. This pin transitions to a logic high after both CONVST A and CONVST B rising edges and indicates that the conversion process has started. The BUSY output remains high until the conversion process for all channels is complete. The falling edge of BUSY signals that the conversion data is being latched into the output data registers and will be available to be read after a time, $t_4$ . Any data read while BUSY is high should be complete before the falling edge of BUSY occurs. Rising edges on CONVST A or CONVST B have no effect while the BUSY signal is high.
11	DI	RESET	Reset Input. When set to logic high, the rising edge of RESET resets the AD7609. The part must receive a RESET pulse after power-up. To achieve the specified performance after the RESET signal, the $t_{\text{WAKE\_UP SHUTDOWN}}$ time should elapse between power-on and the RESET pulse. The RESET high pulse should be typically 100 ns wide. If a RESET pulse is applied during a conversion, the conversion is aborted. If a RESET pulse is applied during a read, the contents of the output registers reset to all zeros.
15	DO	FRSTDATA	Digital Output. The FRSTDATA output signal indicates when the first channel, V1, is being read back on either the parallel or serial interface. When the $\overline{\text{CS}}$ input is high, the FRSTDATA output pin is in three-state. The falling edge of $\overline{\text{CS}}$ takes FRSTDATA out of three-state. In parallel mode, the falling edge of $\overline{\text{RD}}$ corresponding to the result of V1 then sets the FRSTDATA pin high, indicating that the result from V1 is available on the output data bus. The FRSTDATA output returns to a logic low following the third falling edge of $\overline{\text{RD}}$ . In serial mode, FRSTDATA goes high on the falling edge of $\overline{\text{CS}}$ as this clocks out the MSB of V1 on DOUTA. It returns low on the 18th SCLK falling edge after the $\overline{\text{CS}}$ falling edge. See the Conversion Control section for more details.
7	DI	$\overline{\text{STBY}}$	Standby Mode Input. This pin is used to place the AD7609 into one of two power-down modes: standby mode or shutdown mode. The power-down mode entered depends on the state of the RANGE pin, as shown in Table 8. When in standby mode, all circuitry except the on-chip reference, regulators, and regulator buffers is powered down. When in shutdown mode, all circuitry is powered down.

Pin No.	Type <sup>1</sup>	Mnemonic	Description
5, 4, 3	DI	OS [2:0]	Oversampling Mode Pins. Logic inputs. These inputs are used to select the oversampling ratio. OS 2 is the MSB control bit, and OS 0 is the LSB control bit. See the Digital Filter section for additional details on the oversampling mode of operation and Table 9 for oversampling bit decoding.
33	DO/DI	DB15	Parallel Output Data Bits, Data Bit 15. When $\overline{\text{PAR/SER SEL}} = 0$ , this pin acts as three-state parallel digital output pin. This pin is used to output DB17 of the conversion result during the first $\overline{\text{RD}}$ pulse and DB1 of the same conversion result during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR/SER SEL}} = 1$ , this pin should be tied to AGND.
32	DO/DI	DB14	Parallel Output Data Bits, Data Bit 14. When $\overline{\text{PAR/SER SEL}} = 0$ , this pin acts as three-state parallel digital output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB16 of the conversion result during the first $\overline{\text{RD}}$ pulse and DB0 of the same conversion result during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR/SER SEL}} = 1$ , this pin should be tied to AGND.
31 to 27	DO	DB[13:9]	Parallel Output Data Bits, Data Bit 13 to Data Bit 9. When $\overline{\text{PAR/SER SEL}} = 0$ , these pins act as three-state parallel digital input/output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB15 to DB11 of the conversion result during the first $\overline{\text{RD}}$ pulse and output 0 during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR/SER SEL}} = 1$ , these pins should be tied to AGND.
24	DO	DB7/D <sub>OUTA</sub>	Parallel Output Data Bit 7 (DB7)/Serial Interface Data Output Pin (D <sub>OUTA</sub> ). When $\overline{\text{PAR/SER SEL}} = 0$ , this pin acts as a three-state parallel digital input/output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB9 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$ , this pin functions as D <sub>OUTA</sub> and outputs serial conversion data. See the Conversion Control section for further details.
25	DO	DB8/D <sub>OUTB</sub>	Parallel Output Data Bit 8 (DB8)/Serial Interface Data Output Pin (D <sub>OUTB</sub> ). When $\overline{\text{PAR/SER SEL}} = 0$ , this pin acts as a three-state parallel digital input/output pin. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, this pin is used to output DB10 of the conversion result. When $\overline{\text{PAR/SER SEL}} = 1$ , this pin functions as D <sub>OUTB</sub> and outputs serial conversion data. See the Conversion Control section for further details.
22 to 16	DO	DB[6:0]	Parallel Output Data Bits, Data Bit 6 to Data Bit 0. When $\overline{\text{PAR/SER SEL}} = 0$ , these pins act as three-state parallel digital input/output pins. When $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are low, these pins are used to output DB8 to DB2 of the conversion result during the first $\overline{\text{RD}}$ pulse and output 0 during the second $\overline{\text{RD}}$ pulse. When $\overline{\text{PAR/SER SEL}} = 1$ , these pins should be tied to AGND.

<sup>1</sup> Refers to classification of pin type; P denotes power, AI denotes analog input, REF denotes reference, DI denotes digital input, DO denotes digital output.



TYPICAL PERFORMANCE CHARACTERISTICS

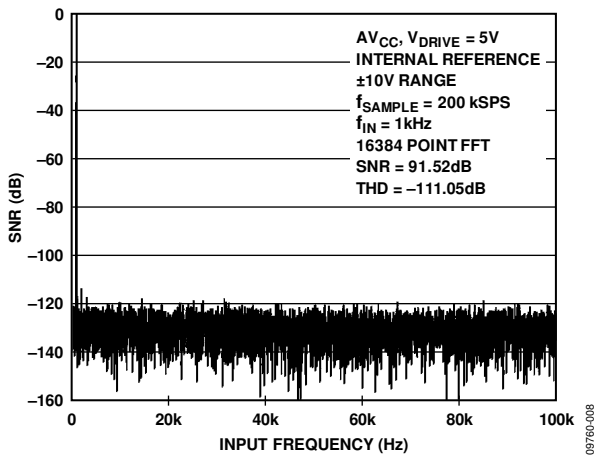


Figure 8. FFT Plot, ±10V Range

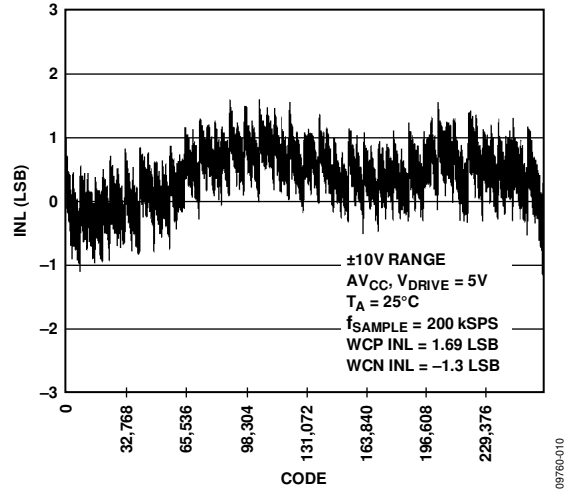


Figure 11. Typical INL, ±10V Range

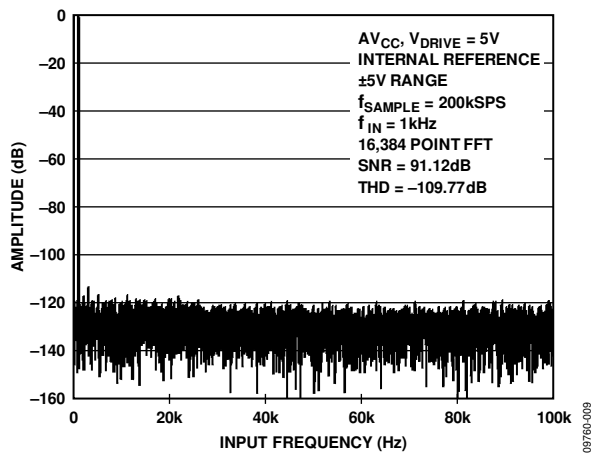


Figure 9. FFT Plot, ±5V Range

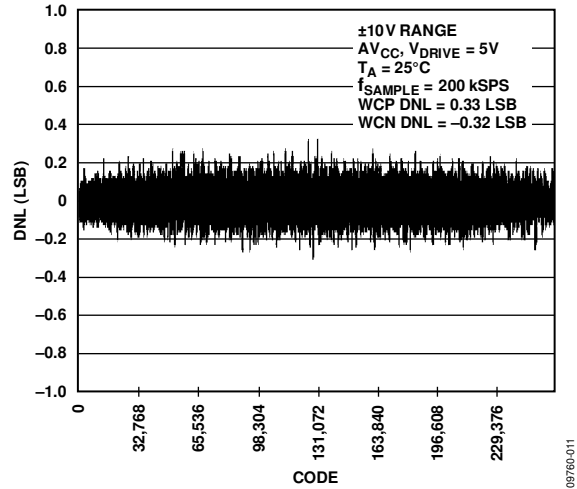


Figure 12. Typical DNL, ±10V Range

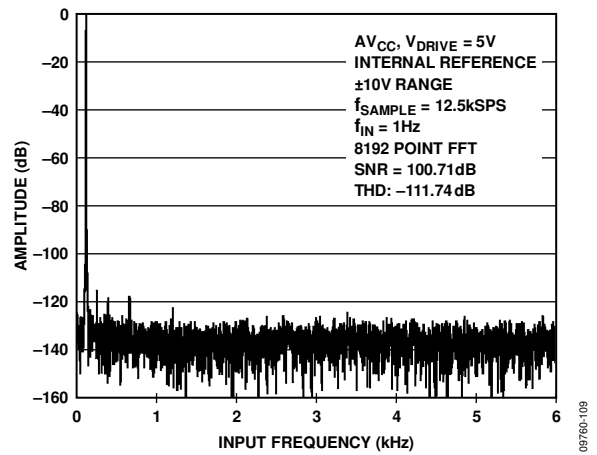


Figure 10. FFT Plot, ±10V Range

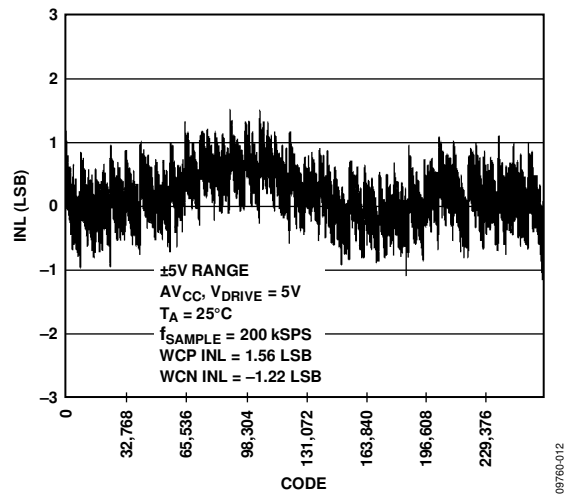


Figure 13. Typical INL, ±5V Range

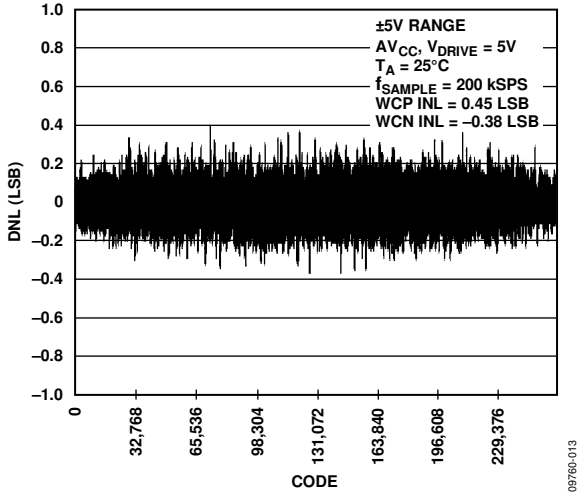


Figure 14. Typical DNL, ±5V Range

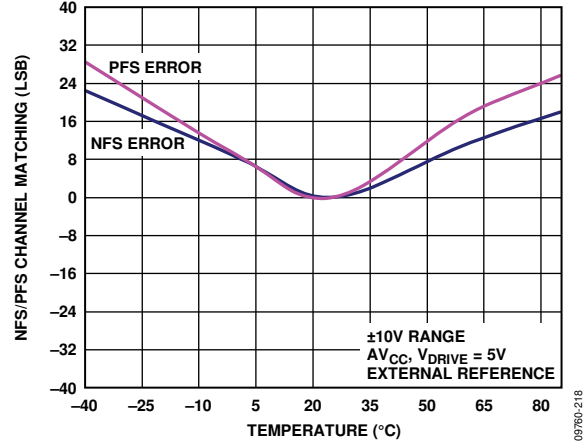


Figure 17. NFS and PFS Error Matching

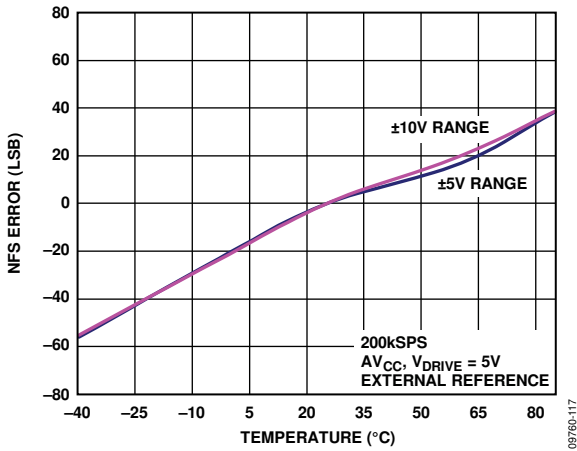


Figure 15. NFS Error vs. Temperature

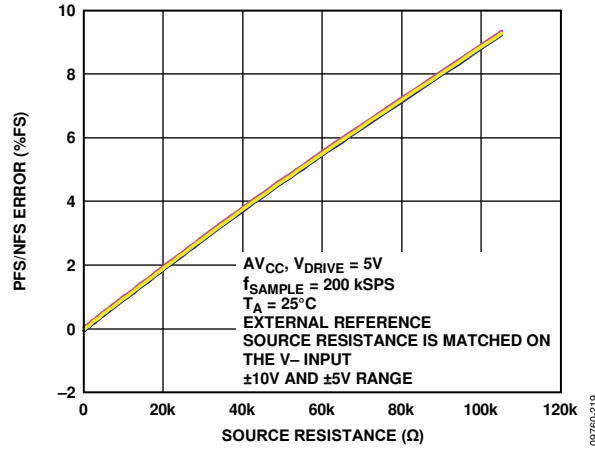


Figure 18. PFS and NFS Error vs. Source Resistance

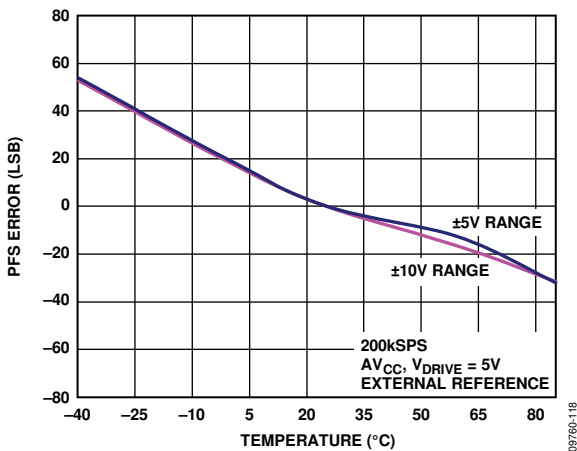


Figure 16. PFS Error vs. Temperature

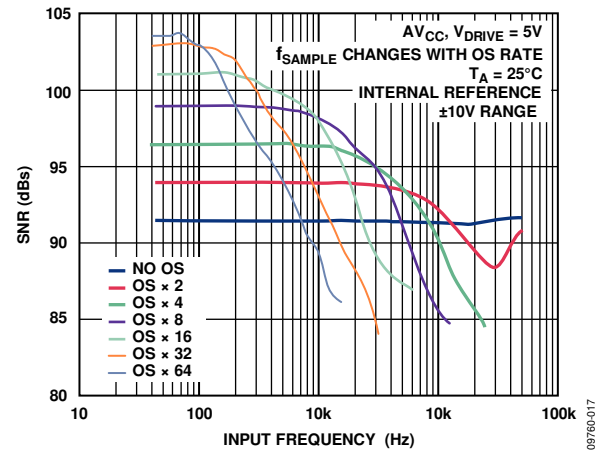


Figure 19. SNR vs. Input Frequency, ±10V Range

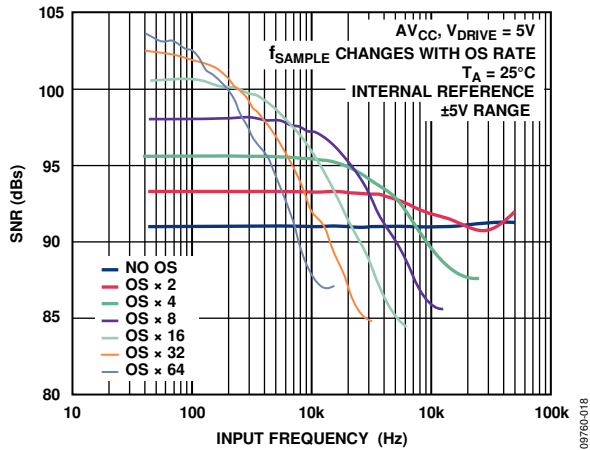


Figure 20. SNR vs. Input Frequency, ±5 V Range

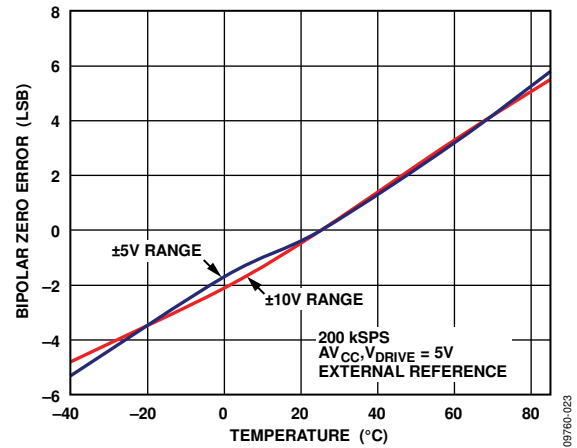


Figure 23. Bipolar Zero Code Error vs. Temperature

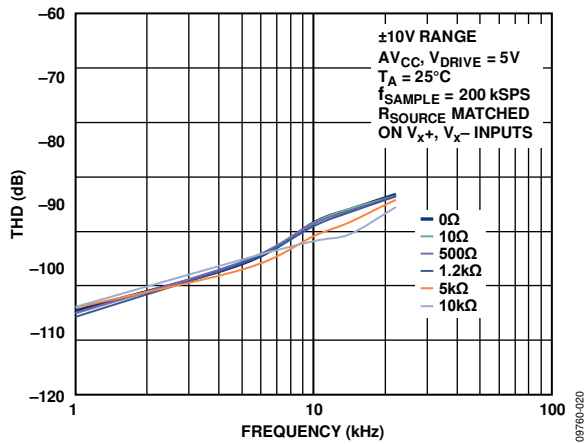


Figure 21. THD vs. Input Frequency for Various Source Impedances, ±10 V Range

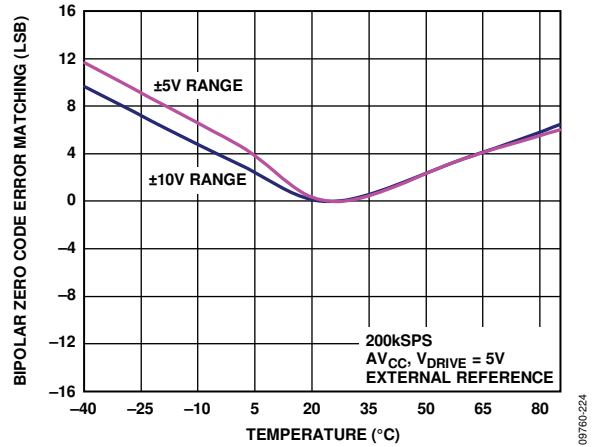


Figure 24. Bipolar Zero Code Error Matching Between Channels

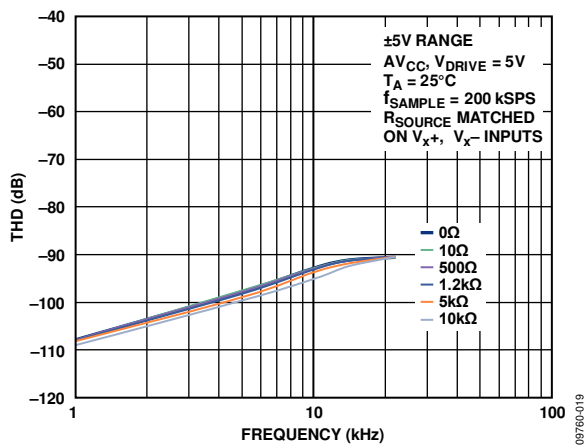


Figure 22. THD vs. Input Frequency for Various Source Impedances, ±5 V Range

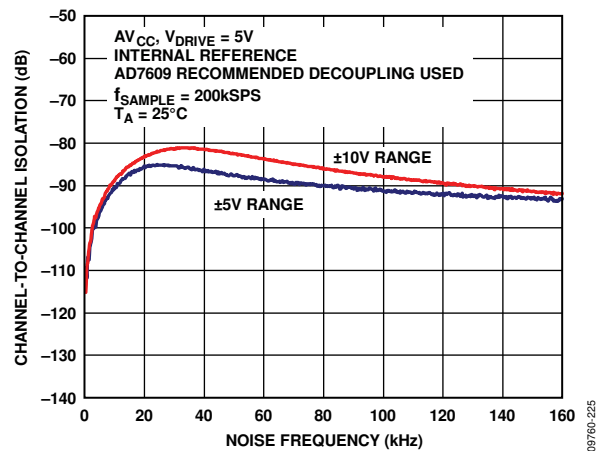


Figure 25. Channel-to-Channel Isolation

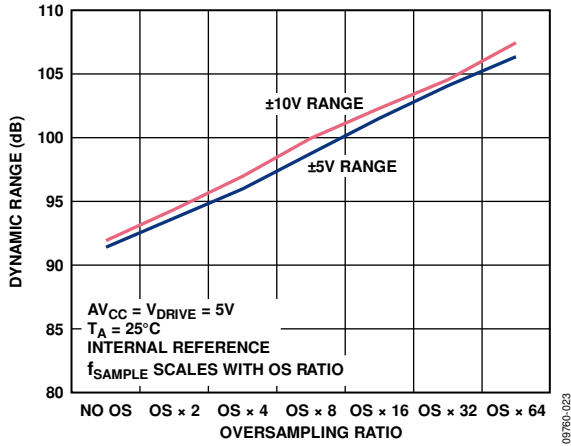


Figure 26. Dynamic Range vs. Oversampling Ratio

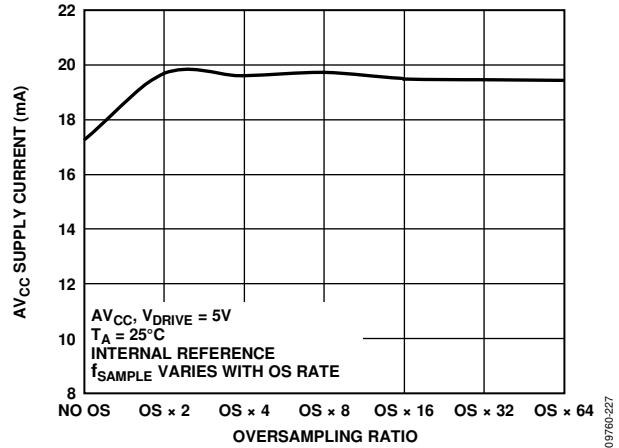


Figure 29. Supply Current vs. Oversampling Rate

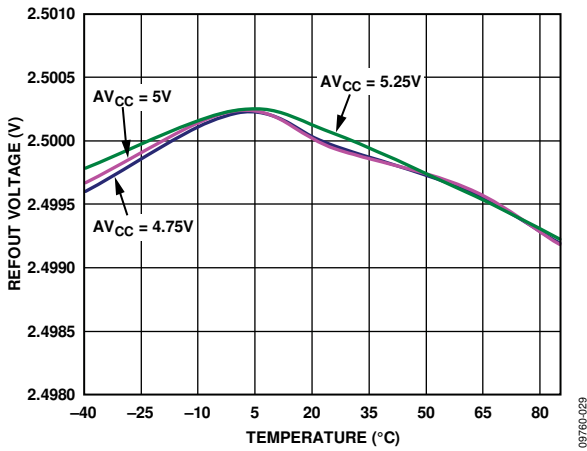


Figure 27. Reference Output Voltage vs. Temperature for Different Supply Voltages

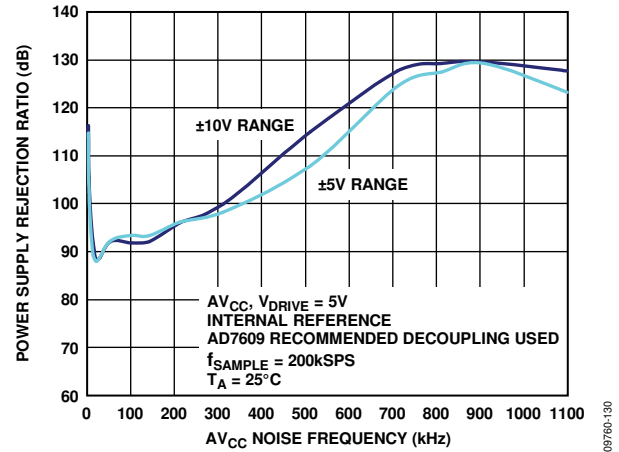


Figure 30. PSRR

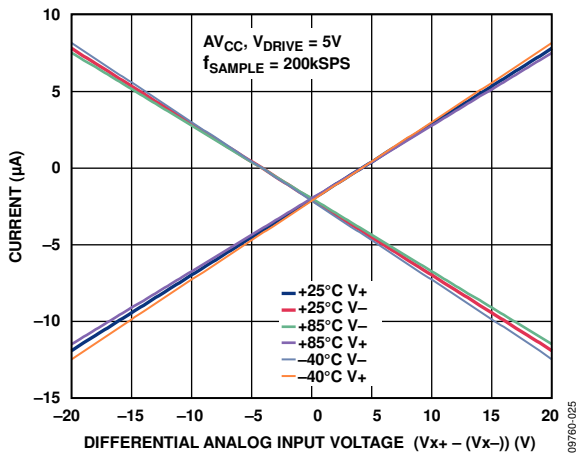


Figure 28. Analog Input Current vs. Input Voltage Over Temperature

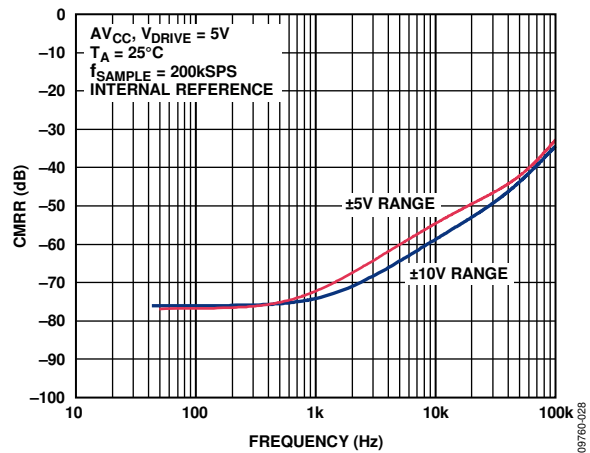


Figure 31. CMRR vs. Common-Mode Ripple Frequency

## TERMINOLOGY

### Integral Nonlinearity

The maximum deviation from a straight line passing through the endpoints of the ADC transfer function. The endpoints of the transfer function are zero scale, a ½ LSB below the first code transition, and full scale at ½ LSB above the last code transition.

### Differential Nonlinearity

The difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

### Bipolar Zero Code Error

The deviation of the midscale transition (all 1s to all 0s) from the ideal  $V_{IN}$  voltage, that is, AGND.

### Bipolar Zero Code Error Match

The difference in bipolar zero code error between any two input channels.

### Positive Full-Scale Error

The last transition (from 011 . . . 10 to 011 . . . 11 in twos complement coding) should occur for an analog voltage 1½ LSB below the nominal full scale (9.99977 V for the ±10 V range and 4.99988 V for the ±5 V range). The positive full-scale error is the deviation of the actual level of the last transition from the ideal level.

### Positive Full-Scale Error Match

The difference in positive full-scale error between any two input channels.

### Negative Full-Scale Error

The first transition (from 100 . . . 00 to 100 . . . 01 in twos complement coding) should occur for an analog voltage ½ LSB above the negative full scale (−9.999923 V for the ±10 V range and −4.9999618 for the ±5 V range). The negative full-scale error is the deviation of the actual level of the first transition from the ideal level.

### Negative Full-Scale Error Match

The difference in negative full-scale error between any two input channels.

### Track-and-Hold Acquisition Time

The track-and-hold amplifier returns to track mode at the end of the conversion. The track-and-hold acquisition time is the time required for the output of the track-and-hold amplifier to reach its final value, within ±1 LSB, after the end of the conversion. See the Track-and-Hold Amplifiers section for more details.

### Signal-to-(Noise + Distortion) Ratio

The measured ratio of signal-to-(noise + distortion) at the output of the ADC. The signal is the rms amplitude of the fundamental. Noise is the sum of all nonfundamental signals up to half the sampling frequency ( $f_s/2$ , excluding dc). The ratio depends on the number of quantization levels in the digitization process: the more levels, the smaller the quantization noise. The theoretical signal-to-(noise + distortion) ratio for an ideal N-bit converter with a sine wave input is given by

$$\text{Signal-to-(Noise + Distortion)} = (6.02 N + 1.76) \text{ dB}$$

Thus, for an 18-bit converter, this is 110.12 dB.

### Total Harmonic Distortion (THD)

The ratio of the rms sum of the harmonics to the fundamental. For the AD7609, it is defined as

$$\text{THD (dB)} = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2 + V_7^2 + V_8^2 + V_9^2}}{V_1}$$

where:

$V_1$  is the rms amplitude of the fundamental.

$V_2$  to  $V_9$  are the rms amplitudes of the second through ninth harmonics.

### Peak Harmonic or Spurious Noise

The ratio of the rms value of the next largest component in the ADC output spectrum (up to  $f_s/2$ , excluding dc) to the rms value of the fundamental. Normally, the value of this specification is determined by the largest harmonic in the spectrum, but for ADCs where the harmonics are buried in the noise floor, it is determined by a noise peak.

### Intermodulation Distortion

With inputs consisting of sine waves at two frequencies,  $f_a$  and  $f_b$ , any active device with nonlinearities creates distortion products at sum and difference frequencies of  $m f_a \pm n f_b$ , where  $m, n = 0, 1, 2, 3$ . Intermodulation distortion terms are those for which neither  $m$  nor  $n$  is equal to 0. For example, the second-order terms include  $(f_a + f_b)$  and  $(f_a - f_b)$ , and the third-order terms include  $(2f_a + f_b)$ ,  $(2f_a - f_b)$ ,  $(f_a + 2f_b)$ , and  $(f_a - 2f_b)$ .

The calculation of the intermodulation distortion is per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels (dB).

**Power Supply Rejection (PSR)**

Variations in power supply affect the full-scale transition but not the converter's linearity. Power supply rejection is the maximum change in full-scale transition point due to a change in power supply voltage from the nominal value. The power supply rejection ratio is defined as the ratio of the power in the ADC output at full-scale frequency,  $f$ , to the power of a 200 mV p-p sine wave applied to the ADC  $V_{DD}$  and  $V_{SS}$  supplies of Frequency  $f_s$ .

$$PSRR \text{ (dB)} = 10 \log (P_f/P_{f_s})$$

where:

$P_f$  is equal to the power at Frequency  $f$  in the ADC output.

$P_{f_s}$  is equal to the power at Frequency  $f_s$  coupled onto the  $V_{DD}$  and  $V_{SS}$  supplies.

**Channel-to-Channel Isolation**

Channel-to-channel isolation is a measure of the level of crosstalk between any two channels. It is measured by applying a full-scale, 10 kHz sine wave signal to all unselected input channels and determining the degree to which the signal attenuates in the selected channel with a 1 kHz signal.

**Common-Mode Rejection Ratio (CMRR)**

CMRR is defined as the ratio of the power in the ADC common-mode input at full-scale frequency,  $f$ , to the power in the output of a full-scale p-p sine wave applied to the common-mode voltage of  $V_{INX+}$  and  $V_{INX-}$  of frequency,  $f_s$ ,

$$CMRR \text{ (dB)} = 20 \log (P_f/P_{f_s})$$

where:

$P_f$  is equal to the power at Frequency  $f$  in the ADC input.

$P_{f_s}$  is equal to the power at Frequency  $f_s$  in the ADC output.

## THEORY OF OPERATION

### CONVERTER DETAILS

The AD7609 is a data acquisition system that employs a high speed, low power, charge redistribution successive approximation analog-to-digital converter (ADC) and allows the simultaneous sampling of eight true differential analog input channels. The analog inputs on the AD7609 can accept true bipolar input signals. The RANGE pin is used to select either  $\pm 10$  V or  $\pm 5$  V as the input range. The AD7609 operates from a single 5 V supply.

The AD7609 contains input clamp protection, input signal scaling amplifiers, a second-order antialiasing filter, track-and-hold amplifiers, an on-chip reference, reference buffers, a high speed ADC, a digital filter, and high speed parallel and serial interfaces. Sampling on the AD7609 is controlled using CONVST<sub>x</sub> signals.

### ANALOG INPUT

#### Analog Input Ranges

The AD7609 can handle true bipolar input voltages. The logic level on the RANGE pin determines the analog input range of all analog input channels. If this pin is tied to a logic high, the analog input range is  $\pm 10$  V for all channels. If this pin is tied to a logic low, the analog input range is  $\pm 5$  V for all channels. A logic change on this pin has an immediate effect on the analog input range; however, there is a settling time of 80  $\mu$ s typically, in addition to the normal acquisition time requirement. The recommended practice is to hardwire the RANGE pin according to the desired input range for the system signals.

During normal operation, the applied analog input voltage should remain within the analog input range selected via the RANGE pin. A RESET pulse must be applied to the part to ensure the analog input channels are configured for the range selected.

When in a power-down mode, it is recommended to tie the analog inputs together or both analog input pins ( $V_{x+}$ ,  $V_{x-}$ ) to GND. As per the Analog Input Clamp Protection section, the overvoltage clamp protection is recommended for use in transient overvoltage conditions, and should not remain active for extended periods. Stressing the analog inputs outside of these conditions may degrade the Bipolar Zero Code error and THD performance of the AD7609.

#### Analog Input Impedance

The analog input impedance of the AD7609 is 1 M $\Omega$ . This is a fixed input impedance and does not vary with the AD7609 sampling frequency. This high analog input impedance eliminates the need for a driver amplifier in front of the AD7609 allowing for direct connection to the source or sensor. With the need for a driver amplifier eliminated, bipolar supplies can be removed from the signal chain, which are often a source of noise in a system.

#### Analog Input Clamp Protection

Figure 32 shows the analog input structure of the AD7609. Each AD7609 analog input contains clamp protection circuitry. Despite a single 5 V supply operation, this analog input clamp protection allows for an input overvoltage up to  $\pm 16.5$  V.

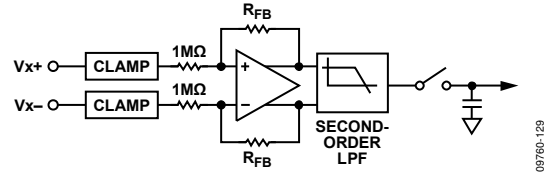


Figure 32. Analog Input Circuitry

Figure 33 shows the current vs. voltage characteristic of the clamp circuit. For input voltages up to  $\pm 16.5$  V, no current flows in the clamp circuit. For input voltages above  $\pm 16.5$  V, the AD7609 clamp circuitry turns on and clamps the analog input to  $\pm 16.5$  V. A series resistor should be placed on the analog input channels to limit the current to  $\pm 10$  mA for input voltages above  $\pm 16.5$  V. In an application where there is a series resistance on an analog input channel,  $V_{INx+}$ , a corresponding resistance is required on the  $V_{INx-}$  channel (see Figure 34). If there is no corresponding resistor on the  $V_{x-}$  channel, this results in an offset error on that channel. It is recommended that the input overvoltage clamp protection circuitry be used to protect the AD7609 against transient overvoltage events. It is not recommended to leave the AD7609 in a condition where the clamp protection circuitry is active (in normal or power-down conditions) for extended periods because this may degrade the bipolar zero code error performance of the AD7609.

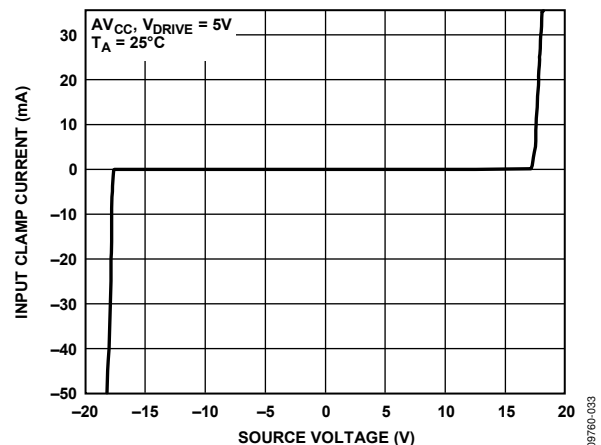


Figure 33. Input Protection Clamp Profile

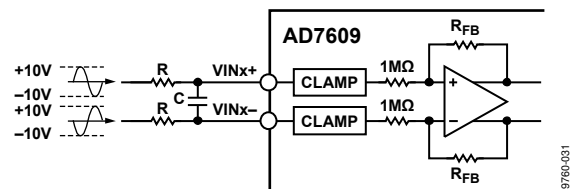


Figure 34. Input Resistance Matching on the Analog Input

**Analog Input Antialiasing Filter**

An analog antialiasing filter is also provided on the AD7609. The filter is a second-order Butterworth. Figure 35 and Figure 36 show the frequency and phase response respectively of the analog antialiasing filter. In the ±5 V range, the -3 dB frequency is typically 23 kHz. In the ±10 V range, the -3 dB frequency is typically 32 kHz.

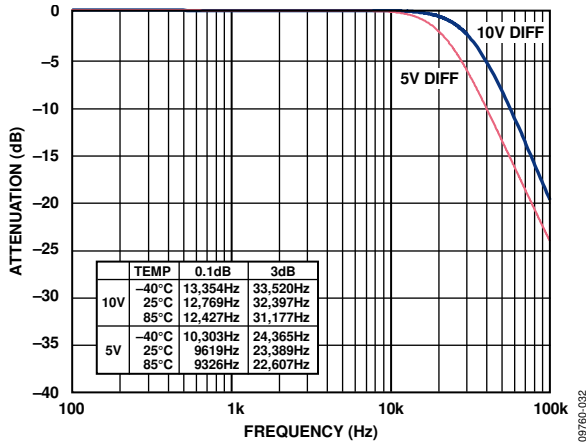


Figure 35. Analog Antialiasing Filter Frequency Response

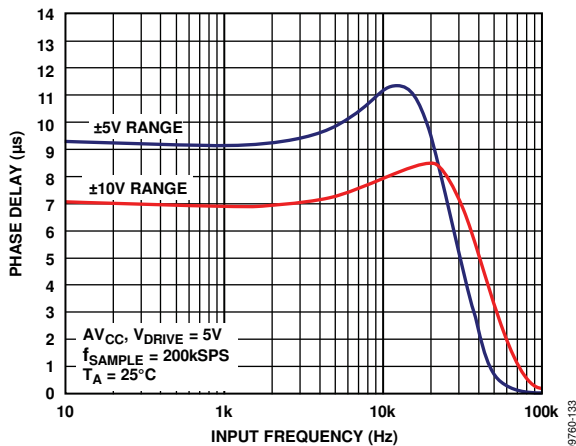


Figure 36. Analog Antialiasing Filter Phase Response

**Track-and-Hold Amplifiers**

The track-and-hold amplifiers on the AD7609 allow the ADC to accurately acquire an input sine wave of full-scale amplitude to 18-bit resolution. The track-and-hold amplifiers sample their respective inputs simultaneously on the rising edge of CONVST x. The aperture time for track-and-hold (that is, the delay time between the external CONVST x signal and the track-and-hold actually going into hold) is well matched, by design, across all eight track-and-holds on one device and from device to device. This matching allows more than one AD7609 device to be sampled simultaneously in a system.

The end of the conversion process across all eight channels is indicated by the falling edge of BUSY; and it is at this point that the track-and-holds return to track mode and the acquisition time for the next set of conversions begins.

The conversion clock for the part is internally generated, and the conversion time for all channels is 4 µs on the AD7609. The BUSY signal returns low after all eight conversions to indicate the end of the conversion process. On the falling edge of BUSY, the track-and-hold amplifiers return to track mode. New data can be read from the output register via the parallel, or serial interface after BUSY goes low; or, alternatively, data from the previous conversion can be read while BUSY is high. Reading data from the AD7609 while a conversion is in progress has little effect on performance and allows a faster throughput to be achieved. With a VDRIVE > 3.3 V, the SNR is reduced by ~1.5 dB when reading during a conversion.

**ADC TRANSFER FUNCTION**

The output coding of the AD7609 is twos complement. The designed code transitions occur midway between successive integer LSB values, that is, 1/2 LSB, 3/2 LSB. The LSB size is FSR/262,144 for the AD7609. The FSR for the AD7609 is 40 V for the ±10 V range and 20 V for the ±5 V range. The ideal transfer characteristic for the AD7609 is shown in Figure 37.

$$\pm 10V \text{ CODE} = \frac{V + \pm (V-)}{20V} \times 131,072 \times \frac{REF}{2.5V}$$

$$\pm 5V \text{ CODE} = \frac{V + \pm (V-)}{10V} \times 131,072 \times \frac{REF}{2.5V}$$

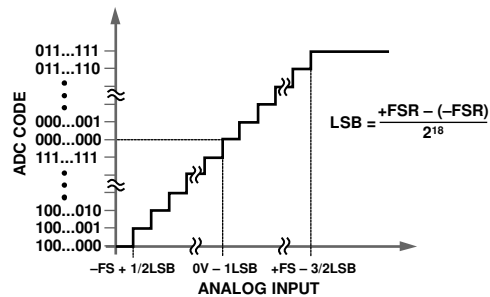


Figure 37. AD7609 Transfer Characteristic

The LSB size is dependent on the analog input range selected (see Table 7).

**Table 7. Output Codes and Ideal Input Values**

Description	Analog Input (V+ - (V-)) 10 V Range	Analog Input V+ - (V-) 5 V Range	Digital Output Code (Hex)
FSR - 0.5 LSB	+19.99992 V	9.999961 V	0x1FFFF
Midscale + 1 LSB	+152.58 µV	76 µV	0x00001
Midscale	0 V	0 V	0x00000
Midscale - 1 LSB	-152.58 µV	-76 µV	0x3FFFF
-FSR + 1 LSB	-19.99984 V	-9.99992 V	0x20001
-FSR	-20 V	-10 V	0x20000



## INTERNAL/EXTERNAL REFERENCE

The AD7609 contains an on-chip 2.5 V band gap reference. The REFIN/REFOUT pin allows access to the 2.5 V reference that generates the on-chip 4.5 V reference internally, or it allows an external reference of 2.5 V to be applied to the AD7609. An externally applied reference of 2.5 V is also amplified to 4.5 V using the internal buffer. This 4.5 V buffered reference is the reference used by the SAR ADC.

The REF SELECT pin is a logic input pin that allows the user to select between the internal reference and the external reference. If this pin is set to logic high, the internal reference is selected and is enabled; if this pin is set to logic low, the internal reference is disabled and an external reference voltage must be applied to the REFIN/REFOUT pin. The internal reference buffer is always enabled. After a reset, the AD7609 operates in the reference mode selected by the REF SELECT pin. Decoupling is required on the REFIN/REFOUT pin for both the internal or external reference options. A 10  $\mu\text{F}$  ceramic capacitor is required on the REFIN/REFOUT to ground close to the REFGND pins. The AD7609 contains a reference buffer configured to amplify the REF voltage up to  $\sim 4.5$  V, as shown in Figure 38. The REFCAPA and REFCAPB pins must be shorted together externally and a ceramic capacitor of 10  $\mu\text{F}$  applied to REFGND to ensure the reference buffer is in closed-loop operation. The reference voltage available at the REFIN/REFOUT pin is 2.5 V.

When the AD7609 is configured in external reference mode, the REFIN/REFOUT pin is a high input impedance pin. For applications using multiple AD7609 devices, the following configurations are recommended depending on the application requirements.

### External Reference Mode

One ADR421 external reference can be used to drive the REFIN/REFOUT pins of all AD7609 devices (see Figure 39). In this configuration, each AD7609 REFIN/REFOUT pin should be decoupled with a 100 nF decoupling capacitor.

### Internal Reference Mode

One AD7609 device, configured to operate in the internal reference mode, can be used to drive the remaining AD7609 devices, which are configured to operate in external reference mode (see Figure 40). The REFIN/REFOUT pin of the AD7609, configured in internal reference mode, should be decoupled using a 10  $\mu\text{F}$  ceramic decoupling capacitor. The other AD7609 devices, configured in external reference mode, should use a 100 nF decoupling capacitor on their REFIN/REFOUT pins.

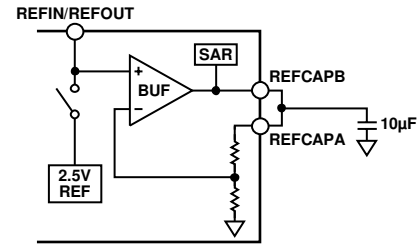


Figure 38. Reference Circuitry

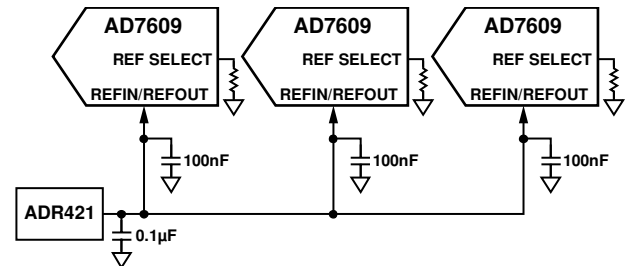


Figure 39. Single External Reference Driving Multiple AD7609 REFIN/REFOUT Pins

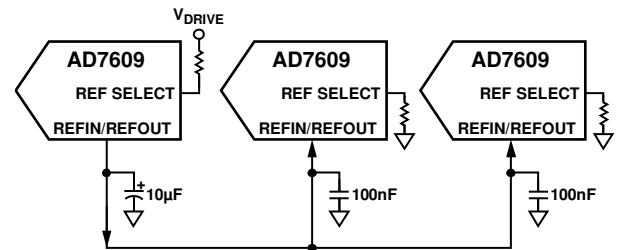


Figure 40. Internal Reference Driving Multiple AD7609 REFIN Pins

## TYPICAL CONNECTION DIAGRAM

Figure 41 shows the typical connection diagram for the AD7609. There are four  $AV_{CC}$  supply pins on the part that can be tied together and decoupled using a 100 nF capacitor at each supply pin and a 10  $\mu$ F capacitor at the supply source. The AD7609 can operate with the internal reference or an externally applied reference. In this configuration, the AD7609 is configured to operate with the internal reference. When using a single AD7609 device on the board, the REFIN/REFOUT pin should be decoupled with a 10  $\mu$ F capacitor. In an application with multiple AD7609 devices, see the Internal/External Reference section. The REFCAPA and REFCAPB pins are shorted together and decoupled with a 10  $\mu$ F ceramic capacitor.

The  $V_{DRIVE}$  supply is connected to the same supply as the processor. The voltage on  $V_{DRIVE}$  controls the voltage value of the output logic signals. For layout, decoupling, and grounding hints, see the Layout Guidelines section.

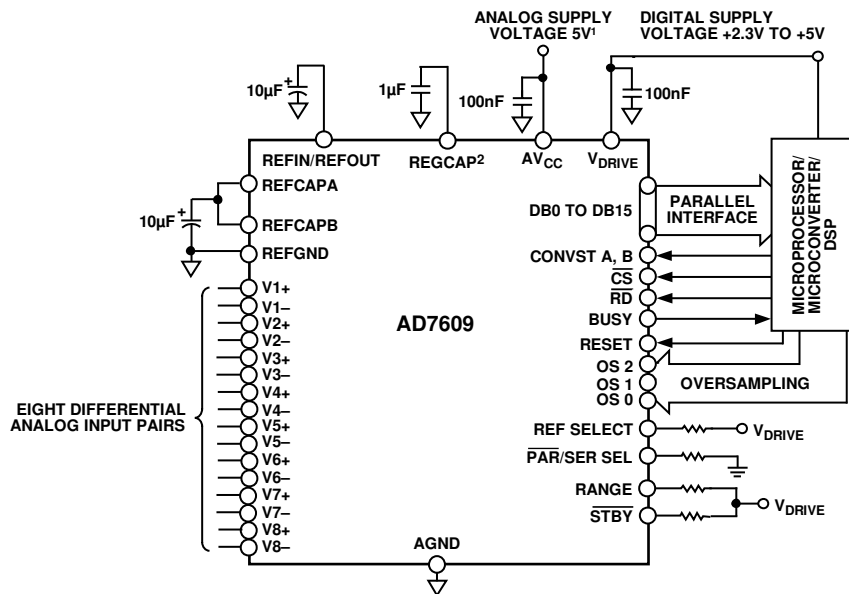
After supplies are applied to the AD7609, a reset should be applied to the AD7609 to ensure that it is configured for the correct mode of operation.

## POWER-DOWN MODES

There are two power-down modes available on the AD7609. The STBY pin controls whether the AD7609 is in normal mode or one of the two power-down modes. The two power-down modes available are standby mode and shutdown mode. The power-down mode is selected through the state of the RANGE pin when the STBY pin is low. Table 8 shows the configurations required to choose the desired power-down mode. When the AD7609 is placed in standby mode, the current consumption is 8 mA maximum and power-up time is approximately 100  $\mu$ s because the capacitor on the REFCAPA/REFCAPB pins must charge up. In standby mode, the on-chip reference and regulators remain powered up and the amplifiers and ADC core are powered down. When the AD7609 is placed in shutdown mode, the current consumption is 11  $\mu$ A maximum and power up time is about 13 ms. In shutdown mode, all circuitry is powered down. When the AD7609 is powered up from shutdown mode, a reset signal must be applied to the AD7609 after the required power-up time has elapsed.

**Table 8. Power-Down Mode Selection**

Power-Down Mode	STBY	RANGE
Standby	0	1
Shutdown	0	0



<sup>1</sup>DECOUPLING SHOWN ON THE  $AV_{CC}$  PIN APPLIES TO EACH  $AV_{CC}$  PIN (PIN 1, PIN 37, PIN 38, PIN 48). DECOUPLING CAPACITOR CAN BE SHARED BETWEEN  $AV_{CC}$  PIN 37 AND PIN 38.

<sup>2</sup>DECOUPLING SHOWN ON THE REGCAP PIN APPLIES TO EACH REGCAP PIN (PIN 36, PIN 39).

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Figure 41. Typical Connection Diagram