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Evaluating the AD7656-1/AD7657-1/AD7658-1, 250 kSPS, 6-Channel, Simultaneous Sampling, Bipolar 16-/14-/12-Bit ADCs

FEATURES

- Full featured evaluation board for the AD7656-1/AD7657-1/AD7658-1
- PC control in conjunction with the system demonstration platform (EVAL-SDP-CB1Z)
- PC software for control and data analysis (time and frequency domain)
- Standalone capability

EVALUATION KIT CONTENTS

- EVAL-AD7656-1SDZ, EVAL-AD7657-1SDZ, or EVAL-AD7658-1SDZ evaluation board
- Evaluation software CD for the AD7656-1/AD7657-1/AD7658-1
- 9 V mains power supply adapter

ADDITIONAL EQUIPMENT NEEDED

- EVAL-SDP-CB1Z system demonstration platform, includes a USB cable
- Precision analog signal source
- SMB cables
- PC running Windows XP SP2, Windows Vista, or Windows 7 with USB 2.0 port

ONLINE RESOURCES

Documents

- AD7656-1/AD7657-1/AD7658-1 data sheet
- EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ user guide

Required Software

- EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ evaluation software

GENERAL DESCRIPTION

The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ are full featured evaluation boards that can be used to easily evaluate all features of the AD7656-1/AD7657-1/AD7658-1. The AD7656-1/AD7657-1/AD7658-1 are 16-/14-/12-bit, 6-channel, 250 kSPS simultaneous sampling ADCs, respectively. Each part contains six 16-, 14-, or 12-bit, low power SAR ADCs and can operate from a single 4.75 V to 5.25 V power supply or dual ±12 V power supplies. The parts feature throughput rates of up to 250 kSPS.

The evaluation boards can be controlled via the system demonstration platform (SDP). The EVAL-SDP-CB1Z board allows the evaluation boards to be controlled via the USB port of a PC using the AD7656-1/AD7657-1/AD7658-1 evaluation software. The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ generates all required power supplies on board and supplies power to the EVAL-SDP-CB1Z controller board.

On-board components include the following:

AD8597: ultralow distortion, ultralow noise op amp (single)
AD8031: 2.7 V, 800 µA, 80 MHz rail-to-rail I/O single amplifier
ADP1613: step-up PWM dc-to-dc switching converter
ADP3303-5: high accuracy anyCAP® 200 mA low dropout linear regulator
ADP2301: 1.2 A, 20 V, 1.4 MHz nonsynchronous step-down switching regulator
ADM1185: quad voltage monitor and sequencer
ADP190: logic controlled, high-side power switch
ADG3308: low voltage, 1.15 V to 5.5 V, 8-channel bidirectional logic level translator
ADR431: ultralow noise XFET® voltage reference with current sink and source capability
AD780: 2.5 V/3.0 V ultrahigh precision band gap voltage reference

A functional block diagram is shown in Figure 1, and various link options are described in the Link Configuration Options section.

For full details on the AD7656-1/AD7657-1/AD7658-1, see the AD7656-1/AD7657-1/AD7658-1 data sheet, which should be consulted in conjunction with this user guide when using these evaluation boards.

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REVISION HISTORY

6/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

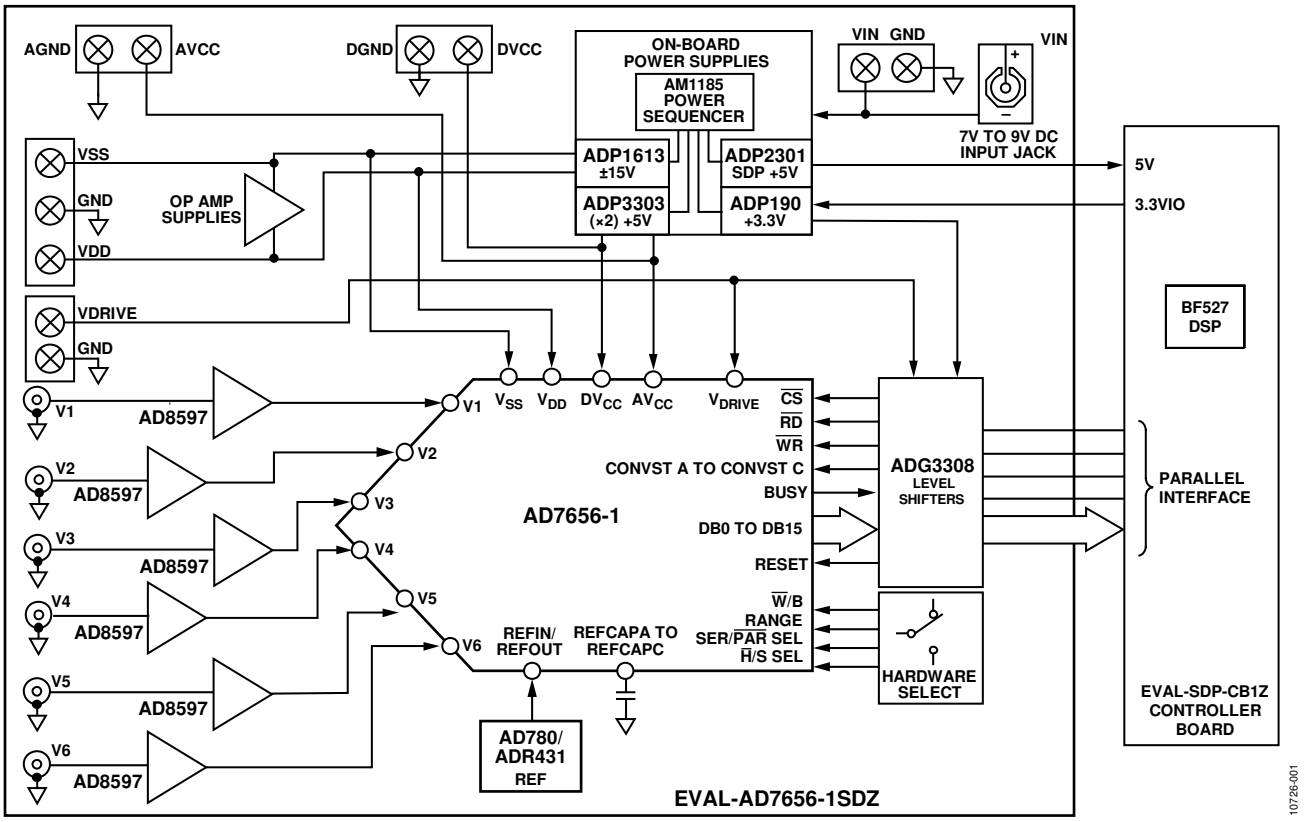


Figure 1.

GETTING STARTED

QUICK START STEPS

To begin using the evaluation board, do the following:

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, install the AD7656-1/AD7657-1/AD7658-1 evaluation board software from the CD included in the evaluation board kit. The PC must be restarted after the software installation is complete. (For complete software installation instructions, see the Software Installation Procedures section.)
2. Connect the EVAL-SDP-CB1Z board to the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board as shown in Figure 2. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
3. Connect the 9 V power supply adapter included in the evaluation board kit to Connector J702 on the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board.
4. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable. (If you are using Windows® XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
5. Launch the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ software from the **Analog Devices** subfolder in the **Programs** menu.

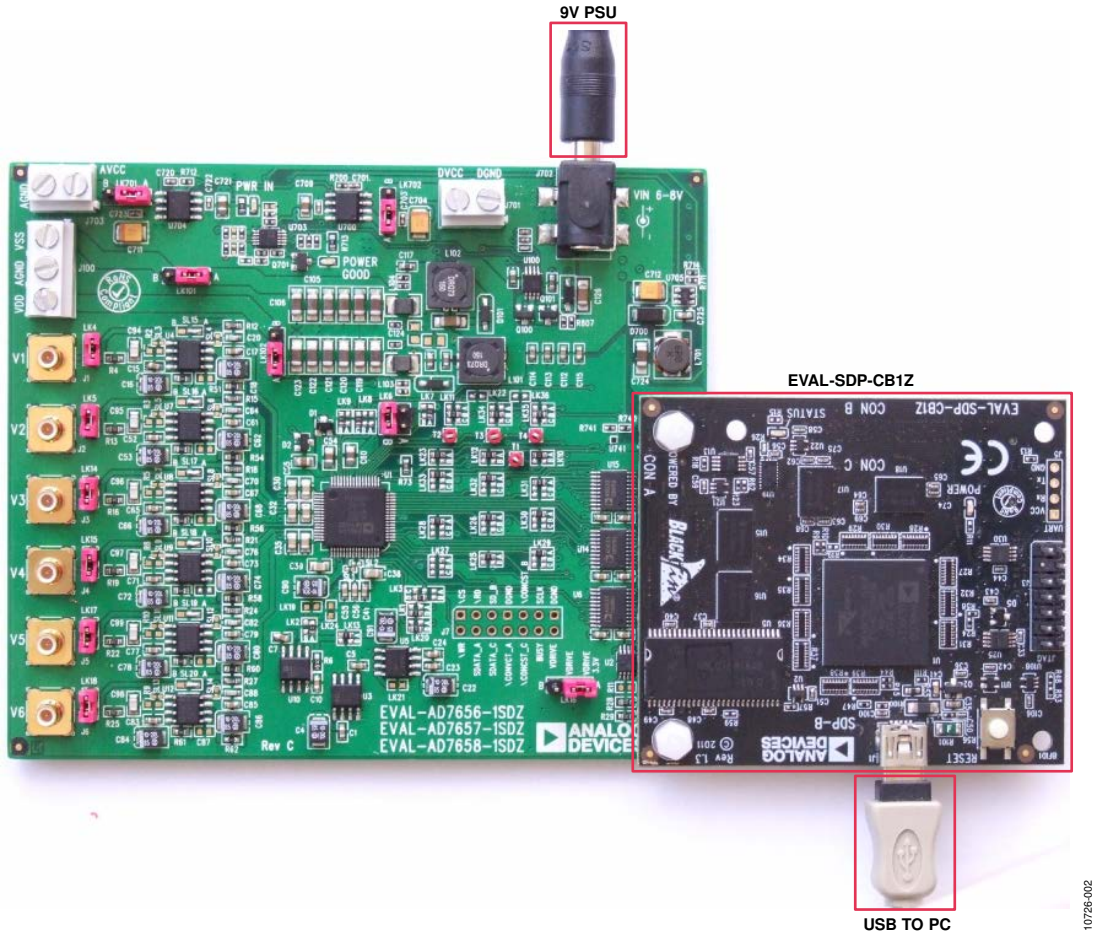


Figure 2. Hardware Configuration—Setting up the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ (EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ on Left and EVAL-SDP-CB1Z on Right)

SOFTWARE INSTALLATION PROCEDURES

The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ evaluation kit includes a CD containing software to be installed on your PC before you begin using the evaluation board.

There are two parts to the installation:

- AD7656-1/AD7657-1/AD7658-1 evaluation board software installation
- EVAL-SDP-CB1Z system demonstration platform board drivers installation

Warning

The evaluation board software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Installing the AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software

To install the AD7656-1/AD7657-1/AD7658-1 evaluation board software,

1. With the EVAL-SDP-CB1Z board disconnected from the USB port of the PC, insert the installation CD into the CD-ROM drive.
2. Double-click the **setup.exe** file to begin the evaluation board software installation. The software is installed to the following default location: **C:\Program Files\Analog Devices\AD7656-1_57-1_58-1**.
3. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.

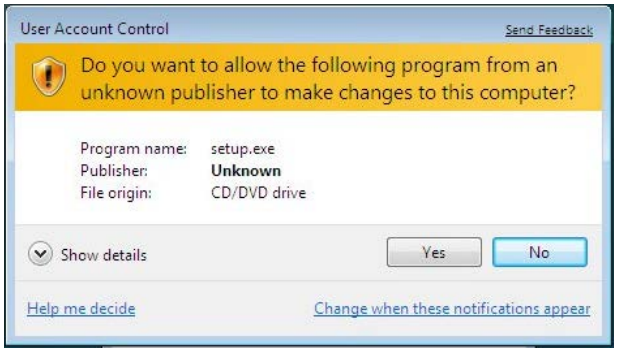


Figure 3. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software Installation: Granting Permission for Program to Make Changes

4. Select the location to install the software, and then click **Next**.

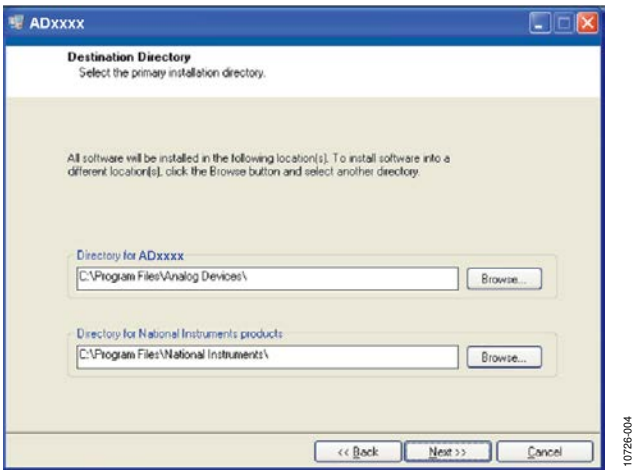


Figure 4. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software Installation: Selecting the Location for Software Installation

5. A license agreement appears. Read the agreement, and then select **I accept the License Agreement** and click **Next**.

Figure 5. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software Installation: Accepting the License Agreement

6. A summary of the installation is displayed. Click **Next** to continue.

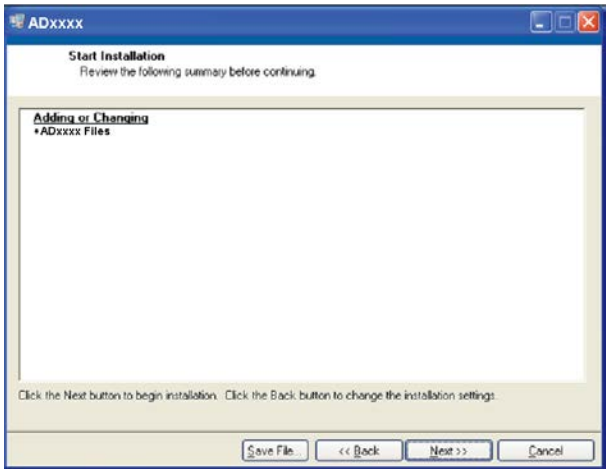


Figure 6. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software Installation: Reviewing a Summary of the Installation

7. A dialog box informs you when the installation is complete. Click **Next**.

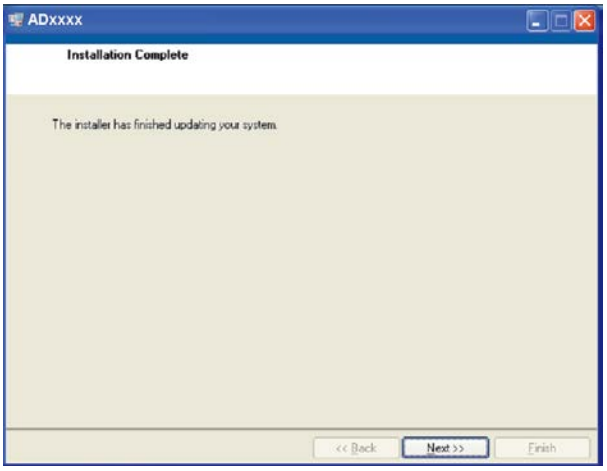


Figure 7. AD7656-1/AD7657-1/AD7658-1 Evaluation Board Software Installation: Indicating When the Installation Is Complete

Installing the EVAL-SDP-CB1Z System Demonstration Platform Board Drivers

After the installation of the evaluation board software is complete, a welcome window is displayed for the installation of the EVAL-SDP-CB1Z system demonstration platform board drivers.

1. With the EVAL-SDP-CB1Z board still disconnected from the USB port of the PC, make sure that all other applications are closed, and then click **Next**.

Figure 8. EVAL-SDP-CB1Z Drivers Setup: Beginning the Drivers Installation

2. Select the location to install the drivers, and then click **Next**.

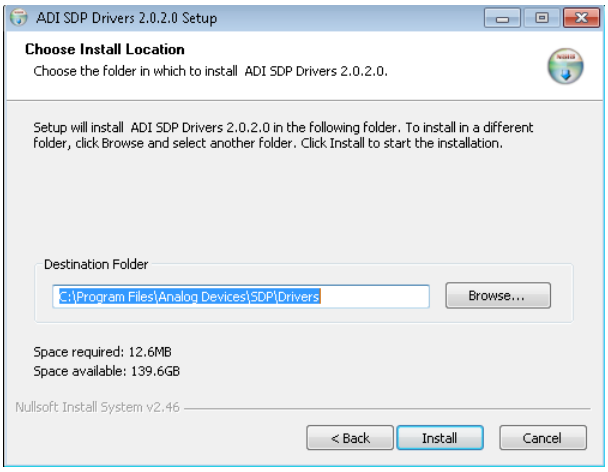


Figure 9. EVAL-SDP-CB1Z Drivers Setup: Selecting the Location for Drivers Installation

3. Click **Install** to confirm that you would like to install the drivers.

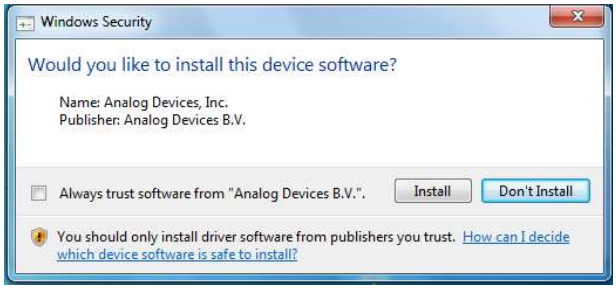


Figure 10. EVAL-SDP-CB1Z Drivers Setup: Granting Permission to Install Drivers

4. To complete the drivers installation, click **Finish**, which closes the installation wizard.

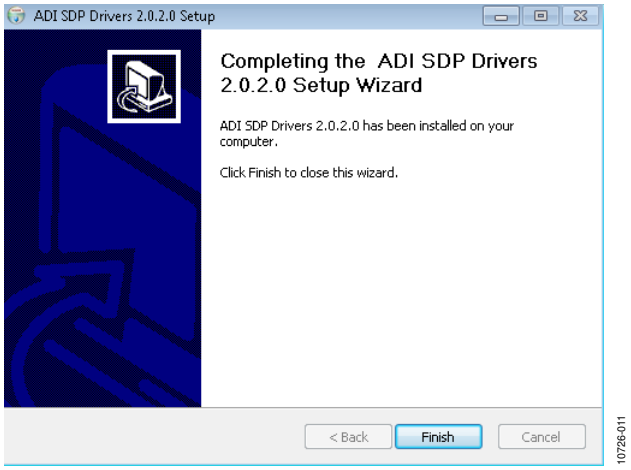


Figure 11. EVAL-SDP-CB1Z Drivers Setup: Completing the Drivers Setup Wizard

5. Before using the evaluation board, you must restart your computer. A dialog box opens, giving you the following options: **Restart**, **Shut Down**, **Restart Later**. Click the appropriate button.

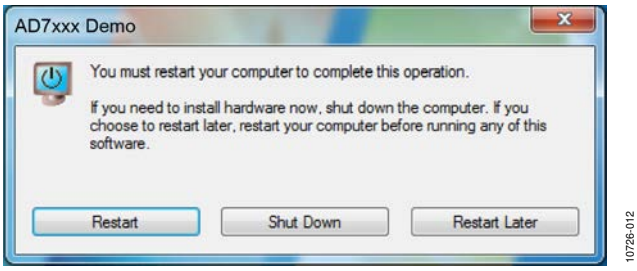


Figure 12. EVAL-SDP-CB1Z Drivers Setup: Restarting the Computer

EVALUATION BOARD SETUP PROCEDURES

The AD7656-1/AD7657-1/AD7658-1 evaluation board connects to the EVAL-SDP-CB1Z system demonstration board. The EVAL-SDP-CB1Z board is the controller board, which is the communication link between the PC and the main evaluation board. Figure 2 shows a photograph of the connections made between the AD7656-1/AD7657-1/AD7658-1 daughter board and the EVAL-SDP-CB1Z board.

After following the instructions in the Software Installation Procedures section, set up the evaluation and SDP boards as detailed in this section.

Warning

The evaluation software and drivers must be installed before connecting the evaluation board and EVAL-SDP-CB1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

Configuring the Evaluation and SDP Boards

1. Connect the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board to Connector A or Connector B of the EVAL-SDP-CB1Z board (see Figure 2).
   a. Screw the two boards together using the nylon screw-nut set included in the evaluation board kit to ensure that the boards are connected firmly together.
2. Connect the 9 V power supply adapter included in the evaluation kit to Connector J702 of the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board. (See Table 1 for more information about the connections and options for the required power supplies.)
3. Connect the EVAL-SDP-CB1Z board to the PC using the supplied USB cable.

EVALUATION BOARD HARDWARE

AD7656-1/AD7657-1/AD7658-1 DEVICE DESCRIPTION

The AD7656-1/AD7657-1/AD7658-1 are reduced decoupling pin- and software-compatible versions of the AD7656/AD7657/AD7658. Each AD7656-1/AD7657-1/AD7658-1 device contains six 16-/14-/12-bit, fast, low power successive approximation ADCs in a package designed on the *i*CMOS® process (industrial CMOS). *i*CMOS is a process combining high voltage silicon with submicron CMOS and complementary bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts could achieve.

The AD7656-1/AD7657-1/AD7658-1 feature throughput rates of up to 250 kSPS. The parts contain low noise, wide bandwidth track-and-hold amplifiers that can handle input frequencies of up to 4.5 MHz.

For more information about these devices, refer to the AD7656-1/AD7657-1/AD7658-1data sheet, which should be used in conjunction with this user guide.

POWER SUPPLIES

The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ can be used in two modes: SDP controlled mode and standalone mode (see the Modes of Operation section for more information).

When the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board is used in conjunction with the EVAL-SDP-CB1Z board (SDP controlled mode), connect the 9 V dc supply to Connector J702 on the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board. The V_{DD}, V_{SS}, AV_{CC}, and DV_{CC} supplies are generated on board. When the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ board is used in standalone mode, the V_{DD}, V_{SS}, AV_{CC}, and DV_{CC} supplies must be sourced from external sources (see Table 1).

In SDP controlled mode and standalone mode, each supply is decoupled on the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ using 10 µF and 0.1 µF capacitors. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

Table 1. External Power Supplies Required

Power Supply	Connector	Voltage Range	Purpose
V_{IN}[1]	J702	7 V to 9 V	Supplies all on-board power supplies, generating all required voltages to run the evaluation board
V_{DD}	J100	+12 V to +16.5 V	Supplies the positive rail of the amplifier
V_{SS}	J100	−12 V to −16.5 V	Supplies the negative rail of the amplifier
AV_{CC}	J703	4.75 V to 5.25 V	Supplies the AV_{CC} analog supply on the ADC
DV_{CC}	J701	4.75 V to 5.25 V	Supplies the DV_{CC} digital supply on the ADC

[1] When V_{IN} is supplied, all other power supplies are available on board. If the V_{IN} supply is not used, all other power supplies must be sourced from an external source.

LINK CONFIGURATION OPTIONS

There are multiple jumper (LKx) and solder link (SLx) options that must be set correctly to select the appropriate operating setup before you begin using the evaluation board. The functions of these options are outlined in Table 2.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as required by the operating mode. There are two modes in which to operate the evaluation board. The evaluation board can be operated in SDP controlled mode to be used with the SDP board, or the evaluation board can be used in standalone mode.

Table 3 shows the default positions in which the links are set when the evaluation board is packaged. When the board is shipped, it is assumed that you are going to operate the evaluation board with the SDP board (SDP controlled mode).

Table 2. Link Option Functions

Link No.	Function
LK1	$\overline{H}$/S SEL selection.
	Position A: the software input is selected.
	Position B: the hardware input is selected.
LK2	V_{REF} buffer signal selection.
	Position A: the V_{REF} signal is unbuffered.
	Position B: the V_{REF} signal is buffered by the AD8031 op amp (U10).
LK3	$\overline{WR}$/$REF_{EN/\overline{DIS}}$ signal selection.
	Position A: the $\overline{WR}$/$REF_{EN/\overline{DIS}}$ pin is connected to EVAL-SDP-CB1Z.
	Position B: the $\overline{WR}$/$REF_{EN/\overline{DIS}}$ pin is connected to the J7-2 external socket.
	Position C: the $\overline{WR}$/$REF_{EN/\overline{DIS}}$ pin is connected to GND.
	Position D: the $\overline{WR}$/$REF_{EN/\overline{DIS}}$ pin is connected to V_{DRIVE}.
LK4	V1 input jumper.
	Inserted: the V1 input is shorted to GND.
LK5	V2 input jumper.
	Inserted: the V2 input is shorted to GND.
LK6	RANGE signal selection.
	Position A: the RANGE pin is connected to V_{DRIVE}.
	Position B: the RANGE pin is connected to GND. The input range is set to $\pm 4 \times V_{REF}$.
LK7	$\overline{STBY}$ signal selection.
	Position A: the $\overline{STBY}$ pin is connected to V_{DRIVE}. Normal operation is selected.
	Position B: the $\overline{STBY}$ pin is connected to GND.
LK8	RESET signal selection.
	Position A: the RESET pin is connected to V_{DRIVE}.
	Position B: the RESET pin is connected to GND.
	Position C: the RESET pin is connected to EVAL-SDP-CB1Z.
LK9	$\overline{W}$/B signal selection.
	Position A: the $\overline{W}$/B pin is connected to V_{DRIVE}.
	Position B: the $\overline{W}$/B pin is connected to GND. Word mode is selected.
LK10	BUSY signal selection.
	Position A: the BUSY pin is connected to EVAL-SDP-CB1Z.
	Position B: the BUSY pin is connected to the J7-12 external socket.
LK11	CONVST A signal selection.
	Position A: the CONVST A pin is connected to the J7-8 external socket.
	Position B: the CONVST A pin is connected to EVAL-SDP-CB1Z.
	Position C: the CONVST A pin is connected to GND.
LK12	$\overline{CS}$ source signal selection.
	Position A: the $\overline{CS}$ pin is connected to EVAL-SDP-CB1Z.
	Position B: the $\overline{CS}$ pin is connected to the J7-1 external socket.
LK13	REFIN/REFOUT source signal selection.
	Position A: the REFIN/REFOUT signal is sourced from AD780 (U5).
	Position B: the REFIN/REFOUT signal is sourced from ADR431 (U3).
LK14	V3 input jumper.
	Inserted: the V3 input is shorted to GND.

Link No.	Function
LK15	V4 input jumper. Inserted: the V4 input is shorted to GND.
LK16	V_{DRIVE} source signal selection. Position A: the V_{DRIVE} signal is sourced from the on-board 3.3 V supply. (Requires the EVAL-SDP-CB1Z board to be connected.) Position B: the V_{DRIVE} pin is connected to the J7-14 external socket.
LK17	V5 input jumper. Inserted: the V5 input is shorted to GND.
LK18	V6 input jumper. Inserted: the V6 input is shorted to GND.
LK19	REFIN/REFOUT input selection. Inserted: the V_{REF} signal is connected to the REFIN/REFOUT pin.
LK20	SER/$\overline{PAR}$ SEL selection. Position A: the SER/$\overline{PAR}$ SEL pin is connected to V_{DRIVE}. Position B: the SER/$\overline{PAR}$ SEL pin is connected to GND. Parallel mode is selected.
LK21	AD780 (U5) voltage output selection. Inserted: the AD780 voltage output is 3 V. Removed: the AD780 voltage output is 2.5 V.
LK22	CONVST A/CONVST B link selection. Inserted: Connects CONVST A to CONVST B.
LK23	$\overline{RD}$ source signal selection. Position A: the $\overline{RD}$ pin is connected to EVAL-SDP-CB1Z. Position B: the $\overline{RD}$ pin is connected to the J7-3 external socket.
LK24	REFCAPA source signal selection. Inserted: an external reference is connected to REFCAPA. Removed: an external reference is disconnected from REFCAPA.
LK25	DB10/DOUT C destination selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: data is sent to the J7-4 external socket.
LK26	DB7/HBEN/DCEN selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: the DB7/HBEN/DCEN pin is connected to V_{DRIVE}. Position C: the DB7/HBEN/DCEN pin is connected to GND.
LK27	DB9/DOUT B destination selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: not used. Position C: data is sent to the J7-5 external socket.
LK28	DB8/DOUT A destination selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: not used. Position C: data is sent to the J7-6 external socket.
LK29	DB14/REFBUF$\overline{EN/DIS}$ selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: the DB14/REFBUF$\overline{EN/DIS}$ pin is connected to V_{DRIVE}. Position C: the DB14/REFBUF$\overline{EN/DIS}$ pin is connected to GND.
LK30	DB6/SCLK selection. Position A: the DB6/SCLK pin is connected to EVAL-SDP-CB1Z. Position B: not used. Position C: the DB6/SCLK pin is connected to the J7-11 external socket.
LK31	DB2/SEL C selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: the DB2/SEL C pin is connected to V_{DRIVE}. Position C: the DB2/SEL C pin is connected to GND.
LK32	DB1/SEL B selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: the DB1/SEL B pin is connected to V_{DRIVE}. Position C: the DB1/SEL B pin is connected to GND.

Link No.	Function
LK33	DB0/SEL A selection. Position A: data is sent to EVAL-SDP-CB1Z. Position B: the DB0/SEL A pin is connected to V_{DRIVE}. Position C: the DB0/SEL A pin is connected to GND.
LK34	CONVST B selection. Position A: the CONVST B pin is connected to the J7-9 external socket. Position B: the CONVST B pin is connected to EVAL-SDP-CB1Z. Position C: the CONVST B pin is connected to GND.
LK35	CONVST C selection. Position A: the CONVST C pin is connected to the J7-10 external socket. Position B: the CONVST C pin is connected to EVAL-SDP-CB1Z. Position C: the CONVST C pin is connected to GND.
LK36	CONVST A/CONVST C link selection. Inserted: Connects CONVST A to CONVST C.
LK101	V_{SS} signal source selection (op amp negative supply). Position A: the V_{SS} signal is sourced from the on-board supply generation circuitry (−12 V). Position B: the V_{SS} signal is sourced from the J100 external socket.
LK102	V_{DD} signal source selection (op amp positive supply). Position A: the V_{DD} signal is sourced from the on-board supply generation circuitry (+12 V). Position B: the V_{DD} signal is sourced from the J100 external socket.
LK103 to LK106	Sets the V_{DD} and V_{SS} levels when using the on-board supplies as follows (where POP = place both 0 Ω resistors, and NOPOP = neither 0 Ω resistor is placed).

Link	±12 V	±15 V
LK103	POP	NOPOP
LK104	NOPOP	POP
LK105	NOPOP	POP
LK106	POP	NOPOP

LK701	AV_{CC} signal source selection. Position A: the AV_{CC} signal is sourced from the on-board supply generation circuitry. Position B: the AV_{CC} signal is sourced from the J703 external socket.
LK702	DV_{CC} signal source selection. Position A: the DV_{CC} signal is sourced from the on-board supply generation circuitry. Position B: the DV_{CC} signal is sourced from the J701 external socket.
SL1	REFCAPA/REFCAPB link selection. Inserted: Connects REFCAPA to REFCAPB when soldered.
SL2	REFCAPB/REFCAPC link selection. Inserted: Connects REFCAPB to REFCAPC when soldered.
SL3 to SL14	Not used. Leave unsoldered.
SL15	V1 buffer selection. Position A: the V1 input signal is buffered through U4. Position B: the V1 input signal is taken directly from J1.
SL16	V2 buffer selection. Position A: the V2 input signal is buffered through U7. Position B: the V2 input signal is taken directly from J2.
SL17	V3 buffer selection. Position A: the V3 input signal is buffered through U8. Position B: the V3 input signal is taken directly from J7.
SL18	V4 buffer selection. Position A: the V4 input signal is buffered through U9. Position B: the V4 input signal is taken directly from J4.
SL19	V5 buffer selection. Position A: the V5 input signal is buffered through U11. Position B: the V5 input signal is taken directly from J5.
SL20	V6 buffer selection. Position A: the V6 input signal is buffered through U12. Position B: the V6 input signal is taken directly from J6.

Table 3. Default Link Positions for Packaged EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ

Link No.	Position	Function
LK1	A	Software input is selected.
LK2	A	V_{REF} is not buffered.
LK3	A	The $\overline{WR}$/$REF_{EN/\overline{DIS}}$ pin is connected to EVAL-SDP-CB1Z.
LK4	Inserted	The V1 input is grounded.
LK5	Inserted	The V2 input is grounded.
LK6	B	The RANGE pin is connected to GND. The input range is set to ±4 × V_{REF} (can be overridden by control registers in software).
LK7	A	The $\overline{STBY}$ pin is connected to V_{DRIVE}. Normal operation is selected.
LK8	C	The RESET pin is connected to EVAL-SDP-CB1Z.
LK9	B	The $\overline{W}$/B pin is connected to GND. Word mode is selected.
LK10	A	The BUSY pin is connected to EVAL-SDP-CB1Z.
LK11	B	The CONVST A pin is connected to EVAL-SDP-CB1Z.
LK12	A	The $\overline{CS}$ pin is connected to EVAL-SDP-CB1Z.
LK13	A	The REFIN/REFOUT signal is sourced from AD780.
LK14	Inserted	The V3 input is grounded.
LK15	Inserted	The V4 input is grounded.
LK16	A	The V_{DRIVE} signal is sourced from the on-board 3.3 V supply. (Requires the EVAL-SDP-CB1Z board to be connected.)
LK17	Inserted	The V5 input is grounded.
LK18	Inserted	The V6 input is grounded.
LK19	Removed	An external V_{REF} is disconnected.
LK20	B	The SER/$\overline{PAR}$ SEL pin is connected to GND. Parallel mode is selected.
LK21	Removed	The AD780 voltage output is 2.5 V.
LK22	Removed	The CONVST A and CONVST B pins are not linked.
LK23	A	The $\overline{RD}$ pin is connected to EVAL-SDP-CB1Z.
LK24	Removed	An external V_{REF} is disconnected.
LK25	A	The DB10/DOUT C pin is connected to EVAL-SDP-CB1Z.
LK26	A	The DB7/HBEN/DCEN pin is connected to EVAL-SDP-CB1Z.
LK27	A	The DB9/DOUT B pin is connected to EVAL-SDP-CB1Z.
LK28	A	The DB8/DOUT A pin is connected to EVAL-SDP-CB1Z.
LK29	A	The DB14/$REFBUF_{\overline{EN}/DIS}$ pin is connected to EVAL-SDP-CB1Z.
LK30	A	The DB6/SCLK pin is connected to EVAL-SDP-CB1Z.
LK31	A	The DB2/SEL C pin is connected to EVAL-SDP-CB1Z.
LK32	A	The DB1/SEL B pin is connected to EVAL-SDP-CB1Z.
LK33	A	The DB0/SEL A pin is connected to EVAL-SDP-CB1Z.
LK34	B	The CONVST B pin is connected to EVAL-SDP-CB1Z.
LK35	B	The CONVST C pin is connected to EVAL-SDP-CB1Z.
LK36	Removed	The CONVST A and CONVST C pins are not linked.
LK101	A	The on-board op amp power is used.
LK102	A	The on-board op amp power is used.
LK103	NOPOP[1]	The op amp supply rails are set to ±15 V.
LK104	POP[1]	The op amp supply rails are set to ±15 V.
LK105	POP[1]	The op amp supply rails are set to ±15 V.
LK106	NOPOP[1]	The op amp supply rails are set to ±15 V.
LK701	A	The on-board AV_{CC} is used.
LK702	A	The on-board DV_{CC} is used.
SL1	Removed	The REFCAPA and REFCAPB pins are not linked.
SL2	Removed	The REFCAPB and REFCAPC pins are not linked.
SL3 to SL14	Removed	Not used.
SL15	A	The V1 input is buffered.
SL16	A	The V2 input is buffered.
SL17	A	The V3 input is buffered.
SL18	A	The V4 input is buffered.
SL19	A	The V5 input is buffered.
SL20	A	The V6 input is buffered.

[1] POP = place both 0 Ω resistors; NOPOP = neither 0 Ω resistor is placed.

EVALUATION BOARD CIRCUITRY

ANALOG INPUTS

The V1 to V6 inputs allow a signal to be connected to the board via SMB connectors.

The analog inputs on the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ are filtered and buffered by the AD8597 ultralow distortion, ultralow noise (single) op amps. Additional filtering is provided by an R-C filter directly before the AD7656-1/AD7657-1/AD7658-1 inputs. Alternatively, the op amps can be bypassed, and the inputs can be fed directly to the AD7656-1/AD7657-1/AD7658-1 via the R-C filter.

REFERENCE OPTIONS

The following two on-board reference supplies are available:

- ADR431: ultralow noise XFET voltage reference with current sink and source capability
- AD780: 2.5 V/3.0 V ultrahigh precision band gap voltage reference

Alternatively, the AD7656-1/AD7657-1/AD7658-1 can supply an internal reference voltage.

SOCKETS/CONNECTORS

Table 4. Socket/Connector Functions

Socket	Function	
VIN0	Analog Input VIN0. Buffered to the $V_{IN}0$ pin on the AD7656-1/AD7657-1/AD7658-1.	
VIN1	Analog Input VIN1. Buffered to the $V_{IN}1$ pin on the AD7656-1/AD7657-1/AD7658-1.	
VIN2	Analog Input VIN2. Buffered to the $V_{IN}2$ pin on the AD7656-1/AD7657-1/AD7658-1.	
VIN3	Analog Input VIN3. Buffered to the $V_{IN}3$ pin on the AD7656-1/AD7657-1/AD7658-1.	
J1	VIN. Apply a bipolar signal to this pin. This signal is biased up on J3.	
J2	Socket for EVAL-SDP-CB1Z evaluation controller board.	
J3	VIN BIASED. Unipolar version of signal applied to J1.	
J5	V_{REF}. External reference voltage.	
J8	V_{DRIVE}. External screw connection for V_{DRIVE}.	
J9	Analog Input VIN4 to Analog Input VIN15. Buffered to $V_{IN}4$ to $V_{IN}15$ pins of the AD7656-1/AD7657-1/AD7658-1.	
	Odd Pins	**Even Pins**
	Pin 1—$V_{IN}4$	Pin 2—AGND
	Pin 3—$V_{IN}5$	Pin 4—AGND
	Pin 5—$V_{IN}6$	Pin 6—AGND
	Pin 7—$V_{IN}7$	Pin 8—AGND
	Pin 9—$V_{IN}8$	Pin 10—AGND
	Pin 11—$V_{IN}9$	Pin 12—AGND
	Pin 13—$V_{IN}10$	Pin 14—AGND
	Pin 15—$V_{IN}11$	Pin 16—AGND
	Pin 17—$V_{IN}12$	Pin 18—AGND
	Pin 19—$V_{IN}13$	Pin 20—AGND
	Pin 21—$V_{IN}14$	Pin 22—AGND
	Pin 23—$V_{IN}15$	Pin 24—AGND
J100	Op amp power supply screw terminal connectors. Supply rails for op amps.	
J701	DV_{CC} screw terminal connector.	
J702	The 7 V to 9 V dc transformer power connector.	
J703	AV_{CC} screw terminal connector.	

MODES OF OPERATION

SDP CONTROLLED MODE

The AD7656-1/AD7657-1/AD7658-1 uses a high speed parallel interface that allows sampling rates of up to 250 kSPS. For more information about the operation of the parallel interface, refer to the AD7656-1/AD7657-1/AD7658-1 data sheet.

The AD7656-1/AD7657-1/AD7658-1 uses the parallel interface to transfer data to the EVAL-SDP-CB1Z.

The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ communicates with the EVAL-SDP-CB1Z board using level shifters. The EVAL-SDP-CB1Z operates at a 3.3 V logic level, which allows logic voltages that exceed 3.3 V to be used without damaging the SDP interface.

STANDALONE MODE

The EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ can also be used without the EVAL-SDP-CB1Z controller board. In this case, the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ is connected to the serial interface using the J7 socket. For more information about the operation of the serial interface, refer to the AD7656-1/AD7657-1/AD7658-1 data sheet.

HOW TO USE THE SOFTWARE FOR EVALUATING THE AD7656-1/AD7657-1/AD7658-1

SETTING UP THE SYSTEM FOR DATA CAPTURE

After completing the steps in the Software Installation Procedures and Evaluation Board Setup Procedures sections, set up the system for data capture as follows:

1. Allow the **Found New Hardware Wizard** to run after the EVAL-SDP-CB1Z board is plugged into your PC. (If you are using Windows XP, you may need to search for the EVAL-SDP-CB1Z drivers. Choose to automatically search for the drivers for the EVAL-SDP-CB1Z board if prompted by the operating system.)
2. Check that the board is connected to the PC correctly using the **Device Manager** of the PC.
   a. Access the **Device Manager** as follows:
      i. Right-click **My Computer** and then click **Manage**.
      ii. A dialog box appears asking for permission to allow the program to make changes to your computer. Click **Yes**.
      iii. The **Computer Management** box appears. From the list of **System Tools**, click **Device Manager** (see Figure 13).
   b. Under **ADI Development Tools**, **Analog Devices System Development Platform (32MB)** should appear, indicating that the EVAL-SDP-CB1Z driver software is installed and that the board is connected to the PC correctly.

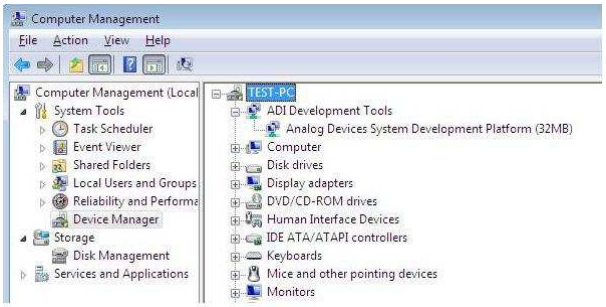


Figure 13. Device Manager: Checking that the Board Is Connected to the PC Correctly

Launching the Software

After completing the steps in the Setting Up the System for Data Capture section, launch the AD7656-1/AD7657-1/AD7658-1 software as follows:

1. From the **Start** menu, select **Programs** > **Analog Devices** > **AD7656-1_57-1_58-1**. The main window of the software then displays.
2. If the EVAL-AD7656-1SDZ/EVAL-AD7657-1SDZ/EVAL-AD7658-1SDZ evaluation system is not connected to the USB port via the EVAL-SDP-CB1Z when the software is launched, a connectivity error displays (see Figure 14). Connect the evaluation system to the USB port of the PC, wait a few seconds, click **Rescan**, and follow the on-screen instructions.

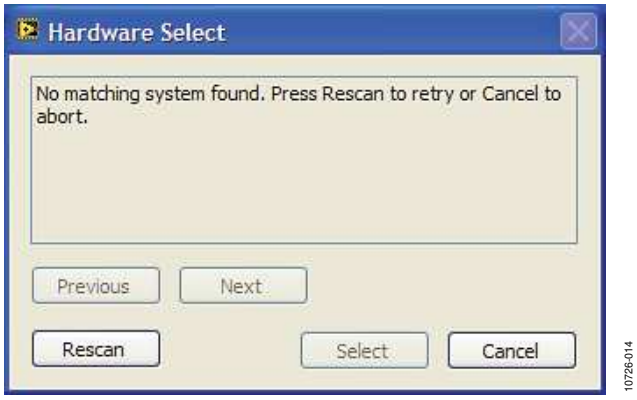
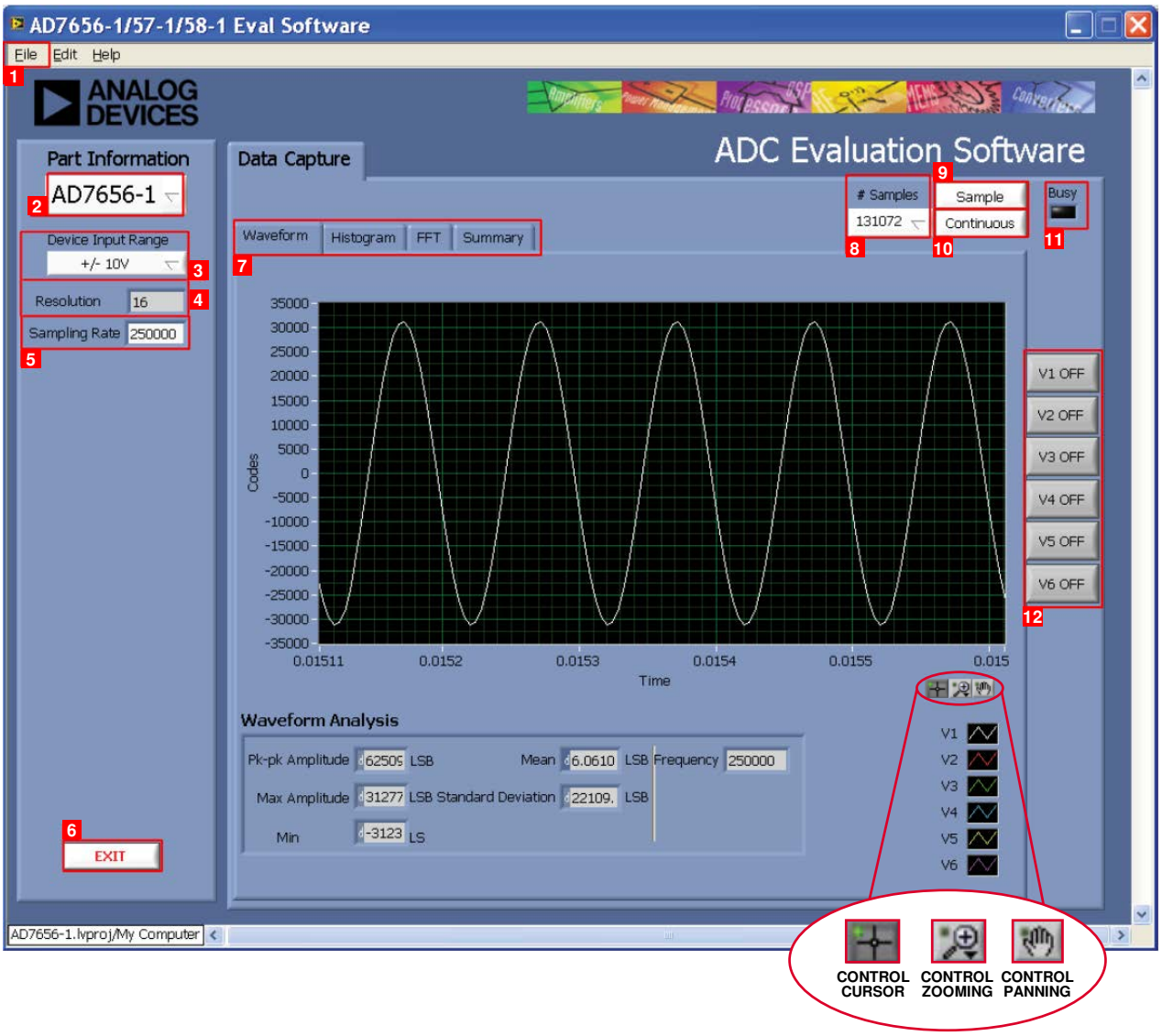


Figure 14. Connectivity Error Alert

When the software starts running, it searches for hardware connected to the PC. A dialog box indicates when the evaluation board attached to the PC is detected, and then the main window appears (see Figure 15).



NOTES
1. FOR DETAILS ABOUT THE AREAS HIGHLIGHTED IN RED, SEE THE OVERVIEW OF THE MAIN WINDOW SECTION.

Figure 15. Evaluation Software Main Window

OVERVIEW OF THE MAIN WINDOW

The main window of the software is shown in Figure 15 and has the features described in this section.

File Menu (Section 1)

The **File** menu (labeled 1 in Figure 15) offers the choice to

- **Load data**: load previously captured data or example files in .tsv (tab separated values) format for analysis (see Figure 16). (The default location for example files is **C:\Program Files\Analog Devices\AD7656-1_57-1_58-1\examples**.)
- **Save Data as .tsv**: save captured data in .tsv format for future analysis (see Figure 17).
- **Print Front Panel Picture**: print the main window to the default printer.
- **Save Picture**: save the current screen capture.
- **Exit**: close the application.

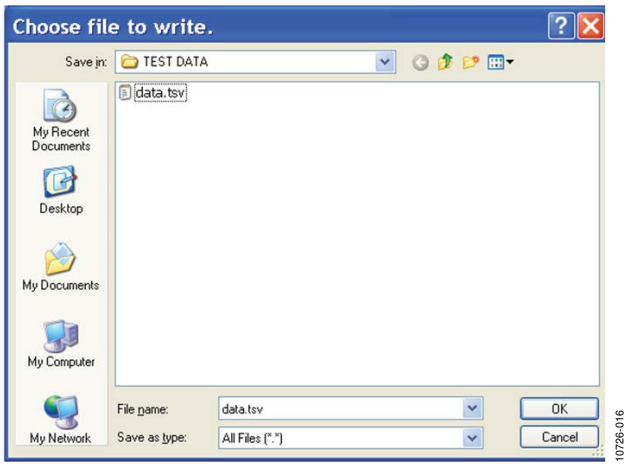


Figure 16. Load File Dialog Box: Loading Previously Captured Data or Example Files in .tsv Format

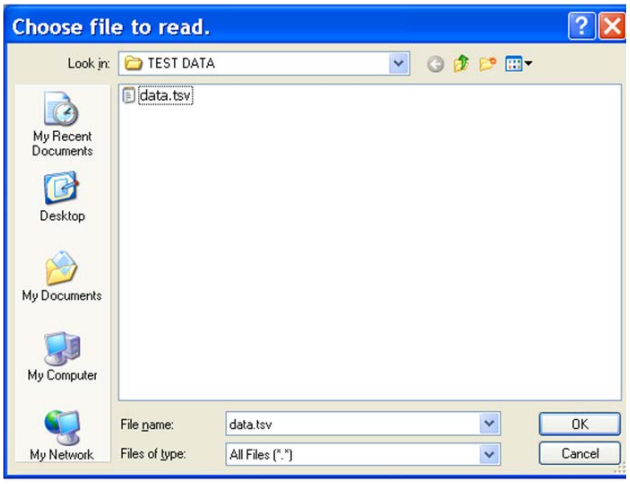


Figure 17. Save File Dialog Box: Saving Data as .tsv

Part Information Box (Section 2)

The **Part Information** box (labeled 2 in Figure 15) allows selecting the generic to be evaluated; choose AD7656-1, AD7657-1, or AD7658-1.

Device Input Range Box (Section 3)

The **Device Input Range** box (labeled 3 in Figure 15), in conjunction with hardware settings, is used to select the voltage range.

Resolution Box (Section 4)

The **Resolution** box (labeled 4 in Figure 15) displays the resolution of the selected part in bits.

Sampling Rate Box (Section 5)

The default sampling frequency in the **Sampling Rate** box (labeled 5 in Figure 15) matches the maximum sample rate of the ADC being evaluated. Although you can adjust the sampling frequency, there are limitations in terms of the sample frequencies that can be entered. If an unusable sample frequency is input, the software automatically adjusts the sample frequency accordingly. Units can be entered as, for example, 10k for 10,000 Hz. The software automatically adjusts the sample frequency according to the ability of the ADC being evaluated. For example, if you enter a value that is beyond the ability of the device, the software indicates this and reverts to the maximum sample frequency.

Exit Button (Section 6)

Clicking **Exit** (labeled 6 in Figure 15) closes the software. Alternatively, you can select **Exit** from the **File** menu.

Tabs Area (Section 7)

There are four tabs available in the tabs area (labeled 7 in Figure 15) of the main window: **Waveform**, **Histogram**, **FFT**, and **Summary**. These tabs display the data in different formats. Navigation tools are provided within each tab to allow you to control the cursor, zooming, and panning (see Figure 15) within the graphs displayed.

Each tab is described in more detail in the Generating a Waveform Analysis Report; Generating a Histogram of the ADC Code Distribution; Generating a Fast Fourier Transform of AC Characteristics; and Generating a Summary of the Waveform, Histogram, and Fast Fourier Transform sections.

Samples Box (Section 8)

The **# Samples** box (labeled 8 in Figure 15) allows you to select the number of samples to analyze. When **Sample** or **Continuous** is clicked, the software requests this number of samples to be taken. This is the total number of samples taken on all channels.

Sample Button (Section 9)

Clicking **Sample** (labeled 9 in Figure 15) performs a single capture, acquiring a set number of samples at the selected sampling rate.

Continuous Button (Section 10)

Clicking **Continuous** (labeled 10 in Figure 15) performs a continuous capture from the ADC. Clicking **Continuous** a second time stops sampling.

Busy LED (Section 11)

The **Busy** LED (labeled 11 in Figure 15) indicates when a read from the EVAL-SDP-CB1Z board is in progress.

Channel Display Buttons (Section 12)

Clicking the buttons in this area (labeled 12 in Figure 15) allows you to display multiple channel reads. (Note that for FFT analysis, you can select only one channel to be displayed.)

GENERATING A WAVEFORM ANALYSIS REPORT

Figure 18 illustrates the waveform capture tab for a 10 kHz sine wave input signal.

The **Waveform Analysis** area (labeled 1 in Figure 18) reports the amplitudes recorded from the captured signal and the frequency of the signal tone.

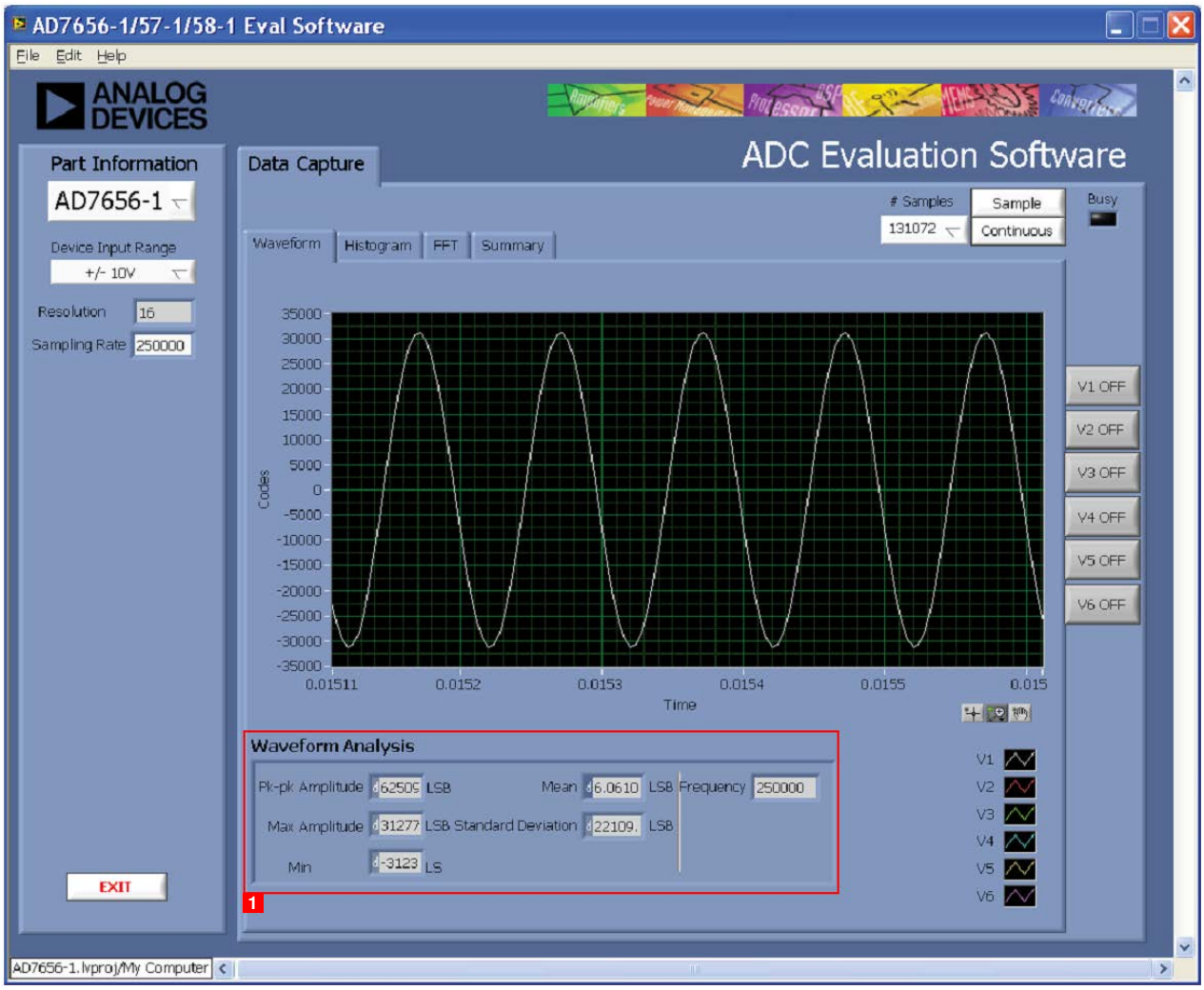


Figure 18. Waveform Tab

GENERATING A HISTOGRAM OF THE ADC CODE DISTRIBUTION

The **Histogram** tab can be used to perform ac testing or, more commonly, dc testing. This tab shows the ADC code distribution of the input and computes the mean and standard deviation, which are displayed as **Mean** and **Transition Noise**, respectively, in the **Histogram Analysis** area (labeled 1 in Figure 19).

Figure 19 shows the histogram with ac input for a 10 kHz sine wave applied to the ADC input and the resulting calculations.

AC Input

To perform a histogram test of ac input,

1. Apply a signal source to the selected analog input on the board.
2. Click the **Histogram** tab from the main window.
3. Click **Sample**.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

DC Input

A histogram test of dc input can be performed with or without an external source because the evaluation board has a buffered $V_{REF}/2$ source at the ADC input.

To perform a histogram test of dc input,

1. If an external source is being used, apply a signal source to the selected analog input. It may be required to filter the signal to ensure that the dc source is noise-compatible with the ADC.
2. Click the **Histogram** tab from the main window.
3. Click **Sample**.

Raw data is then captured and passed to the PC for statistical computations, and various measured values are displayed in the **Histogram Analysis** area.

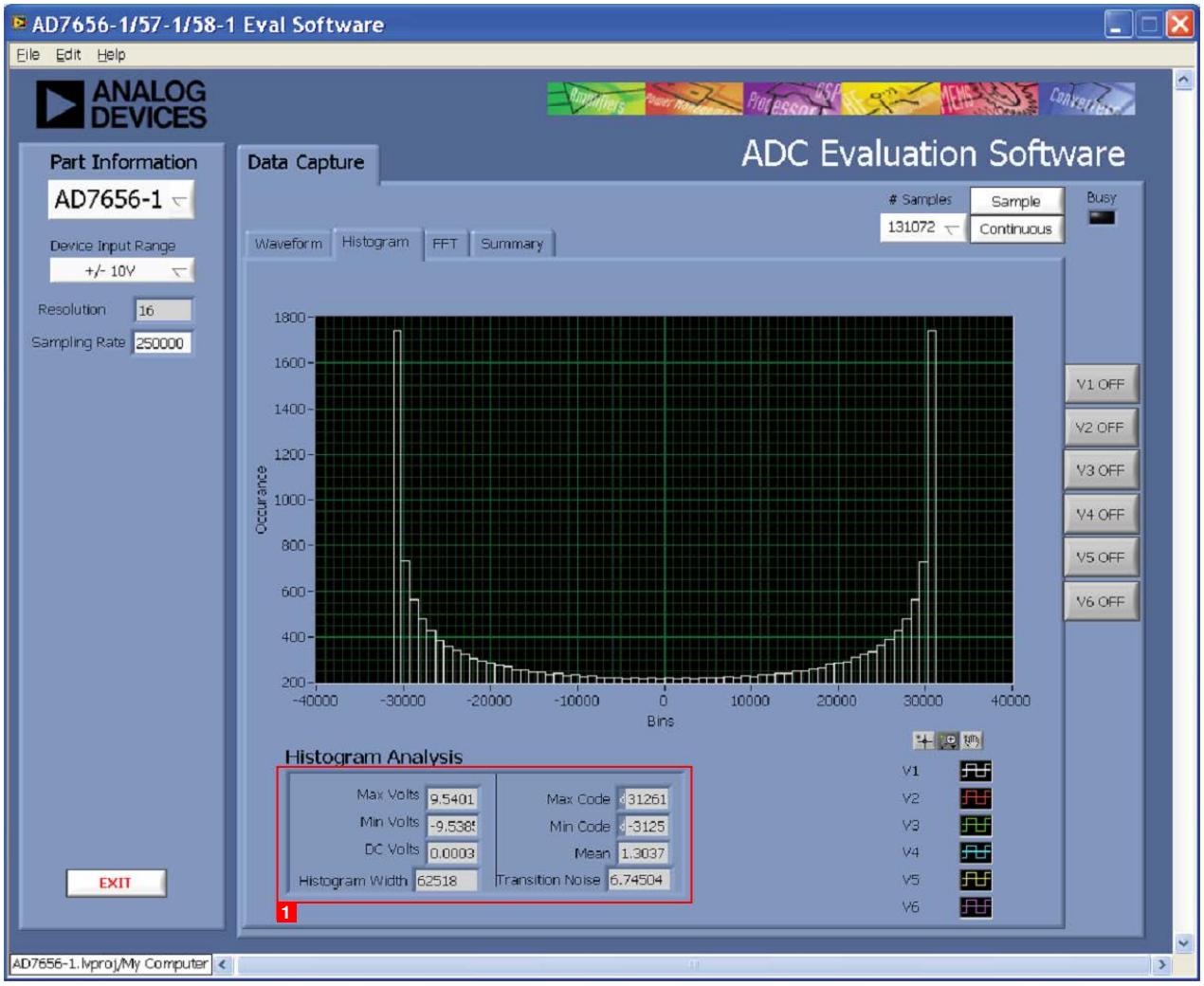


Figure 19. Histogram Tab

GENERATING A FAST FOURIER TRANSFORM OF AC CHARACTERISTICS

Figure 20 shows the **FFT** tab. This feature tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results.

To perform an ac FFT test,

1. Apply a sinusoidal signal with low distortion (better than 115 dB) to the evaluation board at the selected analog input. To attain the requisite low distortion, which is necessary to allow true evaluation of the part, one option is to
   a. Filter the input signal from the ac source. Choose an appropriate band-pass filter based on the sinusoidal signal applied.
   b. If a low frequency band-pass filter is used when the full-scale input range is more than a few volts peak-to-peak, use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.
2. Click the **FFT** tab from the main window.
3. Click **Sample**.

As in the histogram test, raw data is then captured and passed to the PC, which performs the FFT and displays the resulting SNR, THD, and SINAD.

The **Spectrum Analysis** box displays the results of the captured data.

- The area labeled 1 in Figure 20 shows the input signal information.
- The area labeled 2 in Figure 20 displays the fundamental frequency and amplitude in addition to the second to fifth harmonics.
- The area labeled 3 in Figure 20 displays the performance data, including the SNR, THD, and SINAD.

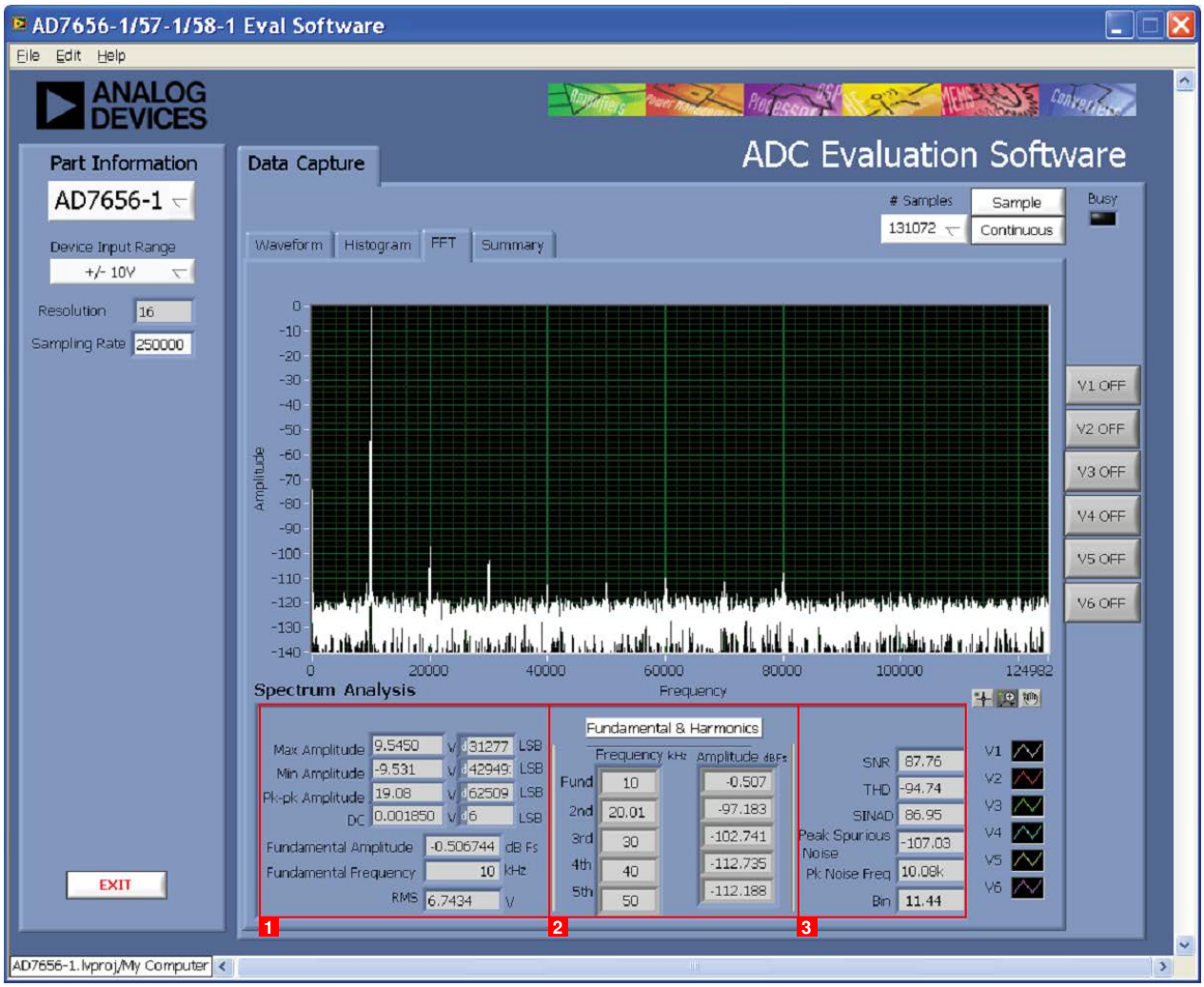


Figure 20. FFT Tab

GENERATING A SUMMARY OF THE WAVEFORM, HISTOGRAM, AND FAST FOURIER TRANSFORM

Figure 21 shows the **Summary** tab. The **Summary** tab captures all the display information and provides it in one panel with a synopsis of the information, including key performance parameters such as SNR and THD.

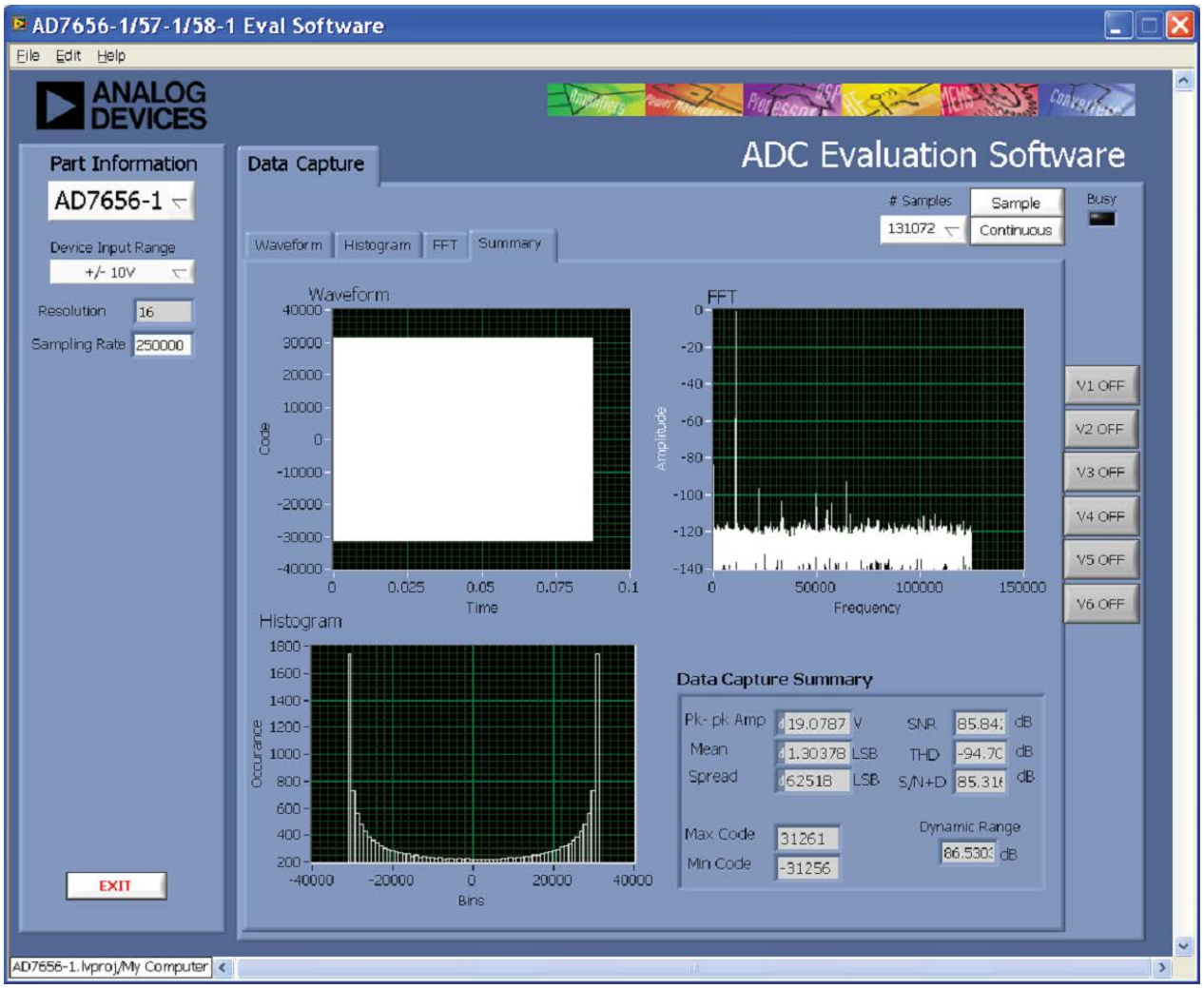


Figure 21. Summary Tab

RELATED LINKS

Resource	Description
AD7656-1	Product Page: 250 kSPS, 6-Channel, Simultaneous Sampling, Bipolar 16-Bit ADC
AD7657-1	Product Page: 250 kSPS, 6-Channel, Simultaneous Sampling, Bipolar 14-Bit ADC
AD7658-1	Product Page: 250 kSPS, 6-Channel, Simultaneous Sampling, Bipolar 12-Bit ADC
AD8597	Product Page: Ultralow Distortion, Ultralow Noise Op Amp (Single)
AD8031	Product Page: 2.7 V, 800 µA, 80 MHz Rail-to-Rail I/O Single Amplifier
ADP1613	Product Page: 650 kHz/1.3 MHz Step-Up PWM DC-to-DC Switching Converter with 2.0 A Current Limit
ADP3303-5	Product Page: High Accuracy anyCAP 200 mA Low Dropout Linear Regulator
ADP2301	Product Page: 1.2 A, 20 V, 1.4 MHz Nonsynchronous Step-Down Switching Regulator
ADM1185	Product Page: Quad Voltage Monitor and Sequencer
ADP190	Product Page: Logic Controlled, High-Side Power Switch
ADG3308	Product Page: Low Voltage, 1.15 V to 5.5 V, 8-Channel Bidirectional Logic Level Translator
ADR431	Product Page: Ultralow Noise XFET 2.5 V Voltage Reference with Current Sink and Source Capability
AD780	Product Page: 2.5 V/3.0 V Ultrahigh Precision Band Gap Voltage Reference
EngineerZone	Online Community: Analog Devices Online Technical Support Community
Circuits from the Lab	Reference Circuits: Circuit Designs that Have Been Built and Tested to Ensure Function and Performance and that Address Common Analog, RF/IF, and Mixed-Signal Design Challenges by Applying Analog Devices' Vast Applications Expertise

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

UG10726-0-6/13(0)