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Evaluation Board for AD7779 24-Bit, 8-Channel, Simultaneous Sampling, Sigma-Delta ADC with Power Scaling

FEATURES

- Full featured evaluation board for the AD7779
- PC control in conjunction with the Analog Devices, Inc., system demonstration platform (SDP), EVAL-SDP-CH1Z
- PC software control and data analysis
- Time and frequency domain
- Standalone hardware capability

ONLINE RESOURCES

- Evaluation Kit Contents
  - EVAL-AD7779FMCZ evaluation board
  - AD7779 evaluation software
- Documents Needed
  - AD7779 data sheet
  - EVAL-AD7779FMCZ user guide
- Required Software
  - AD7779 evaluation software

EQUIPMENT NEEDED

- EVAL-AD7779FMCZ evaluation board
- System demonstration platform—high speed (SDP-H1) controller board (EVAL-SDP-CH1Z)
- DC/AC signal source (Audio Precision or similar)
- USB cable
- PC running Windows 7 with USB 2.0 port
- External +9 V supply (for standalone use)

GENERAL DESCRIPTION

The EVAL-AD7779FMCZ evaluation kit features the AD7779 24-bit, analog-to-digital converter (ADC). The board interfaces with the System Demonstration Platform SDP-H1 controller board (EVAL-SDP-CH1Z). This controller board supplies power to the EVAL-AD7779FMCZ evaluation board and also connects to a PC using a Windows® operating system via a USB cable. The AD7779 evaluation software fully configures the AD7779 device register functionality and provides dc and ac time domain analysis in the form of waveform graphs, histograms, and associated noise analysis for ADC performance evaluation.

The EVAL-AD7779FMCZ is an evaluation board that allows the user to evaluate the features of the ADC. The user PC software executable controls the AD7779 over the USB cable through the SDP-H1 controller board.

Full specifications on the AD7779 are available in the product data sheet, which should be consulted in conjunction with this user guide when working with the evaluation board.

TABLE OF CONTENTS

REVISION HISTORY

2/16—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH

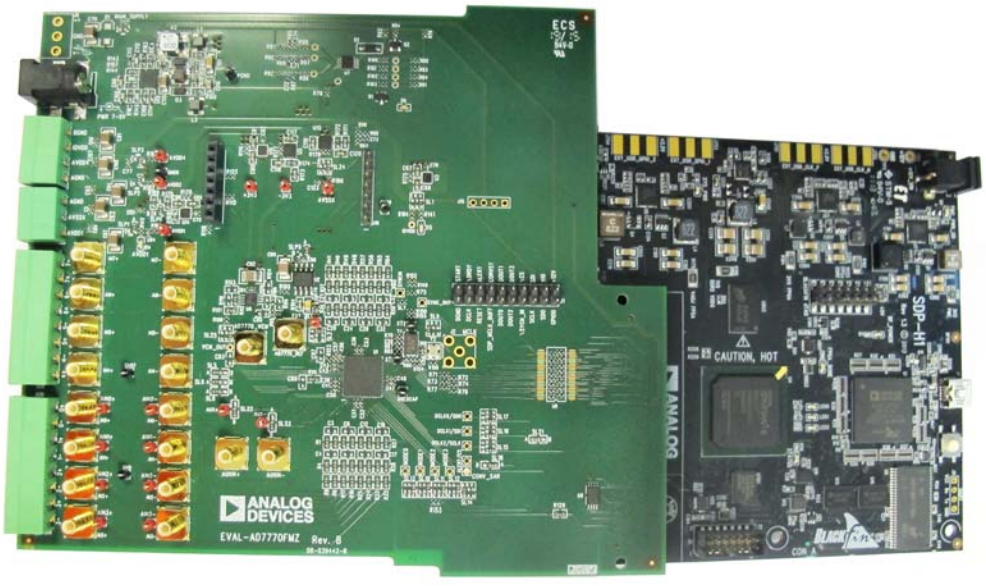


Figure 1. EVAL-AD7779FMCZ Evaluation Board with SDP-H1 Controller Board

EVAL-AD7779FMCZ QUICK START GUIDE

To begin using the evaluation board, take the following steps:

1. Ensure the evaluation board is disconnected from the USB port of the PC. Install the AD7779 evaluation software from the CD included in the evaluation board kit. Restart the PC after the software installation is complete. (For complete software installation instructions, see the Software Installation section.)
2. Connect the SDP-H1 board to the evaluation board: CON J4 of the SDP-H1 board adapts to the receiving socket on the EVAL-AD7779FMCZ printed circuit board (PCB).
3. Ensure that the boards are connected firmly together.
4. By default, the power for the evaluation board is supplied from the SDP-H1 controller board. A number of power options available; see Table 3 for more information.
5. Connect the SDP-H1 board to the PC using the supplied USB cable.
6. Launch the AD7779 evaluation software from the **Analog Devices** subfolder in the **Programs** menu.

Note that pin control mode is not directly supported in the Rev. H version of the software.

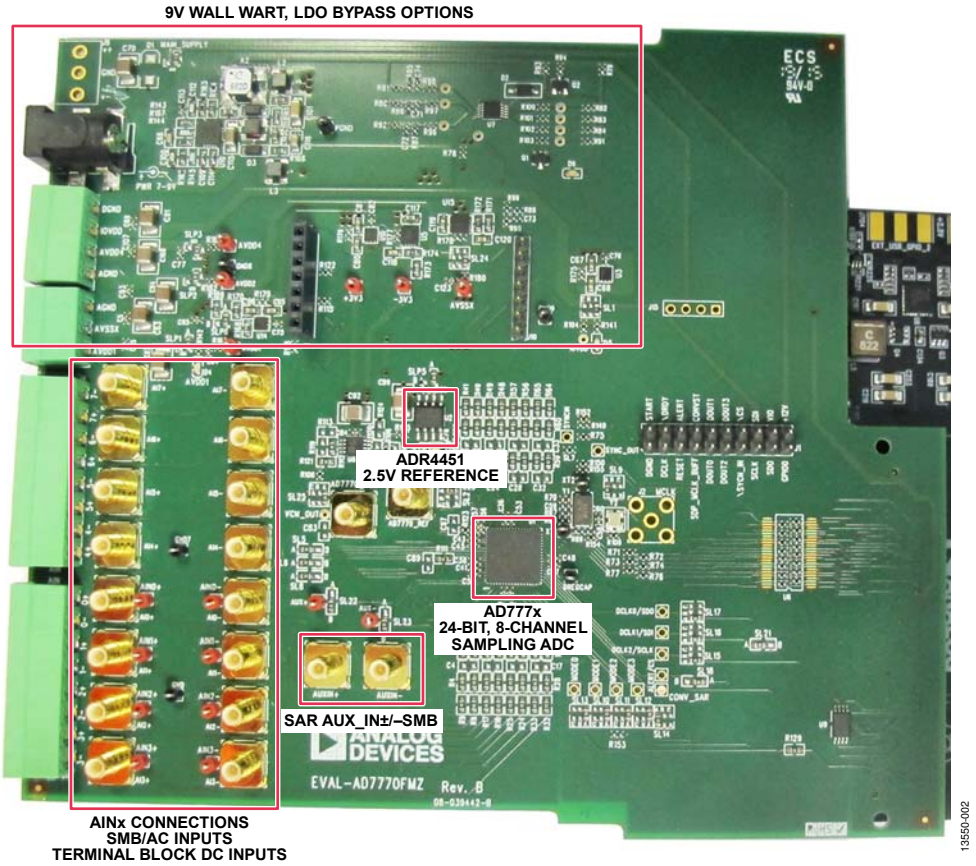


Figure 2. Hardware Configuration—Setting Up the EVAL-AD7779FMCZ

ANALOG INPUTS AND FRONT-END CIRCUIT

As shown in Figure 2, the AIN0± to AIN7± analog Σ-Δ inputs are available on SMB or terminal block inputs. The AUXIN± inputs to the auxiliary SAR converter are available through the SMB inputs.

Figure 2 shows these connectors to the ADC input terminals. Each analog input differential pair has a second-order RC filter option and common-mode option to center the input signal at AVDD1A/2. An option is available to place an additional VCM buffer in U8 to add drive strength and also gain, attenuation, or filtering to this VCM signal. Channel 7 has the option to evaluate an external drive amplifier on J7/J10 using the analog device amplifier surfboard. The SL3, SL4, SL19, and SL20 solder link options select between applying the AIN±7 analog inputs directly to the RC filter and ADC, or to the surfboard inputs. The evaluation board includes a buffer (AD8659) connected to AIN±0 and AIN±2, and a multiplexer that can be connected to the AIN0± to AIN7± Σ-Δ inputs when the SAR is used for redundancy. If this function is required, solder a 0 Ω, 0402 size resistor to the unpopulated resistor footprints (see Figure 16 for more details), and move SL22 and SL23 to Position A.

The default configuration of the board is as follows:

- Connect the input signal from the input terminals through the second-order RC filter (do not populate) to the ADC channels.
- The board accepts ac signals from −1.25 V to +1.25 V.
- The ADR441 2.5 V, low noise reference is used by default, allowing an absolute input range of 0 V to 2.5 V on each input.
- No external buffers are populated.

EVALUATION BOARD HARDWARE

DEVICE DESCRIPTION

The AD7779 is an 8-channel, simultaneously sampled, 24-bit, Σ-Δ ADC with an additional diagnostics 12-bit SAR. The AD7779 offers an ADC per channel with synchronized sampling.

To cater to application specific ADC power scaling requirements, the user can select either the high resolution mode or low power mode. In high resolution mode, the ADC operates at 16 kSPS maximum, with 111 dB signal-to-noise ratio (SNR), and consumes 16 mW per channel. In low power mode, the ADC operates at 4 kSPS maximum, with 111 dB of SNR, and consumes 5.5 mW per channel.

The AD7779 also provide a low latency, sinc3 filter for digital filtering. The notches of the digital filter are automatically set to remove harmonics at the sampling frequency and the PGA chopping frequency.

The sample rate converter allows the user to fine tune the decimation rate to maintain a number of samples per line cycle for varying input frequencies. Choosing a low output data rate increases the dynamic range, reducing the noise. Decimation rates can be programmed via the AD7779 evaluation software.

Embedded analog functionality on each ADC channel eases system design. The AD7779 has a fully buffered PGA on each channel to reduce analog input current. The AD7779 also has a reference buffer on each channel, which provides a high impedance input reference to the external precision reference.

Complete specifications for the AD7779 are provided in the product data sheet, which should be consulted in conjunction with this user guide when using the evaluation board. Full details about the EVAL-SDP-CH1Z are available on the Analog Devices, Inc., website at www.analog.com/SDP-H1.

HARDWARE LINK OPTIONS

The default power link options are listed in Table 1, Table 2, and Table 3. The evaluation board can be powered by different sources, as described in Table 1.By default, the supply required for the evaluation board comes from the SDP-H1 controller board. The supply is regulated by the on-board ADP5070 SMPS, which generates the dual supply, and the ADP7118 and the ADP7182 low dropout (LDO) regulators reduce noise and generate the low noise, regulated, positive and negative rails.

Table 1. Default Link and Solder Link Options for Power Supply

Link No.	Default Option	Description
MAIN_SUPPLY	A	Unregulated input voltage source selection. Position A: the unregulated supply to the on-board LDOs is taken from the SDP-H1 12 V supply. Position B: the unregulated external supply to the on-board LDOs is taken from the J5 9 V wall wart input or from the J6 connector.
SL1	A	IOVDD supply selection. Position A: IOVDD is supplied from the SDP-H1 board. Set to 3.3 V by default. Position B: IOVDD is supplied from ADP7118 3.3 V, precision LDO. Position C: EXT_IOVDD. IOVDD can be supplied from the J17-3 terminal block (1.8 V to 3.3 V). The SDP-H1 only supports 3.3 V logic. If IOVDD is operated below 3.3 V, populate the U6 buffer to avoid electrical problems.
SLP1	A	AVDD1 supply selection. Position A: AVDD1 is taken from U14, the ADP7118 LDO. See SLP6 for more options. Position B: AVDD1 is taken from the J3-1, AVDD1 external supply.
SLP2	A	AVDD2 supply selection. Position A: AVDD2 is taken from U14, the ADP7118 LDO. See SLP6 for more options. Position B: AVDD2 is taken from the J17-1 external source.
SLP3	A	AVDD4 supply selection. Position A: AVDD4 is taken from U14, the ADP7118 LDO. See SLP6 for more options. Position B: AVDD4 is taken from the J17-2 external source.
SLP6	A	On-board regulated positive rail selection. Position A: 1.65 V. Use this option for dual-supply operation. Position B: 3.3 V. Use this option for single-supply operation.
SL24	A	Regulated negative rail selection. Position A: AVSSx is taken from U15, the ADP7182 1.65 V LDO. Use this option for dual-supply operation. Position B: AGND. Use this option for single-supply operation. Position C: AVSSx is supplied by J3-2, the AVSSx external supply.

Table 2. AFE Options

Link No.	Default Option	Description
SL22	B	SAR AUX+ input selection. Position A: AUXIN+ is connected to the on-board multiplexer, which is controlled by the AD7779 GPIO pins. If the multiplexer needs to be used, solder the unpopulated resistor that connects the multiplexer inputs to the Σ-Δ ADC inputs. The evaluation board includes an op amp connected to Channel 0 and Channel 2 of the Σ-Δ ADC. Position B: direct connection from source to AUXIN+ SMB connector.
SL23	B	SAR AUX− input selection. Position A: AUXIN− is connected to the on-board multiplexer which is controlled by the AD7779 GPIO pins. If the multiplexer needs to be used, solder the unpopulated resistor that connects the multiplexer inputs to the Σ-Δ ADC inputs. The evaluation board includes an op amp connected to Channel 0 and Channel 2 of the Σ-Δ ADC. Position B: direct connection from source to AUXIN− SMB connector.
SL3, SL19	A	AIN7+ input driver selection. Position A: direct connection from source to AIN7+. Position B: surfboard connection J7/J10 drives the analog inputs.
SL4, SL20	A	AIN7− input driver selection. Position A: direct connection from source to AIN7−. Position B: surfboard connection J7/J10 drives the analog inputs.
SLP5	A	ADR441 external voltage reference supply selection. Position A: the reference is powered by the ADP5070. Use this option if the board is powered by the on-board regulators. Position B: the reference is powered by the AVDD1 supply. Use this option if the board is powered by J3 and J17.
SL2	A	Voltage reference selection. Position A: the ADR441 is used as a voltage reference. Position B: the AD7779 internal reference is used. Position C: the ADR441 is buffered and used as a reference. Open: an external voltage reference can be connected to the AD7779_REF SMB connector.
SL25	A	Common-mode voltage output (V_{CM}) selection. Position A: V_{CM} signal to analog front-end signal is AGND. Use this option for dual-supply operation. Position B: the VCM pin is buffered through the U8 output. Position C: the V_{CM} signal to the analog front end is taken directly from the AD7779 VCM pin. Open: an external V_{CM} signal can be connected to the AD7779_VCM SMB connector.

Table 3. Digital Connections

Link No.	Default Option	Description
K0 to K15	Inserted	Digital input/output solder links. These links are inserted by default for unbuffered digital input/output connection between the controller board and the evaluation board. Remove and insert U6 for buffered digital inputs/outputs.
SL5, SL6	A	Data interface format pins. The evaluation software only supports SPI control mode. The default condition is SPI configuration. See the AD7779 data sheet for more information.
SL7	Inserted	SL7 provides a path between $\overline{\text{SYNC\_OUT}}$ and $\overline{\text{SYNC\_IN}}$. The user can provide an asynchronous start signal to the device. On the next MCLK falling edge, the AD7779 outputs a $\overline{\text{SYNC\_OUT}}$ signal, which is synchronous to the MCLK. This signal synchronizes multiple AD7779 devices or resets the SD modulators when phase compensation is used.
SL8	A	Clock select option. Position A: the CLK_SEL pin is pulled low and selects the CMOS clock option. Position B: the CLK_SEL pin is pulled high and selects the crystal oscillator placed in Y1. To select this crystal oscillator, remove the SL9 connections and insert R69 and R70.
SL9	A	CMOS clock input selection: Position A: the on-board CMOS clock is selected (Y2). Position B: J2 can be used to provide an external CMOS clock through the SMB input terminal. Position C: MCLK is supplied from the J1 connector.

Link No.	Default Option	Description
SL10, SL11, SL13	A	GPIO/mode pins. In SPI control mode, Pin 13 to Pin 16 act as GPIOs. See the AD7779 data sheet for more information about additional functionality of these pins for hardware sample rate update source. Position A: Pin 13 to Pin 16 are connected to the GPIOx net that controls the on-board multiplexer, or can be used to update the SRC (R153 needs to be populated with a 0 Ω resistor). In pin control mode, Pin 13 to Pin 16 (along with SL12) are used to set up the configuration of the device. For more information on GPIO configuration or pin mode, see the AD7779 data sheet. Position B: Pin 13 to Pin 16 are connected to IOVDD. Position C: Pin 13 to Pin 16 are connected to DGND.
SL12	A	Alert/mode. In SPI control mode, this pin operates as an alert flag. Position A: error flag. This pin is connected to the J1 and J4 connectors. See SL21 for more details. In pin control mode, this pin becomes the Mode 3 input pin. Used in conjunction with the GPIO/mode pins to set up the device configuration. See the AD7779 datasheet for more details. Position B: the pin is connected to IOVDD. Position C: the pin is connected to DGND.
SL14	A	CONVST_SAR selection. In SPI control mode, this link selects the conversion signal source. Position A: the SAR ADC is controlled through the J1 connector. In pin control mode, CONVST_SAR (Pin 17), along with SL5 and SL6, set up the serial interface used to read back the conversions from the Σ-Δ ADC. Position A: CONVST_SAR (Pin 17) is connected to IOVDD. Position B: CONVST_SAR (Pin 17) is connected to DGND.
SL15, SL16, SL17	A	SPI data interface lines. In SPI mode configuration, SCLK, SDI, and SDO are used as digital interface pins. Position A: the SPI data interface lines are connected to the FMC-LPC connector. In pin control mode, these pins define the DCLK frequency used to read back the Σ-Δ data through the DOUT interface. See the AD7779 data sheet for more details. Position B: IOVDD. Position C: DGND.
SL18	A	SPI data interface line. In SPI mode configuration, $\overline{CS}$ (Pin 18) is used as a digital interface pin. Position A: $\overline{CS}$ (Pin 18) is connected to the FMC-LPC connector. In pin control mode, $\overline{CS}$ (Pin 18) acts as an alert pin. Position B: error flag, $\overline{CS}$ (Pin 18) is connected to the J1 and J4 connectors. See SL21 for more details.
SL21	A	Alert connection. Position A: SPI control mode. Position B: pin control mode.

On-Board Connectors

Table 4 provides information about the external connectors on the EVAL-AD7779FMCZ.

Table 4. On-Board Connectors

Connector	Function
J1	General connector for debugging purpose or to connect an external controller
J2	MCLK connector, supplies the external square wave clock
J3	External power supply connector
J4	FMC connector
J5	External power supply connector
J6	External 9 V wall wart connection
J7	Channel 7 surfboard evaluation header
J8, J9	8-pin connector for input to Channel 0 through Channel 3
J10	Channel 7 surfboard evaluation header
J13, J14	8-pin connector for input to Channel 4 through Channel 7
J15	External power supply, supplies all rails independent of LDO supplies

SERIAL CONFIGURATION INTERFACE

The AD7779 can be configured by the FPGA via a 4-wire SPI interface. Format 0 and Format 1 must be shorted to Position A for this mode to be active.

To operate the EVAL-AD7779FMCZ evaluation board in standalone mode,

1. Connect a power supply (see Table 1 for options).
2. Connect the DSP, microcontroller, or FPGA to the J1 interface connector.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

The EVAL-AD7779FMCZ evaluation kit includes software on a CD. Click the **setup.exe** file from the CD to run the installer. The default installation location for the software is **C:\Program Files\Analog Devices\EVAL-AD7779FMCZ**.

Install the evaluation software before connecting the evaluation board and SDP-H1 board to the USB port of the PC to ensure that the evaluation system is correctly recognized when it is connected to the PC.

There are two sections to the installation:

- AD7779 evaluation software installation
- SDP-H1 board drivers installation

Place the software and drivers in the appropriate locations by proceeding through all of the installation steps. Connect the SDP-H1 board to the PC only after the software and drivers are installed. The installer may prompt for permission to make changes to the computer. Click **Yes** to proceed (see Figure 4).

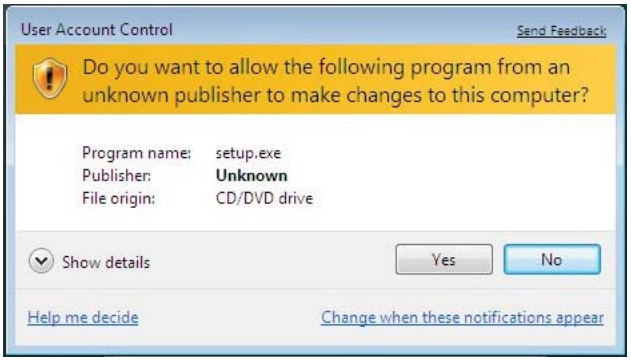


Figure 3. User Account Control Permission Dialog Box

A security warning may appear as part of the SDP-H1 controller board driver installation. Click **Install** to proceed with the installation of the driver (see Figure 5). Without this confirmation, the software cannot operate correctly.

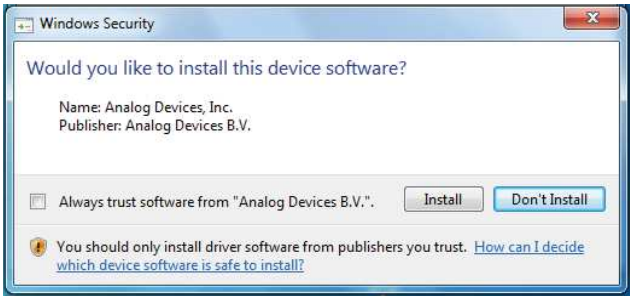


Figure 4. EVAL-SDP-CB1Z Drivers Installation Confirmation Dialog Box

After installation is complete, connect the evaluation board to the SDP-H1 controller board. Connect the SDP-H1controller board via the USB cable to the computer. Follow these steps to verify that the SDP-H1 controller board driver are installed and working correctly:

1. Allow the **Found New Hardware Wizard** to run.
2. After the drivers are installed, check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be found by right clicking **My Computer**, selecting **Manage**, then **Device Manager** from the list of **System Tools** (see Figure 6).
3. The SDP-H1 board appears under **ADI Development Tools** as **Analog Devices SDP-H1** or similar. The installation is complete.

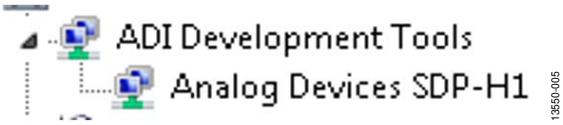


Figure 5. Device Manager

LAUNCHING THE SOFTWARE

The AD7779 evaluation software can be launched when the evaluation board and the SDP-H1 controller board are correctly connected to the PC.

To launch the software, take the following steps:

1. From the **Start** menu, click **Programs**, **Analog Devices**, then **EVAL-AD7779FMCZ**. The main window of the software then displays (see Figure 8).
2. If the AD7779 evaluation system is not connected to the USB port via the SDP-H1 board when the software is launched, the **Select Interface…** dialog box appears. Connect the evaluation board to the USB port of the PC, wait a few seconds, and then click the green arrows to rescan the USB ports. When the connection is established, click **Work Online** to proceed.

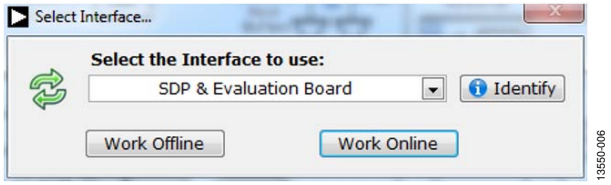


Figure 6. Select Interface Dialog Box

SOFTWARE OPERATION

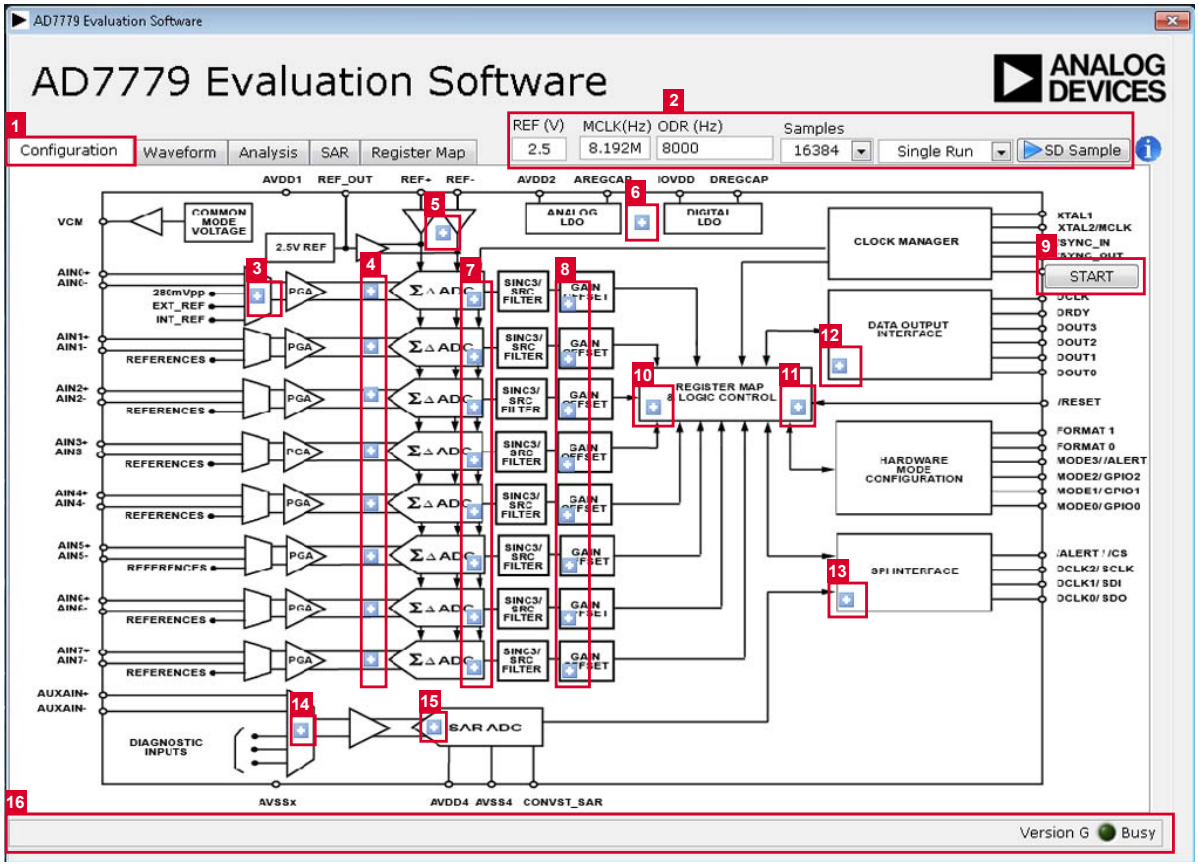


*Figure 7. **Configuration** Tab of the AD7779 Evaluation Software*

OVERVIEW OF THE MAIN WINDOW

The main window of the software displays the significant control buttons and analysis indicators of the EVAL-AD7779FMCZ evaluation board software (see Figure 7). This window is divided into five tabs.

CONFIGURATION TAB

General Configuration

The general configuration controls (Label 2 in Figure 7) define the voltage reference, external clock, the output data rate, number of samples, and if the SD is read continuously or one time only.

When changing the **ODR (Hz)** value, click away from the field to process the update. The software programs the SRC registers accordingly.

Click **SD Sample** to acquire samples from the AD7779.

Σ-Δ ADC Diagnostic Pop-Up Button

The Σ-Δ ADC diagnostic pop-up button (Label 3) selects the internal diagnostic inputs from the multiplexer. This input is common for all eight ADCs.

SD Input Configuration Pop-Up Buttons

The SD input configuration pup-up buttons (Label 4) select the ADC gain, enable the diagnostic mux to be the input for the channel (Rx), disable the SD channel, or configure the channel to monitor the voltage reference. Clicking this button selects the SD reference as VDD3/AVSSx for all channels and the input diagnostic mux as the input for this channel.

Reference Voltage Pop-Up Buttons

The reference voltage pop-up buttons (Label 5) set the reference voltage used for calculating the results in the **Waveform** and **Histogram** tabs. The evaluation board has an external 2.5 V ADR441 reference; however, this reference can be bypassed using this pop-up button, and the user can change the external reference voltage value to ensure correct calculation of results in the **Waveform** and **Histogram** tabs. Internal reference and reference buffers can be selected using these pop-up buttons. If AVDD3/AVSSx is selected as the reference, the **REF (V)** value must be updated accordingly.

Regulators Pop-Up Button

The regulators pop-up button (Label 6) allows the user to overdrive the internal LDOs externally, and also provides information about the error detected on the regulators.

SD Errors Pop-up Buttons

The SD errors pop-up buttons (Label 7) show the errors detected on the SD channel.

Gain, Offset, and Phase Pop-up Buttons

The gain, offset, and phase pop-up buttons (Label 8) allow the user to calibrate the offset and gain of each specific SD channel. After the phase compensation is updated, click **START** to apply the change.

START Button

Clicking **START** (Label 9) generates a pulse on the START pin to reset the internal sinc filter, which ensures that any update on the phase compensation register is correctly applied.

Control Configuration Pop-Up Button

The control configuration pop-up button (Label 10) allows the user to configure features such as the power mode (must be set to high power mode, unless a different clock is provided), the common-mode voltage (VCM), the internal oscillator, and the mode to update the ODR (SRC registers).

It is recommended not to change the SRC load source (Bit 7 in the SRC load source and load update register, Address 0x64[7]), because the GUI only support software updates. Selecting SRC_LOAD_SOURCE 0x64 [7] is not supported on the evaluation board.

The SRC register can be updated manually; however, the update is not reflected in the **ODR (Hz)** field.

Errors related to the memory map appear in this pop-up.

Error Test Pop-Up Button

The error test pop-up button (Label 11) enables and disables the different error checkers implemented in the AD7779.

Data Output Interface Pop-Up Button

The data output interface pop-up button (Label 12) adjusts the DOUT header and driver strength.

SPI Interface Pop-Up Button

The SPI interface pop-up button (Label 13) adjusts the various parameters for the SPI and shows any SPI errors.

SAR Input Pop-Up Button

The SAR input pop-up button (Label 14) allows the user to select the input signal for the SAR ADC.

SAR Power Pop-Up Button

The SAR power pop-up button (Label 15) enables and disables the SAR ADC. If the SAR is disabled, the SAR input mux is disabled as well.

Status Bar

The status bar (Label 16) displays the status of the board and indicates if the board is busy and cannot perform any other action.

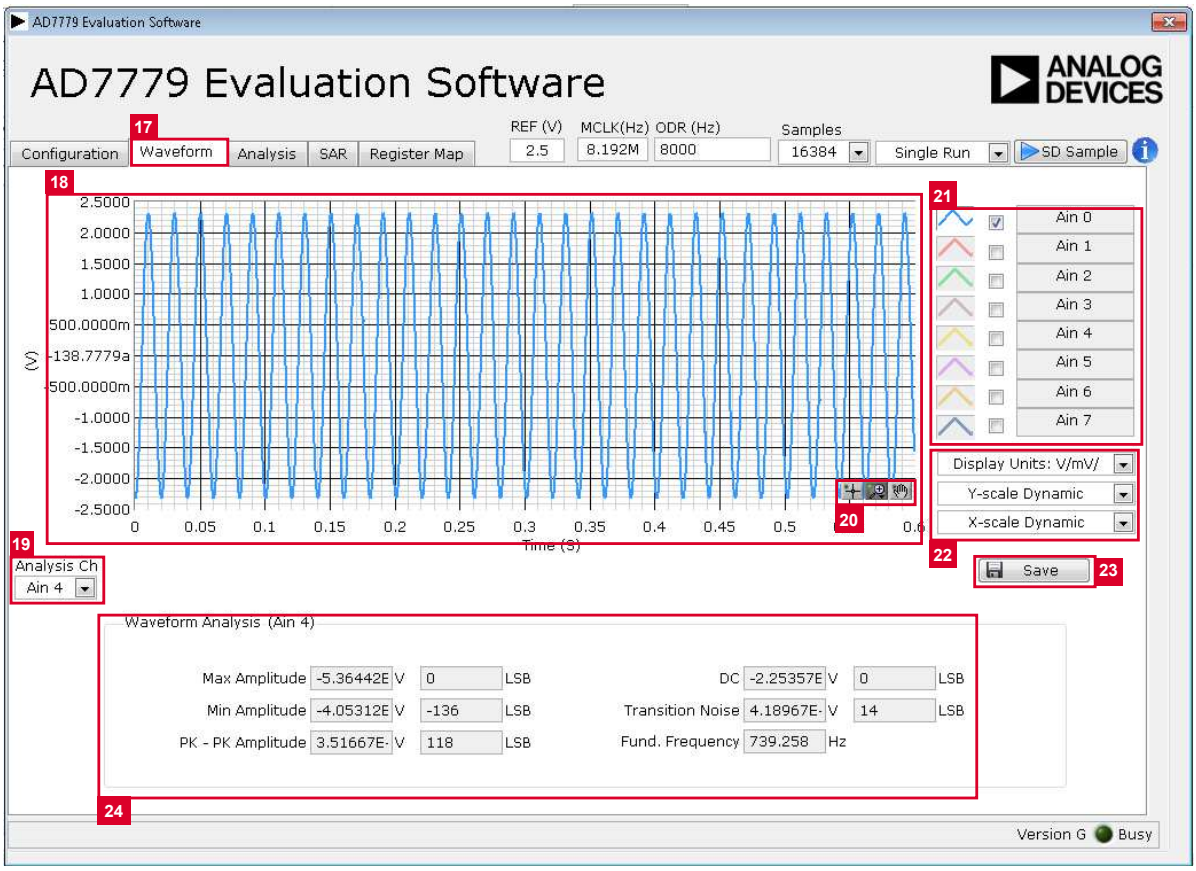


*Figure 8. **Waveform** Tab of the AD7779 Evaluation Software*

WAVEFORM TAB

Waveform Graph and Controls

The data waveform (Label 18) shows each successive sample of the ADC output. The control tools (Label 20) in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel

The noise/waveform analysis section (Label 24) and histogram graph show the analysis of the channel selected via the **Analysis Ch** drop-down box (Label 19).

Channel Selection

The channel selection control (Label 21) allows the user to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

Display Units and Axis Controls

Use the **Display Units** drop-down box (Label 22) to select whether the data graph displays in units of voltages or codes. This affects both the waveform graph and the histogram graph. The axis controls can be switched between dynamic and fixed. When dynamic is selected, the axis automatically adjusts to show the entire range of the ADC results after each batch of samples. When fixed is selected, the user can program the axis ranges manually, and the ranges do not adjust automatically after each sample batch.

If the value is selected as hex, the x-axis of the graph shows the original data (second complement). Due to the limitations of the software, the number shows as signed 32 bits rather than signed 24 bits.

Save Data

Click **Save** (Label 23) to save the samples to an external file.

Waveform Analysis

The **Waveform Analysis** section (Label 24) displays the results of the noise analysis for the selected analysis channel. The rms noise is only applicable with a constant dc value.

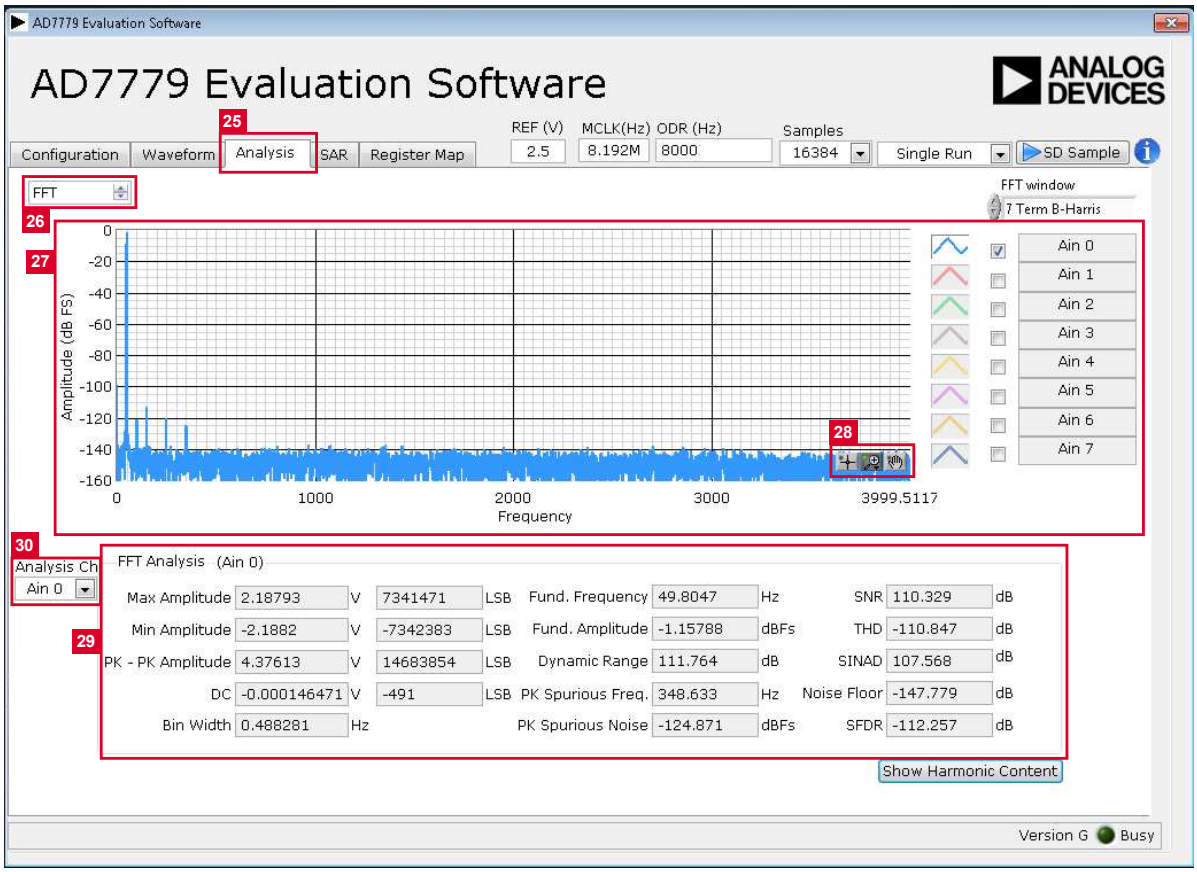


*Figure 9. **Analysis** Tab of the AD7779 Evaluation Software*

ANALYSIS TAB

FFT Graph and Histogram Selection

Use the FFT/histogram selection box (Label 26) to select between histogram and frequency analysis of the data.

FFT Graph and Controls

The FFT graph (Label 27) shows the fast Fourier transform of the sampled signal. Note that the windows applied is the 7-term Blackman Harris. The frequency is displayed on the x-axis and the amplitude is graphed on the y-axis. Use the control tools (Label 28) to zoom in on the data. Harmonic content can be selected by clicking **Show Harmonic Content**.

Analysis Channel

The noise/waveform analysis section (Label 29) and the FFT graph show the analysis of the channel selected via the **Analysis Ch** control (Label 30).

Channel Selection

The **Analysis Ch** control (Label 30) allows the user to choose which channels display on the data waveform. It also shows the analog inputs for that channel labeled next to the on and off controls. These controls only affect the display of the channels and do not have any effect on the channel settings in the ADC register map.

FFT Window Selection

The **FFT window** control allows the user to choose which external windowing method to apply to calculate the discrete Fourier transform.

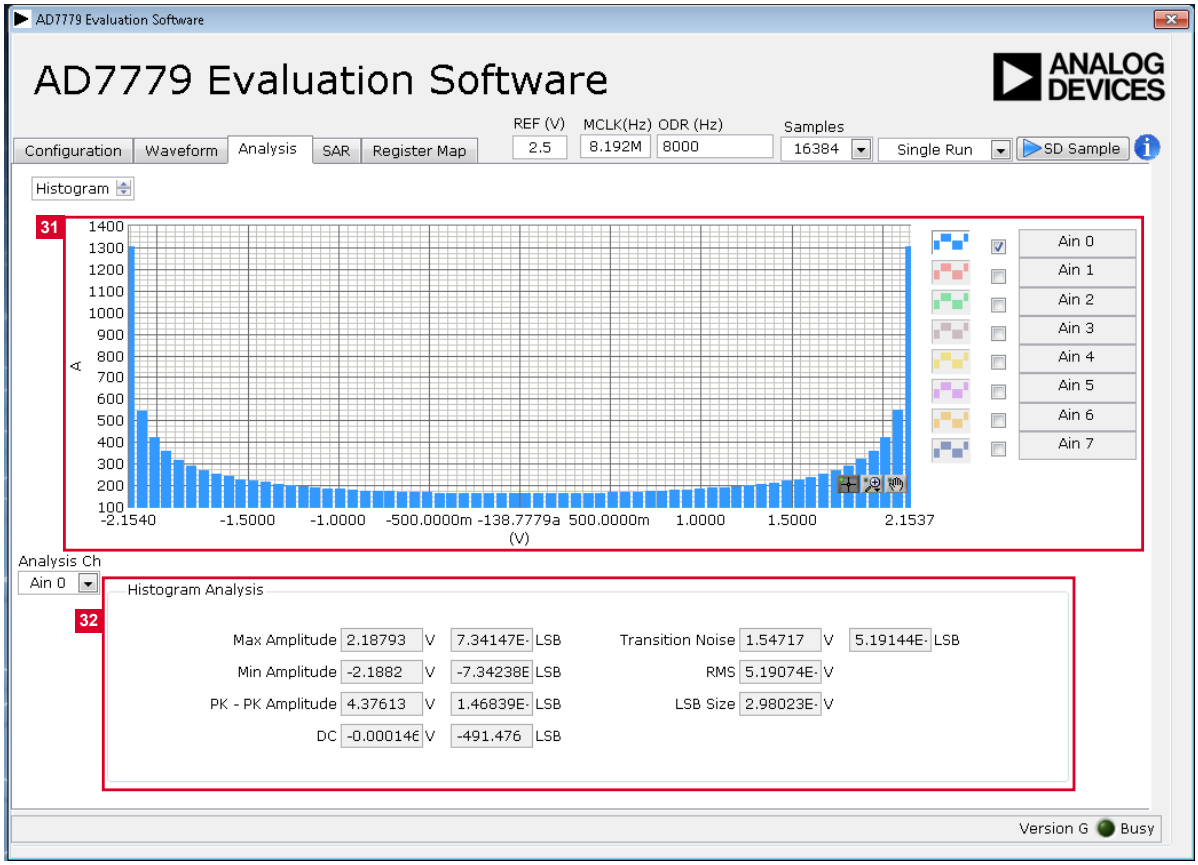


Figure 10. Histogram Tab of the AD7779 Evaluation Board Software

Histogram and Controls

The data histogram (Label 31) shows the number of times each sample of the ADC output occurs. The control tools in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

Histogram Analysis

The **Histogram Analysis** section (Label 32) shows the analysis of the channel selected via the **Analysis Ch** control.

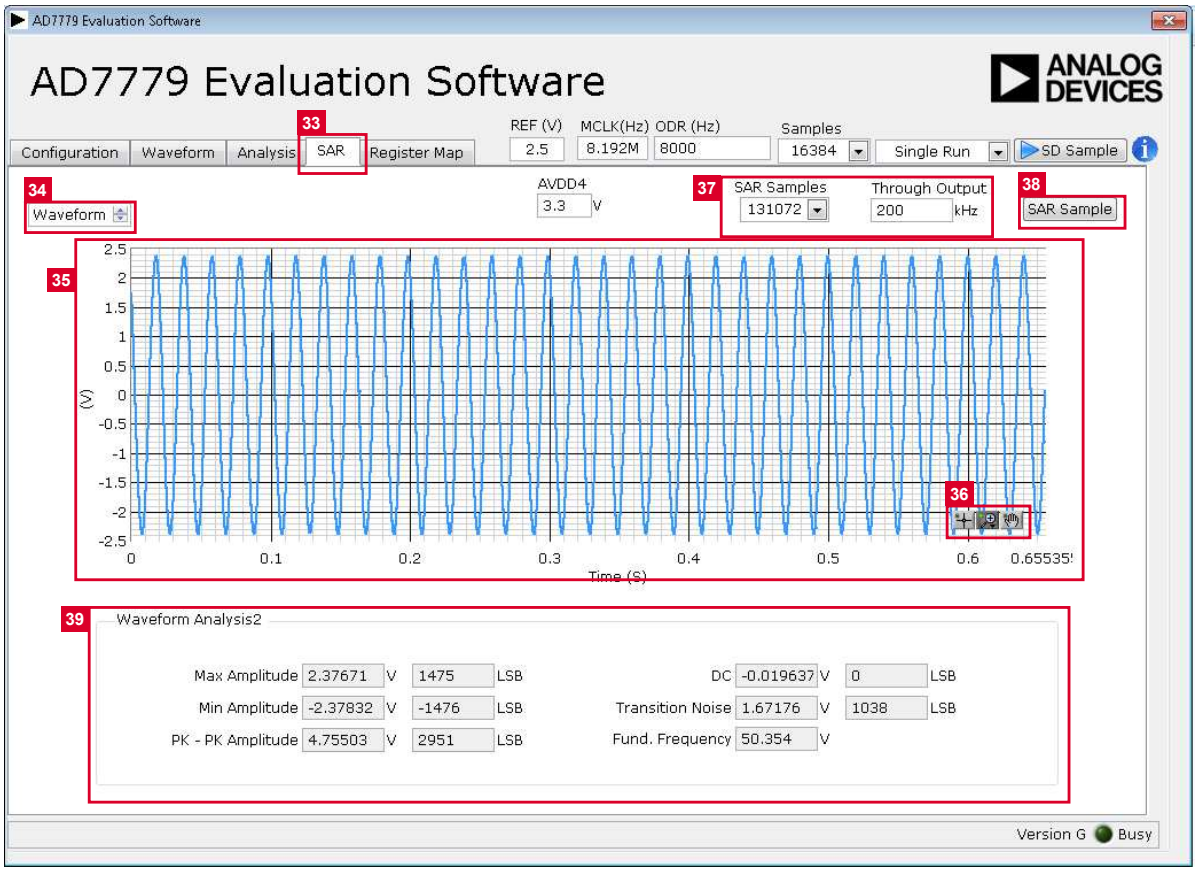


Figure 11. SAR Waveform Tab of the AD7779 Evaluation Software

SAR TAB

When the SAR ADC is enabled through the SAR power pop-up button (Label 15 in Figure 7), the **SAR** tab allows the user to sample and analyze data from the SAR ADC.

FFT Graph and Waveform Selection

Use the FFT/waveform selection box (Label 34) to select between waveform and frequency analysis of the data.

Waveform Graph and Controls

The data waveform (Label 35) shows each successive sample of the ADC output. The control tools (Label 36) in the graph allow the user to zoom in on the data. Change the scales on the graph by typing values into the x-axis and y-axis.

Analysis Channel

The noise/waveform analysis section (Label 39) and histogram graph show the analysis of the channel selected via the **Analysis Ch** control.

SAR Configuration

The SAR configuration controls (Label 37) allow the user to define the number of samples and the through output channel.

SAR sample

Click **SAR Sample** (Label 38) to gather samples from the SAR.

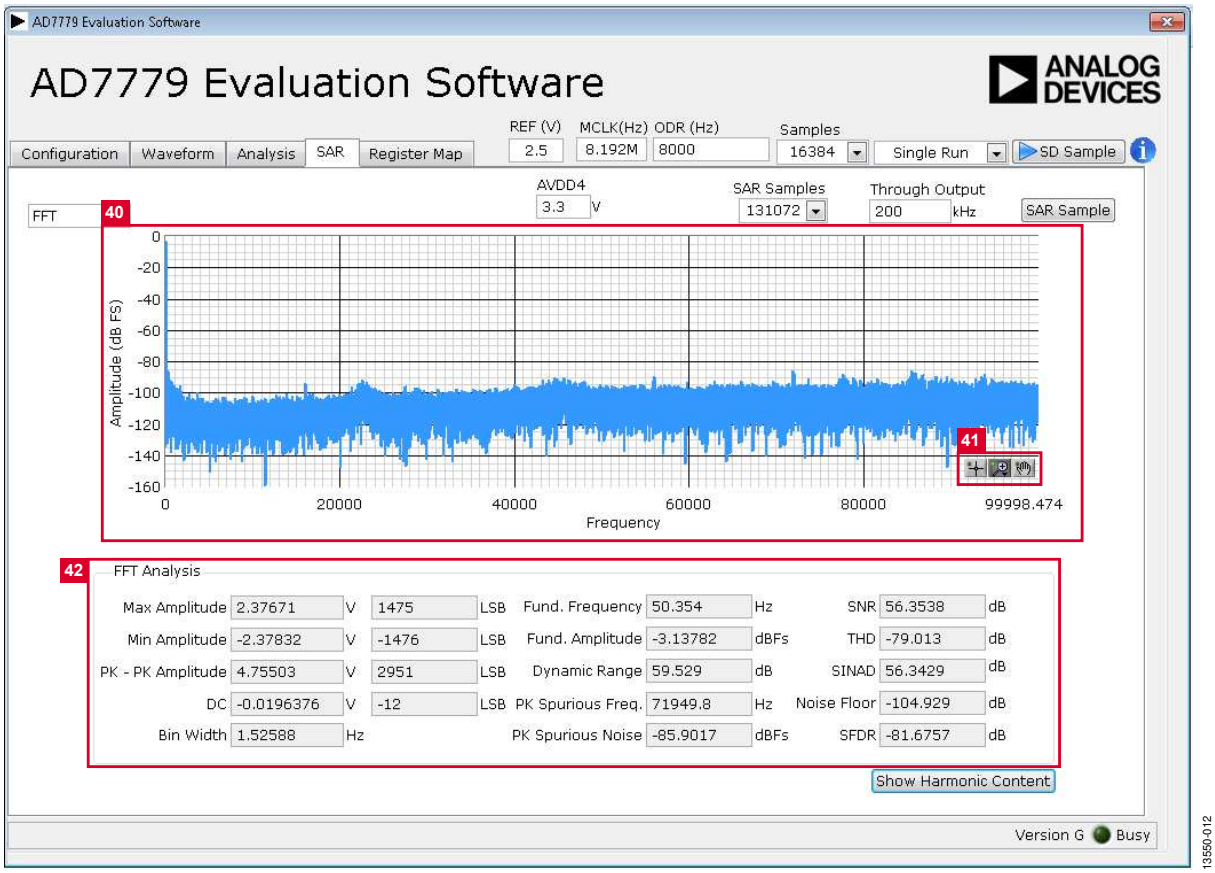


Figure 12. SAR FFT Tab of the AD7779 Evaluation Software

FFT Graph and Controls

The FFT graph (Label 40) shows the fast Fourier transform of the sampled signal. The frequency is displayed on the x-axis and the amplitude is graphed on the y-axis. Use the control tools (Label 41) to zoom in on the data. Harmonic content can be selected by clicking **Show Harmonic Content**.

Analysis Channel

The noise/waveform analysis section (Label 42) and FFT graph show the analysis of the channel selected via the **Analysis Ch** control.

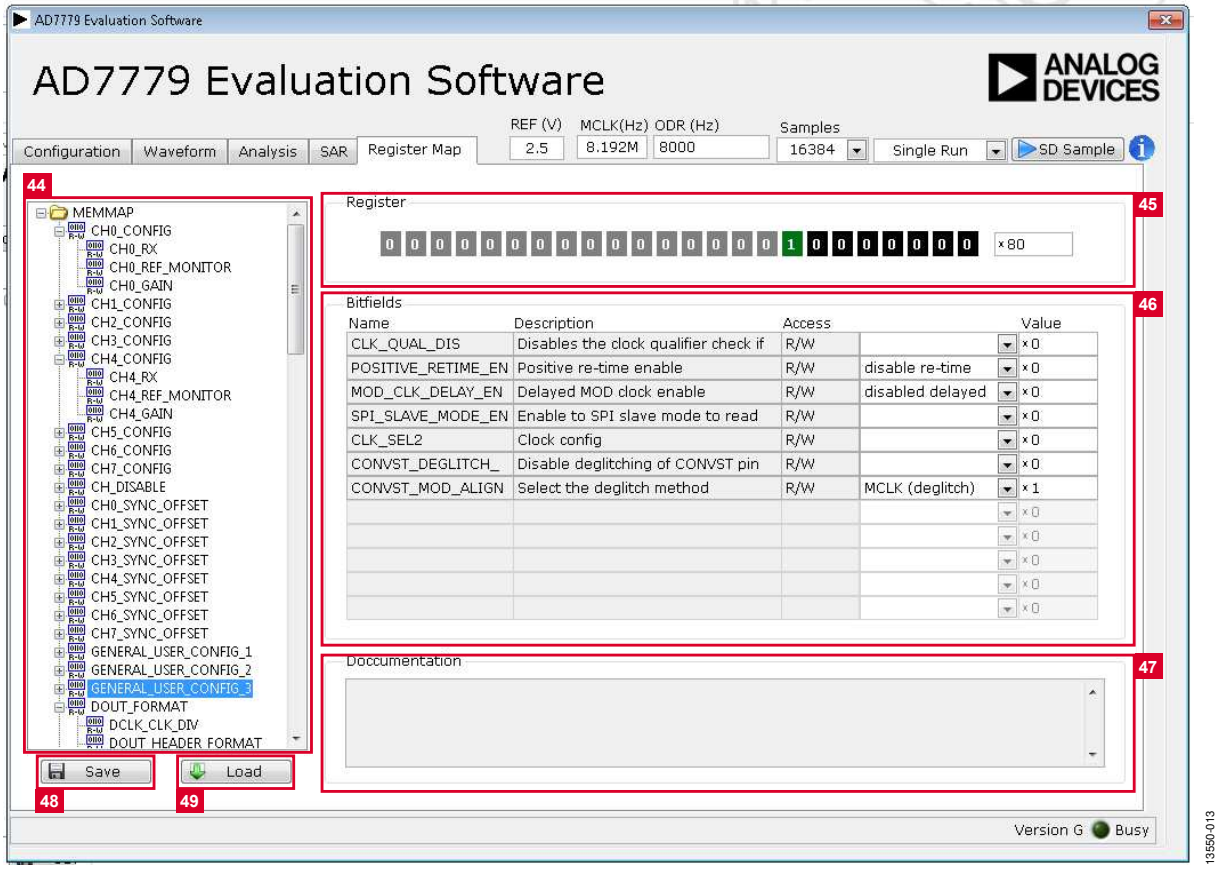


Figure 13. Register Map and Configuration

REGISTER MAP TAB

Register Tree

The register tree (Label 44) shows the full register map in a tree control. Each register is shown. Click the expand button next to each register to show all the bitfields contained within that register.

Register Control

The **Register** control (Label 45) allows the user to change the individual bits of the register selected in the register tree (Label 44). Click on each bit to toggle the value, or program the register value directly into the number control field on the right.

Bitfields List

The **Bitfields** list (Label 46) shows all the bitfields of the register selected in the register tree (Label 44). The values can be changed using the drop-down box or by entering a value directly into the number control on the right.

Documentation

The **Documentation** section (Label 47) contains the documentation for the register and bitfield selected in the register tree (Label 44).

Save and Load

The **Save** and **Load** buttons (Label 48 and Label 49) allow the user to save the current register map setting to a file and load the setting from the same file.

EXITING THE SOFTWARE

To exit the software, click the close button at the top, right corner of the main window.

EVALUATION BOARD SCHEMATICS AND LAYOUT

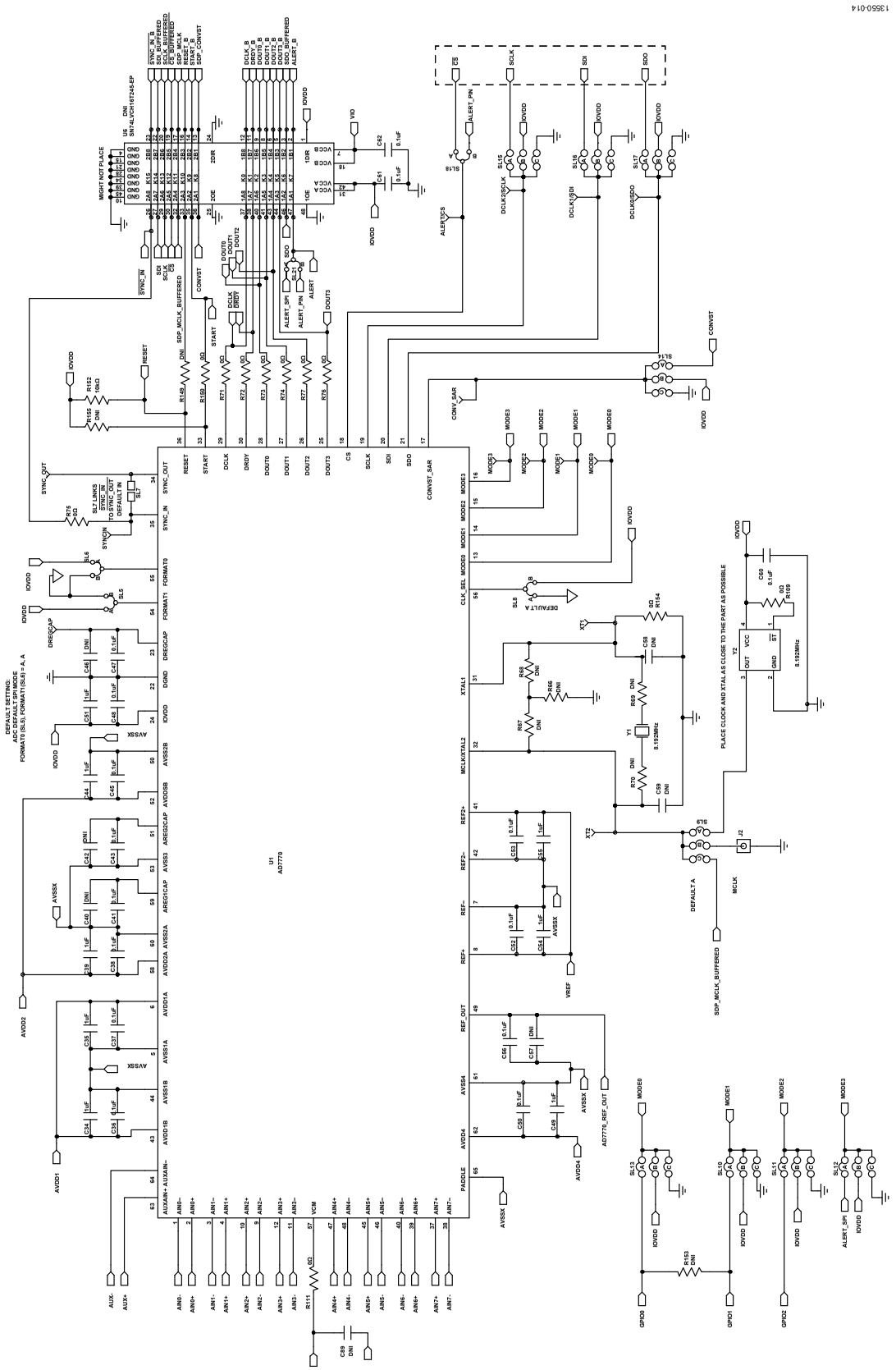


Figure 14. Evaluation Board Schematic—Page 1

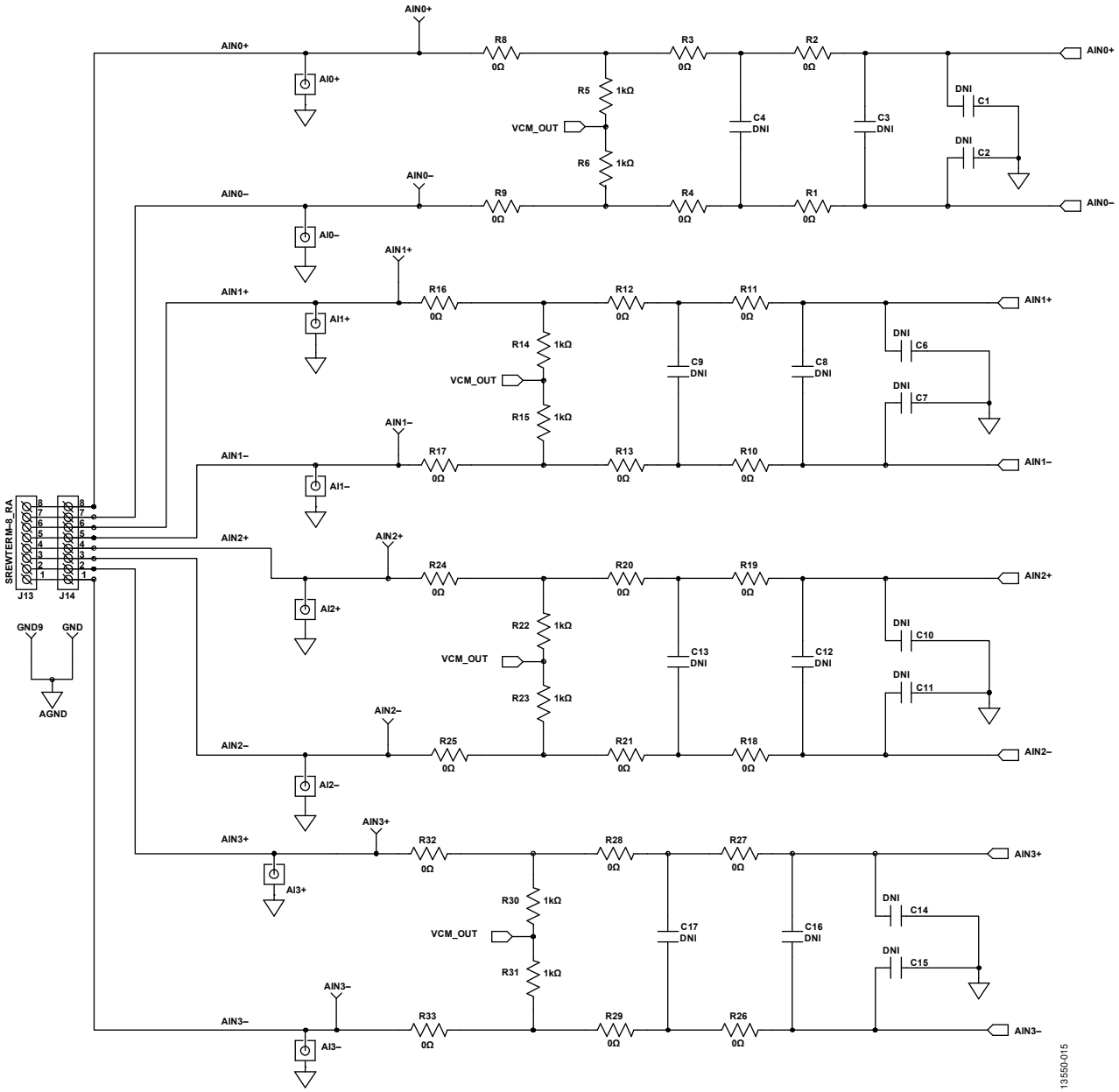
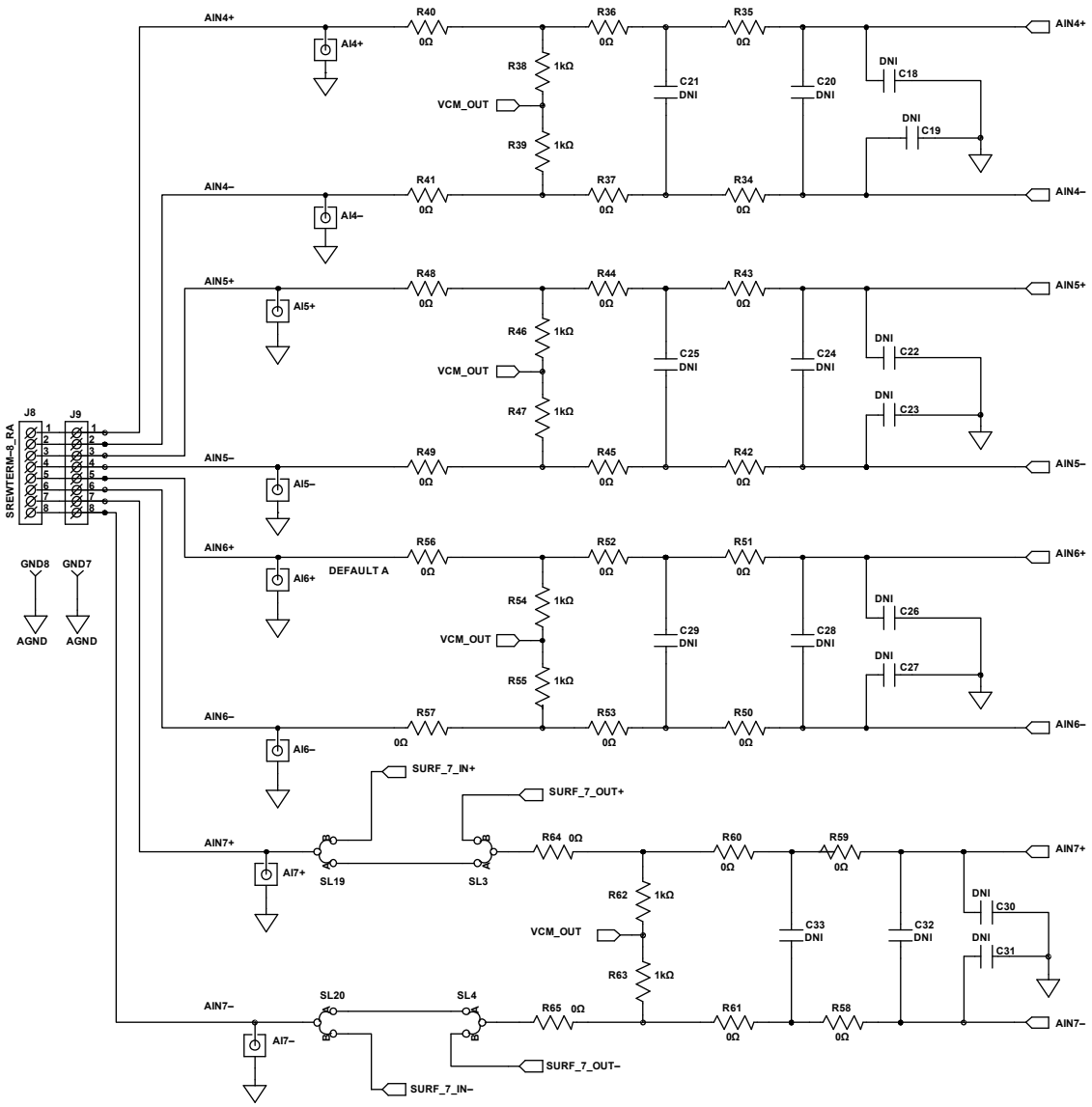


Figure 15. Evaluation Board Schematic—Page 2



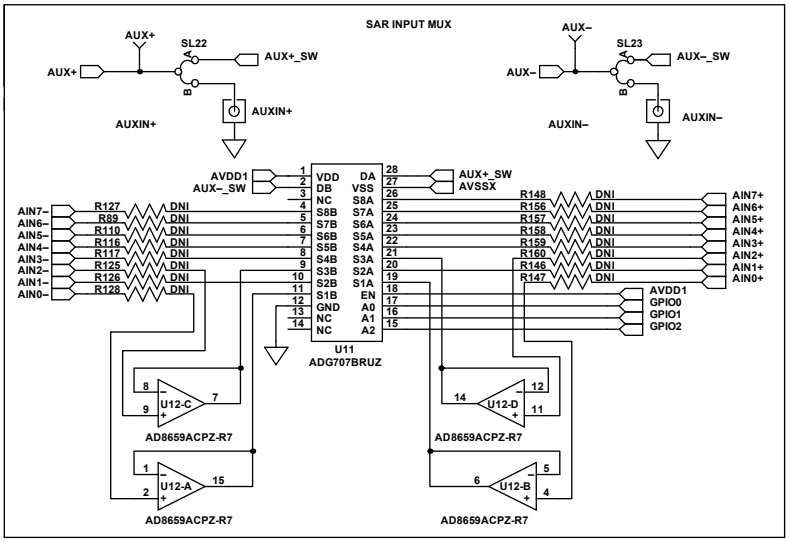


Figure 16. Evaluation Board Schematic—Page 3

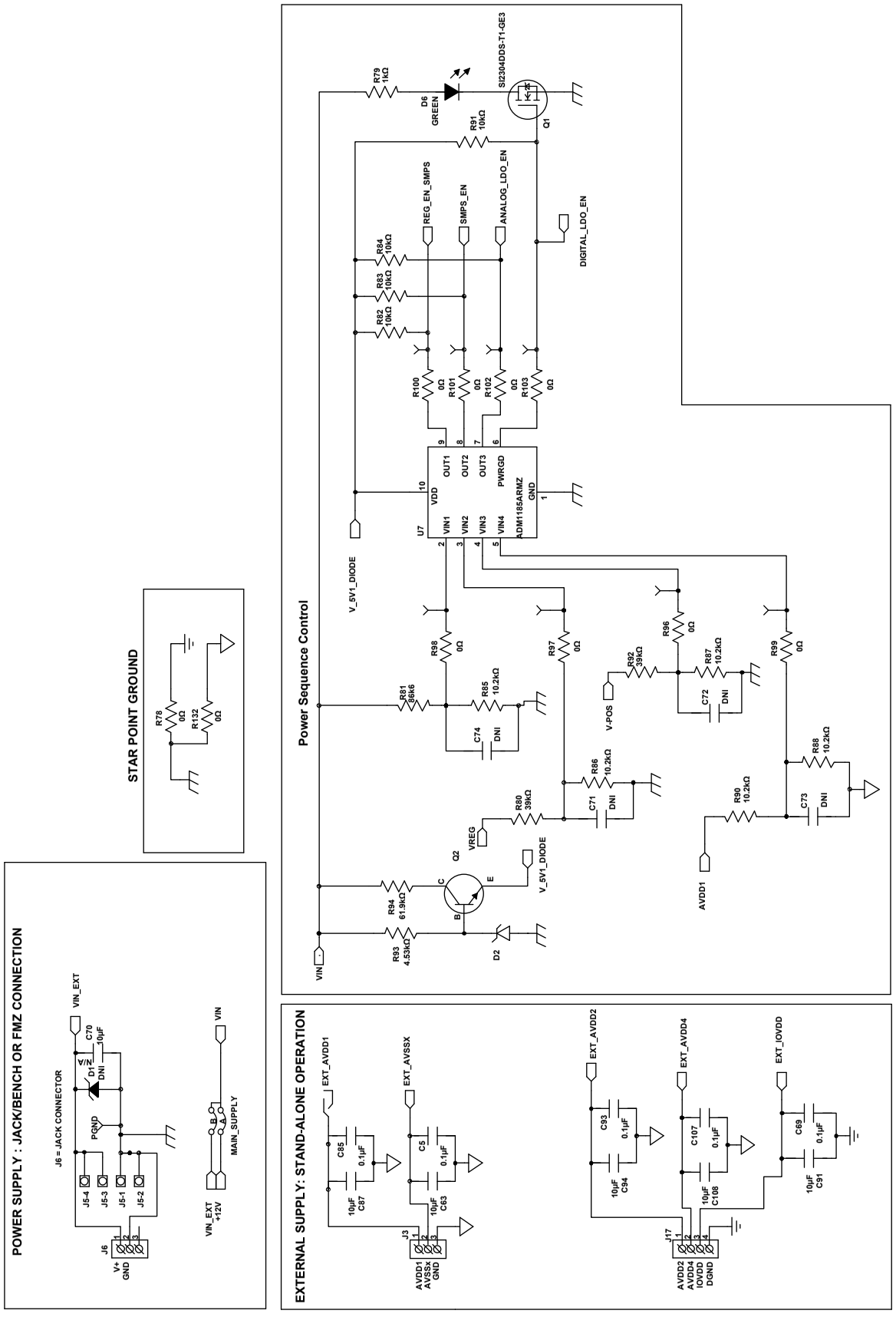


Figure 17. Evaluation Board Schematic—Page 4

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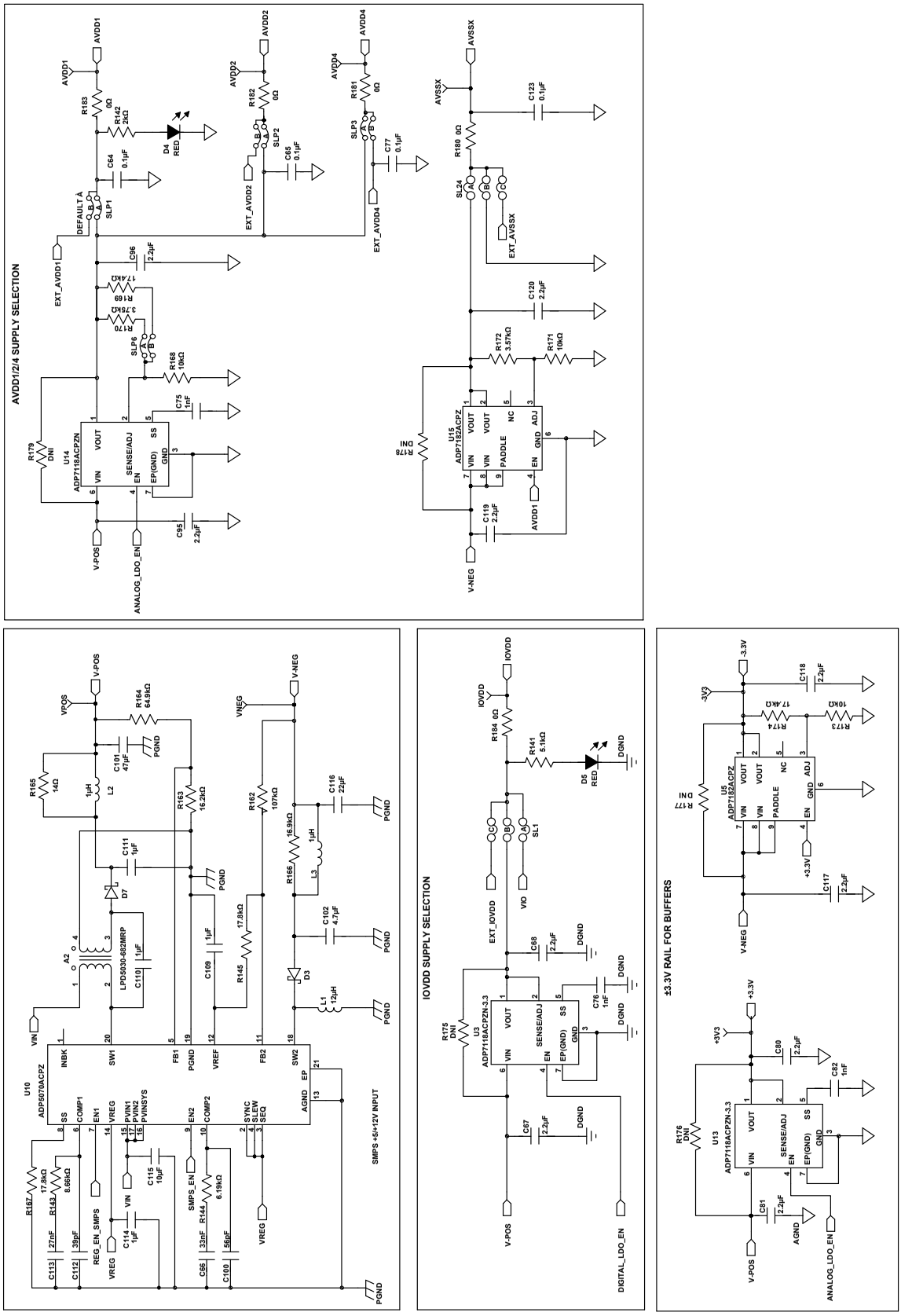

Figure 18. Evaluation Board Schematic—Page 5

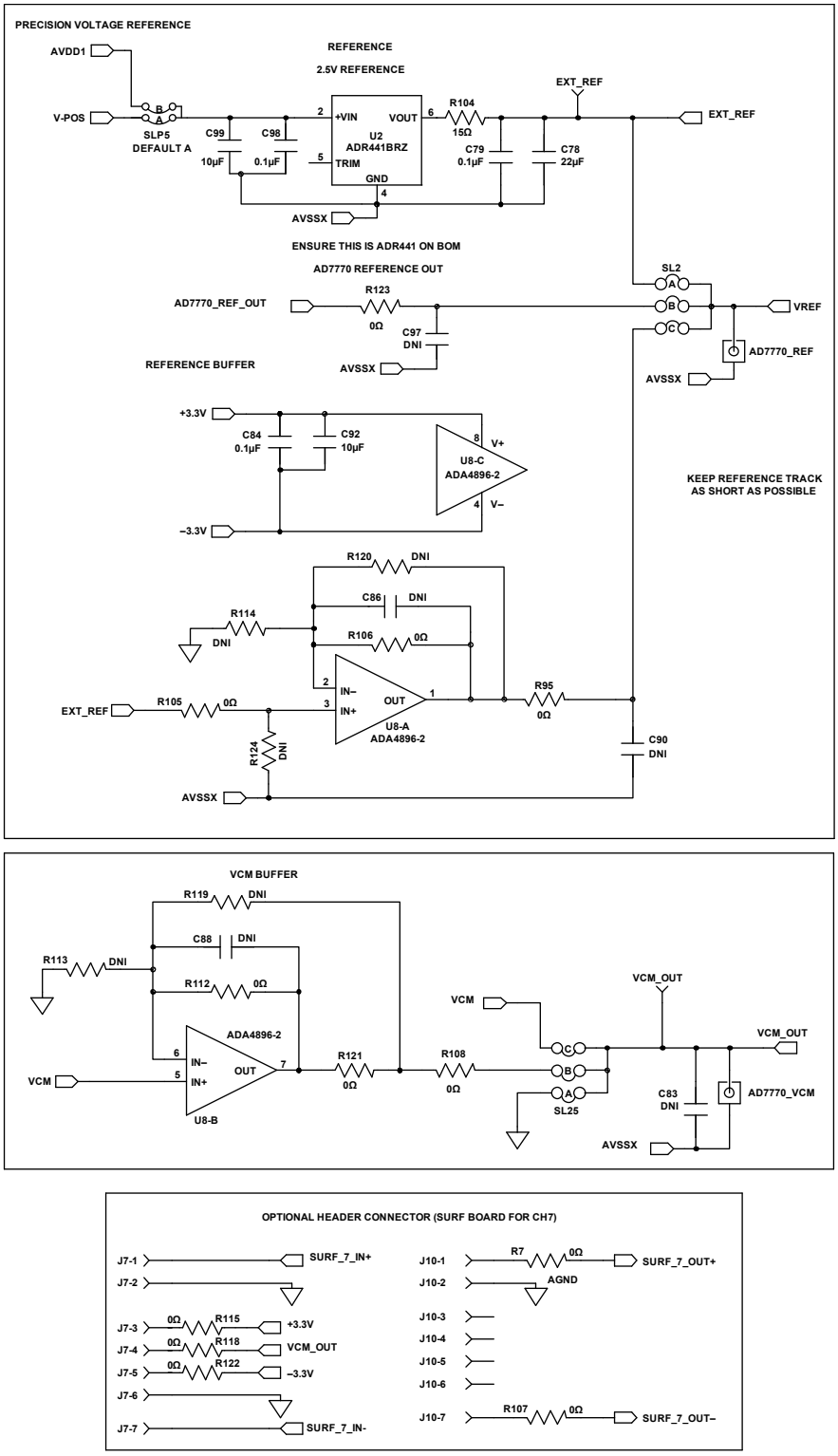

Figure 19. Evaluation Board Schematic—Page 6

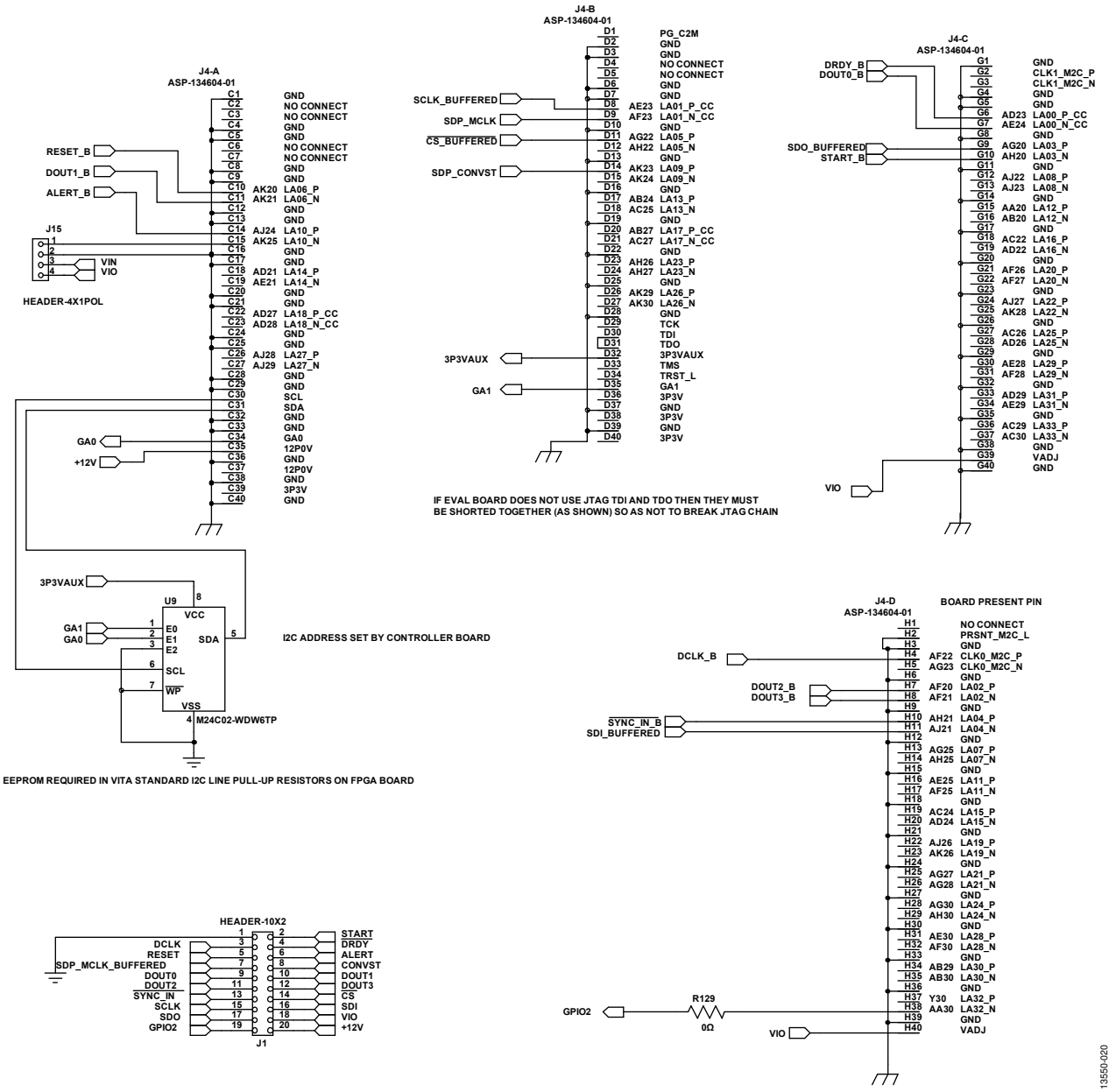

Figure 20. Evaluation Board Schematic—Page 7