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Evaluation Board for 12-/10-Bit, 8 Channel Parallel ADCs with a Sequencer

EVAL-AD7938CB/EVAL-AD7939CB/EVAL-AD7938-6CB

FEATURES

Full featured evaluation boards for the AD7938, AD7939, and AD7938-6 devices
Evaluation control board (EVAL-CONTROL-BRD2) compatible
Standalone capability
On-board analog buffering and voltage reference
On-board single-ended-to-differential conversion
Various linking options
PC software for control and data analysis when used with EVAL-CONTROL-BRD2

GENERAL DESCRIPTION

This data sheet describes the evaluation boards used to test the AD7938, AD7939, and AD7938-6 devices. These devices are 12- and 10-bit, high speed, low power successive approximation ADCs. These parts operate from a single 2.7 V to 5.25 V power supply and feature throughput rates of up to 1.5 MSPS.

The AD7938/AD7939 and AD7938-6 device data sheets should be used in conjunction with this data sheet.

On-board components for this evaluation board include:

- One AD780, which is a pin-programmable +2.5 V or +3 V ultra high precision band gap reference
- One AD713 quad op amp
- One AD8022 dual op amp
- Six AD8021 single op amps
- Two AD8138 differential amplifiers
- One P174FCT digital buffer

Various link options are provided in Table 1.

This evaluation board has a 96-way connector, which is compatible with the EVAL-CONTROL-BRD2, which is also available from Analog Devices, Inc. External sockets are provided for various signals, including the VREF input, analog inputs, and digital inputs and outputs. Note that the EVAL-CONTROL-BRD2 operates with all Analog Devices evaluation boards with part numbers ending in the letters CB.

FUNCTIONAL BLOCK DIAGRAM

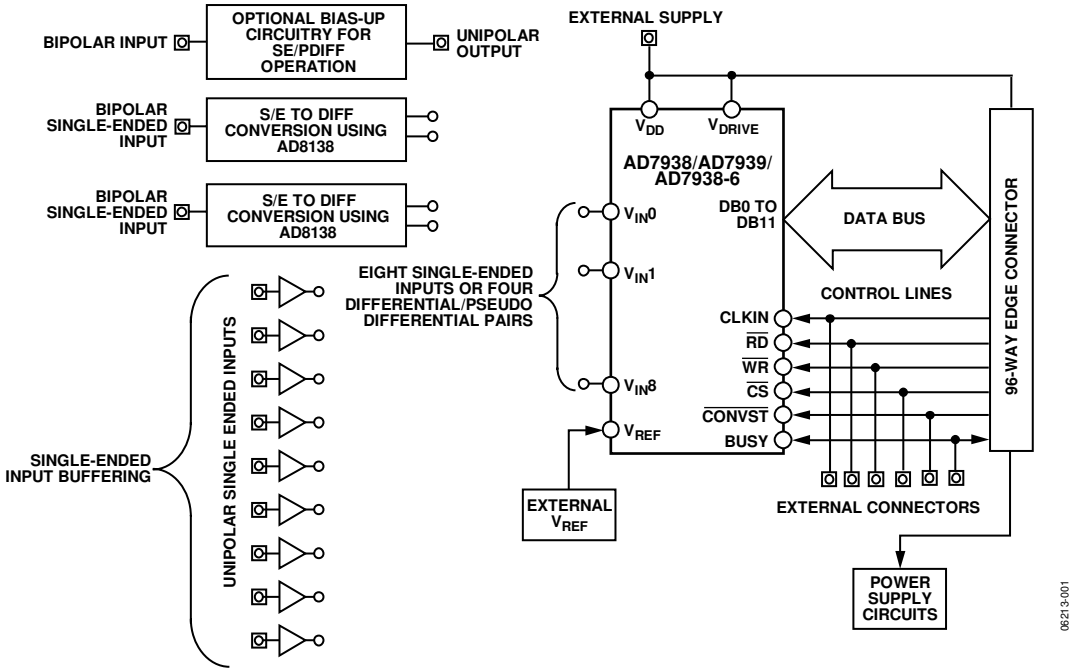

Figure 1.

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Tel: 781.329.4700 www.analog.com
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REVISION HISTORY

10/06—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

Before applying power and signals to the evaluation board, ensure that all links are properly set per the required operating mode.

The evaluation board has over 60 available link options. These options must be set for the required operating configuration. The functions of the options are outlined in Table 1.

Table 1. Link Option Functions

Link No.	Function
LK1	Selects the source of the V_{DD} +5 V supply used to supply the AD8138 differential amplifiers. In Position A, the V_{DD} is supplied from the EVAL-CONTROL-BRD2. In Position B, the V_{DD} must be supplied from an external source via the power connector J3.
LK2	This link option selects the source of the VSS −5 V supply used to supply the AD8138 differential amplifiers. In Position A, the V_{SS} is supplied from the EVAL-CONTROL-BRD2. In Position B, the V_{SS} must be supplied from an external source via the power connector J3.
LK3	This link option selects the source of the V_{DD} supply for the AD7938/AD7939/AD7938-6. In Position A, V_{DD} is supplied from the EVAL-CONTROL-BRD2. In Position B, V_{DD} must be supplied from an external source via J2.
LK4	This link option selects the source of the V_{DRIVE} supply for the digital interface. In Position A, V_{DRIVE} is tied to V_{DD}. In Position B, V_{DRIVE} is supplied via the EVAL-CONTROL-BRD2. In Position C, V_{DRIVE} must be supplied from an external source via J4.
LK5	This link selects the source of the $\overline{WR}$ input to the ADC. In Position A, $\overline{WR}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{WR}$ must be supplied from an external source via P16.
LK6	This link selects where the BUSY output from the ADC appears. In Position A, the BUSY output may be read by the EVAL-CONTROL-BRD2. In Position B, the BUSY may be read via the external socket, P15.
LK7	This link selects the source of the $\overline{CONVST}$ input to the ADC. In Position A, $\overline{CONVST}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{CONVST}$ must be supplied from an external source via P14.
LK8	This link selects the source of the $\overline{RD}$ input to the ADC. In Position A, $\overline{RD}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{RD}$ must be supplied from an external source via P13.
LK9	This link selects the source of the $\overline{CS}$ input to the ADC. In Position A, $\overline{CS}$ is supplied by the EVAL-CONTROL-BRD2. In Position B, $\overline{CS}$ must be supplied from an external source via P12.
LK10	This link selects the state of the W/$\overline{B}$ input. In Position A, W/$\overline{B}$ is tied low. In Position B, W/$\overline{B}$ is tied high.
LK11	This link selects the source of the CLKIN input to the ADC. In Position A, CLKIN is supplied by the EVAL-CONTROL-BRD2. In Position B, CLKIN must be supplied from an external source via P11.
LK12	If an external reference is being used, place this link in Position A. If an internal reference is being used, place this link in Position B.
LK13	This link selects the input to the $V_{IN}4$ pin on the ADC. In Position A, the input is coming from Pin $V_{IN}4$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK14	This link selects the input to $V_{IN}0$ pin on the ADC. In Position A, the input is coming from Pin $V_{IN}0$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.

Link No.	Function
LK15	This link selects the input to $V_{IN}1$ on the ADC. In Position A, the input is coming from $V_{IN}1$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK16	This link selects the input to $V_{IN}2$ on the ADC In Position A, the input is coming from $V_{IN}2$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK17	This link selects the analog input to be applied to the buffer, U8, which is used when operating in single-ended mode and when using $V_{IN}3$ to $V_{IN}7$. If the single-ended input applied to $V_{IN}3$ to $V_{IN}7$ is unipolar, this link should be in Position A, and the analog input should be applied at P10 with LK33 in Position B. If the single-ended input applied to $V_{IN}3$ to $V_{IN}7$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK18	This link option adds a 50 Ω termination to AGND at the $V_{IN}3$ to $V_{IN}7$ socket (P10) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK19	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}2$ to $V_{IN}6$ is a single-ended analog input, then LK19 should be in Position B as this input is applied to the op amp buffer. If the analog input applied to $V_{IN}2$ through $V_{IN}6$ is part of a differential pair with $V_{IN}3$ through $V_{IN}7$, then LK19 should be in Position A as this input is applied to the AD8138 differential amplifier (U7).
LK20	This link selects the analog input to be applied to the buffer, U6, which is used when operating in single-ended mode or pseudo differential mode and when using $V_{IN}2$ through $V_{IN}6$. If the single-ended input applied to $V_{IN}2$ through $V_{IN}6$ is unipolar, this link should be in Position A, and the analog input should be applied at P7 with LK19 in Position B. If the single-ended input applied to $V_{IN}2$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK21	This link selects the analog input to be applied to the buffer, U5, which is used when operating in single-ended mode and when using $V_{IN}1$ through $V_{IN}5$. If the single-ended input applied to $V_{IN}1$ through $V_{IN}5$ is unipolar, this link should be in Position A, and the analog input should be applied at P3 with LK34 in Position A. If the single-ended input applied to $V_{IN}1$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK22	This link option adds a 50 Ω termination to AGND at the $V_{IN}1$ through $V_{IN}5$ socket (P3) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK23	This link option adds a 50 Ω termination to AGND at the $V_{IN}2$ through $V_{IN}6$ socket (P7) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK24	This link selects the input to the input of the AD8138 differential amplifier (U4). If the user applies a fully differential signal to $V_{IN}0$ and $V_{IN}1$ or $V_{IN}4$ and $V_{IN}5$, and only requires buffering of this signal before its applied to the ADC, then LK24 should be in Position A. When applying a single-ended input to $V_{IN}0$ through $V_{IN}4$ requiring the use of the AD8138 to perform single-ended-to-differential conversion, this link should be in Position B. In this case, no input is applied to $V_{IN}1$ through $VI_{N}5$.
LK25	This link selects the input to the input of the AD8138 differential amplifier (U7). If the user applies a fully differential signal to $V_{IN}2$ and $V_{IN}3$ or $V_{IN}6$ and $V_{IN}7$, and only requires buffering of this signal before its applied to the ADC, then Link 16 should be in Position A. When applying a single-ended input to $V_{IN}2$ through $V_{IN}6$ requiring the use of the AD8138 to perform single-ended-to-differential conversion, this link should be in Position B. In this case, no input is applied to $V_{IN}3$.
LK26	This link option adds a 50 Ω termination to AGND at the $V_{IN}1$ through $V_{IN}5$ socket (P1) for the single-ended input. This link should be inserted if a 50 Ω termination is required on the analog input.
LK27	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}0$ through $V_{IN}4$ is a single-ended analog input then LK27 should be in Position A as this input is applied to the op amp buffer. If the analog input applied to $V_{IN}0$ through $V_{IN}4$ is part of a differential pair with $V_{IN}1$ through $V_{IN}5$, then LK27 should be in Position B as this input is applied to the AD8138 differential amplifier (U4).

Link No.	Function
LK28	This link selects the analog input to be applied to the buffer, U2, which is used when operating in single-ended mode or pseudo differential mode and when using $V_{IN}0$ through $V_{IN}4$. If the single-ended input applied to $V_{IN}0$ through $V_{IN}4$ is unipolar, this link should be in Position A, and the analog input should be applied at P1 with LK27 in Position A. If the single-ended input applied to $V_{IN}0$ is bipolar, this link should be in Position B and the analog input should be biased up using the bias circuit by applying it to P18.
LK29	This link option selects the source of the $V_{IN}0$ through $V_{IN}4$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}0$ through $V_{IN}4$. In Position B, $V_{IN}0$ through $V_{IN}4$ is supplied from the positive output of the AD8138 (U4) differential amplifier to provide half a differential pair with $V_{IN}1$ through $V_{IN}5$. In Position C, an external $V_{IN}0$ through $V_{IN}4$ is applied to the ADC via P4. In Position D, $V_{IN}0$ through $V_{IN}4$ is tied to AGND. Do this when $V_{IN}0$ through $V_{IN}4$ is not being used and when power supplies are first applied to the board.
LK30	This link option selects the source of the $V_{IN}1$ through $V_{IN}5$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}1$ through $V_{IN}5$. In Position B, $V_{IN}1$ through $V_{IN}5$ is supplied from the negative output of the AD8138 (U4) differential amplifier to provide half a differential pair with $V_{IN}0$ through $V_{IN}4$. In Position C, an external $V_{IN}1$ through $V_{IN}5$ is applied to the ADC via P5. In Position D, $V_{IN}1$ through $V_{IN}5$ is tied to AGND. Do this when $V_{IN}1$ through $V_{IN}5$ is not being used and when power supplies are first applied to the board.
LK31	This link option selects the source of the $V_{IN}2$ through $V_{IN}6$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}2$ through $V_{IN}6$. In Position B, $V_{IN}2$ through $V_{IN}6$ is supplied from the positive output of the AD8138 (U7) differential amplifier to provide half a differential pair with $V_{IN}3$ through $V_{IN}7$. In Position C, an external $V_{IN}2$ through $V_{IN}6$ is applied to the ADC via P6. In Position D, $V_{IN}2$ through $V_{IN}6$ is tied to AGND. Do this when $V_{IN}2$ through $V_{IN}6$ is not being used and when power supplies are first applied to the board.
LK32	This link option selects the source of the $V_{IN}3$ through $V_{IN}7$ analog input to be applied to the ADC. In Position A, a single-ended, buffered signal is applied to $V_{IN}3$ through $V_{IN}7$. In Position B, $V_{IN}3$ through $V_{IN}7$ is supplied from the negative output of the AD8138 (U7) differential amplifier to provide half a differential pair with $V_{IN}2$ through $V_{IN}6$. In Position C, an external $V_{IN}3$ through $V_{IN}7$ is applied to the ADC via P9. In Position D, $V_{IN}3$ through $V_{IN}7$ is tied to AGND. Do this when $V_{IN}3$ through $V_{IN}7$ is not being used and when power supplies are first applied to the board.
LK33	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}3$ through $V_{IN}7$ is part of a differential pair with $V_{IN}2$ through $V_{IN}6$, then LK33 should be in Position A as this input is applied to the AD8138 differential amplifier. If the analog input applied to $V_{IN}3$ through $V_{IN}7$ is a single-ended analog input then LK33 should be in Position B as this input is applied to the op amp buffer.
LK34	This link is used to choose between a single-ended analog input or a fully differential pair. If the analog input applied to $V_{IN}1$ through $V_{IN}5$ is a single-ended analog input then LK34 should be in Position A as this input is applied to the op amp buffer. If the analog input applied to $V_{IN}1$ through $V_{IN}5$ is part of a differential pair with $V_{IN}0$, then LK34 should be in Position B as this input is applied to the AD8138 differential amplifier.
LK35	This link selects the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U7). When in Position A, an external common-mode input must be applied via P8. When in Position B, VREF is applied to the V_{OCM} pin of the AD8138 (U7). When in Position C, VREF/2 is applied to the V_{OCM} pin of the AD8138 (U7).
LK36	This link selects the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4). When in Position A, an external common-mode input must be applied via P2. When in Position B, VREF is applied to the V_{OCM} pin of the AD8138 (U4). When in Position C, VREF/2 is applied to the V_{OCM} pin of the AD8138 (U4).

Link No.	Function
LK37	This link selects the input to $V_{IN}3$ pin on the ADC. In Position A, the input is coming from $V_{IN}3$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK38	This link selects whether the signal is applied to $V_{IN}0$ or $V_{IN}4$. In Position A, the signal is applied to $V_{IN}0$. In Position B, the signal is applied to $V_{IN}4$.
LK39	This link selects the input to $V_{IN}5$ on the ADC. In Position A, the input is coming from $V_{IN}5$, either in singled-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK40	This link selects the input to $V_{IN}6$ pin on the ADC. In Position A, the input is coming from $V_{IN}6$, either in single-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK41	This link selects the input to $V_{IN}7$ pin on the ADC. In Position A, the input is coming from $V_{IN}7$, either in single-ended mode or as one channel of a differential pair. In Position B, the input to the ADC is tied to ground.
LK42	This link selects whether the signal is applied to $V_{IN}1$ or $V_{IN}5$. In Position A, the signal is applied to $V_{IN}1$. In Position B, the signal is applied to $V_{IN}5$.
LK43	This link selects whether the signal is applied to $V_{IN}2$ or $V_{IN}6$. In Position A, the signal is applied to $V_{IN}2$. In Position B, the signal is applied to $V_{IN}6$.
LK44	This link selects whether the signal is applied to $V_{IN}3$ or $V_{IN}7$. In Position A, the signal is applied to $V_{IN}3$. In Position B, the signal is applied to $V_{IN}7$.
LK45	This link option adds a 50 Ω termination to AGND at the COM1 socket (P2) for the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4). This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4) with LK36 in Position A.
LK46	This link option adds a 50 Ω termination to AGND at the COM2 socket (P2) for the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4). This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4) with LK35 in Position A.
LK53	Always insert.
LK54	Always insert.
LK55	In Position A, REF is buffered to supply VREF to the common-mode voltage of the differential amplifier and to the bias up circuit. In Position B, REF is divided down by two, and then buffered to supply VREF/2 to the common-mode voltage of the AD8138 differential amplifier.
LK56	When VREF/2 is not used, insert LK56 to ensure that the inputs to U13-C are not floating.
LK57	This link chooses the source of an external reference input. In Position A, an external reference should be applied via P17. In Position B, the V_{OUT} of the AD780 reference chip is applied to the VREF circuit. In Position C, three-quarters of the AD780 V_{OUT} is applied to the VREF circuit. The resistors R35 and R52 can be changed if the user requires an alternative reference input.
LK58	This link determines whether the output of the AD780 reference chip is applied directly to LK57 or if it is divided down before being applied to LK57. In Position A, the output of the AD780 is applied to LK57. In Position B, the output of the AD780 is divided down before being applied to LK57.
LK59	This link option controls the program pin of the AD780 reference. When this pin is inserted, the AD780 output voltage is set to 3 V. When this pin is removed, the AD780 output voltage is set to 2.5 V.

Link No.	Function
LK60	This link option determines the source of the VCC (+5 V) digital supply. When inserted, VCC is supplied via the EVAL-CONTROL-BRD2. When removed, VCC must be supplied to the external connector, J5.
LK61	This link selects the dc voltage to be applied to the bias up circuit, which is used when a single-ended, bipolar signal needs to be converted to a unipolar signal. In Position A, VREF is applied to the bias up circuit. In Position B, the dc input to the bias up circuit is tied to AGND. Do this if the bias up circuit is not being used.
LK62	This link selects which portion of the VREF input is applied to the bias up circuit. The choice depends on the nature of the user's analog input signal. In Position A, one-fourth of the reference is applied to the bias up circuit In Position B, one-half of the reference is applied to the bias up circuit. If the bias up circuit is not used, then this link can be removed.
LK63	This link option adds a 50 Ω termination to AGND if a 50 Ω termination is required on the analog input.
LK64	This link option selects the source of the +12 V power supply. In Position A, the +12 V is supplied by the EVAL-CONTROL-BRD2. In Position B, the +12 V must be supplied from an external source via J6.
LK65	This link option selects the source of the −12 V power supply. In Position A, the −12 V is supplied via the EVAL-CONTROL-BRD2. In Position B, the −12 V must be supplied from an external source via J6.
LK66	When the reference output of the AD780 is not being divided down, this link should be inserted so that the input of U10 is not floating.

INITIAL SETUP CONDITIONS

This evaluation board can be operated in different modes. For example, the evaluation board can be operated with the EVAL-CONTROL-BRD2 or it can be used it as a standalone board. The board can either be setup to accept eight single-ended inputs, four differential inputs, four pseudo differential inputs, or seven pseudo differential inputs. The link settings for the different modes of operation are detailed in Table 2 through Table 6.

The AD7938/AD7939/AD7938-6 can accept four fully differential analog input pairs. These can either be applied as two pairs to P1, P3 and P7, P10 or single-ended-to-differential conversion can be performed on a single-ended input applied to P1 and P7.

DIFFERENTIAL MODE

The link positions described in Table 2 are required for operating the evaluation board in differential mode.

Table 2 outlines the default positions of all links when the board is shipped. All the links are set so that all power supplies and control signals are supplied by the EVAL-CONTROL-BRD2. Initially, all analog inputs are tied to ground to ensure that they are not floating on power up. Change these link positions depending upon which analog inputs are used.

Table 2. Differential Mode — Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	A	VDD for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK2	A	VSS for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK3	A	VDD for the AD7938/AD7939/AD7938-6 ADCs is supplied by the EVAL-CONTROL-BRD2.
LK4	B	VDRIVE is supplied by the EVAL-CONTROL-BRD2.
LK5	A	$\overline{WB}$ is supplied by the EVAL-CONTROL-BRD2.
LK6	A	BUSY is read by the EVAL-CONTROL-BRD2.
LK7	A	$\overline{CONVST}$ is supplied by the EVAL-CONTROL-BRD2.
LK8	A	$\overline{RD}$ is supplied by the EVAL-CONTROL-BRD2.
LK9	A	$\overline{CS}$ is supplied by the EVAL-CONTROL-BRD2.
LK10	B	ADC is set up to operate in word mode.
LK11	A	CLKIN is supplied by the EVAL-CONTROL-BRD2.
LK12	A	An external reference is supplied to the V_{OUT} pin from the AD780.
LK13	A	With LK13 in position A, a single-ended input or half a differential input is applied to $V_{IN}4$. If $V_{IN}4$ is not used, ground $V_{IN}4$ by installing LK13 in Position B.
LK14	A	With LK14 in position A, a single-ended input or half a differential input is applied to $V_{IN}0$. If $V_{IN}0$ is not used, ground $V_{IN}0$ by installing LK14 in Position B.
LK15	A	With LK15 in position A, a single-ended input or half a differential input is applied to $V_{IN}1$. If $V_{IN}1$ is not used, ground $V_{IN}1$ by installing LK15 in Position B.
LK16	A	With LK16 in position A, a single-ended input or half a differential input is applied to $V_{IN}2$. If $V_{IN}2$ is not used, ground $V_{IN}2$ by installing LK13 in Position B. LK16 should be in Position B if $V_{IN}2$ is not in use.
LK17	B	The input to U8 is tied to Vbiased, so it is not floating.
LK18	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P10, LK18 can be removed if a 50 Ω termination is not required.
LK19	A	If either a single-ended input or half a differential input is applied to $V_{IN}2$ through $V_{IN}6$ (P7).
LK20	B	The input to U6 is tied to Vbiased, so it is not floating.
LK21	B	The input to U5 is tied to Vbiased, so it is not floating.
LK22	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P3, LK22 can be removed if a 50 Ω termination is not required.
LK23	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P7, LK23 can be removed if a 50 Ω termination is not required.
LK24	B	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}0$ through $V_{IN}4$ (P1). This link should be placed in Position A if half a differential input is applied to P3.
LK25	B	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}2$ through $V_{IN}6$ (P7). This link should be placed in Position A if half a differential input is applied to P10.
LK26	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	B	If either a single-ended input or half a differential input is applied to $V_{IN}0$ through $V_{IN}4$ (P1).
LK28	B	The input to U3 is tied to Vbiased, so it is not floating.

Link No.	Position	Function
LK29	D	On power-up, the analog input applied to $V_{IN}0$ and/or $V_{IN}4$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ through $V_{IN}4$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK29 in Position B.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ and/or $V_{IN}5$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P3, $V_{IN}1$ through $V_{IN}5$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK30 in Position B.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ and/or $V_{IN}6$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ through $V_{IN}6$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK31 in Position B.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ and/or $V_{IN}7$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P10, $V_{IN}3$ through $V_{IN}7$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK32 in Position B.
LK33	Removed	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}2$ through $V_{IN}6$ (P7).This link should be placed in Position A if half a differential input is applied to P10.
LK34	Removed	If single-ended-to-differential conversion is being performed on a single-ended input applied to $V_{IN}0$ through $V_{IN}4$ (P1). This link should be placed in Position B if half a differential input is applied to P3.
LK35	B	VREF is applied to the V_{OCM} pin of the AD8138 differential amplifier to set up the common-mode voltage.
LK36	B	VREF is applied to the V_{OCM} pin of the AD8138 differential amplifier to set up the common-mode voltage.
LK37	A	With LK37 in position A, a single-ended input or half a differential input is applied to $V_{IN}3$. If $V_{IN}3$ is not used, ground $V_{IN}3$ by installing LK37 in Position B.
LK38	A and B	Both A and B are inserted in LK38 when applying half a differential input signal to $V_{IN}0$ and $V_{IN}4$.
LK39	A	With LK39 in position A, a single-ended input or half a differential input is applied to $V_{IN}5$. If $V_{IN}5$ is not used, ground $V_{IN}5$ by installing LK39 in Position B.
LK40	A	With LK40 in position A, a single-ended input or half a differential input is applied to $V_{IN}6$. If $V_{IN}6$ is not used, ground $V_{IN}6$ by installing LK40 in Position B.
LK41	A	With LK41 in position A, a single-ended input or half a differential input is applied to $V_{IN}7$. If $V_{IN}7$ is not used, ground $V_{IN}4$ by installing LK41 in Position B.
LK42	A and B	Both A and B are inserted in LK42 when applying half a differential input signal to $V_{IN}1$ and $V_{IN}5$.
LK43	A and B	Both A and B are inserted in LK43 when applying half a differential input signal to $V_{IN}2$ and $V_{IN}6$.
LK44	A and B	Both A and B are inserted in LK44 when applying half a differential input signal to $V_{IN}3$ and $V_{IN}7$.
LK45	Removed	This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4) with LK36 in Position A.
LK46	Removed	This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U7) with LK35 in Position A.
LK53	Inserted	Always insert.
LK54	Inserted	Always insert.
LK55	A and B	The inputs to U13-A-and-U13-B are not floating.
LK56	Inserted	The input to U13-C is not floating.
LK57	B	VREF is supplied by the V_{OUT} pin from the AD780.
LK58	A	The output of the AD780 supplies the reference to the ADC.
LK59	Removed	The output of the AD780 is 2.5 V.
LK60	Inserted	VCC is supplied by the EVAL-CONTROL-BRD2.
LK61	B	DC input to the bias up circuit is tied to AGND .as it is not used in this mode.
LK62	Removed	Bias up circuit not used in this mode.
LK63	Inserted	Analog input to the bias up circuit is tied to AGND as it is not used in this mode.
LK64	A	+12 V is supplied by the EVAL-CONTROL-BRD2.
LK65	A	−12 V is supplied by the EVAL-CONTROL-BRD2.
LK66	Inserted	The output of the AD780 is not divided down so the input to U10 is tied to AGND.

SINGLE-ENDED MODE

The AD7938/AD7939/AD7938-6 can operate with eight single-ended analog inputs. To operate the evaluation board in single-ended mode, change the link positions as shown in Table 3. Initially, all analog inputs are tied to ground to ensure that they are not floating on power up. Change the link positions depending on which analog inputs the links are using.

Table 3. Single-Ended Mode — Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	A	VDD for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK2	A	VSS for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK3	A	VDD for the AD7938/AD7939/AD7938-6 ADC is supplied by the EVAL-CONTROL-BRD2.
LK4	B	VDRIVE is supplied by the EVAL-CONTROL-BRD2.
LK5	A	$\overline{WR}$ is supplied by the EVAL-CONTROL-BRD2.
LK6	A	BUSY is read by the EVAL-CONTROL-BRD2.
LK7	A	$\overline{CONVST}$ is supplied by the EVAL-CONTROL-BRD2.
LK8	A	$\overline{RD}$ is supplied by the EVAL-CONTROL-BRD2.
LK9	A	$\overline{CS}$ is supplied by the EVAL-CONTROL-BRD2.
LK10	B	ADC is set up to operate in word mode.
LK11	A	CLKIN is supplied by the EVAL-CONTROL-BRD2.
LK12	A	An external reference is supplied to the V_{OUT} pin from the AD780.
LK13	A	With LK13 in position A, a single-ended input or half a differential input is applied to $V_{IN}4$. If $V_{IN}4$ is not used, ground $V_{IN}4$ by installing LK13 in Position B.
LK14	A	With LK14 in position A, a single-ended input or half a differential input is applied to $V_{IN}0$. If $V_{IN}0$ is not used, ground $V_{IN}0$ by installing LK14 in Position B.
LK15	A	With LK15 in position A, a single-ended input or half a differential input is applied to $V_{IN}1$. If $V_{IN}1$ is not used, ground $V_{IN}1$ by installing LK15 in Position B.
LK16	A	With LK16 in position A, a single-ended input or half a differential input is applied to $V_{IN}2$. If $V_{IN}2$ is not used, ground $V_{IN}2$ by installing LK16 in Position B.
LK17	A	A single-ended, unipolar input must be supplied to $V_{IN}3$ through $V_{IN}7$ (P10) and is buffered by U8.
LK18	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P10, LK18 can be removed if a 50 Ω termination is not required.
LK19	B	The analog input signal applied to P7 is applied to the single buffer (U6).
LK20	A	A single-ended, unipolar input must be supplied to $V_{IN}2$ through $V_{IN}6$ (P7) and is buffered by U6.
LK21	A	A single-ended, unipolar input must be supplied to $V_{IN}1$ through $V_{IN}5$ (P3) and is buffered by U5.
LK22	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P3, LK22 can be removed if a 50 Ω termination is not required.
LK23	Inserted	On power- up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P7, LK23 can be removed if a 50 Ω termination is not required.
LK24	B	The negative input to the AD8138 is tied to AGND.
LK25	B	The negative input to the AD8138 is tied to AGND.
LK26	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	A	The analog input signal applied to P1 is applied to the single buffer (U3).
LK28	A	A single-ended, unipolar input must be supplied to $V_{IN}0$ through $V_{IN}4$ (P1) and is buffered by U3.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ and/or $V_{IN}4$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ through $V_{IN}4$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK29 in Position A.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ and/or $V_{IN}5$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P3, $V_{IN}1$ through $V_{IN}5$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK30 in Position A.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ and/or $V_{IN}6$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ through $V_{IN}6$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK31 in Position A.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ and/or $V_{IN}7$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P10, $V_{IN}3$ through $V_{IN}7$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK32 in Position A.
LK33	B	The analog input signal applied to P10 is applied to a single buffer (U8).
LK34	A	The analog input signal applied to P3 is applied to the single buffer (U5).

Link No.	Position	Function
LK35	A	Since the AD8138 is not being used, tie the common-mode voltage to ground with LK46 inserted.
LK36	A	Since the AD8138 is not being used, tie the common-mode voltage to ground with LK45 inserted.
LK37	A	With LK37 in position A, a single-ended input or half a differential input is applied to $V_{IN}3$. If $V_{IN}3$ is not used, ground $V_{IN}3$ by installing LK37 in Position B.
LK38	A and B	Both A and B are inserted in LK38 when applying a single-ended input signal to $V_{IN}0$ and $V_{IN}4$.
LK39	A	With LK39 in position A, a single-ended input or half a differential input is applied to $V_{IN}5$. If $V_{IN}5$ is not used, ground $V_{IN}5$ by installing LK39 in Position B.
LK40	A	With LK40 in position A, a single-ended input or half a differential input is applied to $V_{IN}6$. If $V_{IN}6$ is not used, ground $V_{IN}6$ by installing LK40 in Position B.
LK41	A	With LK41 in position A, a single-ended input or half a differential input is applied to $V_{IN}7$. If $V_{IN}7$ is not used, ground $V_{IN}7$ by installing LK41 in Position B.
LK42	A and B	Both A and B are inserted in LK42 when applying a single-ended input signal to $V_{IN}1$ and $V_{IN}5$.
LK43	A and B	Both A and B are inserted in LK43 when applying a single-ended input signal to $V_{IN}2$ and $V_{IN}6$.
LK44	A and B	Both A and B are inserted in LK44 when applying a single-ended input signal to $V_{IN}3$ and $V_{IN}7$.
LK45	Inserted	This link should be inserted if a 50 Ω termination is required on the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4) with LK36 in Position A.
LK46	Inserted	This link should be inserted if a 50 Ω termination is required on the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U7) with LK35 in Position A.
LK53	Inserted	Always insert.
LK54	Inserted	Always insert.
LK55	A and B	The inputs to U13-A and U13-B are not floating.
LK56	Inserted	The input to U13-C is not floating.
LK57	B	VREF is supplied by the V_{OUT} pin from the AD780.
LK58	A	The output of the AD780 supplies the reference to the ADC.
LK59	Removed	The output of the AD780 is 2.5 V.
LK60	Inserted	VCC is supplied by the EVAL-CONTROL-BRD2.
LK61	B	DC input to the bias up circuit is tied to AGND as it is not used in this mode.
LK62	Removed	Bias up circuit not used in this mode.
LK63	Inserted	Analog input to the bias up circuit is tied to AGND as it is not used in this mode.
LK64	A	+12 V is supplied by the EVAL-CONTROL-BRD2.
LK65	A	−12 V is supplied by the EVAL-CONTROL-BRD2.
LK66	Inserted	The output of the AD780 is not divided down so the input to U10 is tied to AGND.

PSEUDO DIFFERENTIAL MODE

The AD7938/AD7939/AD7938-6 can accept four pseudo differential analog input pairs. To operate the evaluation board in pseudo differential mode, change the link positions as shown in Table 4. All other links are per Table 2.

Table 4. Pseudo Differential Mode — Powered and Controlled by the EVAL-CONTROL-BRD2

Link No.	Position	Function
LK1	Removed	No power supply is connected to +V of the AD8138 differential amplifiers as they are not used in pseudo differential mode.
LK2	Removed	No power supply is connected to –V of the AD8138 differential amplifiers as they are not used in pseudo differential mode.
LK17	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}3$ through $V_{IN}7$.
LK19	B	The ac portion of the pseudo differential input applied to P7 is connected to the buffer U6 before being applied to $V_{IN}2$ through $V_{IN}6$ of the ADC.
LK20	A	The ac portion of the pseudo differential input applied to P7 is connected to the buffer U6 before being applied to $V_{IN}2$ through $V_{IN}6$ of the ADC.
LK21	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}1$ through $V_{IN}5$.
LK27	A	The ac portion of the pseudo differential input applied to P1 is connected to the buffer U3 before being applied to $V_{IN}0$ through $V_{IN}4$ of the ADC.
LK28	A	The ac portion of the pseudo differential input applied to P1 is connected to the buffer U3 before being applied to $V_{IN}0$ through $V_{N}4$ of the ADC.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ and/or $V_{IN}4$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ through $V_{IN}4$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK29 in Position A.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ and/or $V_{IN}5$ of the ADC is tied to AGND so that it is not floating. Following power-up, keep these inputs tied to AGND. Another option is to apply an external dc voltage either directly to P5 or to P3 and buffer it before it is applied to $V_{IN}1$ through $V_{IN}5$ in Position B or Position C.
LK31	D	On power-up, the analog input applied to $V_{IN}2$ and/or $V_{IN}6$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, connect $V_{IN}2$ through $V_{IN}6$ of the ADCs to the positive output of the AD8138 amplifier by placing LK31 in Position A.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ and/or $V_{IN}7$ of the ADC is tied to AGND so that it is not floating. Following power-up, either keep tied to AGND, or apply an external dc voltage either directly to P9 or to P10 and buffer it before it is applied to $V_{IN}3$ through $V_{IN}7$ in Position B or Position C.
LK33	B	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}3$ through $V_{IN}7$.
LK34	A	If the dc portion of the pseudo differential input is to be buffered before being applied to $V_{IN}1$ through $V_{IN}5$.
LK35	A	The AD8138 is not being used so the common-mode voltage needs to be tied to ground with LK46 inserted.
LK36	B	The AD8138 is not being used so the common-mode voltage needs to be tied to ground with LK45 inserted.
LK45	Inserted	This link should be inserted if a 50 Ω termination is required on the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U4) with LK36 in Position A.
LK46	Inserted	This link should be inserted if a 50 Ω termination is required on the input to the V_{OCM} pin (common-mode input) of the AD8138 differential amplifier (U7) with LK35 in Position A.

USING THE BIAS UP CIRCUIT

The bias up circuit can be used to bias up single-ended, bipolar signals to an appropriate dc voltage to make them unipolar to comply with the input requirements of the ADC. See Table 5 below for links changes. All other links remain as shown in Table 3.

Table 5. Using the Bias Up Circuit in Single-ended or Pseudo Differential Mode

Link No.	Position	Function
LK17	B	While operating in single-ended mode, when applying a bipolar input signal to the bias up circuit, it is applied to the buffer U8 via LK17.
LK20	B	While operating in single-ended mode, when applying a bipolar input signal to the bias up circuit, it is applied to the buffer U8 via LK20.
LK21	B	While operating in single-ended mode, when applying a bipolar input signal to the bias up circuit, it is applied to the buffer U8 via LK21.
LK28	B	While operating in single-ended mode, when applying a bipolar input signal to the bias up circuit, it is applied to the buffer U8 via LK28.
LK61	A	VREF is applied to the bias up circuit to setup the dc bias voltage.
LK62	A or B	Depending on what bias voltage is required.
LK63	Removed	Bias up circuit is used.

STANDALONE MODE

The evaluation board can be operated as a standalone evaluation board. It is necessary to supply all power supplies and control signals. The link options listed in Table 6 are for standalone operation with single-ended unipolar inputs. Change the links appropriately for differential or pseudo differential inputs and if the bias up circuit is to be used. Any unused ADC analog input should be tied to AGND. To write to or read from the ADC data bus in standalone mode, use the 96-way connector, the pinout of which is shown in Table 7.

Table 6. Standalone Mode with Single-Ended, Unipolar Inputs

Link No.	Position	Function
LK1	A	VDD for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK2	A	VSS for the AD8138 amplifiers is supplied by the EVAL-CONTROL-BRD2.
LK3	B	An external supply is required to power the ADC via J2 (VDD_EXT.)
LK4	A or B	VDRIVE is taken from VDD or an external VDRIVE should be applied via J3 (VDRIVE).
LK5	B	The $\overline{WR}$ control input should be applied via P16.
LK6	B	The BUSY output should be read via P15.
LK7	B	The $\overline{CONVST}$ control input should be applied via P14.
LK8	B	The $\overline{RD}$ control input should be applied via P13.
LK9	B	The $\overline{CS}$ control input should be applied via P12.
LK10	B	ADC is set up to operate in WORD mode.
LK11	B	The CLKIN should be applied via P11.
LK12	A	VREF is supplied by the AD780 reference chip.
LK13	A	With LK13 in position A, a single-ended input or half a differential input is applied to $V_{IN}4$. If $V_{IN}4$ is not used, ground $V_{IN}4$ by installing LK13 in Position B.
LK14	A	With LK14 in position A, a single-ended input or half a differential input is applied to $V_{IN}0$. If $V_{IN}0$ is not used, ground $V_{IN}0$ by installing LK14 in Position B.
LK15	A	With LK15 in position A, a single-ended input or half a differential input is applied to $V_{IN}1$. If $V_{IN}1$ is not used, ground $V_{IN}1$ by installing LK15 in Position B.
LK16	A	With LK16 in position A, a single-ended input or half a differential input is applied to $V_{IN}2$. If $V_{IN}2$ is not used, ground $V_{IN}2$ by installing LK16 in Position B.
LK17	A	A single-ended unipolar input is applied to the U8 buffer.
LK18	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P10, LK18 can be removed if a 50 Ω termination is not required.
LK19	B	The single-ended, unipolar, analog input applied to P7 is connected to the U6 buffer.
LK20	A	A single-ended, unipolar input is applied to the U6 buffer.
LK21	A	A single-ended, unipolar input is applied to the U5 buffer.
LK22	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P3, LK22 can be removed if a 50 Ω termination is not required.
LK23	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P7, LK23 can be removed if a 50 Ω termination is not required.
LK24	B	The negative input to the AD8138 is tied to AGND as it is not used.
LK25	B	The negative input to the AD8138 is tied to AGND as it is not used.
LK26	Inserted	On power-up, the inputs to the op amps are tied to ground so they are not floating. Once a signal is applied to P1, LK26 can be removed if a 50 Ω termination is not required.
LK27	A	The single-ended, unipolar, analog input applied to P1 is connected to the U3 buffer.
LK28	A	A single-ended, unipolar input is applied to the U3 buffer.
LK29	D	On power-up, the analog input applied to $V_{IN}0$ and/or $V_{IN}4$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P1, $V_{IN}0$ through $V_{IN}4$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK29 in Position A. Alternatively, the user can apply an analog input signal directly to P4, in this case LK29 should be in Position C.
LK30	D	On power-up, the analog input applied to $V_{IN}1$ and/or $V_{IN}5$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P3, $V_{IN}1$ through $V_{IN}5$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK30 in Position A. Alternatively, the user can apply an analog input signal directly to P5, in this case LK30 should be in Position C.

Link No.	Position	Function
LK31	D	On power-up, the analog input applied to $V_{IN}2$ and/or $V_{IN}6$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P7, $V_{IN}2$ through $V_{IN}6$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK31 in Position A. Alternatively, the user can apply an analog input signal directly to P6, in this case LK31 should be in Position C.
LK32	D	On power-up, the analog input applied to $V_{IN}3$ and/or $V_{IN}7$ of the ADC is tied to AGND so that it is not floating. Once an analog input signal is applied to P10, $V_{IN}3$ through $V_{IN}7$ of the ADC should be connected to the positive output of the AD8138 amplifier by placing LK32 in Position A. Alternatively, the user can apply an analog input signal directly to P9, in this case LK32 should be in Position C.
LK33	B	The single-ended, unipolar, analog input applied to P10 is connected to the buffer (U8).
LK34	A	The analog input signal applied to P3 is applied to the single buffer (U5).
LK35	A	The AD8138 is not being used so the common-mode voltage needs to be tied to ground, with LK46 inserted.
LK36	B	The AD8138 is not being used so the common-mode voltage needs to be tied to ground, with LK45 inserted.
LK37	A	With LK37 in position A, a single-ended input or half a differential input is applied to $V_{IN}3$. If $V_{IN}3$ is not used, ground $V_{IN}3$ by installing LK37 in Position B.
LK38	A and B	Both A and B are inserted in LK38 when applying a single-ended input signal to $V_{IN}0$ and $V_{IN}4$.
LK39	A	With LK39 in position A, a single-ended input or half a differential input is applied to $V_{IN}5$. If $V_{IN}5$ is not used, ground $V_{IN}5$ by installing LK39 in Position B.
LK40	A	With LK40 in position A, a single-ended input or half a differential input is applied to $V_{IN}6$. If $V_{IN}6$ is not used, ground $V_{IN}6$ by installing LK40 in Position B.
LK41	A	With LK41 in position A, a single-ended input or half a differential input is applied to $V_{IN}7$. If $V_{IN}7$ is not used, ground $V_{IN}7$ by installing LK41 in Position B.
LK42	A and B	Both A and B are inserted in LK42 when applying a single-ended input signal to $V_{IN}1$ and $V_{IN}5$
LK43	A and B	Both A and B are inserted in LK43 when applying a single-ended input signal to $V_{IN}2$ and $V_{IN}6$
LK44	A and B	Both A and B are inserted in LK44 when applying a single-ended input signal to $V_{IN}3$ and $V_{IN}7$
LK45	Inserted	This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} (common-mode input) of the AD8138 differential amplifier (U4) with LK36 in Position A.
LK46	Inserted	This link should be inserted if a 50 Ω termination is required on the input to V_{OCM} (common-mode input) of the AD8138 differential amplifier (U7) with LK35 in Position A.
LK53	Inserted	Always insert.
LK54	Inserted	Always insert.
LK55	A and B	Bias up circuit is not used.
LK56	Inserted	The inputs to U13-C are not floating.
LK57	A or B	The user should apply an external reference via P17 or the reference is supplied by the AD780.
LK58		See Table 1.
LK59		See Table 1.
LK60	Remove	An external 5 V supply for VCC should be applied via J5.
LK61		See Table 1.
LK62		See Table 1.
LK63		See Table 1.
LK64	B	An external +12 V supply should be applied via J6 to supply the op amps and the voltage reference.
LK65	B	An external −12 V supply should be applied via J6 to supply the op amps and the voltage reference

INTERFACING THE EVALUATION BOARDS

Interfacing the EVAL-CONTROL-BRD2 to the evaluation board is accomplished via a 96-way connector, J1.Plug the 96-way connector on the evaluation board directly into the 96-way connector on the EVAL-CONTROL-BRD2.

The 96-way connector is powered from a 12 V ac transformer. Suitable transformers are available from Analog Devices as an accessory under the following part numbers.

- EVAL-110VAC-US (for use in the U.S. or Japan)
- EVAL-220VAC-UK (for use in the U.K.)
- EVAL-220VAC-EU (For use in Europe)

These transformers are also available from Digikey (U.S.) and Campbell Collins (U.K.).

Connection between the EVAL-CONTROL-BRD2 and the serial port of a PC is via a standard Centronics printer port cable, which is provided as part of the EVAL-CONTROL-BRD2 kit.

When interfacing the EVAL-AD7938CB/EVAL-AD7939CB/EVAL-AD7938-6CB evaluation boards directly to the EVAL-CONTROL-BRD2, all supplies and control signals are provided with the EVAL-CONTROL-BRD2.

Due to the nature of the DSP interface on the EVAL-CONTROL-BRD2, sampling rates greater than 800 kSPS are not supported when interfacing this evaluation board directly to EVAL-CONTROL-BRD2.

Figure 2 shows the pinout for the 96-way connector. Table 7 and Table 8 list the pin designations and descriptions.

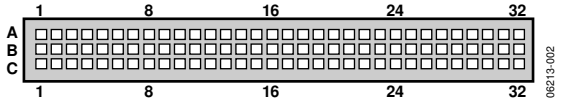

Figure 2. Pin Configuration for the 96-Way Connector J1

Table 7. Pin Designations (unused pins omitted for clarity)

Pin	Row A	Row B	Row C
1			
2		D0	
3		D1	
4	DGND	DGND	DGND
5		D2	
6		D3	
7	SCLK0	D4	SCLK0
8	+5 V	+5 V	+5 V
9	$\overline{RD}$	D5	$\overline{WR}$
10		D6	$\overline{CS}$
11		D7	
12	DGND	DGND	DGND
13		D8	
14		D9	
15		D10	
16	DGND	DGND	DGND
17	FL0	D11	$\overline{IRQ2}$
18			
19			
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30	−12 V	AGND	+12 V
31	AVSS	AVSS	AVSS
32	AVDD	AVDD	AVDD

Table 8. Pin Descriptions

Pin	Description
D0 to D11	Data Bit 0 to Data Bit 11. Three state TTL I/O pins used to read conversion data and to write data to the internal registers of the ADC. D11 is the MSB and D0 the LSB for the AD7938 and D2 the LSB for the AD7939.
SCLK0	Serial Clock. This continuous clock is connected to the CLKIN pin of the ADCs via LK11.
+5 VD	Digital +5 V Supply. This is used to provide a digital supply to the board for the digital logic.
$\overline{RD}$	Read. This is an active low logic input connected to the $\overline{RD}$ pin of the ADCs via LK8.
$\overline{WR}$	Write. This is an active low logic input connected to the $\overline{WR}$ pin of the ADCs via LK5.
$\overline{CS}$	Chip Select. This is an active low logic input connected to the $\overline{CS}$ pin of the ADCs via LK9.
FL0	Flag Zero. This logic input is connected to the $\overline{CONVST}$ input of the ADCs via LK7.
$\overline{IRQ2}$	Interrupt Request 2. This is a logic output and is connected to the BUSY output of the ADCs.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board. This allows the user to provide a digital power supply via the connector along with other digital signals.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
AVDD	Analog +5 V Supply. These lines are connected to the AVDD supply line on the evaluation board via LK1 to provide +5 V to the AD8138 differential amplifiers. They are also connected to the VDD supply of the ADCs via LK3.
AVSS	Analog −5 V Supply. These lines are connected to the AVSS supply line on the evaluation board via LK2 to supply −5 V to the AD8138 differential amplifiers.
±12 V	±12 V Supply. These lines are connected to the ±12 V supply lines on the evaluation board via LK64 and LK65 to supply the AD713, the AD8021, AD8022, and the AD780.

TEST POINTS

There are 13 test points on the inputs to the ADCs on the evaluation board. These test points enable easy access to the signals for probing, evaluation, and debugging.

CONNECTORS

There are six connectors on the EVAL-AD7938CB/EVAL-AD7939CB/EVAL-AD7938-6CB evaluation board as outlined in Table 9.

Table 9. Connector Functions

Connector	Function
J1	96-way connector for the digital interface and power supply connections.
J2	External VDD power connector for the ADC.
J3	External AVDD, AVSS, and AGND power connector.
J4	External VDRIVE power connector.
J5	External digital +5 V power connector.
J6	External +12 V, −12 V, and AGND power connector.

SOCKETS

There are 18 SMB input sockets relevant to the operation of the ADCs on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CONTROL-BRD2, the only necessary external sockets are used to supply the analog inputs to the ADC (that is, P1, P3, P7, and P10). All of the other sockets are optional. If not used, their signals are supplied by the EVAL-CONTROL-BRD2. Most of these sockets are used when operating the board as a standalone unit, as all the signals required are supplied from external sources. The functions of these sockets are outlined in Table 10.

Table 10. Socket Functions

Socket	Function
P1	$V_{IN}0$ through $V_{IN}4$. Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}0$ through $V_{IN}4$ input of the ADC in single-ended mode; or for a bipolar single-ended analog input to be applied to the AD8138 for single-ended-to-differential conversion in differential mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P2	COM1. Subminiature BNC socket for the dc analog input to V_{OCM} on the AD8138 differential amplifier.
P3	$V_{IN}1$ through $V_{IN}5$. Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}1$ through $V_{IN}5$ input of the ADC in single-ended mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P4	Ext_$V_{IN}0$ through $V_{IN}4$. Subminiature BNC socket for a signal to be applied directly to $V_{IN}0$ through $V_{IN}4$ input of the ADC.
P5	Ext_ $V_{IN}1$ through $V_{IN}5$. Subminiature BNC socket for a signal to be applied directly to $V_{IN}1$ through $V_{IN}5$ input of the ADC.
P6	Ext_$V_{IN}2$ through $V_{IN}6$. Subminiature BNC socket for a signal to be applied directly to $V_{IN}2$ through $V_{IN}6$ input of the ADC.
P7	$V_{IN}2$ through V $V_{IN}5$. Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}2$ through $V_{IN}5$ input of the ADC in single-ended mode; or for a bipolar single-ended analog input to be applied to the AD8138 for single-ended-to-differential conversion in differential mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P8	COM2. Subminiature BNC socket for the dc analog input to V_{OCM} on the AD8138 differential amplifier.
P9	Ext_$V_{IN}3$ through $V_{IN}7$. Subminiature BNC socket for a signal to be applied directly to $V_{IN}3$ through $V_{IN}7$ input of the ADC.
P10	$V_{IN}3$ through $V_{IN}7$. Subminiature BNC socket for either a single-ended unipolar analog input to be applied to the $V_{IN}3$ input of the ADC in single-ended mode; or for half a differential signal to be applied to the AD8138 for differential signal buffering.
P11	CLKIN. Subminiature BNC socket for an external clock input.
P12	$\overline{CS}$. Subminiature BNC socket for an external $\overline{CS}$ input.
P13	$\overline{RD}$. Subminiature BNC socket for an external RD input.
P14	$\overline{CONVST}$. Subminiature BNC socket for an external $\overline{CONVST}$ input.
P15	Busy. Subminiature BNC socket for reading the Busy output.
P16	$\overline{WR}$. Subminiature BNC socket for an external $\overline{WR}$ input.
P17	VREF. Subminiature BNC socket for an external VREF input.
P18	V_{IN} S.E. Subminiature BNC socket for the bipolar single-ended or pseudo differential analog input to the bias-up circuit.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7938CB/EVAL-AD7939CB/AD7938-6CB evaluation kit includes self-installing software on CD-ROM. The software is compatible with Microsoft® Windows® 95 or higher.

Install the evaluation board software before connecting the evaluation board to the USB port of the PC. This ensures the evaluation board is correctly recognized when connected to the PC.

1. Start the Windows operating system and insert the CD-ROM.

   The installation software launches automatically. If it does not, use Windows Explorer to locate the file **setup.exe** on the CD-ROM. Select this file to start the installation procedure.

2. At the prompt, select a destination directory, which is **C:\Program Files\Analog Devices\AD7938** by default.

   Once the directory is selected, the installation procedure copies the files into the relevant directories on the hard drive. The installation program creates a program group called **Analog Devices** with subgroup **AD7938** in the **Start** menu of the taskbar.

This program also installs electronic versions of the evaluation board data sheet and the ADC data sheets, as well as the EVAL-CONTROL-BRD2 data sheet.

SOFTWARE OVERVIEW

The Main Screen

The Main Screen, shown in Figure 3, allows you to read a pre-determined number of samples from the evaluation board and display them in both the time and frequency domain. This screen can be divided into three sections.

The upper portion of the screen contains the:

- Control buttons
- Menu bar
- Busy status indicators
- Selection windows.

Control Buttons

Use control buttons to take samples (**Sample**), reset the board (**Reset**), exit the program (**Exit**), and open the **Load Configuration Window** to load a configuration file (**Device Select**). The **Control Reg** button accesses the on-chip registers. Use the drop-down menus to change between the different modes, such as, single-ended and differential. However, use the **Control Reg** button to access the on-chip sequence and shadow registers.

Menu Bar

The menu bar consists of the **File, Config, Channel,** and **About** menus.

The **File** menu offers the following selections:

- **Load Raw Data.** Select this option to load data saved by the software during a previous session.
- **Save Raw Data.** Select this option to save the current set of sample data points. The data can be reloaded to the **EVAL-CONTROL-BRD2** software later or can be used by other programs for further analysis.
- **Save Binary Data.** Select this option to save the current set of sample data points. The data is saved in binary format as a text file. This method is useful for such tasks as examining code flicker and looking for stuck bits.
- **Exit.** Select this option to quit the program.

The **Config** drop-down menu sets up certain operating conditions in the ADC control register, such as power management, output coding, internal or external reference, and the analog input range.

The **Channel** drop-down menu allows the choice of analog input type (single-ended, differential, or pseudo differential).

The **About** drop-down menu provides information about the version of the software.

Frequency, Num Samples, Codes/Volts, and Busy Status Options

The **Frequency** window displays the speed at which the part is running. This can be changed. Note than when using the sequencer, the parts run at the speed chosen, however, this speed is divided down by the number of channels selected at any one time.

The **Num Samples** window allows you to change the sampling frequency and the number of samples to upload.

The **Codes/Volts** button determines whether the data is displayed in volts or codes.

The **Busy Status** indicates when the evaluation board is busy.

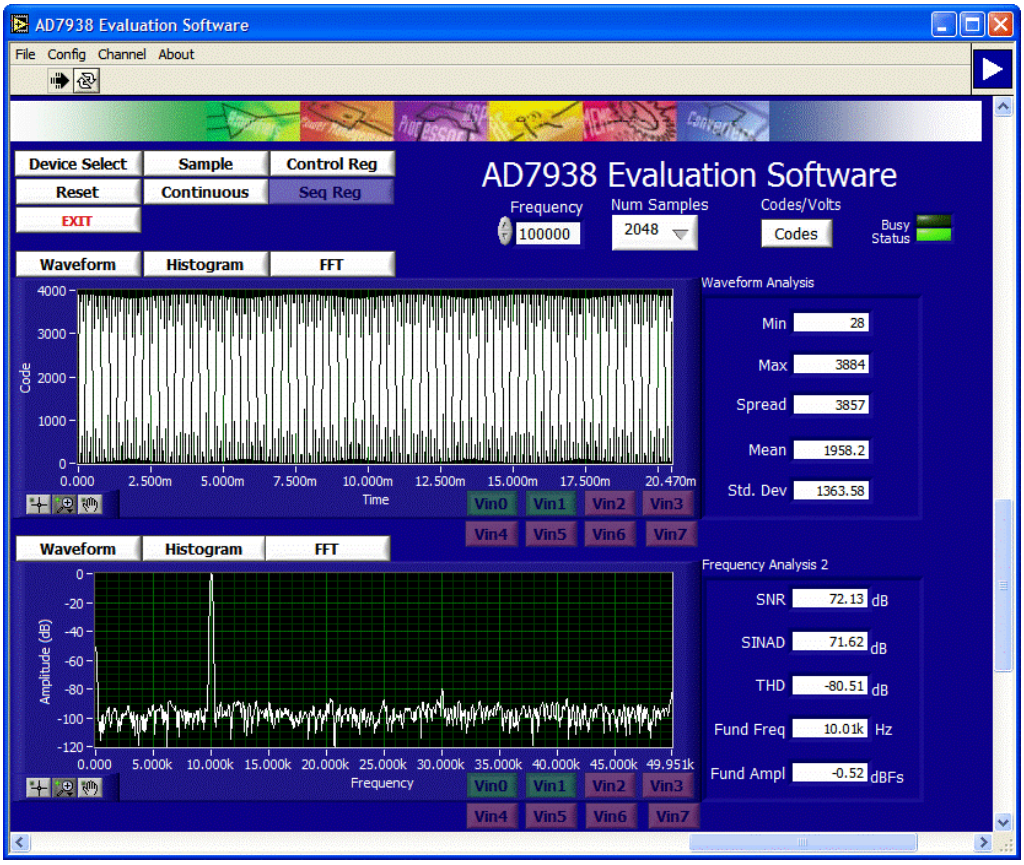

Figure 3. Main Screen

The middle portion of the screen is a Digital Storage Oscilloscope (DSO) for displaying either a **Waveform**, a **Histogram** or an **FFT**. Samples are uploaded from the EVAL-CONTROL-BRD2 are displayed here. Samples can be displayed either as integer values or as voltages. Zoom options are available to the bottom left of the graph. The area to the right of the graphs contains information about the samples taken (Min, Max, Spread, Mean, and Std. Dev)

The lower portion of the screen is also a DSO for displaying either a **Waveform**, a **Histogram** or an **FFT**. Use the FFT (default) option if you are concerned with examining the ADCs performance in the frequency domain. The Histogram gives an indication of the ADCs performance in response to dc inputs. Change the option displayed by clicking on one of the other (Waveform, Histogram or FFT buttons). The right side of the lower portion of this screen contains information about the samples taken.

Load Configuration Screen

The Load Configuration Screen, shown in Figure 4, allows you to load the required configuration file for the evaluation board. The configuration file provides the software with detailed information about the evaluation board and the part connected to the EVAL-CONTROL-BRD2, such as the number of bits, the maximum sampling rate, output coding, maximum sampling rate, and power supply requirements.

The configuration files also indicate to the software the name of the DSP program file to download to the EVAL-CONTROL-BRD2. The Load Configuration Screen allows you to choose the sampling frequency and the number of samples to take.

Figure 4. Load Configuration Screen

Figure 5. Control Register Screen

To use the sequencer register function, first write to the control register. To do this, click on the **Control Reg** button to display the control register panel, as shown in Figure 5.

CHECKING THE EVAL-CONTROL-BRD2

The EVAL-CONTROL-BRD2 and the evaluation board should be connected together as described in the Interfacing the Evaluation Boards section.

At this stage, the red LED on the EVAL-CONTROL-BRD2 should be flashing. This indicates that that EVAL-CONTROL-BRD2 is functional and ready to receive instructions.

Note that the software should be installed before the printer port cable is connected between the EVAL-CONTROL BRD2 and the PC. This ensures that the printer port has been initialized properly.

USING THE SOFTWARE

Once the software is installed and running:

1. Click on the **Device Select** control button on the Main Screen (see Figure 3) to display the Load Configuration Window (see Figure 4). Notice that the available configuration files are listed. The configuration files are text-based files containing formation about the evaluation board to be tested. The information includes the part name, number of samples to be taken, default and maximum sampling frequency, and power supply settings. The configuration file also contains the name of the DSP program file to be downloaded to the EVAL-CONTROL BRD2.
2. Select the relevant configuration file and click **OK**.

   The EVAL-CONTROL BRD2 is reset and the DSP program is downloaded. When the download has been completed, the power supply settings indicated in the configuration file are set (you may hear some of the relays clicking). The selection windows, such as **Num Samples**, have been set to the default values specified by the configuration file. These selections can now be changed.

TAKING SAMPLES

To instruct the EVAL-CONTROL BRD2 to take the required number of samples at the required frequency, follow these steps using the Main Screen shown in Figure 3:

1. Click **Sample**.

   Samples are uploaded and displayed. An FFT and histogram are also calculated and displayed.

2. Click **Continuous** to continue taking samples.
3. Click **EXIT** to stop the process.

SOFTWARE CONFIGURATION FILES:

Software configuration files provide the EVAL-CONTROL-BRD2 with information on how the software and hardware should perform. These files contain formation, such as the name of the DSP program to download, the default and maximum sample frequencies, the number of samples to take, and the power supply settings to use.

What follows is a typical Software Configuration File (*.cfg).

```
 [EVAL-CONTROL BOARD]
partname:AD7938
programname:ad7938.PRG
samplefrequency:100000
maxsamplefrequency:1000000
samples:2048
+/-15 V:on
dvdd:5:on
avdd:5:on
bus:on
;options 2scomp, binary
dataformat:binary
numberofbits:12
inputVmax:2.5
inputVmin:0
[endofconfig]
```

EVALUATION BOARD SCHEMATICS AND ARTWORK

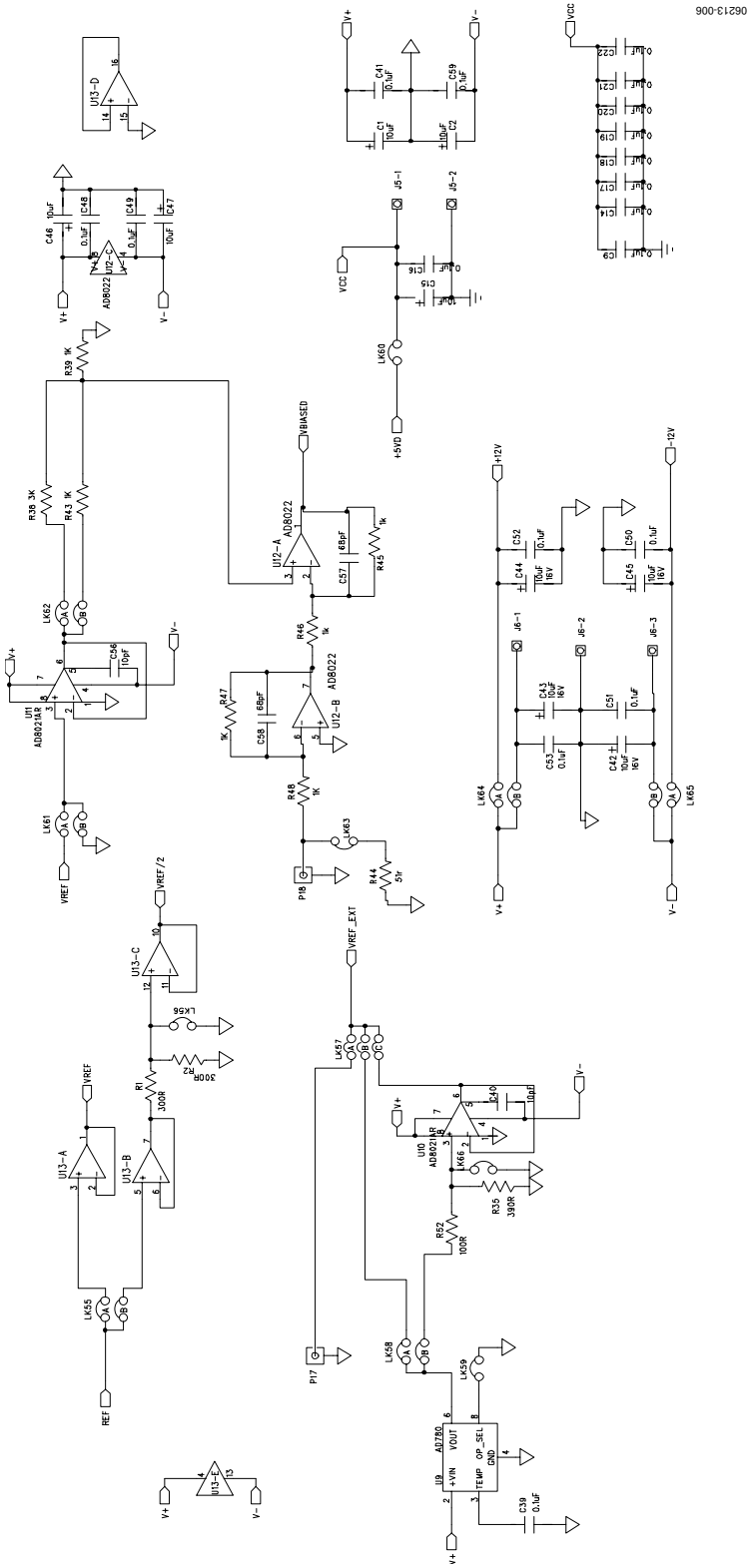

Figure 6. Evaluation Board Circuit Diagram, Page 1

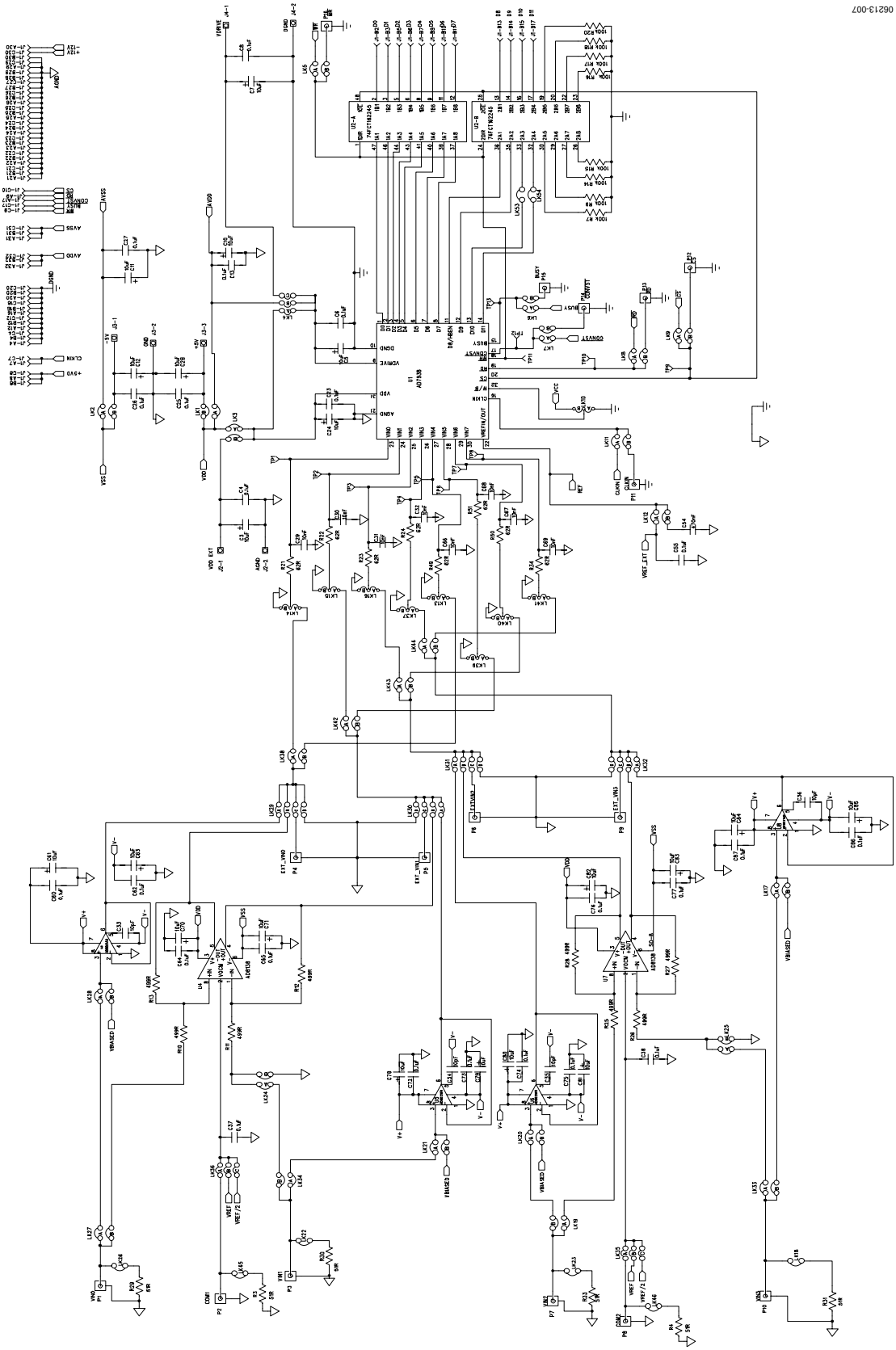

Figure 7. Evaluation Board Circuit Diagram, Page 2

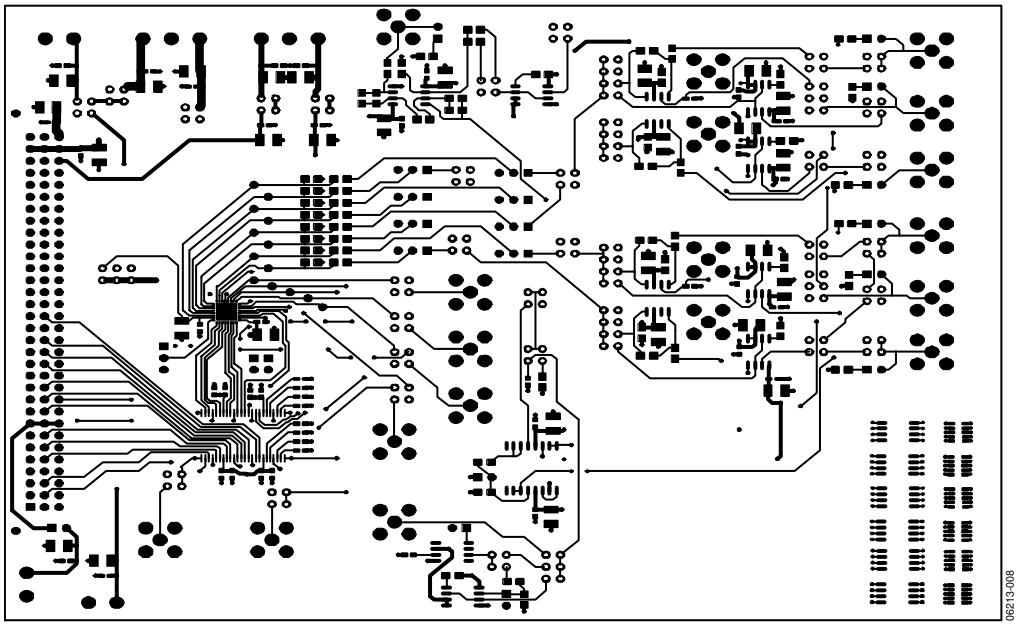

Figure 8. Evaluation Board Layout, Component Side Artwork

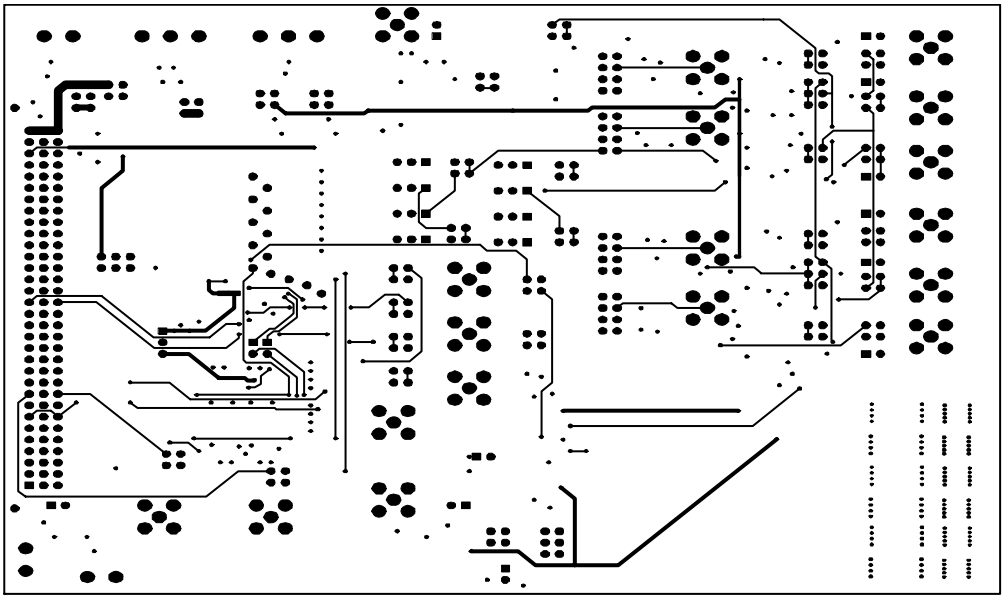

Figure 9. Evaluation Board Layout, Solder Side Artwork

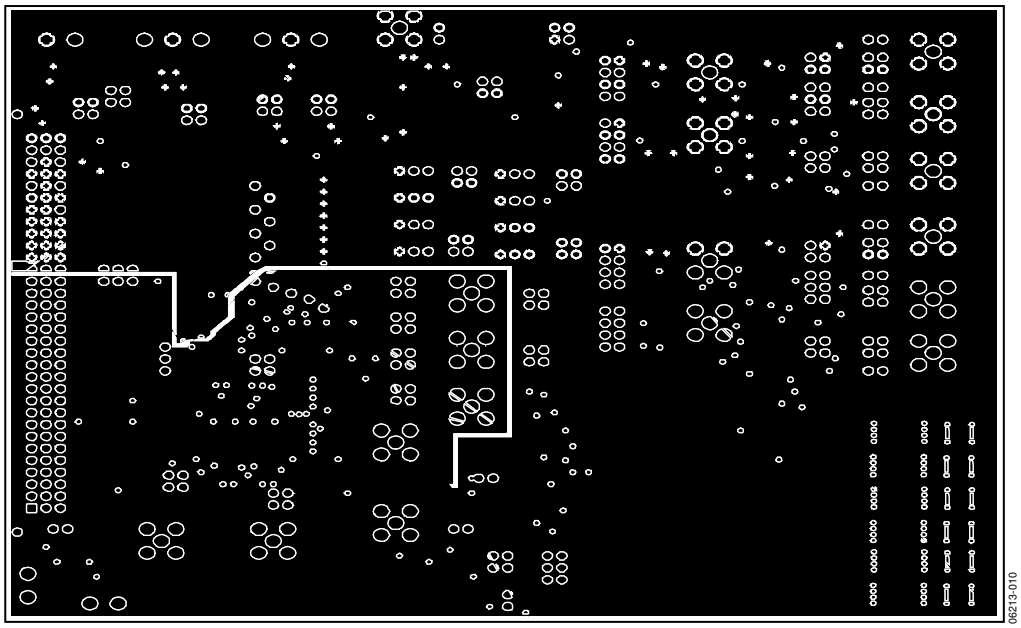

Figure 10. Evaluation Board Layout, Layer 2

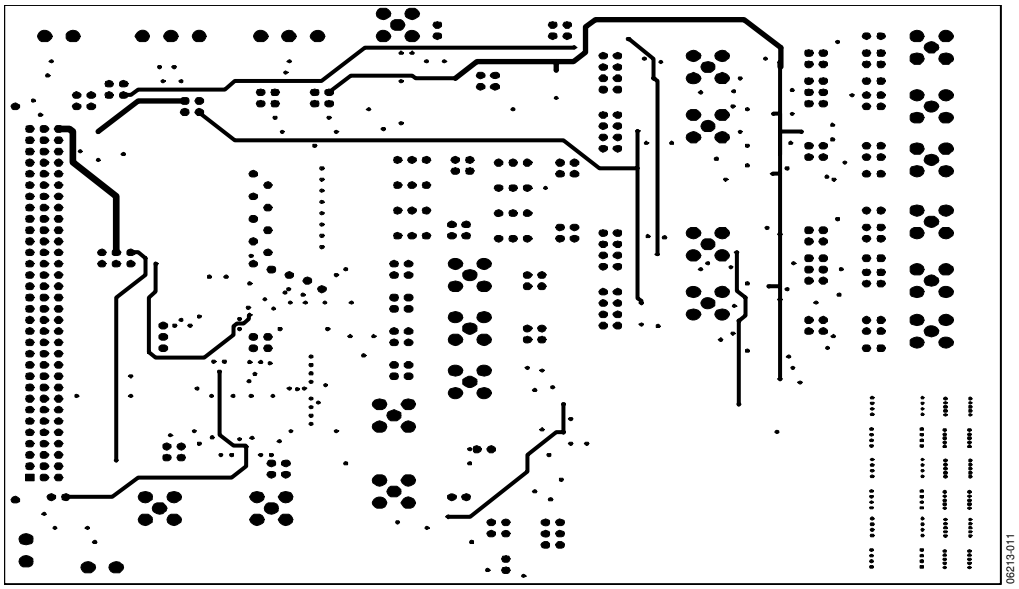

Figure 11. Evaluation Board Layout, Layer 3

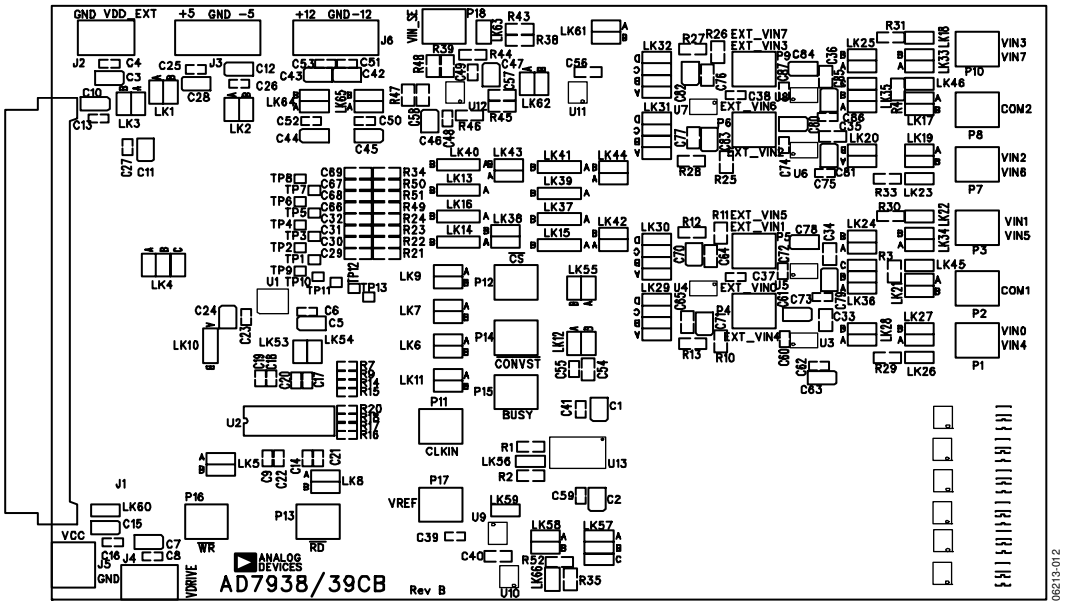

Figure 12. Evaluation Board Layout, Silkscreen