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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



## Evaluating the **AD7961** 16-Bit, 5 MSPS PulSAR Differential ADC

### FEATURES

Full-featured evaluation board for the **AD7961**  
Versatile analog signal conditioning circuitry  
On-board reference, reference buffers, and ADC drivers  
System demonstration board compatible (**EVAL-SDP-CH1Z**)  
PC software for control and data analysis of time and frequency domain

### EVALUATION KIT CONTENTS

**EVAL-AD7961FMCZ** evaluation board

### ADDITIONAL EQUIPMENT AND SOFTWARE NEEDED

System demonstration platform (**EVAL-SDP-CH1Z**)  
Precision source  
World-compatible, 12 V dc supply adapter (enclosed with **EVAL-SDP-CH1Z**)  
Power supply, +7 V/–2.5 V (optional)  
USB cable  
SMA cable

### ONLINE RESOURCES

#### Documents

[AD7961 data sheet](#)  
[EVAL-AD7961FMCZ user guide](#)

#### Required Software

[EVAL-AD7961FMCZ evaluation software](#)

#### Design and Integration Files

[Schematics](#), [layout files](#), [bill of materials](#)

### GENERAL DESCRIPTION

The **EVAL-AD7961FMCZ** is an evaluation board designed to demonstrate the low power **AD7961** performance (16-bit, 5 MSPS PulSAR® differential ADC) and to provide an easy-to-understand interface for a variety of system applications. A full description of the **AD7961** is available in the data sheet and should be consulted when utilizing this evaluation board.

The user PC software executable controls the evaluation board over the USB through the Analog Devices, Inc., system demonstration platform board (SDP), **EVAL-SDP-CH1Z**.

On-board components include the following:

**ADR4520/ADR4540/ADR4550**: high precision, buffered band gap 2.048 V/4.096 V/5.0 V reference options

**AD8031**: reference buffer

**ADA4899-1/ADA4897-1**: a signal conditioning circuit with two op amps and an option to use a differential amplifier (**ADA4932-1**)

**ADP7102, ADP7104, ADP124, and ADP2300**: regulators to derive necessary voltage levels on board

This evaluation board interfaces to the SDP board via a 160-pin FMC connector. SMA connectors, JP1/JP4 and JP2/JP5, are provided for the low noise analog signal source.

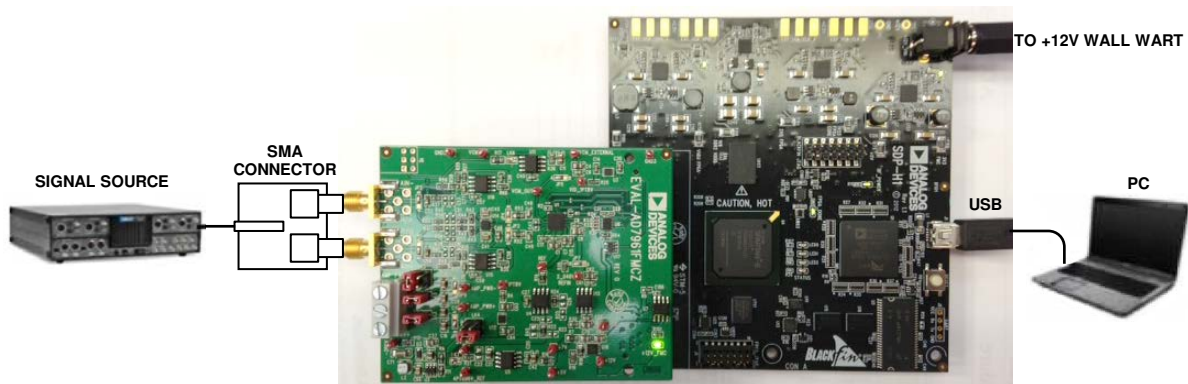


Figure 1. Setting Up the **EVAL-AD7961FMCZ**

11986-001

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**REVISION HISTORY**

8/13—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

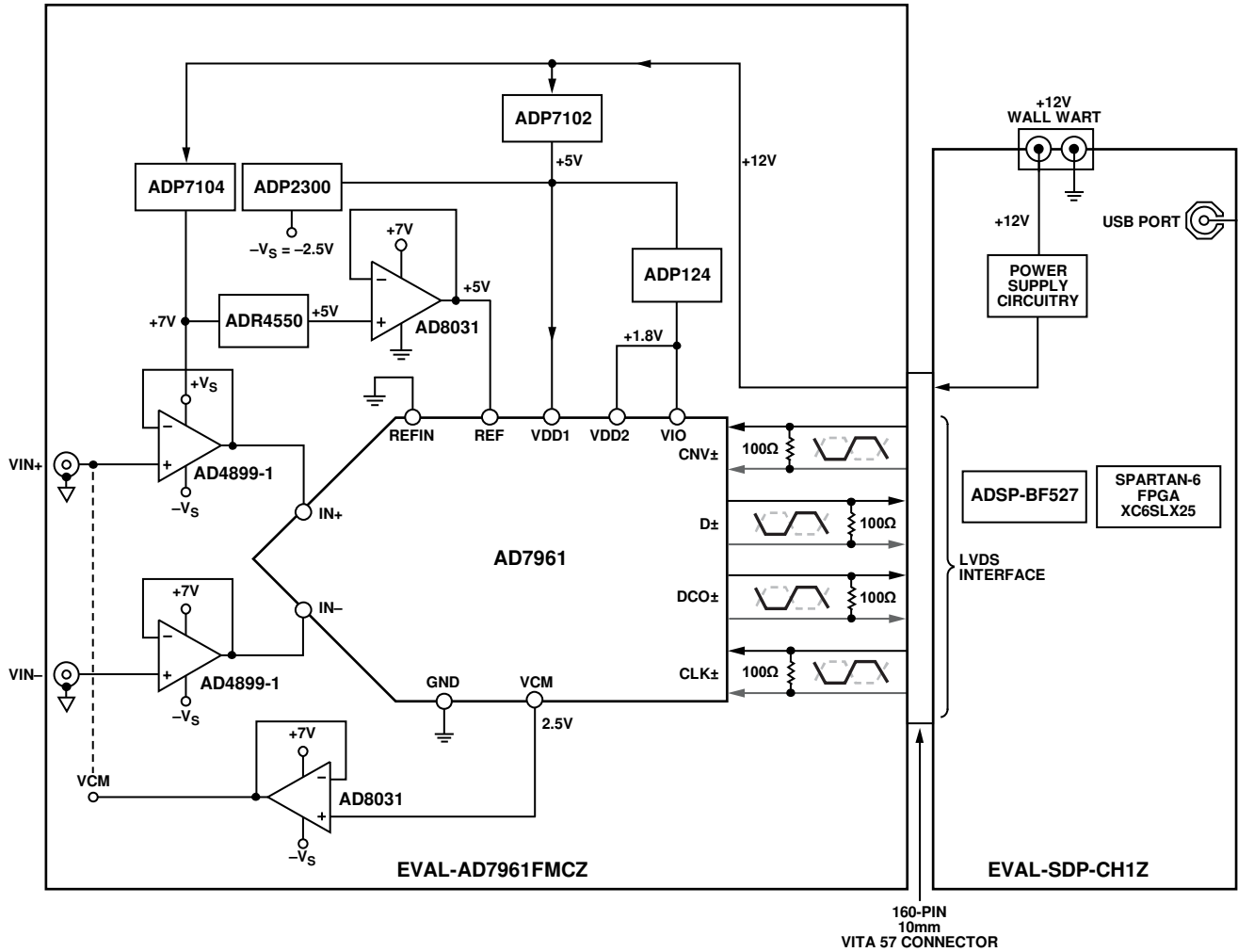


Figure 2.

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## EVALUATION BOARD HARDWARE

### DEVICE DESCRIPTION

The [AD7961](#) is a 5 MSPS, high precision, power efficient, 16-bit ADC that uses SAR-based architecture and does not exhibit any pipeline delay or latency. The [AD7961](#) is specified for use with 5 V and 1.8 V supplies (VDD1, VDD2). The interface from the digital host to the [AD7961](#) uses 1.8 V logic only.

The [AD7961](#) uses an LVDS interface to transfer data conversions. Complete [AD7961](#) specifications are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details on the [EVAL-SDP-CH1Z](#) are available on the Analog Devices website.

### HARDWARE LINK OPTIONS

The function of the link options are described in Table 1. When the user first receives the board, the default link setting on the board are as shown in Table 1 (analog input/reference/power supplies, and so on).

**Table 1. Pin Jumper Descriptions**

Link	Default	Purpose
JP1, JP2	B to center	Connects analog inputs VIN+ and VIN– to the inputs of the ADC driver <a href="#">ADA4899-1</a> or <a href="#">ADA4897-1</a> . A to center sets the fully differential path through <a href="#">ADA4932-1</a> .
JP3, JP4	B to center	Connect outputs from <a href="#">ADA4899-1</a> to inputs of <a href="#">AD7961</a> . A to center set the fully-differential path through <a href="#">ADA4932-1</a> .
JP5	A to center	Connect the VCM output from <a href="#">AD7961</a> to <a href="#">AD8031</a> .
JP7	A to center	Connects REFIN to 2.048 V external reference. B to center connects REFIN to GND.
JP8	B to center	Connects +7 V to amplifier +Vs.
JP9	B to center	Connects –2.5 V to amplifier –Vs.
LK2, LK3	Inserted	Option to use external amplifier supplies + Vs and – Vs.
LK4	A	Connects to +7 V coming from <a href="#">ADP7102</a> .
LK5	B	Connects to –2.5 V coming from <a href="#">ADP2300</a> .
LK6	B	Connects the output of VCM buffer to VCM of amplifier.
LK7	B	Connects the +5 V output from <a href="#">ADR4550</a> to REF buffer <a href="#">AD8031</a> .

**Table 2. On-Board Connectors**

Connector	Function
J1, J2, J4, J5	SMA Analog Input. Connects the low noise analog signal source to the inputs of <a href="#">ADA4899-1</a> or <a href="#">ADA4932-1</a> .
J3	3-Pin Terminal. This option is for using external bench top supplies. Apply external +Vs, –Vs, and GND to power amplifiers on the <a href="#">EVAL-AD7961FMCZ</a> board.
J6	6-Pin (2 × 3) Socket. This option is for interfacing with an external ADC driver board.
J7	160-Pin FMC 10 mm Male VITA 57 Connector. This connector mates with the <a href="#">EVAL-SDP-CH1Z</a> board.

### POWER SUPPLIES

The power (+12 V) for the [EVAL-AD7961FMCZ](#) board comes through a 160-pin FMC connector, J7, from the [EVAL-SDP-CH1Z](#). The customer also has the option of using external bench top supplies to power the on-board amplifiers. On-board regulators generate required levels from the applied +12 V rail.

The [ADP7102](#) (U18) supplies +7 V for the +Vs of the ADC driver amplifiers ([ADA4899-1](#) or [ADA4897-1](#)), external reference [ADR4550](#) (U5), and [ADR4540](#) (U8), while the [ADP7104](#) (U10) delivers +5 V for VDD1 (U1), [ADP2300](#) (U2), and [ADP124](#) (U3 and U12). The [ADP2300](#) (U2), in turn, generates –2.5 V for the amplifier’s –Vs and the [ADP124](#) (U3 and U12), in turn, provides a 1.8 V for VDD2 and VIO (U1).

The +3.3 V supply for the EEPROM (U7) comes from the [EVAL-SDP-CH1Z](#) through a 160-pin FMC connector, J7. Each supply is decoupled where it enters the board and again at each device. A single ground plane is used on this board to minimize the effect of high frequency noise interference.

**Table 3. On-Board Power Supplies Description**

Power Supply	Voltage Range (V)	Purpose
+V <sub>s</sub>	+5 V to +7 V	ADP7104 (U10) and ADP7102 (U18) generate the necessary +5 V and +7 V, respectively, from +12 V coming from EVAL-SDP-CH1Z. The +7 V supply is recommended for on-board amplifier +V <sub>s</sub> . The +5 V supply is provided to VDD1 (U1), ADP2300 (U2), ADR4540/ADR4550 (U5 and U8), and ADP124 (U3 and U12). The user also has an option to use an external bench top supply +V <sub>s</sub> through J3.
-V <sub>s</sub>	-2 V to -5 V	ADP2300 generates -2.5 V for amplifier -V <sub>s</sub> . The user also has an option to use an external bench top supply -V <sub>s</sub> through J3.
+V <sub>s</sub> to -V <sub>s</sub>	12 V <sup>1</sup>	Maximum range of supply for correct operation.
VDD1	5 V <sup>2</sup>	AD7961 Analog Supply Rail.
VDD2, VIO	1.8 V <sup>2</sup>	ADC Supply Rails.

<sup>1</sup>Dictated by ADA4899-1 supply operation.

<sup>2</sup>Refer to the AD7961 data sheet

**SERIAL INTERFACE**

The EVAL-AD7961FMCZ uses the serial interface connection to the EVAL-SDP-CH1Z. The EVAL-AD7961FMCZ operates only in echo-clocked serial interface mode. This mode requires three LVDS pairs (D±, CLK±, and DCO±) between each AD7961 and the digital host. The EVAL-SDP-CH1Z board features include

- XILINX Spartan®-6 FPGA
- DDR2
  - Micron MT47H32M16Hr-25E:G  
-8 Mb × 16 bits × 4 Banks(512 Mb/64 Mb)
- SRAM
  - ISSI IS61WV25616BLL-10BLI  
-256 Kb × 16 bits (4 Mb/512 Kb)
- 1 × 160-pin FMC-LPC connector (refer to the VITA 57 specification)
  - Samtec ASP-134603-01
  - Up to 1080 Mbps LVDS
  - Single-ended LVCMOS
  - Power
- Analog Devices, Inc., ADSP-BF527 Blackfin® processor
  - Core performance up to 600 MHz
  - 208-ball CSP-BGA package
  - 24 MHz CLKIN oscillator
- 32 Mb flash memory
  - Numonyx M29W320EB or
  - Numonyx M25P32
- SDRAM memory
  - Micron MT48LC16M16A2P-6A  
-16 Mb × 16 bits (256 Mb/32 MB)
- 2 × 120-pin small foot print connectors
  - Hirose FX8-120P-SV1(91),120-pin header
- Blackfin processor peripherals exposed
  - SPI
  - SPORT
  - TWI/I<sup>2</sup>C

- GPIO
- PPI
- Asynchronous parallel

**ANALOG INPUTS**

This section provides information on the analog input options and how these options can be configured as well as information on how customers should connect their signal source.

The analog inputs applied to the EVAL-AD7961FMCZ board are J1 and J2 SMA (push-on) connectors. These inputs are buffered with dedicated discrete driver amplifier circuitry (U15 and U16 or U14) as shown in Figure 1.

The circuit allows for different configurations, input range scaling, filtering, the addition of a dc component, use of a different op amp, and a differential amplifier and supplies. The analog input amplifiers are set as unity gain buffers at the factory. The driver amplifiers (U14, U15, and U16) positive rails are driven from +7 V (from ADP7102, U18) and negative rail from -2.5 V; the other reference buffers (U4 and U11) positive rails are driven from +7 V and negative rails are grounded; these could be changed to a different value as required.

The range of supplies possible is listed in Table 3. The default configuration sets both U15 and U16 at mid-scale generated from a buffered reference voltage (VCM) of the AD7961 (U1). The evaluation board is factory configured for providing either a single-ended path or a fully differential path as described in Table 1.

For dynamic performance, an FFT test can be performed by applying a very low distortion source.

For low frequency testing, the audio precision source can be used directly because the outputs on these are isolated. Set the outputs for balanced and floating. Different sources can be used though most are single ended and use a fixed output resistance.

Since the evaluation board uses the amplifiers in unity gain, the noninverting input has a common-mode input with a series 49.9 Ω resistor and it needs to be taken into account when directly connecting a source (voltage divider).

## REFERENCE OPTIONS

The [EVAL-AD7961FMCZ](#) board allows three reference voltage options. The user can select either the 5 V or 4.096 V option using the solder link LK7 or the 2.048 V on-board reference voltage using solder link JP7 as described in Table 1. The various options for using this reference are controlled by the EN1 and EN0 pins (EN bits on software) as described in detail in the [AD7961](#) data sheet.

## LAYOUT GUIDELINES

When laying out the printed circuit board (PCB) for the [AD7961](#), follow the recommended guidelines described in this section to obtain the maximum performance from the converter. Figure 30 to Figure 35 show the recommended layout for the [AD7961](#) evaluation board.

- Solder the [AD7961](#) exposed paddle (Pin 33) directly to the PCB and connect the paddle to the ground plane of the board using multiple vias.
- Decouple all the power supply pins (VDD1, VDD2 and VIO) and the REF pin with low ESR and low ESL ceramic capacitors, typically 10  $\mu$ F and 100 nF, placed close to the DUT (U1) and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.
- Use 50  $\Omega$  single-ended trace and 100  $\Omega$  differential trace.
- Separate analog and digital sections and keep power supply circuitry away from the [AD7961](#).
- Avoid running digital lines under the device and crossover of digital and analog signals because these couple noise into the [AD7961](#).
- Fast switching signals, such as  $CNV_{\pm}$  or  $CLK_{\pm}$ , should not run near analog signal paths.
- Remove the ground and power plane beneath the input (including feedback) and output pins of the amps (U14, U15, and U16) as they create an undesired capacitor.

## BASIC HARDWARE SETUP

The [AD7961](#) evaluation board connects to the ([EVAL-SDP-CH1Z](#)) system demonstration board. The [EVAL-SDP-CH1Z](#) board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 1 shows a photograph of the connections made between the [EVAL-AD7961FMCZ](#) daughter board and the [EVAL-SDP-CH1Z](#) board.

1. Install the [AD7961](#) software. Ensure the [EVAL-SDP-CH1Z](#) board is disconnected from the USB port of the PC while installing the software. The PC must be restarted after the installation.
2. Before connecting power, connect the [EVAL-AD7961FMCZ](#) board's 160-pin FMC connector, J7, to the connector J4 on the [EVAL-SDP-CH1Z](#) board. Nylon screws are included in the [EVAL-AD7961FMCZ](#) evaluation kit and can be used to ensure the [EVAL-AD7961FMCZ](#) and the [EVAL-SDP-CH1Z](#) boards are connected firmly together.
3. Connect the +12 V power supply adapter included in the kit to the [EVAL-SDP-CH1Z](#).
4. Connect the [EVAL-SDP-CH1Z](#) board to the PC via the USB cable. For Windows XP you may need to search for the [EVAL-SDP-CH1Z](#) drivers. Choose to automatically search for the drivers for the [EVAL-SDP-CH1Z](#) board if prompted by the operating system.
5. Launch the [EVAL-AD7961FMCZ](#) software from the **Analog Devices** subfolder in the **Programs** menu. The full software installation procedure is detailed in the Evaluation Board Software section.

# EVALUATION BOARD SOFTWARE

## SOFTWARE INSTALLATION

The evaluation kit software is available to download from the evaluation board page on Analog Devices website. Click the **setup.exe** file to run the install. The default location for the software is **C:\Program Files (x86)\Analog Devices\AD7960\_61 Evaluation Software**.

Install the evaluation software before connecting the evaluation board and **EVAL-SDP-CH1Z** board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts of the software installation process:

- **AD7961** evaluation board software installation
- **EVAL-SDP-CH1Z** board driver installation

Figure 3 to Figure 9 show the separate steps to install the **AD7961** evaluation software and Figure 10 to Figure 14 show the separate steps to install the **EVAL-SDP-CH1Z** drivers. Proceed through all of the installation steps to allow the software and drivers to be placed in the appropriate locations. Only after the software and drivers have been installed, should you connect the **EVAL-SDP-CH1Z** board to the PC.

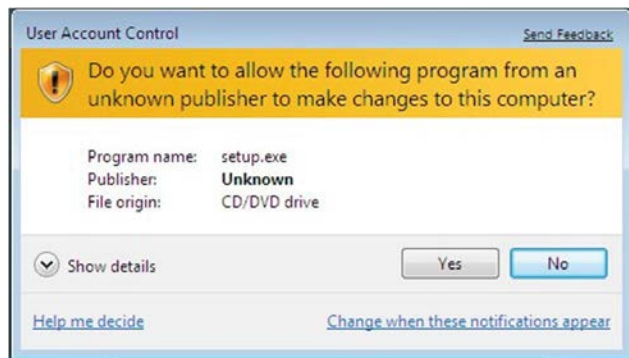


Figure 3. User Account Control

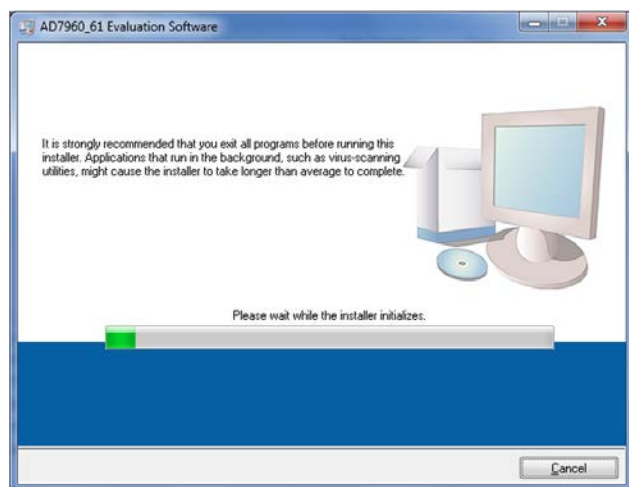


Figure 4. AD7961 Install Window 1

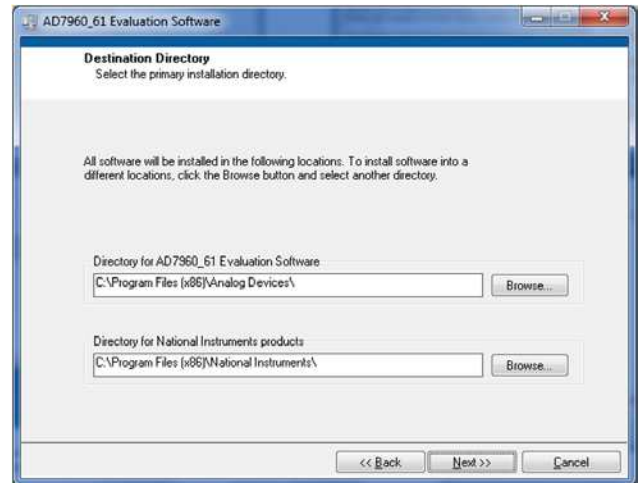


Figure 5. AD7961 Install Window 2

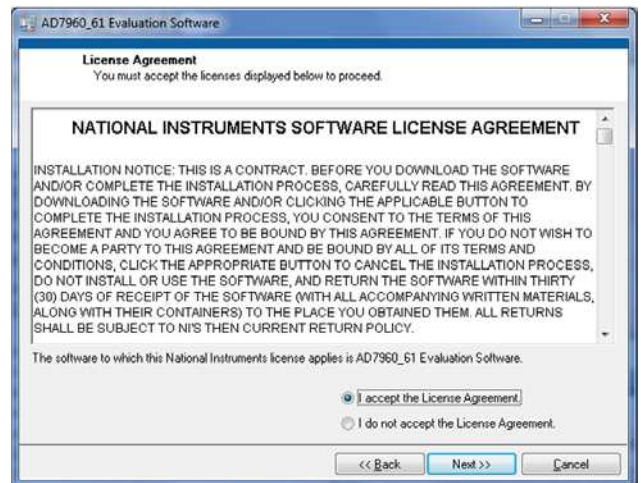


Figure 6. AD7961 Install Window 3

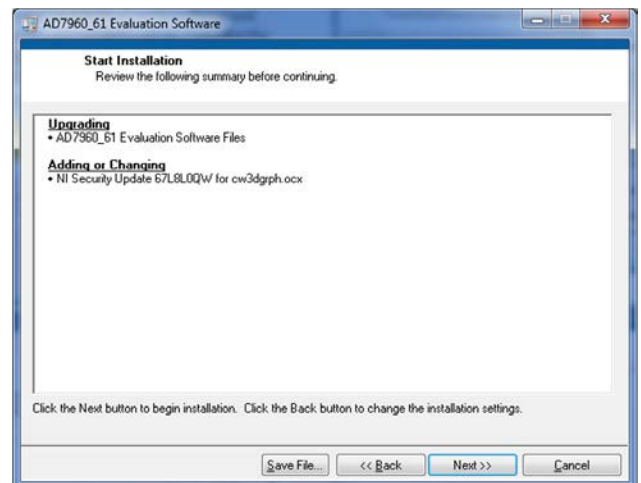


Figure 7. AD7961 Install Window 4



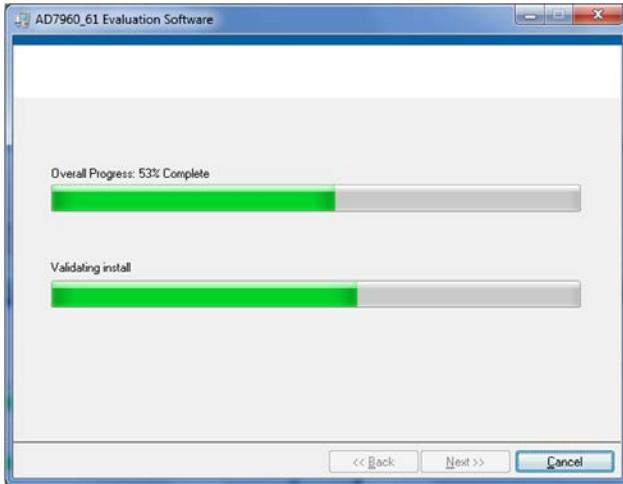


Figure 8. AD7961 Install Window 5

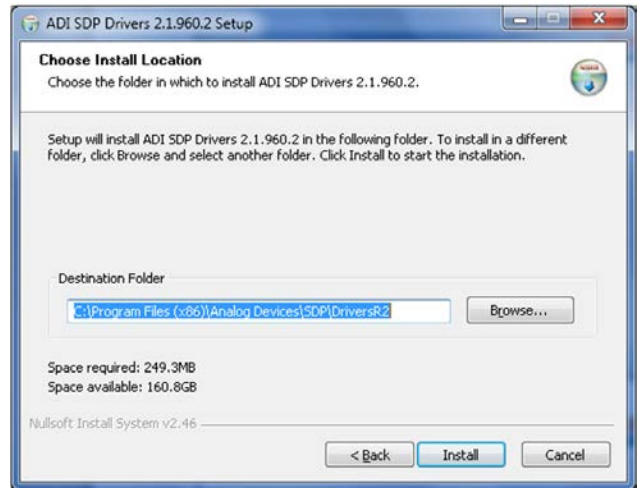


Figure 11. EVAL-SDP-CH1Z Drivers Setup Window 2

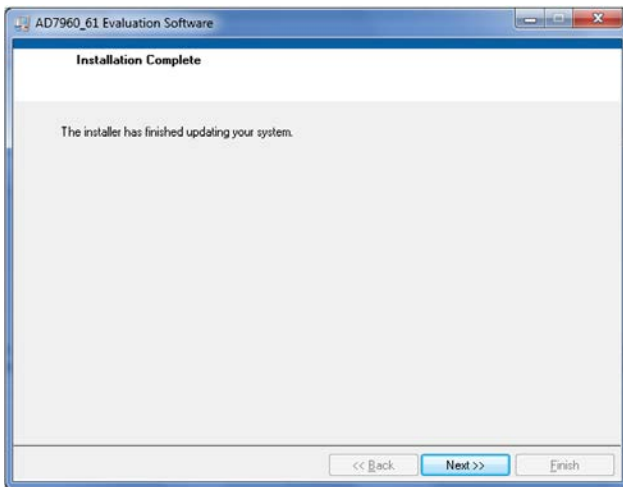


Figure 9. AD7961 Install Window 6

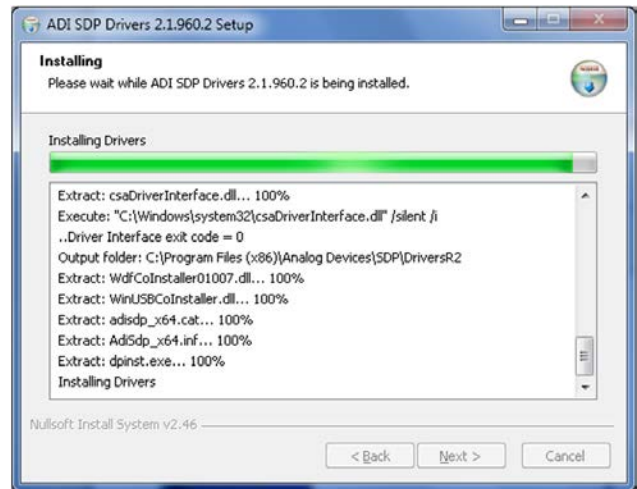


Figure 12. EVAL-SDP-CH1Z Drivers Setup Window 3



Figure 10. EVAL-SDP-CH1Z Drivers Setup Window 1



Figure 13. EVAL-SDP-CH1Z Drivers Setup Window 4



Figure 14. EVAL-SDP-CH1Z Drivers Setup Window 5

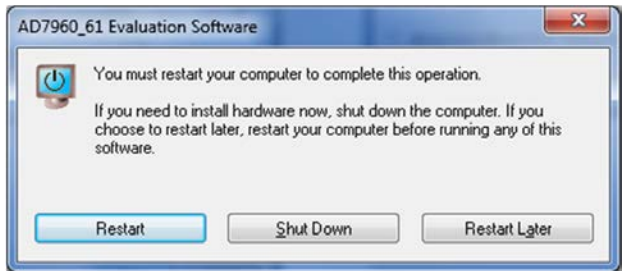


Figure 15. EVAL-SDP-CH1Z Drivers Setup Window 6

After installation is complete, connect the EVAL-AD7961FMCZ to the EVAL-SDP-CH1Z as described in the Evaluation Board Hardware section.

When you first plug in the EVAL-SDP-CH1Z board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Once the drivers are installed, you can check that the board has connected correctly by looking at the **Device Manager** of the PC. The **Device Manager** can be accessed via **My Computer>Manage>Device Manager** from the list of **System Tools**. The EVAL-SDP-CH1Z board should appear under **ADI Development Tools**.

This completes the installation.

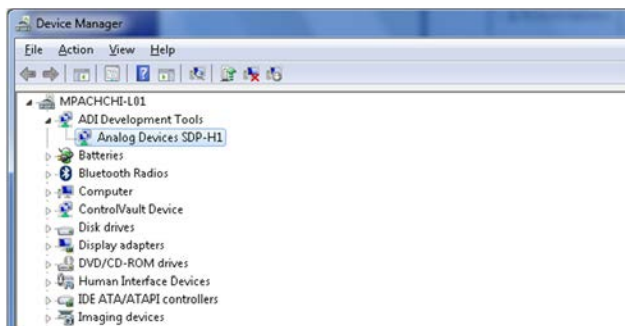


Figure 16. Device Manager

## LAUNCHING THE SOFTWARE

Once the EVAL-AD7961FMCZ and EVAL-SDP-CH1Z are correctly connected to your PC, the AD7961 software can be launched.

1. From the **Start** menu, select **Programs>Analog Devices>AD7960\_61 Evaluation Software**. The main window of the software then displays (see Figure 19). If the evaluation system is not connected to the USB port via the EVAL-SDP-CH1Z when the software is launched, a connectivity error displays (see Figure 17).
2. Connect the evaluation board to the USB port of the PC.
3. Wait for a few seconds and then click **Rescan** (see Figure 18).

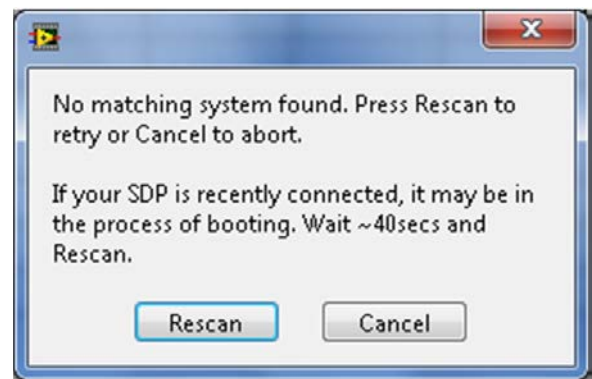


Figure 17. Connectivity Error Alert 1



Figure 18. Connectivity Error Alert 2

## SOFTWARE OPERATION

This section describes the full software operation and all windows that appear. When the software is launched, the panel opens and the software searches for hardware connected to the PC. The user software panel launches as shown in Figure 19. The labels listed in this section correspond to the numbered labels in Figure 19.

### **File Menu (Label 1)**

The **File** menu, labeled 1 in Figure 19, offers the choice to

- **Save Captured Data:** saves data to a .csv file
- **Load Captured Data:** loads data for analysis
- **Take Screenshot:** saves the current screen
- **Print:** prints the window to the default printer
- **Exit:** quits the application

### **Edit Menu (Label 2)**

The **Edit** menu, labeled 2, provides the following offering:

- **Initialize to Default Values:** This option resets the software to its initial state

### **Help Menu (Label 3)**

The **Help** menu, labeled 3, offers help from the

- **Analog Devices website**
- **User Guide**
- **Context Help**
- **About**

### **Throughput (Label 4)**

The default throughput (sampling frequency) is 5,000 kilo samples per second (kSPS). The user can adjust the sampling frequency, however there are limitations around the sample frequency related to the SCLK frequency applied; the sample frequency must be at least 500 kSPS. The [AD7961](#) is capable

of operating a maximum sample frequency up to 5,000 kSPS. If the user enters a value larger than the ability of the [AD7961](#), the software indicates this and the user must revert to the maximum sample frequency.

### **Samples (Label 5)**

Select the number of **Samples** to analyze, when running the software; this number is limited to 131,072 samples.

### **Single Capture (Label 6) and Continuous Capture (Label 7)**

**Single Capture** performs a single capture whereas **Continuous Capture** performs a continuous capture from the ADC.

### **Eval Board Connected (Label 8)**

This indicator shows that the device connected.

### **Voltage Reference (Label 9)**

The various options for using the external reference are controlled by the **Voltage Reference** option. The default value is set to 5 V (**External Buffer**). The other voltage reference voltage options are 4.096 V and 2.048 V. It is recommended to use an on-board [AD8031](#) as an external reference buffer.

### **Tabs**

There are four tabs additional available for displaying the data in different formats.

- Waveform
- Histogram
- FFT
- Summary

To exit the software, go to **File>Exit**.

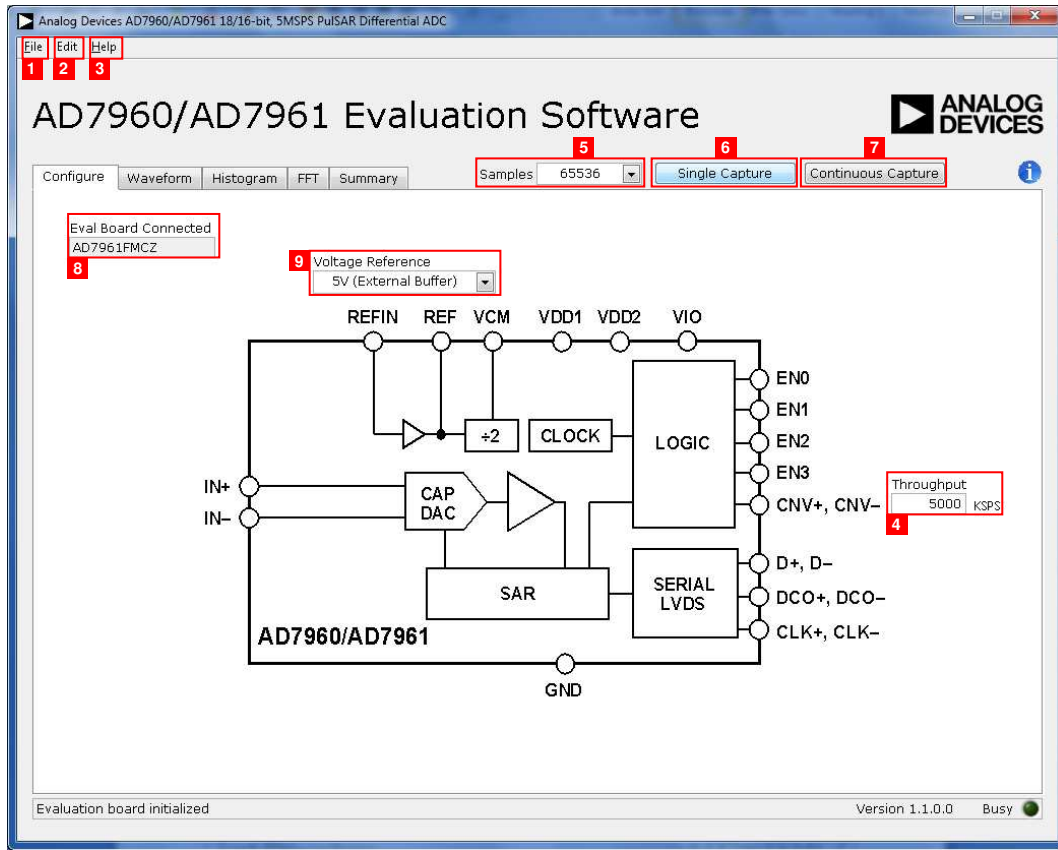


Figure 19. Setup Screen

**WAVEFORM CAPTURE**

Figure 20 illustrates the Waveform tab. The 1 kHz sine-wave input signal was used along with an on-board 5 V external reference.

Note that Label 1 shows the **Waveform Analysis** which reports the amplitudes recorded from the captured signal in addition to the frequency of the signal tone.

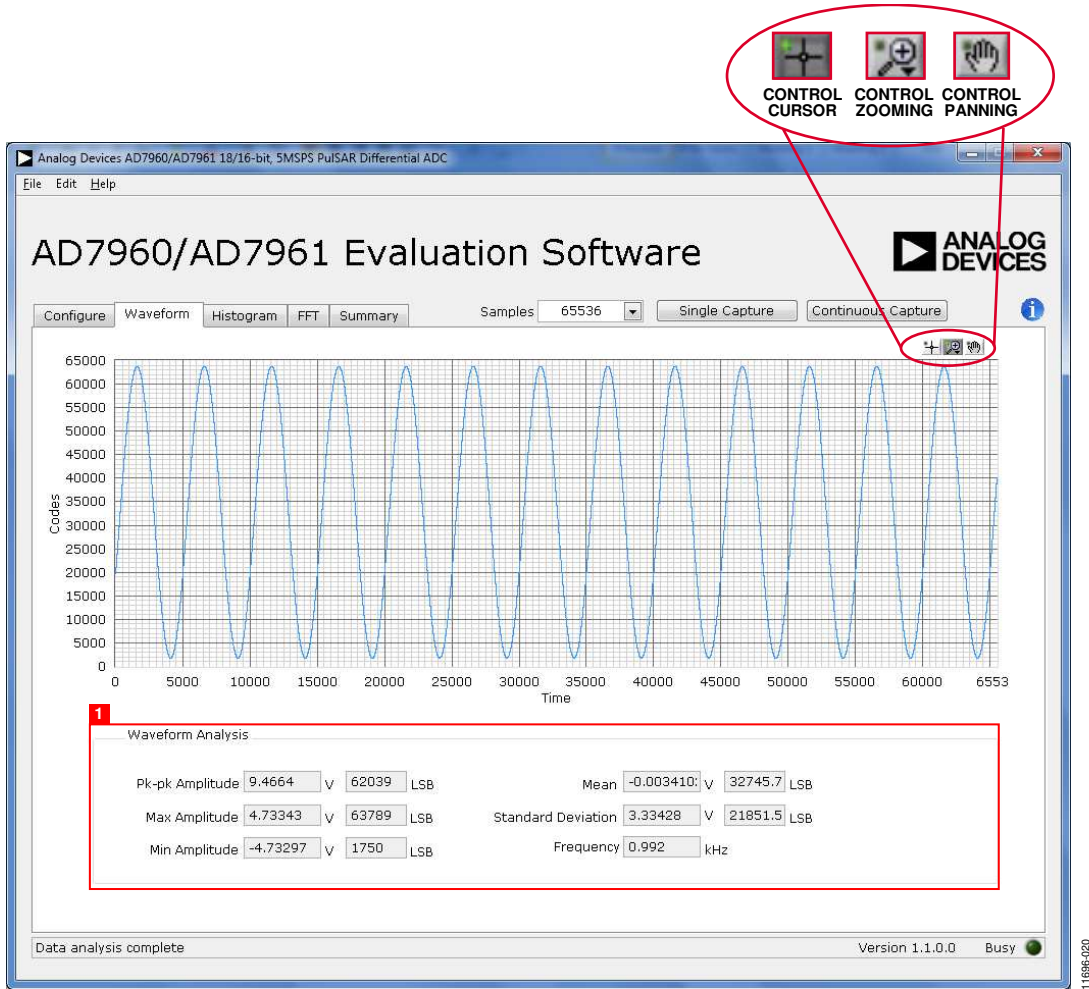


Figure 20. Waveform Capture Tab

**DC TESTING—HISTOGRAM**

The histogram is most often used for dc testing where a user tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise, of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test,

1. Select the Histogram tab.
2. Click **Single Capture** or **Continuous Capture**.

Note that a histogram test can be performed without an external source since the evaluation board has a buffered  $V_{REF}/2$  source at the ADC input.

To test other dc values, apply a source to the J1/J2 inputs. You may be required to filter the signal to make the dc source noise compatible with that of the ADC.

**AC TESTING—HISTOGRAM**

Figure 21 shows the Histogram tab. This tests the ADC for the code distribution for ac input and computes the mean and standard deviation, or transition noise, of the converter and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test,

1. Select the Histogram tab.
2. Click **Single Capture** or **Continuous Capture**.

Note that an ac histogram needs a quality signal source applied to the input J1/J2 connectors.

Figure 21 shows the histogram for a 1 kHz sine wave applied to the ADC input and the results calculated.

The **Histogram Analysis** (Label 1) illustrates the various measured values for the data captured.

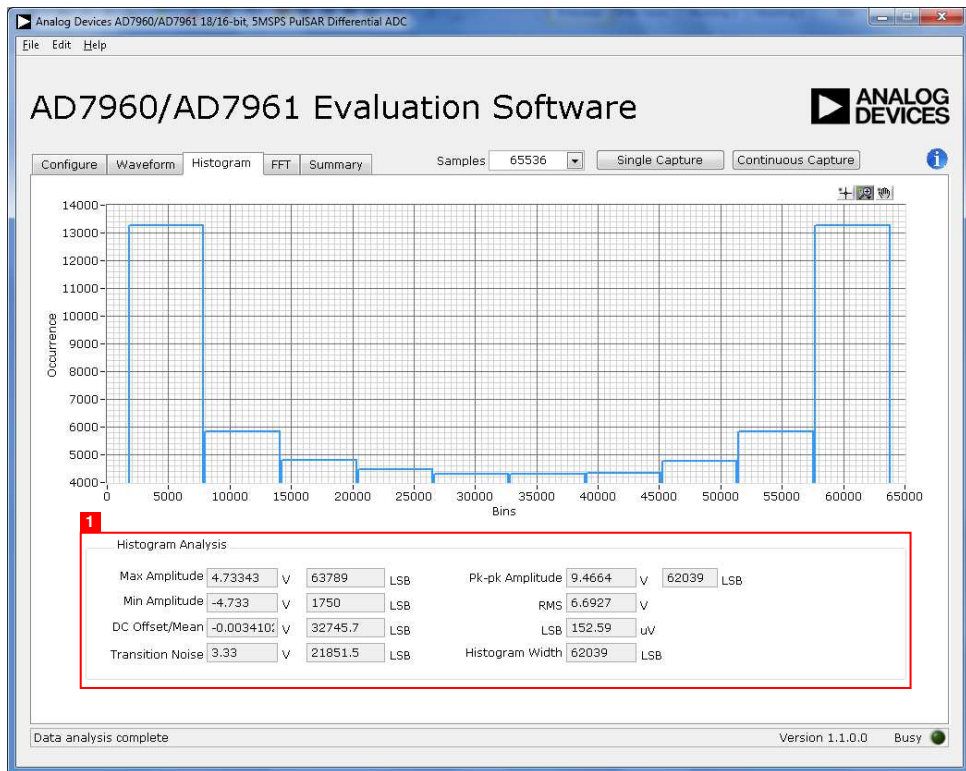


Figure 21. Histogram Capture Tab

## AC TESTING—FFT CAPTURE

Figure 22 shows the FFT tab. This tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD, and SFDR.

To perform an ac test, apply a sinusoidal signal to the evaluation board at the SMA inputs J1/J2. Very low distortion, better than 130 dB input signal source (such as audio precision) is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but carefully consider the choices.

Furthermore, if using a low frequency band-pass filter when the full-scale input range is more than a few V p-p, it is recommended to use the on-board amplifiers to amplify the signal, thus preventing the filter from distorting the input signal.

Figure 22 displays the results of the captured data.

- Shows the input signal information (see Label 1)
- Displays the fundamental frequency and amplitude in addition to the 2<sup>nd</sup> to 5<sup>th</sup> harmonics (see Label 2)
- Displays the performance data, including SNR, dynamic range, THD, SINAD, and noise performance (see Label 3)

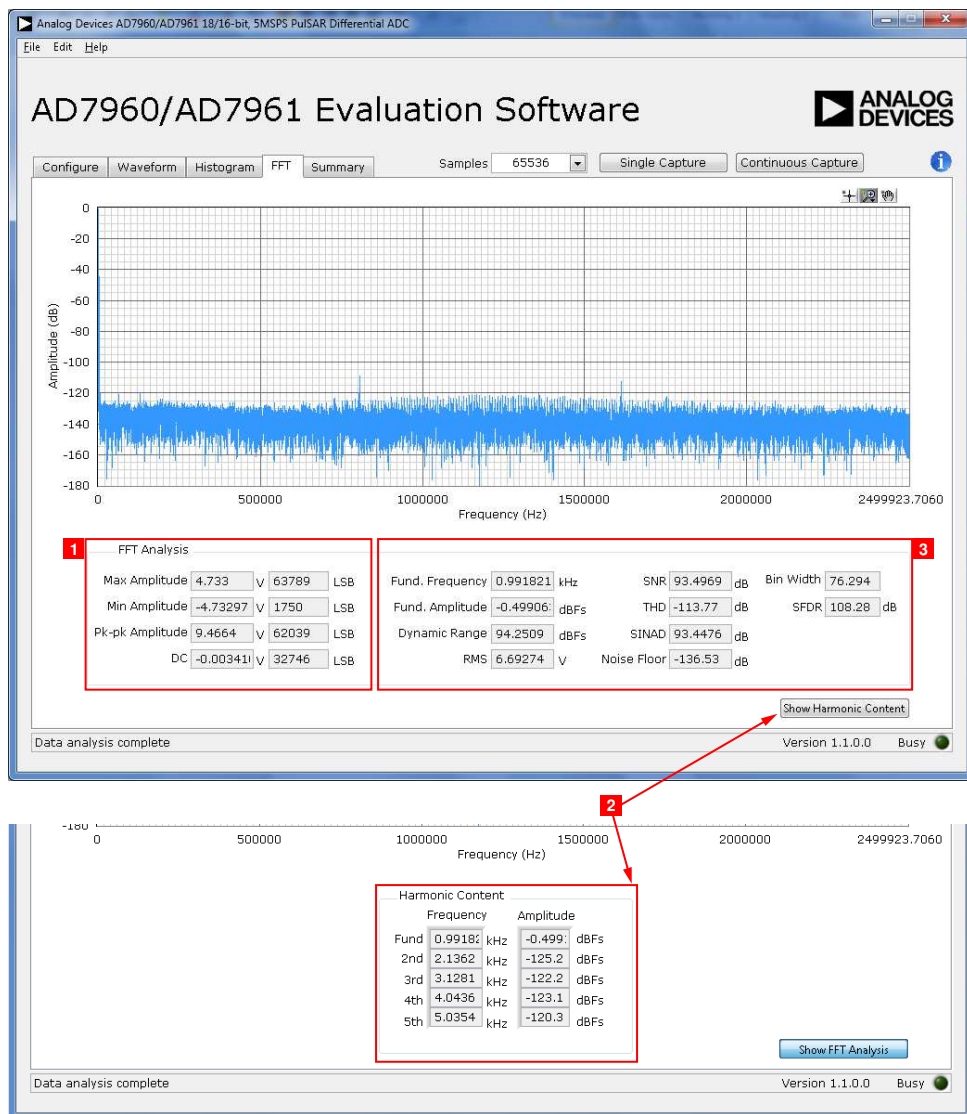


Figure 22. FFT Capture Tab

**SUMMARY TAB**

Figure 23 shows the Summary tab which captures all the display information and provides it in one panel with a synopsis of the

information, including key performance parameters, such as SNR and THD.

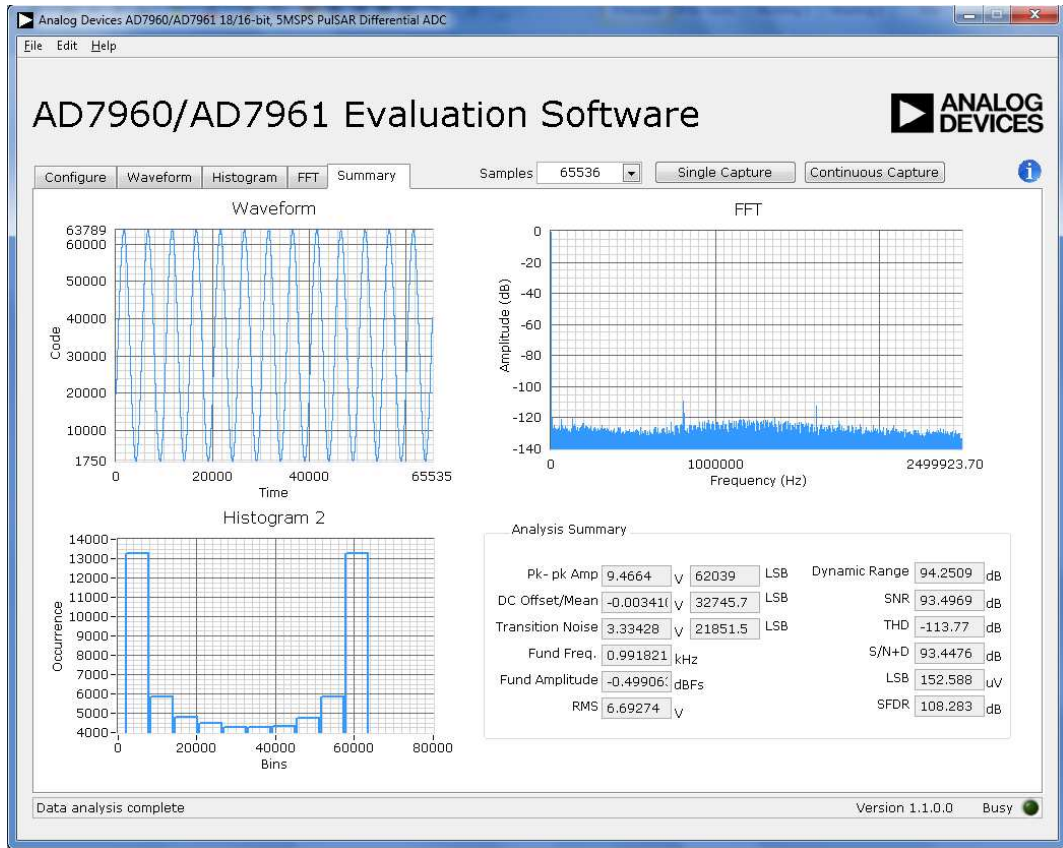


Figure 23. Summary Tab



## TROUBLESHOOTING

This section provides hints on how to prevent problems and what to check when you encounter problems with the software and hardware.

### SOFTWARE

Review the following points regarding software:

- Always install the software prior to connecting the hardware to the PC.
- Always allow the install to fully complete (the software installation is a two-part process: installing the ADC software and the SDP drivers). This may require a restart.
- When you first plug in the [EVAL-SDP-CH1Z](#) board via the USB cable provided, allow the new **Found Hardware Wizard** to run. Though this may take time, do this prior to starting the software.
- If the board does not appear to be functioning, ensure that the ADC evaluation board is connected to the [EVAL-SDP-CH1Z](#) board and that the board is recognized in the **Device Manager**, as shown in Figure 7.
- If connected to a slower USB port where the [EVAL-SDP-CH1Z](#) cannot read quickly, a timeout error may occur. In this case, it is advised not to read continuously or, alternatively, to lower the number of samples taken.
- Note that when reading continuously from the ADC, the recommended number of samples is up to 65,536.

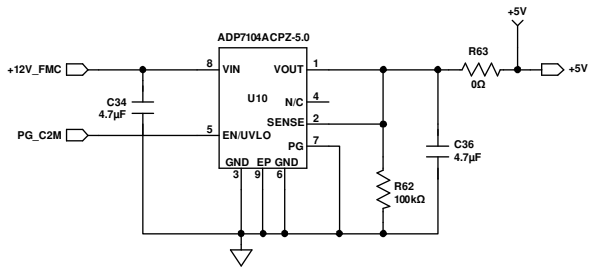
### HARDWARE

If the software does not read any data back,

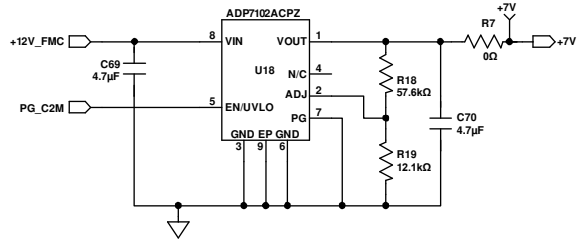
- With the +12 V wall wart plugged in to the [EVAL-SDP-CH1Z](#) board, check to make sure that the voltage applied is within the ranges shown in Table 3.
- Using a DMM, measure the voltage present at +12 V and the VADJ test points, which should read +12 V and 2.5 V, respectively. The +12V\_FMC LED of the [EVAL-AD7961FMCZ](#) board and LEDs of the [EVAL-SDP-CH1Z](#) board (FMC\_PWR\_GO, SYS\_PWR, FPGA\_DONE, BF\_POWER, LED0, and LED2) should all be lit.
- Launch the software and read the data. If nothing happens, exit the software.
- Remove the +12 V wall wart and USB from the [EVAL-SDP-CH1Z](#) board and then reconnect them and relaunch the software.
- If this is not successful, confirm that the [EVAL-AD7961FMCZ](#) and [EVAL-SDP-CH1Z](#) boards are connected together so that the [EVAL-AD7961FMCZ](#) is recognized in the **Device Manager**, as shown in Figure 7.

Note that when working with the software in standalone/offline mode (no hardware connected), if you later choose to connect hardware, first close and then relaunch the software.

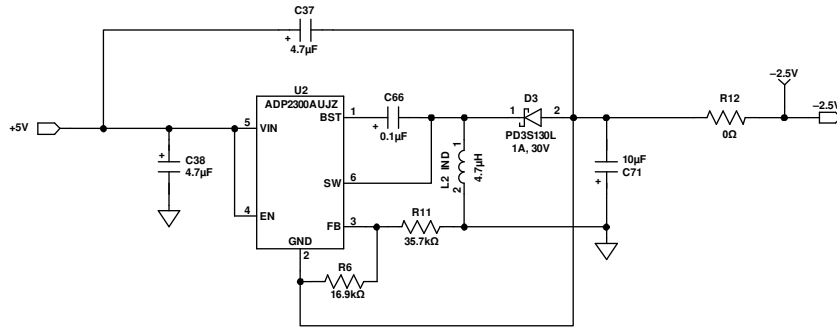
EVALUATION BOARD SCHEMATICS AND ARTWORK



VIN = +12V, VOUT = +5V, IOU = UP TO 500mA



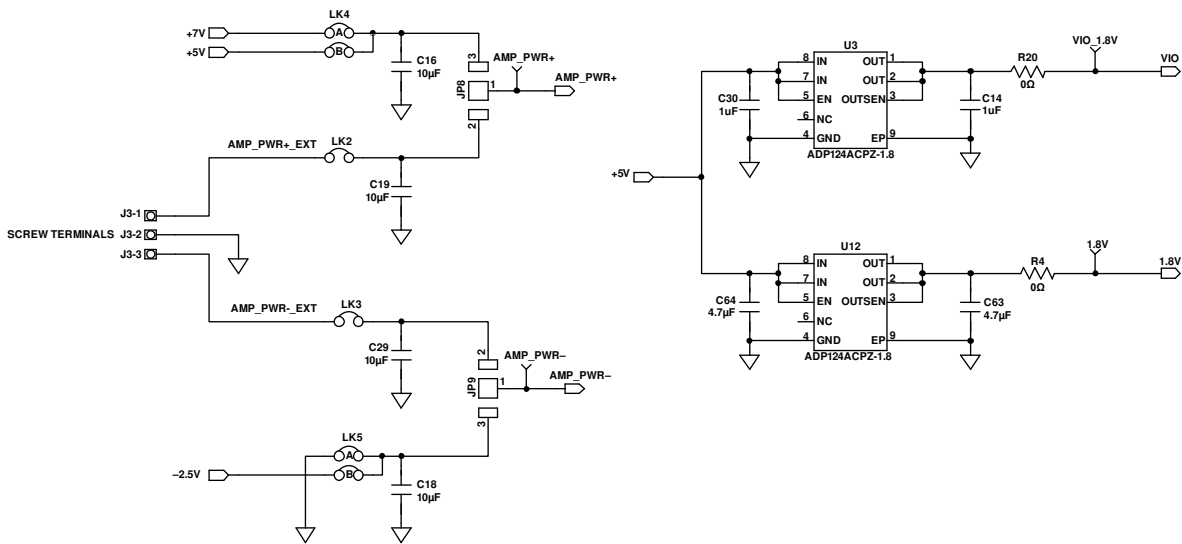
VIN = +12V, VOUT = +7V, IOU = UP TO 300mA



VIN = +5V, VOUT = -2.5V, IOU = 250mA

Figure 24. Schematic Page 1

11696-024



OP-AMP POWER SUPPLY OPTIONS

THE ADP124 IS AVAILABLE IN 2mm x 2mm LFCSF PACKAGES.

Figure 25. Schematic Page 2

11696-025

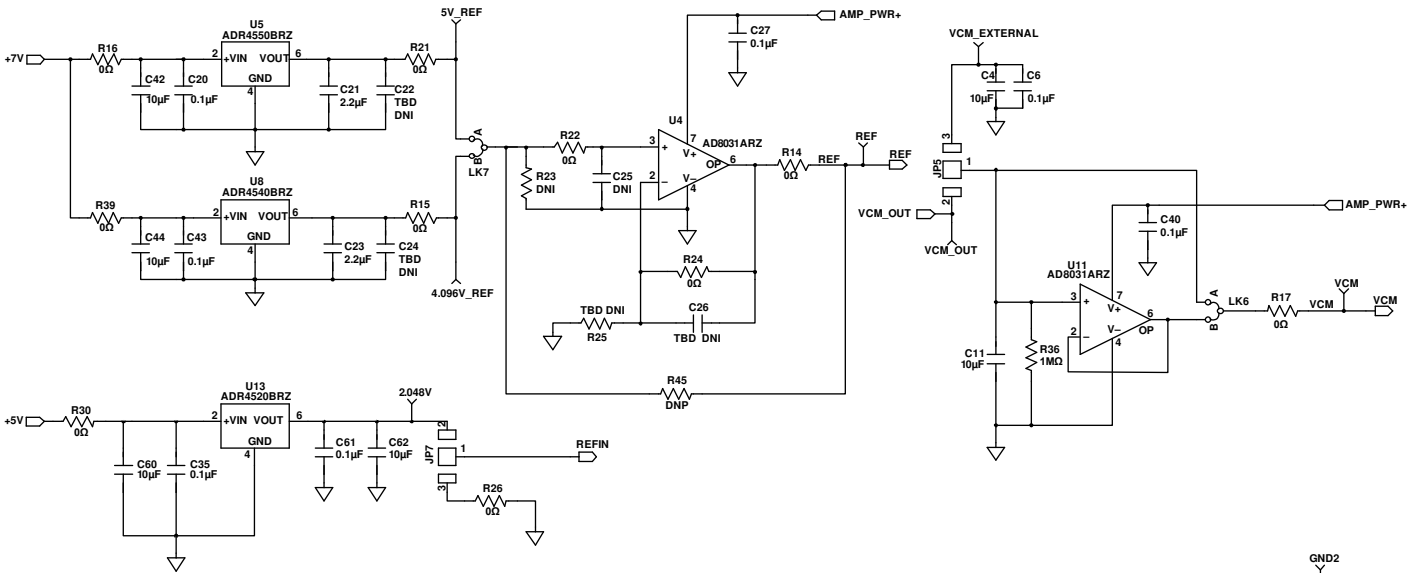


Figure 26. Schematic Page 3

THERE ARE 3 OPTIONS FOR USING AN EXTERNAL REFERENCE:  
 1) EXTERNALLY BUFFERED REFERENCE SOURCE OF 5V APPLIED TO THE REF PIN.  
 2) EXTERNALLY BUFFERED REFERENCE SOURCE OF 4.096V APPLIED TO THE REF PIN.  
 3) EXTERNAL REFERENCE OF 2.048V APPLIED TO THE REFIN PIN (HIGH IMPEDANCE INPUT). THE ON-CHIP BUFFER GAINS THIS BY 2 AND DRIVES THE REF PIN WITH 4.096V.

GND2

11696-026

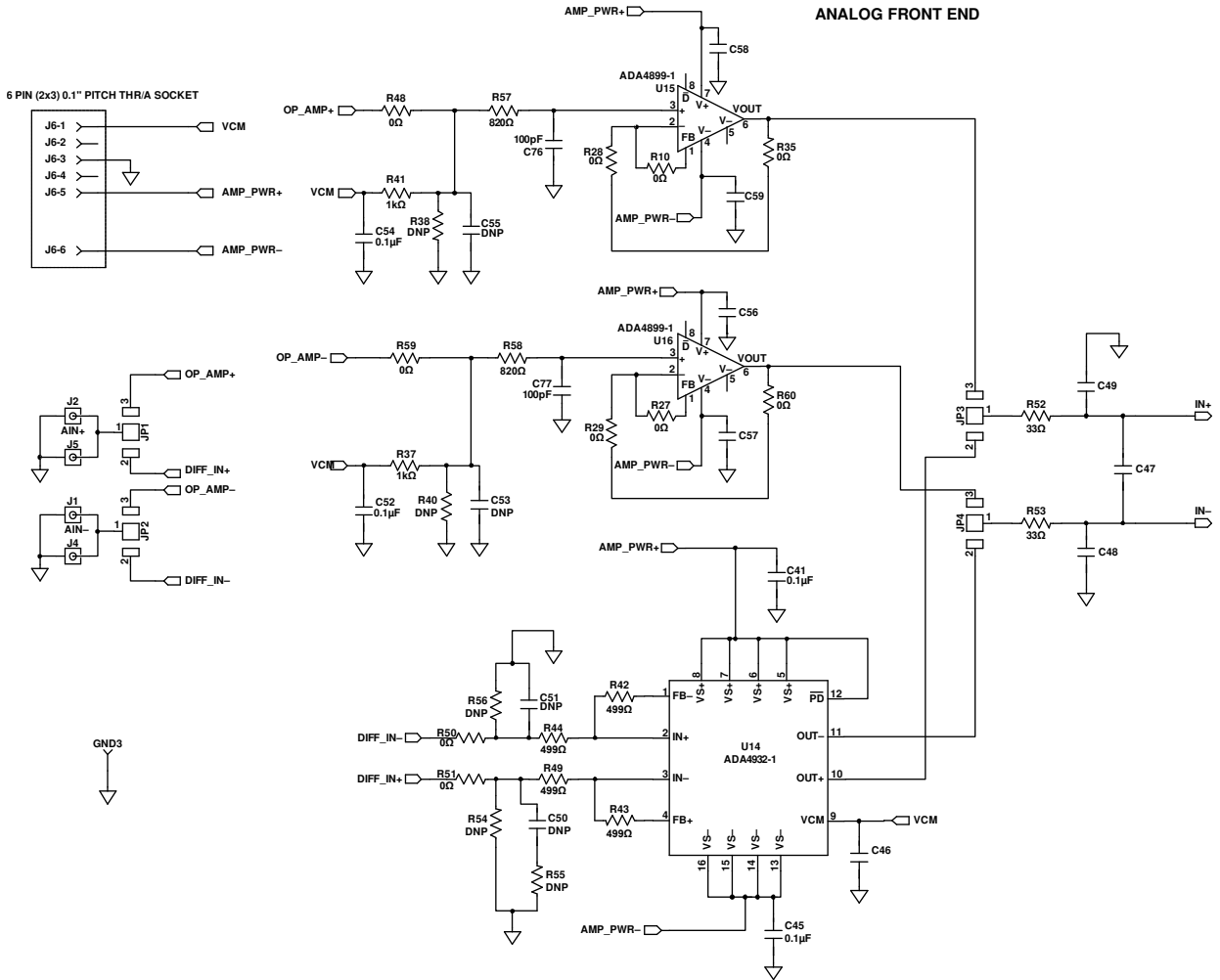


Figure 27. Schematic Page 4

11696-027

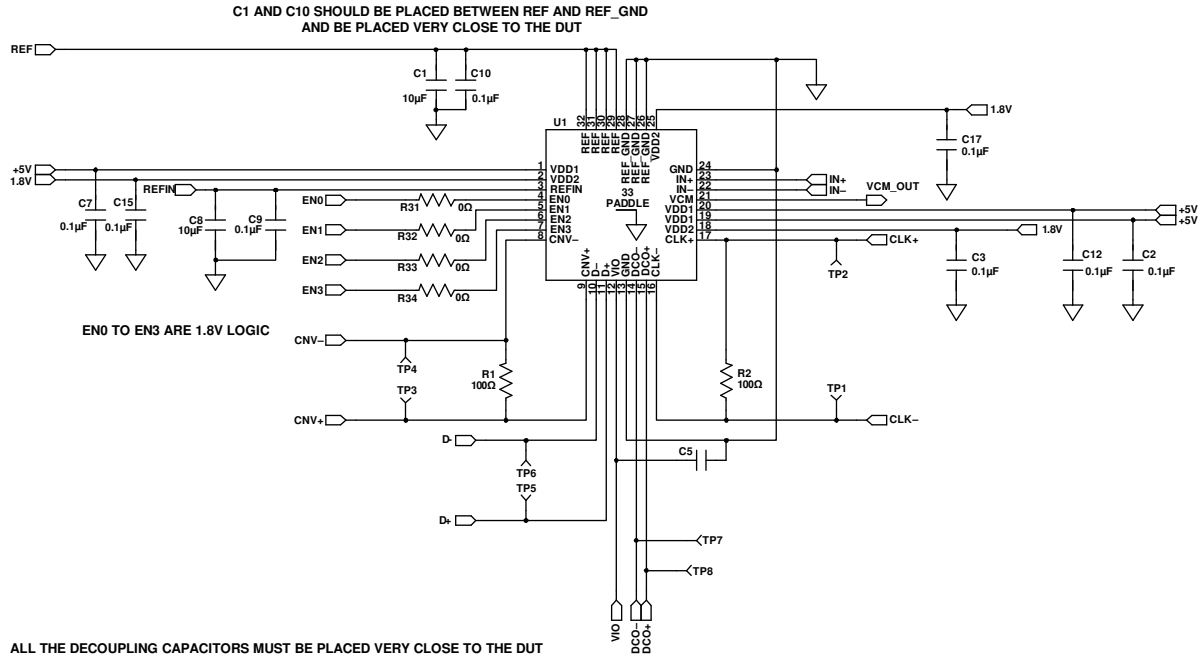


Figure 28. Schematic Page 5

11696-028

FMC-LPC MALE CONNECTOR

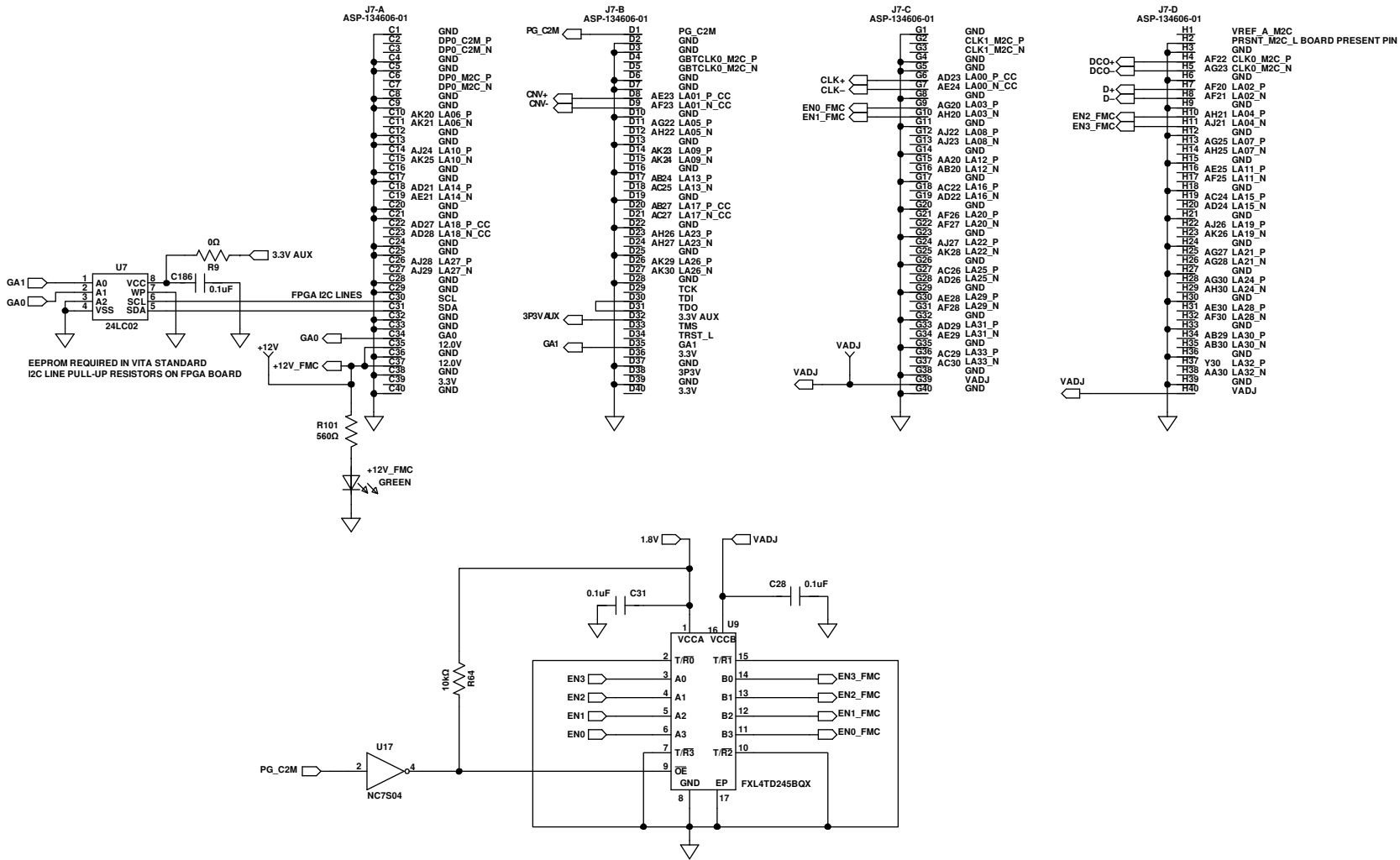


Figure 29. Schematic Page 6

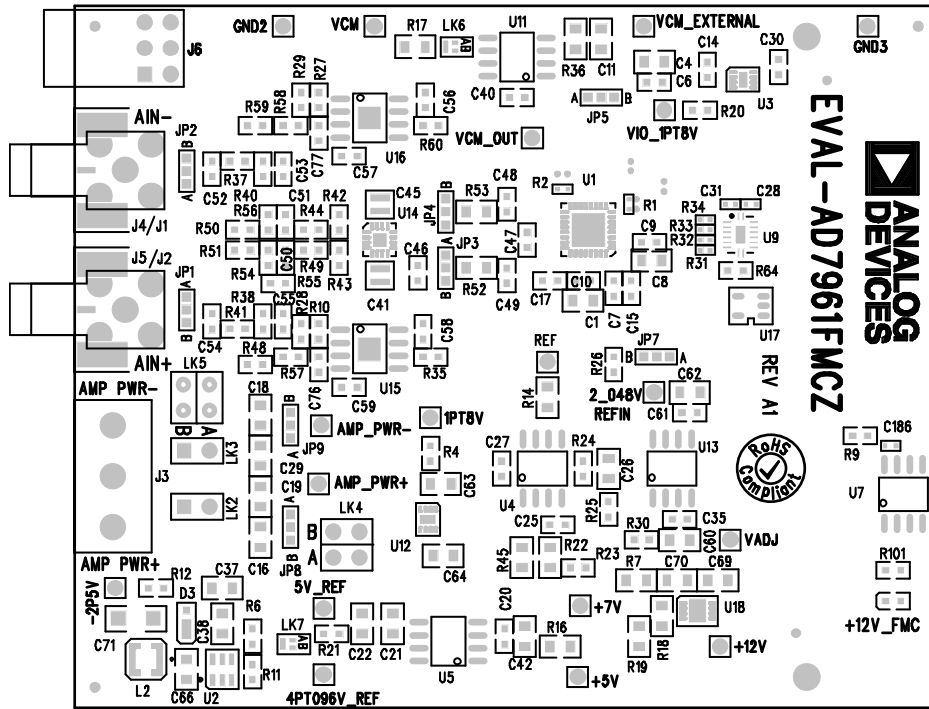


Figure 30. EVAL-AD7961FMCZ Evaluation Board Silkscreen—Top Assembly

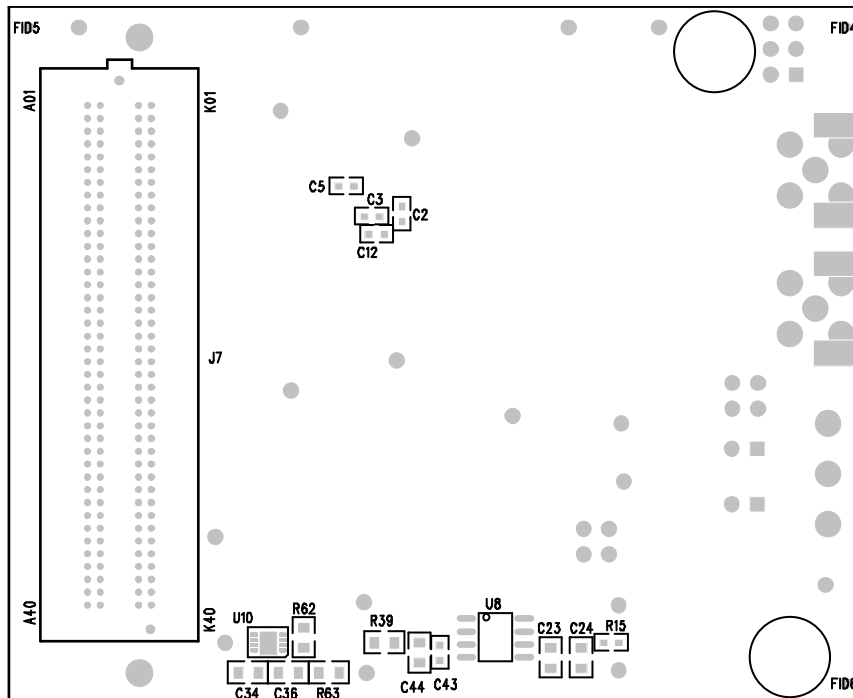
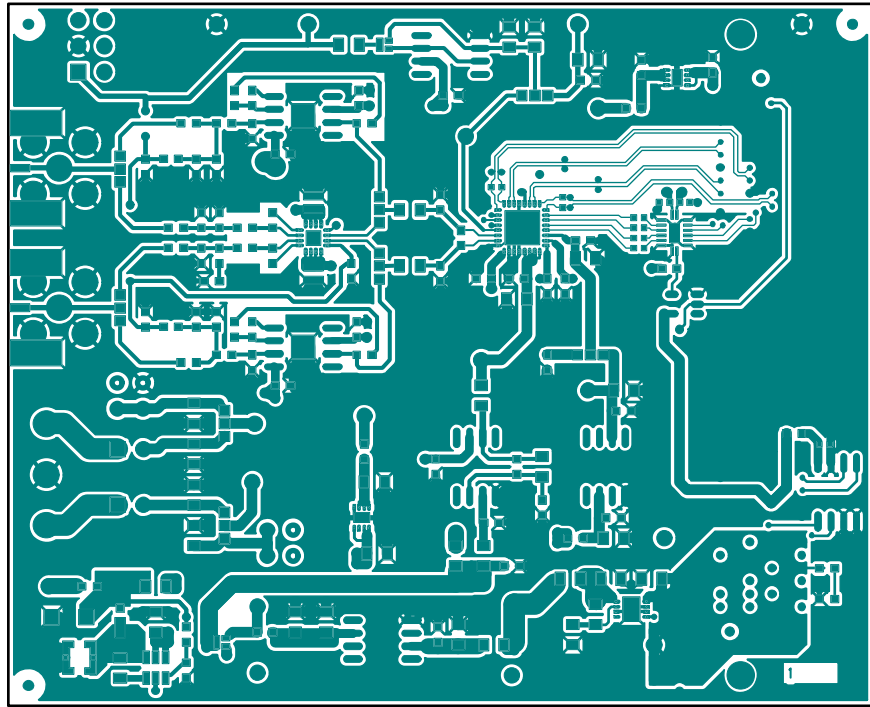
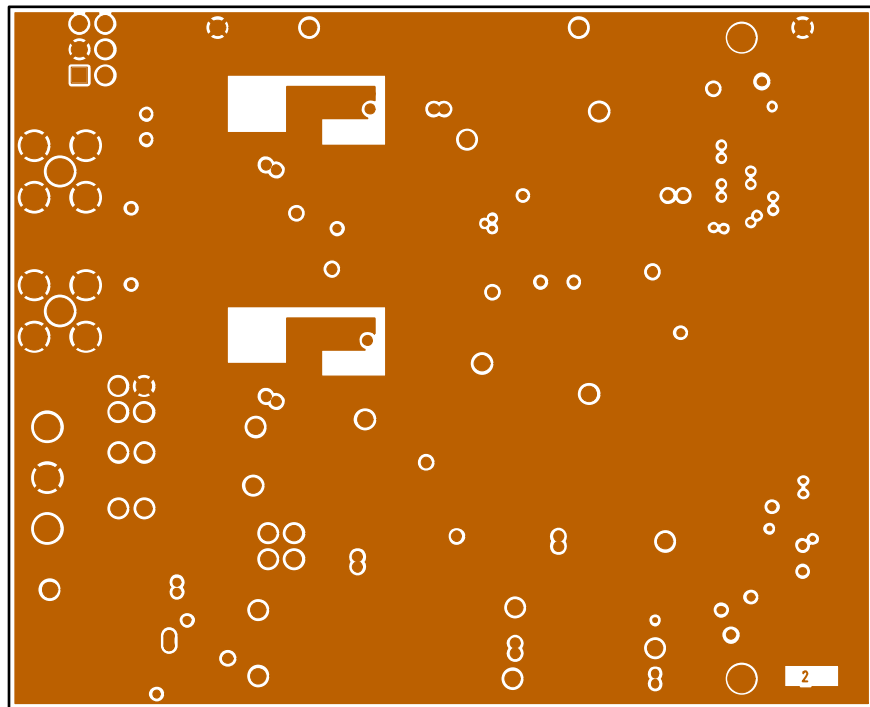


Figure 31. EVAL-AD7961FMCZ Evaluation Board Silkscreen—Bottom Assembly



11696-032

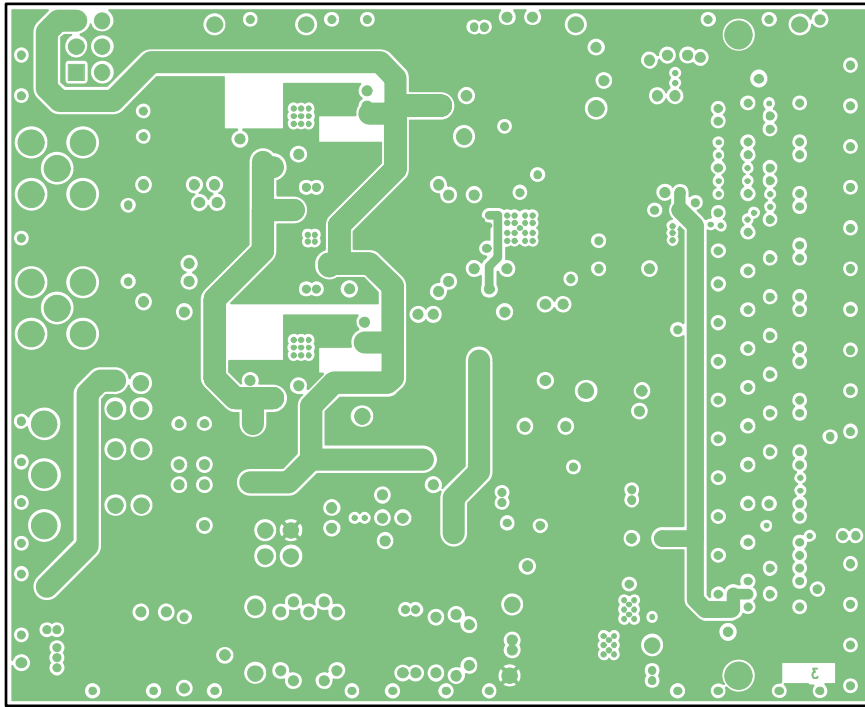
Figure 32. EVAL-AD7961FMCZ Evaluation Board—Top Layer



11696-033

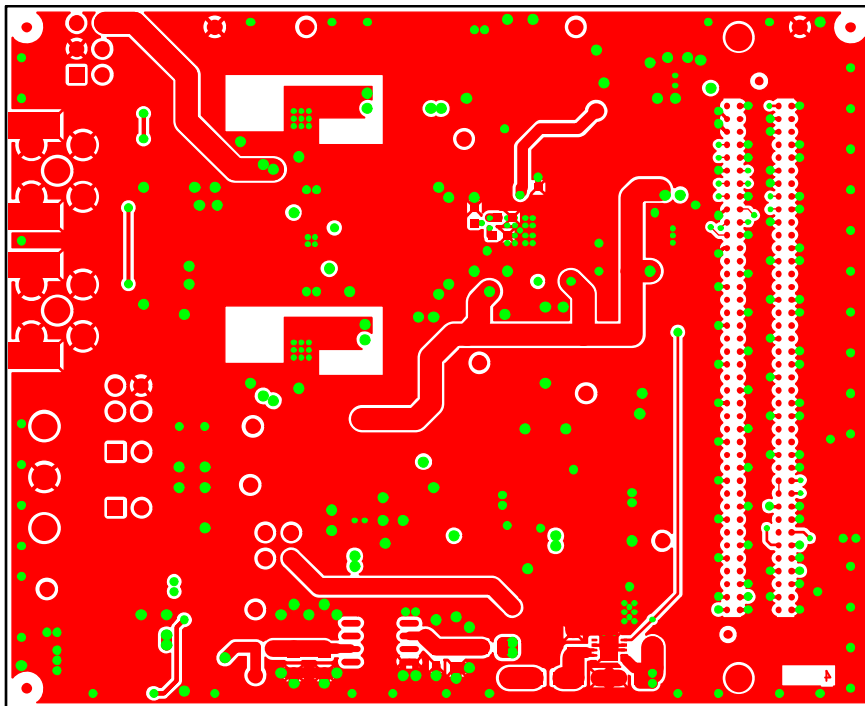
Figure 33. EVAL-AD7961FMCZ Evaluation Board Layer 2—Ground





11696-034

Figure 34. EVAL-AD7961FMCZ Evaluation Board Layer 3—Power



11696-035

Figure 35. EVAL-AD7961FMCZ Evaluation Board Bottom Layer

## BILL OF MATERIALS

Table 4.

Name	Part Description	Manufacturer	Part Number	Stock Code
U1	16-bit, 5 MSPS, PulSAR differential ADC	Analog Devices	AD7961BCPZ	AD7961BCPZ
U2	Step-down regulator	Analog Devices	ADP2300AUJZ	ADP2300AUJZ
U3	Adjustable LDO regulator	Analog Devices	ADP124CPZ-1.8	ADP124ACPZ-1.8-R7
U4	Op amp	Analog Devices	AD8031ARZ	AD8031ARZ
U5	Voltage reference	Analog Devices	ADR4550BRZ	ADR4550BRZ
U7	IC, EEPROM serial 2K, 24LC02, SOIC8	Microchip Technology	24LC02B-I/SN	FEC 1196818
U8	Voltage reference	Analog Devices	ADR4540BRZ	ADR4540BRZ
U9	IC translator, dual 4-bit, 16-DQFN	Fairchild Semiconductor	FXL4TD245BQX	Digi-Key FXL4TD245BQXCT-ND
U10	Linear regulator ADJ, 20 V, 300 mA, ultralow noise, CMOS	Analog Devices	ADP7104ACPZ-5.0	ADP7104ACPZ-5.0-R7
U11	Op amp	Analog Devices	AD8031ARZ	AD8031ARZ
U12	Adjustable LDO regulator	Analog Devices	ADP124ACPZ-1.8	ADP124ACPZ-1.8-R7
U13	Voltage reference	Analog Devices	ADR4520BRZ	ADR4520BRZ
U14	Differential ADC driver	Analog Devices	ADA4932-1	ADA4899-1YCPZ-R2
U15	Low noise, high speed amplifier for 16-bit systems	Analog Devices	ADA4899-1	ADA4899-1YRDZ
U16	Low noise, high speed amplifier for 16-bit systems	Analog Devices	ADA4899-1	ADA4899-1YRDZ
U17	Single INV	Fairchild	NC7504	FEC 1013809
U18	Linear regulator ADJ, 20 V, 300 mA, ultralow noise, CMOS	Analog Devices	ADP7102ACPZ	ADP7102ACPZ-R7
C1, C4, C8, C11, C16, C18, C19, C29, C42, C44, C60, C62	Capacitor, 0805, 10 $\mu$ F, 16 V, 10%	Murata	GRM219R61C106-KA73D	FEC 1845747
C2, C3, C5, C6, C7, C9, C10, C12, C15, C17, C20, C27, C28, C31, C35, C40, C41, C43, C45, C46, C52, C54, C56 to 59, C61	MLCC, 0603, X7R, 50 V, 0.1 $\mu$ F, 10%	Multicomp	MCCA000255	FEC 1759122
C14, C30	Capacitor, ceramic, 1 $\mu$ F, 10 V, X7R, 0603, 10%	TAIYO YUDEN	LMK107B7105KA-T	FEC 1683674
C21, C23	Capacitor, ceramic, 2.2 $\mu$ F, 16 V, X7R, 0805, 10%	TAIYO YUDEN	EMK212B7225KG-T	FEC 1683654
C34, C36 to 38, C63, C64, C69, C70	Capacitor, ceramic, 4.7 $\mu$ F, 16 V, X7R, 0805, 10%	TAIYO YUDEN	EMK212B7475KG-T	FEC 1853520
C22, C24 to 26, C47, C50, C51, C53, C55	SMD capacitor, 10%	TAIYO YUDEN	-	Do not place
C41, C45	Capacitor, 0508, 0.1 $\mu$ F, 25 V, X7R, $\pm$ 20%	Murata	LLL216R71E104MA01L	FEC 1294646
C48, C49	MLCC, 0603, NP0, 50 V, 56 pF, 5%	Multicomp	MCCA000201	FEC 1759063
C66	Capacitor, 0805, 0.1 $\mu$ F, 50 V, X7R, 10%	Kemet	C0805C104K5RACTU	FEC 1414664
C71	Capacitor, ceramic, 10 $\mu$ F, 16 V, X7R, 1206, 10%	TDK	C3216X7R1C106M	FEC 1844317
C76, C77	Capacitor, 0603, 100 pF, 50 V, 10%	YAGEO (Phycomp)	CC0603KRX7R9BB101	FEC 722110