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ANALOG DEVICES

EVAL-ADAS3022EDZ User Guide

UG-484

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluation Board for the ADAS3022 16-Bit, 8-Channel, 1 MSPS Data Acquisition System

FEATURES

Full-featured evaluation board for the ADAS3022
Versatile analog signal conditioning circuitry
On-board reference, clock oscillator, and buffers
Converter evaluation and development board (EVAL-CED1Z) compatible
PC software for control and data analysis (time and frequency domain)

KIT CONTENTS

EVAL-ADAS3022EDZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

EVAL-CED1Z board
Precision signal source
World-compatible 7 V dc supply (enclosed with EVAL-CED1Z)
USB cable

EVALUATION BOARD DESCRIPTION

The EVAL-ADAS3022EDZ is an evaluation board for the ADAS3022 16-bit data acquisition system (DAS). This device integrates an 8-channel multiplexer, a high impedance programmable gain instrumentation amplifier (PGIA) stage with a high common-mode rejection, a precision 16-bit successive approximation (no latency) analog-to-digital converter and precision 4.096 V reference offering an aggregate throughput of 1 million samples per second (1 MSPS).

The evaluation board is designed to demonstrate the performance of the ADAS3022 and to provide an easy-to-understand interface for a variety of system applications. A full description of this product is available in the data sheet and should be consulted when utilizing this evaluation board.

The evaluation board is intended to be used with the Analog Devices, Inc., converter evaluation and development (CED) board, EVAL-CED1Z, a USB-based capture board connected to P4, the 96-pin interface.

On-board components include a high precision, buffered band gap 4.096 V reference (ADR434), reference buffers (AD8032), passive signal conditioning circuitry, and an FPGA for deserializing the serial conversion results and configuring the ADAS3022 via a 4-wire serial interface.

The P3 connector allows users to test their own interface with or without the optional Altera FPGA, U6 (programmed using the P2 and passive serial EEPROM, U5).

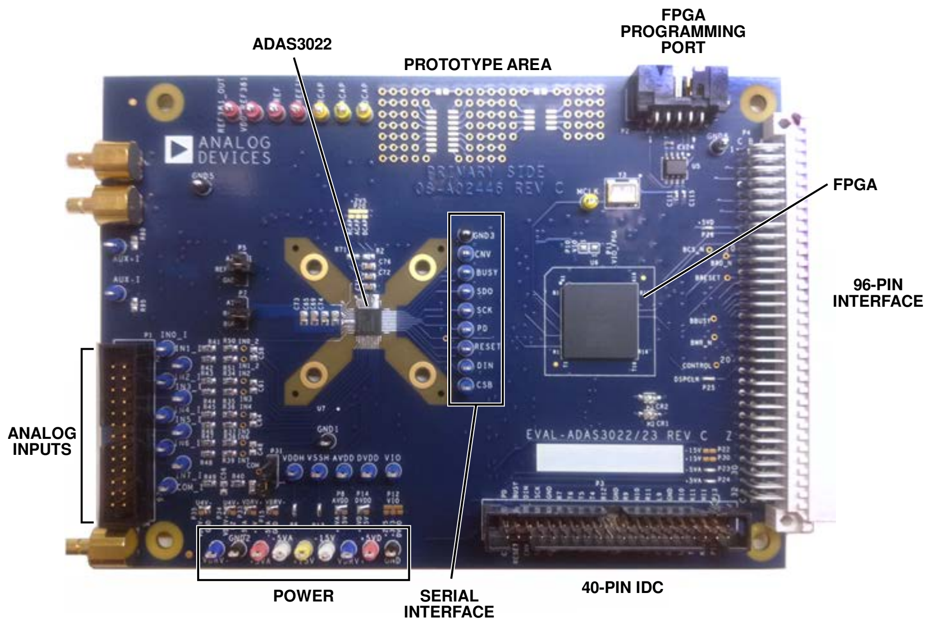

Figure 1. EVAL-ADAS3022EDZ Evaluation Board

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EVALUATION BOARD HARDWARE

OVERVIEW

The EVAL-ADAS3022EDZ evaluation board is designed to offer a simple evaluation of these revolutionary devices. From a block diagram perspective, the board uses a set of analog input test points (or an IDC header), some passive footprints for RC filtering and external reference, the ADAS3022 device, a serial interface to the on-board FPGA, and power that can be supplied locally or via EVAL-CED1Z or externally. Note that the ADAS3022 devices also have an on-chip reference; however, external circuitry is provided for users wanting to test other suitable options.

The small prototyping area can be useful for building additional circuitry, if desired. Each block has a specific function as defined in the following sections.

DEVICE DESCRIPTION

The ADAS3022 is a complete data acquisition system (DAS) on a single chip that is capable of converting up to 1 MSPS and can resolve 8 single-ended inputs or 4 fully differential inputs up to ±24.576 V when using ±15 V supplies. It can accept the commonly used bipolar differential, bipolar single-ended, pseudo bipolar, or pseudo unipolar input signals as shown in Table 1 thus allowing the use of almost any direct sensor interface.

The ADAS3022 is an ideal replacement for a typical 16-bit 1 MSPS precision data acquisition system that simplifies the design challenges by eliminating signal buffering, level shifting, amplification/attenuation, common-mode rejection, settling time, or any of the other analog signal conditioning challenges while allowing smaller form factor, faster time to market, and lower costs.

Data communication to and from the ADAS3022 occurs asynchronously without any pipeline delay using a common 4-wire serial interface compatible with SPI, FPGA, and DSP.

A rising edge on CNV samples the differential analog inputs of a channel or channel pair. The ADAS3022 configuration register allows the user to configure the number of enabled channels, the differential input voltage range, and the interface mode using the evaluation board and software as detailed in this user guide. Complete specifications for the ADAS3022 are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details on the EVAL-CED1Z are available on the Analog Devices website.

Table 1. Typical Input Range Selection

Signals	Input Range, V_{IN} (V)
Differential	
±1 V	±1.28 V
±2.5 V	±2.56 V
±5 V	±10.24 V
±10 V	±20.48 V
Single Ended[1]	
0 V to 1 V	±0.64 V
0 V to 2.5 V	±1.28 V
0 V to 5 V	±2.56 V
0 V to 10 V	±5.12 V

[1] V_{CM} adjusted to half the maximum input voltage.

JUMPERS, SOLDER PADS, AND TEST POINTS

Numerous solder pads and test points are provided on the evaluation board and are detailed fully in Table 4, Table 5, and Table 6. Note the nomenclature for this evaluation board for a signal that is also connected to an IDC connector would be signal_I. The two 3-pin user selectable jumpers are used for the ADCs reference selection and are fully described in the Reference section.

ANALOG INTERFACE

The analog interface is provided with test points for each of the analog inputs IN[7:0] and COM (that is, IN0_I is common to both the test point and to P1). The passive device footprints can be used for filtering, if desired. A simple RC filter made up of 22 Ω and 2700 pF NPO capacitors is provided. Note that the use of stable dielectric capacitors, such as NPO or COG, is required in the analog signal path to preserve the ADAS3022 distortion. Using X5R or other capacitors in the analog signal path greatly reduces the performance of the system. Also, note that many bench top arbitrary waveform generators (AWGs) use 12-bit or 14-bit digital-to-analog converter outputs such that the 16-bit ADAS3022 devices digitize this directly resulting in erroneous looking data. If such an AWG is used, a high-order band-pass filter should be used to filter the unwanted noise from these sources.

The ADAS3022 COM input can be routed to P1 or GND using P31. Set the jumper across Pin 1 and Pin 2 to route to P1. Set the jumper across Pin 2 to Pin 3 to GND COM. This is useful for single-ended applications.

For dynamic performance, an FFT test can be done by applying a very low distortion ac source, such as an Audio Precision System 2702. This source can be set for balanced or unbalanced, and can be floated or grounded depending on the user's choice.

FPGA

The on-board FPGA performs a number of digital functions, one of them being the sample rate conversion controlled using the software. Another function is deserializing the serial conversion results as the CED data capture board uses a 16-bit parallel interface. If desired, the deserialized data can be monitored on the 96-pin edge connecter P1, BD[15:0]. The CED uses a buffered busy signal, BBUSY, as the general interrupt for the data transfer to the CED board.

The FPGA also provides the necessary ADAS3022 asynchronous control signals for RESET and power down (PD).

The signals from the FPGA to the ADAS3022 can be bypassed by modifying the default solder pad connections. As shown in Figure 2, each digital signal on the ADAS3022 is connected to the larger (top) pad of the three. The default configuration is the small pad and larger pad (no text) which connects the FPGA to the ADAS3022 (CNV, BUSY, and SDO signals shown). The labeled pads, CNV_I, BUSY_I, SDO_I, and so on, are the signals that are routed to P3. To use P3 instead of the FPGA, unsolder the default connections and resolder from the large pad to the xxx_I pads. The FPGA will remain powered; however, if all the signals are bypassed in this fashion, it will not have any influence on the ADAS3022.

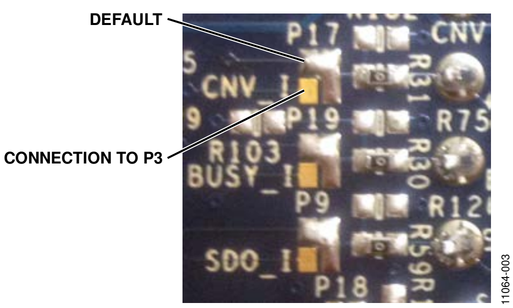


Figure 2. Digital Interface Solder Pads—Partial View

Serial Interface

The 4-wire serial interface consisting of $\overline{CS}$, DIN, SCK, and SDO is present on the digital interface test points and is controlled by the FPGA. The FPGA can be bypassed by using the solder pads.

REFERENCE

The ADAS3022 has an internal 4.096 V reference, along with an internal buffer, useful for using an external reference or one can use an external 4.096 V reference directly, such as the ADR434 provided on the evaluation board. The evaluation board can be configured to use any of these references. Two jumpers (P5 and P9) are used for setting the reference in conjunction with software control.

External Reference–Factory Configuration

The evaluation board includes the ADR434, A1, which is a 4.096 V precision voltage reference. This reference can drive the ADC REF1 or REF2 (REFx) pin directly or it can also be buffered with U20, the AD8032; both of these are set to the factory default setting.

Table 2. Factory Reference Jumper Configuration

Jumper	Setting
P5	REFIN to GND[1]
P9	REF to BUF (U20)

[1] The connection is made through R102 = 10 k to GND.

To use another reference source, there are two methods:

- For an external unbuffered reference, remove the P9 jumper and connect a source to the REF test point.
- Since the ADR434 is a standard 8-lead SOIC, it can also be removed and replaced with the user's reference. In this case, the user reference and the U20 AD8032 buffer can be used as a reference source.

Internal 4.096 V Reference

The ADC has an internal 4.096 V precision reference and can be used on most applications. When enabled, 4.096 V will be present on the ADAS3022 REFx pin and test point, REF. In addition, a voltage will also be present on the ADAS3022 REFIN pin and test point, REFIN. The voltage present on REFIN can be used for other purposes, such as to provide the bias voltage; however, it would need a suitable buffer as the output impedance of the REFIN is on the order of a few kilo ohms and loading this voltage down will degrade the internal reference's performance.

Table 3. Internal Reference Jumper Configuration

Jumper	Setting
P5	Open
P9	Open

Note that the ADAS3022 configuration register needs to be updated either using the included software or by writing the appropriate bits to enable the internal reference.

Internal Reference Buffer

The internal reference buffer is useful when using an external 2.5 V reference. When using the internal reference buffer, applying 2.5 V to REFIN, which is directly connected to the ADC's REFIN pin, produces 4.096 V at the ADCs REFx pin and REF test point.

Note that the ADAS3022 configuration register needs to be updated either using the included software or by writing the appropriate bits to enable the internal reference buffer.

POWER SUPPLIES AND GROUNDING

The on-board ADP3334 low dropout regulators are provided for 2.5 V, 3.3 V, and 5 V and also for the FPGA I/O supply which is user configurable and set to 3.3 V by default. The FPGA core is supplied by a pair of ADP1715 devices set for 1.2 V. Additional power is supplies via the CED board for an alternative +5 V analog and digital 3.3 V/5 V digital through P4.

The ADAS3022 device also requires ±15 V supplies for VDDH and VSSH. These must be supplied by the user using a standard lab supply ensuring that the return paths are at the same potential. Refer to CN-0201 for the complete information on generating these ±15 V supplies from a +5 V single supply. The differential input common-mode voltage (VCM) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). In other words, the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies.

The evaluation board ground plane consists of a solid plane on one PCB layer shared on another layer with the power plane. To attain high resolution performance, the board was designed to ensure that all digital ground return paths do not cross the analog ground return paths, that is, all analog on one side and digital on the other.

EVALUATION BOARD SCHEMATICS/PCB LAYOUT

The evaluation board is a 6-layer board carefully laid out and tested to demonstrate the specific high accuracy performance of the ADAS3022 devices. The Evaluation Board Schematics and Artwork section of this user guide shows the schematics of the evaluation board.

BASIC HARDWARE SETUP

The ADAS3022 evaluation board connects to the EVAL-CED1Z converter evaluation and demonstration board. The EVAL-CED1Z board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 3 shows a photograph of the connections made between the ADAS3022 daughter board and the EVAL-CED1Z board.

1. Before connecting power, ensure that the EVAL-ADAS3022EDZ and the EVAL-CED1Z boards are connected firmly together.
2. Connect the power supplies on the EVAL-ADAS3022EDZ board. The EVAL-ADAS3022EDZ requires external power supplies of ±15 V. Connect them from a bench top power supply.
3. Connect the EVAL-CED1Z board to the PC via the USB cable enclosed in the EVAL-SDPCB1Z kit. If using a Windows® XP platform, you may need to search for the EVAL-CED1Z drivers. Choose to automatically search for the drivers for the EVAL-CED1Z board if prompted by the operating system.
4. Proceed to the Software Installation section to install the software. Note that the EVAL-CED1Z board must not be connected to the PC's USB port until the software is installed. The 7 V dc supply can be connected, however, to check that the board has power (green LED lit).

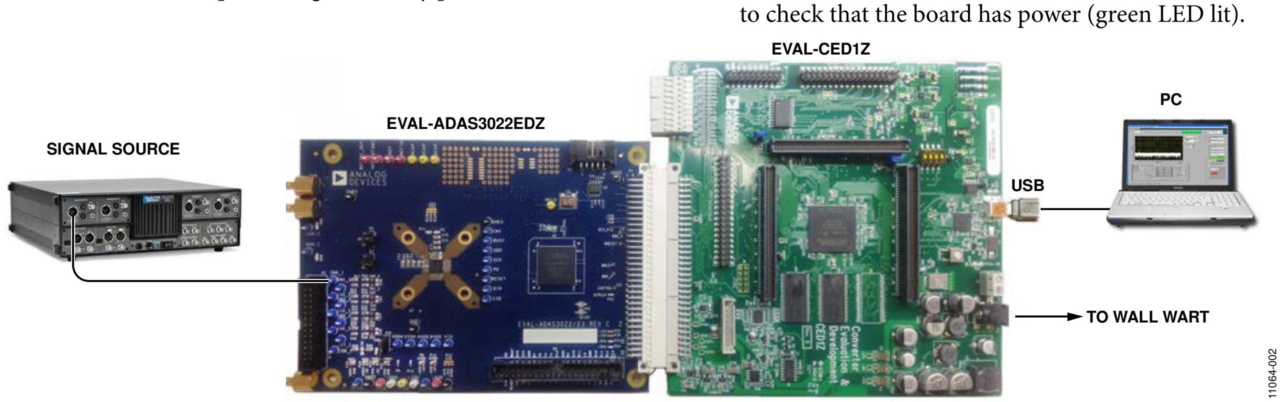


Figure 3. Hardware Configuration—Setting up the EVAL-ADAS3022EDZ

JUMPERS AND TEST POINTS

Three-pin jumpers are used to configure the ADC reference. Refer to the Reference section for further details and settings.

Table 4. Pin Jumper Descriptions

Jumper	Default	Function
P5	REFIN to GND	REFIN Select. Buffered reference input selection. Use in conjunction with P7. Note that the ADAS3022 REFx pin and any other circuit traces/test points will produce 4.096 V when using the buffered reference configuration; P7 must be left in the open position. REFIN to A2: Uses the on-board ADR381, A2 (2.5 V) reference. The ADAS3022 must use the buffered reference configuration. REFIN to GND: Disables the ADAS3022 internal reference. The ADAS3022 must use the full external reference configuration. Open: For use either when using the ADAS3022 on-chip reference or when applying an external 2.5 V source. When using the on chip reference, a voltage is present on Pin 2 and any other circuit traces/test points. When using an external source, the ADAS3022 must use the buffered reference configuration.
P7	REF to BUF	REF Select. External 4.096 V reference input selection. Use in conjunction with P5. Note that the ADAS3022 REFIN pin and any other circuit traces/test points produce 2.5 V when using the internal or external reference configuration and P5 must be left in the open position. REF to A1: Uses the on-board ADR434, A1 (4.096 V), reference. The ADAS3022 must use the external reference configuration. REF to BUF: Uses the on-board ADR434 followed by the AD8032, U20 unity gain buffer. This allows some adjustment to the reference voltage by use of some resistors around the AD8032. The ADAS3022 must use the external reference configuration. Open: For use when using the ADAS3022 on-chip reference or an externally applied source connected directly to Pin 2 or the REF test point.
P31	COM to PIN 1	COM Input Select. Center pin connected to ADAS3022 COM pin. Center pin to PIN1 routes COM to P1. Center to PIN3 routes COM to GND.

Solder pads jumpers are factory configured and can be changed by the user.

Table 5. Analog and Digital Solder Pads Descriptions

Jumper	Name	Default	Function
P9	SDO	1 to 3	SDO Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P34.
P16	DIN	1 to 3	DIN Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P35.
P17	CNV	1 to 3	CNV Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P36.
P18	SCK	1 to 3	SCK Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P33.
P19	BUSY	1 to 3	BUSY Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P37.
P27	RESET	1 to 3	RESET Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P38.
P28	PD	1 to 3	PD Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P39.
P29	$\overline{CS}$	1 to 3	$\overline{CS}$ Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P40.
P25	DSPCLK	Soldered	CED Clock Source.

Table 6. Power Supply Solder Pads

Jumper	Name	Default	Function
P6	VDDH	Soldered	VDDH Supply.
P13	VSSH	Soldered	VSSH Supply.
P8	AVDD	+5VA	AVDD Supply. Selection of +5 V A, analog supply from the CED board or +5 V from U3.
P10	–	Soldered	VIO Supply. This solder pad can be used to power the FPGA VIO and ADAS3022 VIO together.
P11	–	Soldered	FPGA VIO Supply. Supplied from U8, 3.3 V, dedicated digital supply.
P12	VIO	Open	VIO Supply. Selection of 2.5 V (2V5), 3.3 V (3V3), or DVDD (5V). Note that the ADAS3022 digital outputs are set to this level and are directly wired to the FPGA, U6, which is 3.3 V max. When using the 5 V setting, the ADAS3022 outputs, SDO and BUSY must be resistively divided using the 0603 pads provided on the evaluation board. For this reason, P10 is used as the default.
P14	DVDD	+5VD	DVDD Supply. Selection of +5 V digital, +5 V D, and +5 V from U3.
P15	VDRV-	−5VA	U20 V−/P34 Supply. Selection of −5 V A, analog supply from the CED board or GND.
P33	VDRV+	+5VA	U20 V+/P35 Supply. Selection of +5 V A, analog supply from the CED board or +5 V from U3.
P34	U4 V+	VDRV+	U4 V+ Supply. Selection of VDRV+ or U2.
P35	U4 V−	VDRV−	U4 V− Supply. Selection of VDRV− or GND.
P22	−15V	Soldered	−15 V CED Supply.
P23	−5VA	Soldered	−5 V A (Analog) CED Supply.
P24	+5VA	Soldered	+5 V A (Analog) CED Supply.
P26	+5VD	Soldered	+5 V D (Digital) CED Supply.
P30	+15V	Soldered	+15 V (Analog) CED Supply.

Table 7. Test Points (By Signal Type)

Test Point	Type	Description
IN0_I	Analog Input	Path for IN0 Input.
IN1_I	Analog Input	Path for IN1 Input.
IN2_I	Analog Input	Path for IN2 Input.
IN3_I	Analog Input	Path for IN3 Input.
IN4_I	Analog Input	Path for IN4 Input.
IN5_I	Analog Input	Path for IN5 Input.
IN6_I	Analog Input	Path for IN6 Input.
IN7_I	Analog Input	Path for IN7 Input.
COM_I	Analog Input	Path for COM Input.
REF	Analog Input	Direct Connection to ADAS3022 REFx Pin.
REFIN	Analog Input	Direct Connection to ADAS3022 REFIN Pin.
CNV	Digital Input	Direct Connection to ADAS3022 CNV Pin.
BUSY	Digital Output	Direct Connection to ADAS3022 BUSY Pin.
SDO	Digital Output	Direct Connection to ADAS3022 SDO Pin.
SCK	Digital Input	Direct Connection to ADAS3022 SCK Pin.
PD	Digital Input	Direct Connection to ADAS3022 PD Pin.
RESET	Digital Input	Direct Connection to ADAS3022 RESET Pin.
DIN	Digital Input	Direct Connection to ADAS3022 DIN Pin.
CSB	Digital Input	Direct Connection to ADAS3022 $\overline{\text{CS}}$ Pin.
MSCL	Digital Output	Eval Board Master Clock Form Y3, 100 MHz Oscillator.
VDDH	Power	Direct Connection to ADAS3022 VDDH Pin.
VSSH	Power	Direct Connection to ADAS3022 VSSH Pin.
AVDD	Power	Direct Connection to ADAS3022 AVDD Pin.
DVDD	Power	Direct Connection to ADAS3022 DVDD Pin.
VIO	Power	Direct Connection to ADAS3022 VIO Pin.
+5VA	Power	Connected to P24; CED +5 V A.
−5VA	Power	Connected to P23; CED −5 V A.
+15V	Power	Connected to P30; CED +5 V A.
−15V	Power	Connected to P22; CED −5 V A.
+5VD	Power	Connected to P26; CED +5 V D.
GND(s)	Power	Connected to Eval Board GND Plane.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

Close major Windows applications prior to installing the software.

System Requirements

- Windows XP (SP2, 32-bit), Windows Vista (32-bit or 64-bit), or Windows 7 (32-bit or 64-bit)
- USB 2.0 (for CED board)
- Administrator privileges

Website Download

The evaluation board software is available for download from the evaluation board page on Analog Devices website. Click the **setup.exe** file to run the install. The default location for the software is **C:\Program Files (x86)\Analog Devices\ ADAS3022 Evaluation Software**.

Install the evaluation software before connecting the evaluation board and EVAL-CED1Z board to the USB port of the PC to ensure that the evaluation system is correctly recognized when connected to the PC.

There are two parts of the software installation process:

- ADAS3022 evaluation board software installation
- EVAL-CED1Z board driver installation

Figure 4 to Figure 9 show the separate steps to install the ADAS3022 evaluation software, while Figure 10 to Figure 12 show the separate steps to install the EVAL-CED1Z drivers. Proceed through all of the installation steps to allow the software and drivers to be placed in the appropriate locations. Only connect the EVAL-CED1Z board to the PC after the software and drivers are installed.

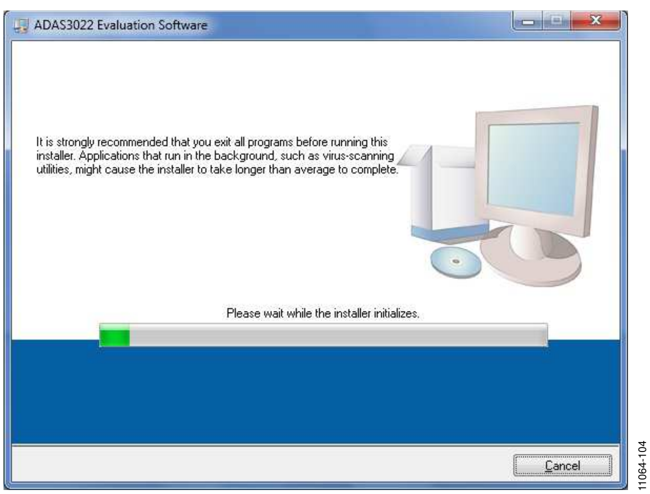


Figure 4. ADAS3022 Evaluation Software Installer

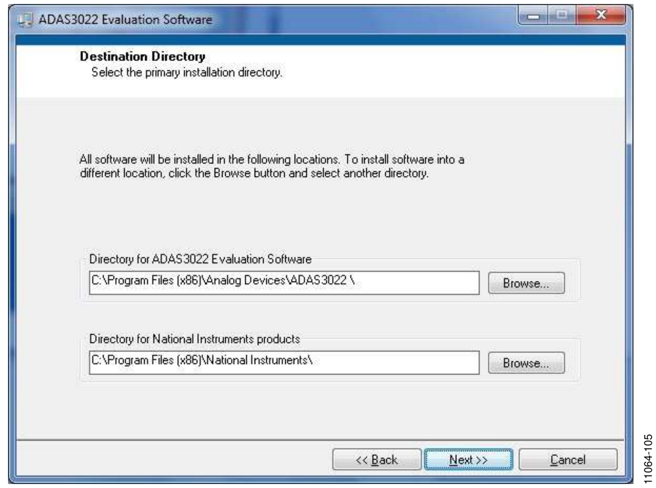


Figure 5. ADAS3022 Evaluation Software Destination Directory

Figure 6. ADAS3022 Evaluation Software License Agreement

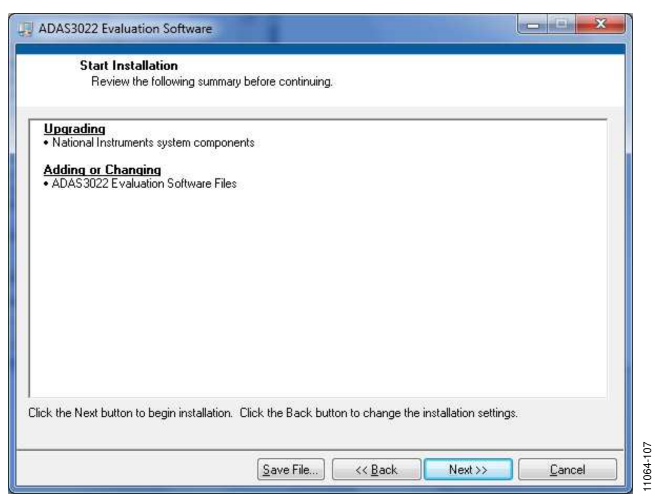


Figure 7. ADAS3022 Evaluation Software Start Installation

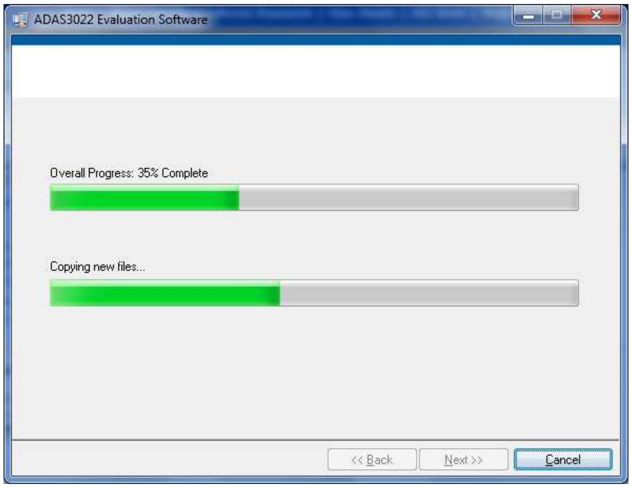


Figure 8. ADAS3022 Evaluation Software, Installation In Progress

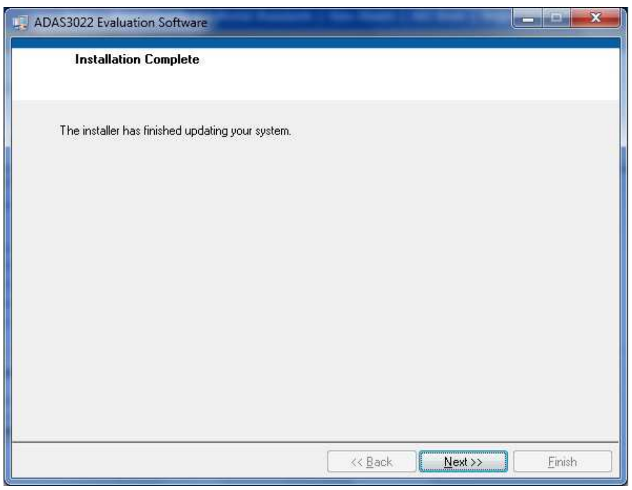


Figure 9. ADAS3022 Evaluation Software Installer, Installation Complete

Figure 10. CED Drivers Install Setup Wizard

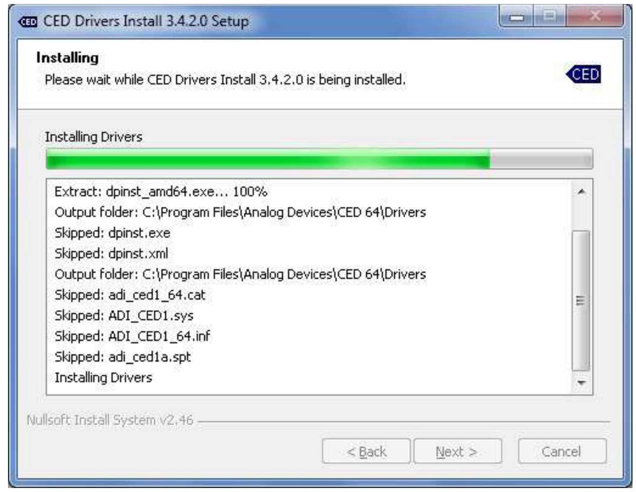


Figure 11. CED Drivers Install Setup Wizard, Installation In Progress

Figure 12. CED Drivers Install Setup Wizard, Installation Completed

Figure 13. Computer Restart Notice

On some PCs, the **Found New Hardware Wizard** may show up. If so, follow the same procedure to install it properly.

The Device Manager can be used to verify that the driver was installed successfully.

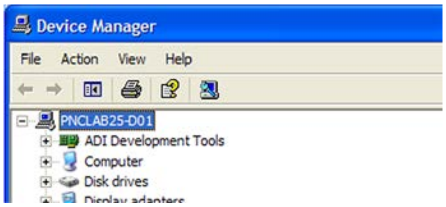


Figure 14. Device Manager

Troubleshooting the Installation

If the driver was not installed successfully, the Device Manager displays a question mark for **Other devices** because Windows does not recognize the EVAL-CED1Z board.

Figure 15. Device Manager Troubleshooting

The USB Device can be opened to view the uninstalled properties.

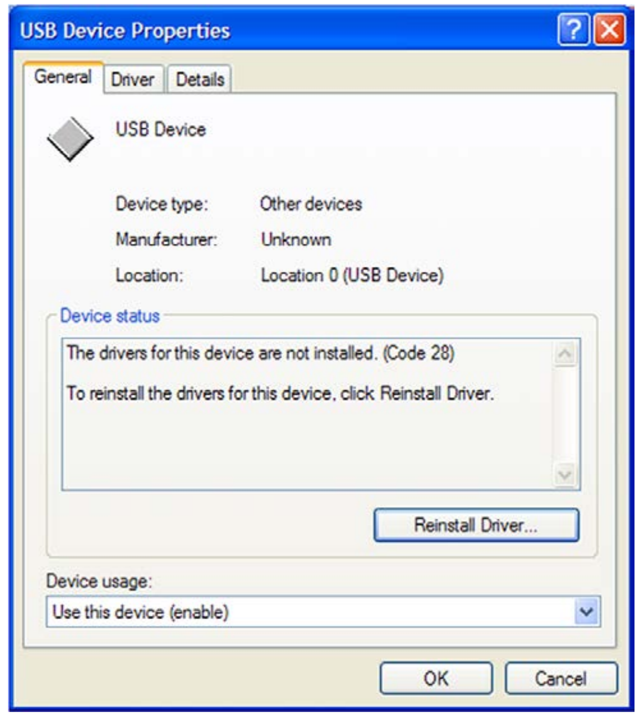
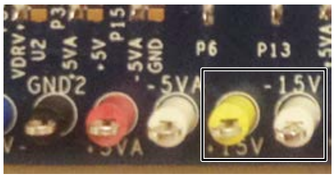


Figure 16. USB Device Properties

This is usually the case if the software and drivers were installed by a user without administrator privileges. If so, log on as an administrator with full privileges and reinstall the software.

POWERING UP THE BOARD

The evaluation board, as configured from the factory, uses the local LDOs for power where necessary. A ±15 V dc lab supply must be connected to the board. Test points (yellow and white) are provided for these external supplies.



11064-009

Figure 17. Test Points

RUNNING THE SOFTWARE WITH THE HARDWARE CONNECTED

The evaluation board includes software for analyzing the ADAS3022. The EVAL-CED1Z is required when using the software. The software is used to perform the following tests:

- Histogram tests for determining code transition noise (dc)
- Time domain analysis
- Fast Fourier transforms (FFT) for signal-to-noise ratio (SNR), SNR and distortion (SINAD), total harmonic distortion (THD), and spurious free dynamic range (SFDR)

This evaluation software should be located at **<local_drive>:\Program Files\Analog Devices\ADAS3022 Evaluation Software**.

In order to launch the software, click **Start>All Programs> Analog Devices\ADAS3022 Evaluation Software**. You can then apply the signal source and capture the data.

To uninstall the program, click **Start**>**Control Panel**>**Add or Remove Programs**>**Analog Devices ADAS3022 Evaluation Software.**

Refer to Figure 18 to Figure 31 for further details and features of the software.

SOFTWARE OPERATION

This section describes the full software operation and all windows that appear. When the software is launched, the panel opens and the software searches for hardware connected to the PC. The user software panel launches, as shown in Figure 18. The labels listed in this section correspond to the numbered labels in Figure 18.

File Menu (Label 1)

The **File** menu, labeled 1 in Figure 18, provides the following:

- **Save Captured Data** saves data to a .csv file.
- **Take Screenshot** saves the current screen.
- **Print** prints the window to the default printer.
- **Exit** quits the application.

Edit Menu (Label 2)

The **Edit** menu, labeled 2, provides the following:

- **Initialize to Default Values**: This option resets the software to its initial state.

Help Menu (Label 3)

The **Help** menu, labeled 3, offers help from the following sources:

- **Analog Devices website**
- **User Guide**
- **Context Help**
- **About**

Throughput (Label 4)

The default throughput (sampling frequency) is 1,000 samples per second (SPS). The ADAS3022 is capable of operating a maximum sample frequency up to 1,000 kSPS.

Samples (Label 5)

Select the number of **Samples** to analyze when running the software. This number is limited to 65,536 samples.

Single Capture (Label 6) and Continuous Capture (Label 7)

Single Capture performs a single capture, whereas **Continuous Capture** performs a continuous capture from the ADC.

Tabs

There are four tabs available for displaying the data in different formats.

- Time Domain
- Histogram
- Spectrum
- Summary

To exit the software, go to **File>Exit**.

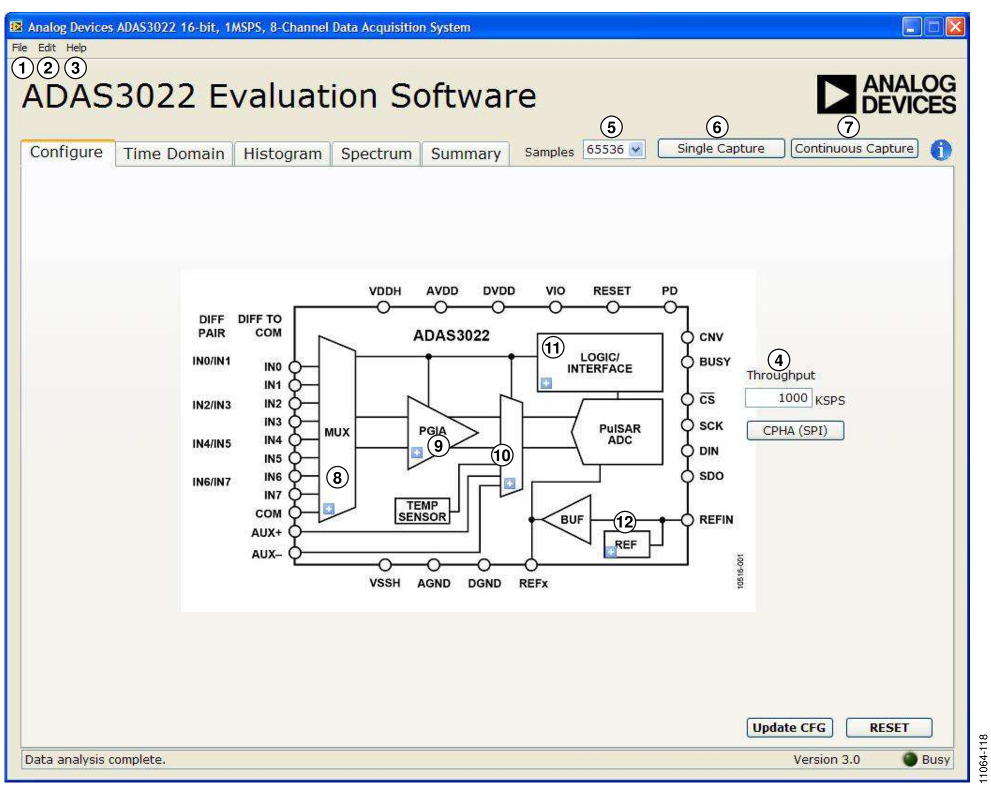


Figure 18. Setup Screen

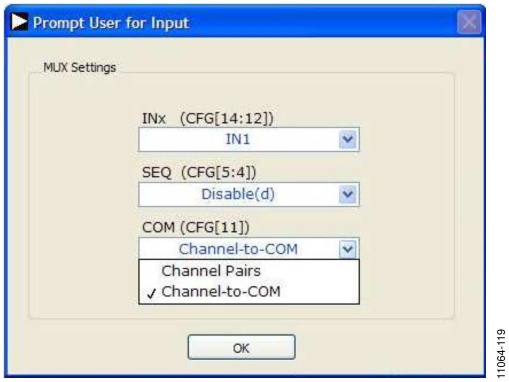


Figure 19. Dialogue Box for Label 8, MUX Settings

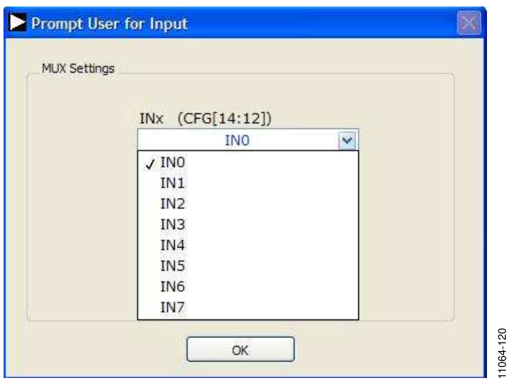


Figure 20. Dialogue Box for Label 8, Input Channel Options

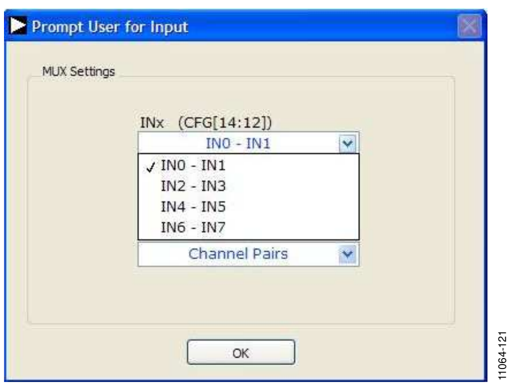


Figure 21. Dialogue Box for Label 8, Alternate Input Channel Options

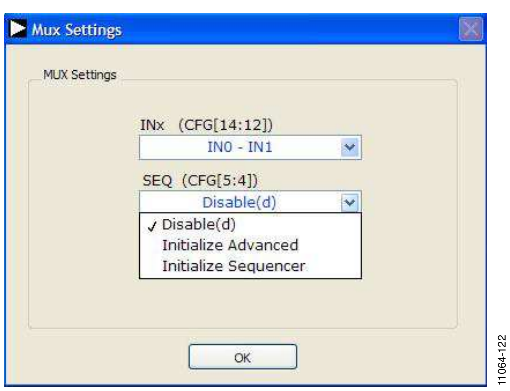


Figure 22. Dialogue Box for Label 8, Sequence Options

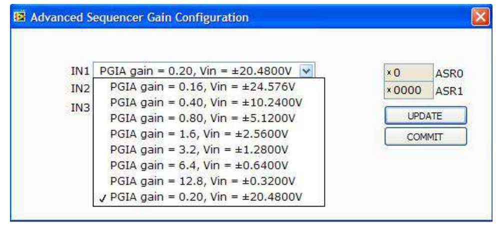


Figure 23. Dialogue Box for Label 8, Advanced Sequencer PGIA Gain Configuration

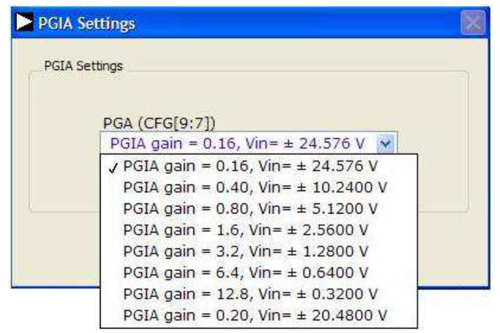


Figure 24. Dialogue Box for Label 9, PGIA Settings

Figure 25. Dialogue Box for Label 10, AUX/MUX Settings

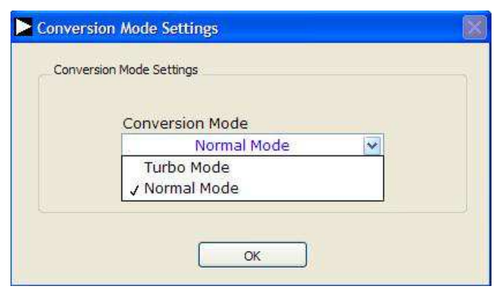


Figure 26. Dialogue Box for Label 11, Conversion Mode Settings

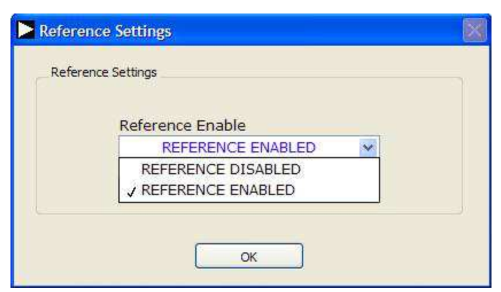


Figure 27. Dialogue Box for Label 12, Reference Settings

Start Up

Refer to the numbered labels in Figure 18. Clicking the blue buttons reveals the dialog boxes shown in Figure 19 through Figure 27.

To begin evaluating the device, the on-board supplies must be enabled.

- **RESET** resets the ADAS3022 device to a known state. Click **RESET** twice: once to reset the ADAS3022 and again to bring it out of the reset state. Note that the CFG is also reset to the default condition.
- Reference Selection: At this time, it is recommended to use the evaluation board's externally generated reference (default). To select the on-chip reference, remove the P5 and P7 jumpers and click the button in the **REF** block to display the **Reference Settings** dialog box, then choose **REFERENCE ENABLED**.
- Auxiliary (AUX±) Channels Selection: The ADAS3022 allows the user to run it in default **MUX ONLY** mode or by clicking on it to select the auxiliary channel input pair (AUX+, AUX−) **IN0–INX AUX** in normal mode or sequencer mode. The **IN0–INX AUX** option converts a dedicated channel through the internal differential auxiliary channel pair (AUX+, AUX−) with the specified input range of $\pm V_{REF}$. This option bypasses the MUX and programmable gain instrumentation amplifier stage, allowing direct access to the SAR ADC core.
- **Update CFG**: If the default configuration (channel, channel configuration, reference, and so on) is acceptable, clicking **Update CFG** writes to the ADAS3022 configuration register (CFG). The ADAS3022 device is configurable using a 16-bit on-chip register, CFG (refer to the ADAS3022 data sheet for more details). Note that after changing any of the CFG register, this button must be clicked for the new setting to take effect.

Input Channel

To select the input channel, make a selection from the pull-down menu (see Figure 20).

Channel Pairing

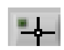
The channels can be paired (up to 4 maximum) or all channels can be referenced to the COM input (see Figure 21).

Programmable Gain

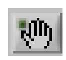
The most useful and innovative feature of the ADAS3022 is the on-chip programmable gain instrumentation amplifier. This amplifier has the added flexibility of allowing for inputs ranging from ±0.64 V to ±24.574 V. Select the appropriate setting for the input voltage span, not including any common-mode signals, since they are rejected. Note that the ADAS3022 devices do not need the usual level shifting that is common in SAR ADC systems. The ADAS3022 devices can accommodate fully differential, single ended, and bipolar input signal types.

Software Controls

Within any of the chart panels, these controls are used to control the display.

 Controls the cursor.

 Controls zooming in and out.

 Controls panning.

TIME DOMAIN TAB

Figure 28 illustrates the Time Domain tab. The ADAS3022 output is twos complement output; however, the software outputs the results in straight binary.

Note that Label 1 shows the **Waveform Analysis** that reports the amplitude recorded from the captured signal in addition to the frequency of the signal tone, and Label 2 shows that Y-axis units can be displayed in volts or code (LSB).

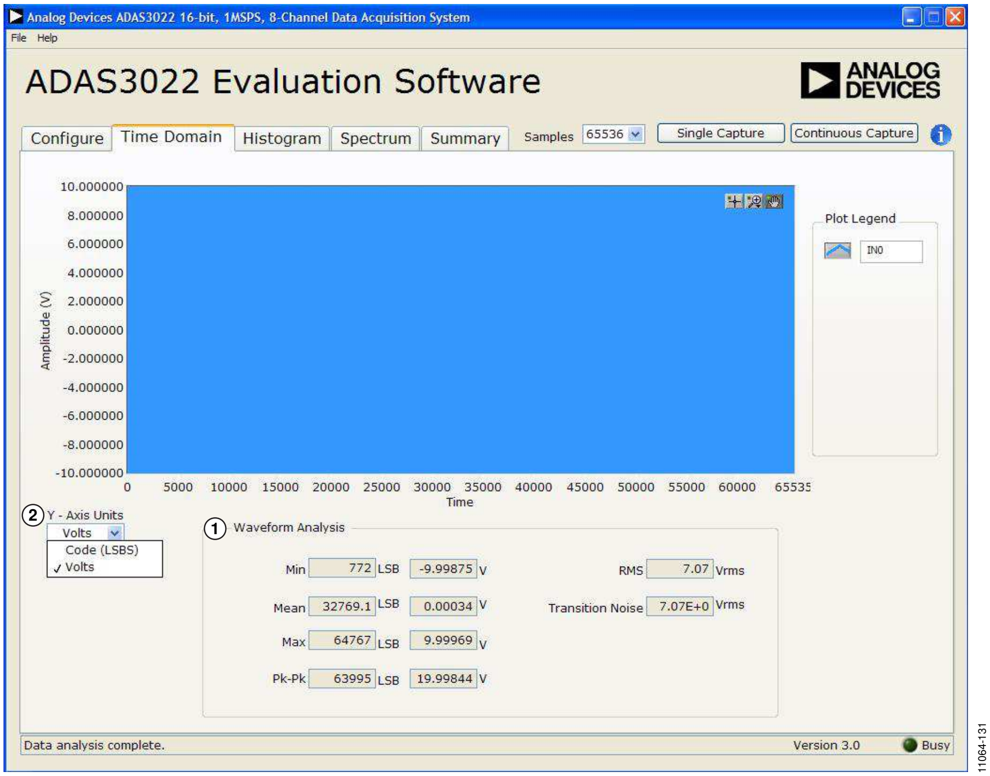


Figure 28. Time Domain Tab

HISTOGRAM TAB

The histogram is most often used for dc testing or ac testing, where a user tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise, of the converter, and displays the results. Raw data is captured and passed to the PC for statistical computations. Figure 29 shows the Histogram tab.

To perform a histogram test,

1. Select the **Histogram** tab.
2. Click **Single Capture** or **Continuous Capture**.

DC Testing

To test other dc values, apply a source to the selected analog inputs IN[7:0]_I via test points or P1. It may be required to filter the signal to make the dc source noise compatible with that of the ADC. Note that 0805 and 0603 SMT pads are provided in each signal path and can be used for filtering the source, if necessary.

AC Testing

Figure 29 shows the histogram for a 1 kHz sine wave applied to the analog inputs IN[7:0]_I via test points or P1 from a quality precision signal source, such as Audio Precision. It may be required to filter the input signal from the ac source. There is no suggested band-pass filter, but consider all choices carefully. The **Waveform Analysis** (Label 1) chart displays the various measured histogram values for the ADAS3022.

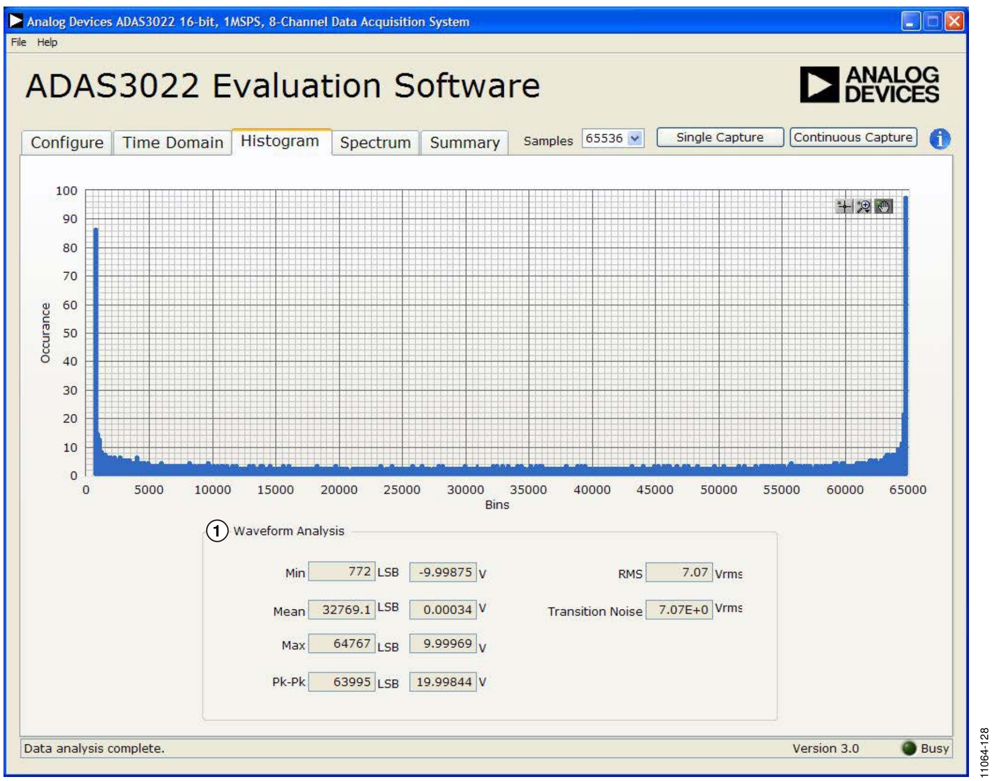


Figure 29. Histogram Tab

SPECTRUM TAB

Figure 30 shows the FFT spectrum capture tab. This tab tests the traditional ac characteristics of the converter and displays a fast Fourier transform (FFT) of the results. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed, displaying SNR, SINAD, THD, and SFDR.

To perform an ac test, apply a sinusoidal signal to the evaluation board to any of the analog inputs IN[7:0]_I, either via test points or P1. Very low distortion—a better than 130 dB input signal source, such as Audio Precision)—is required to allow true evaluation of the part. One possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but carefully consider the choices. Figure 30 displays the results of the captured data.

- The top part of the image displays the FFT results including SNR, dynamic range, THD, SINAD, and noise performance (see Label 1).
- The lower part of the image displays the fundamental frequency and amplitude in addition to the 2nd to 5th harmonics (see Label 2).

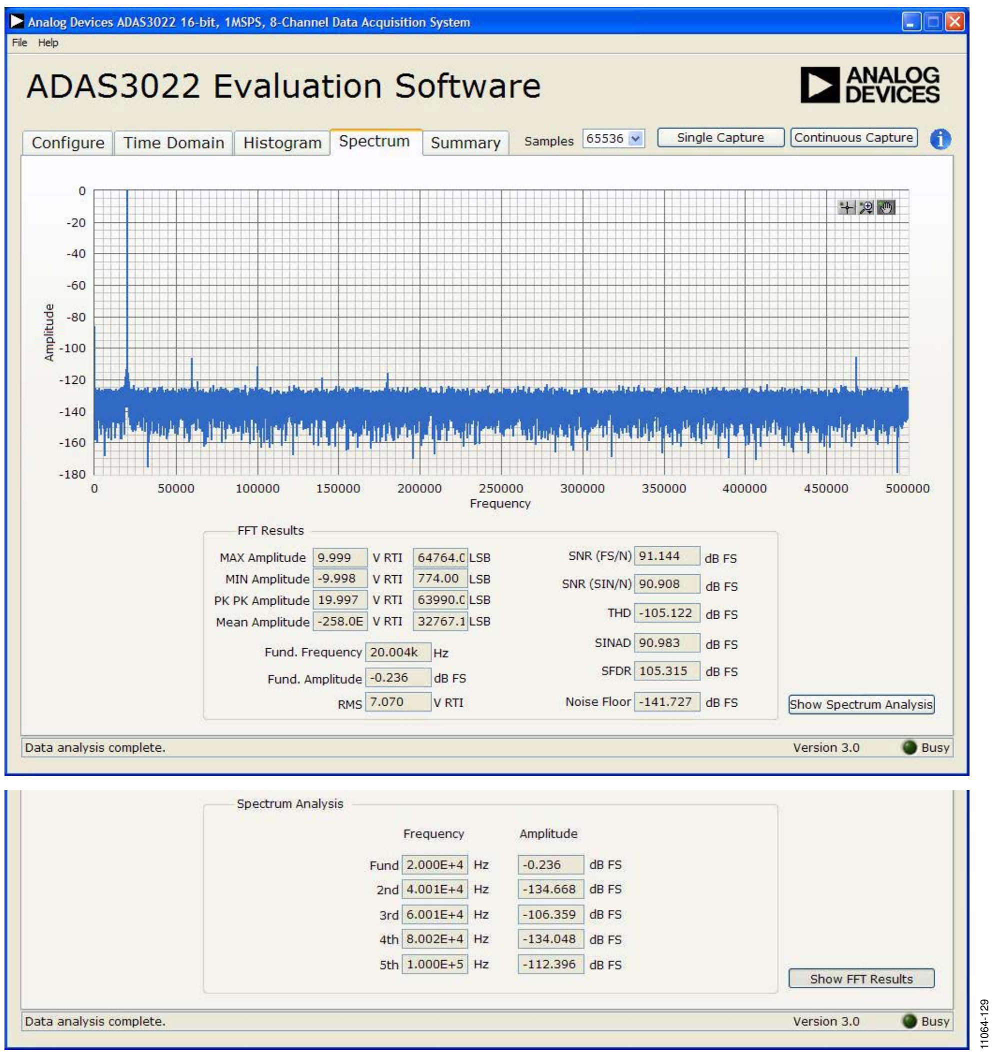


Figure 30. FFT Spectrum with FFT Results (Top) and with Spectrum Analysis Results (Bottom)

SUMMARY TAB

Figure 31 shows the Summary tab, which summarizes all the data capture information and displays it in one panel with a synopsis of the information, including key performance parameters such as SNR, THD, and SINAD.

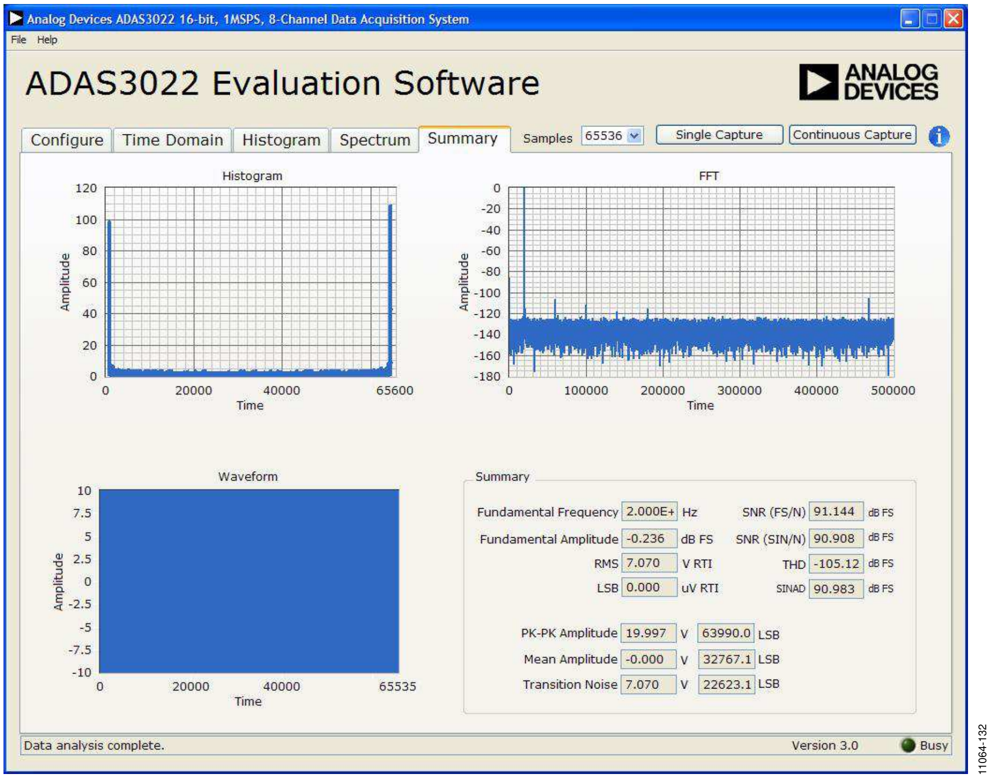


Figure 31. Summary Tab

EVALUATION BOARD SCHEMATICS AND ARTWORK

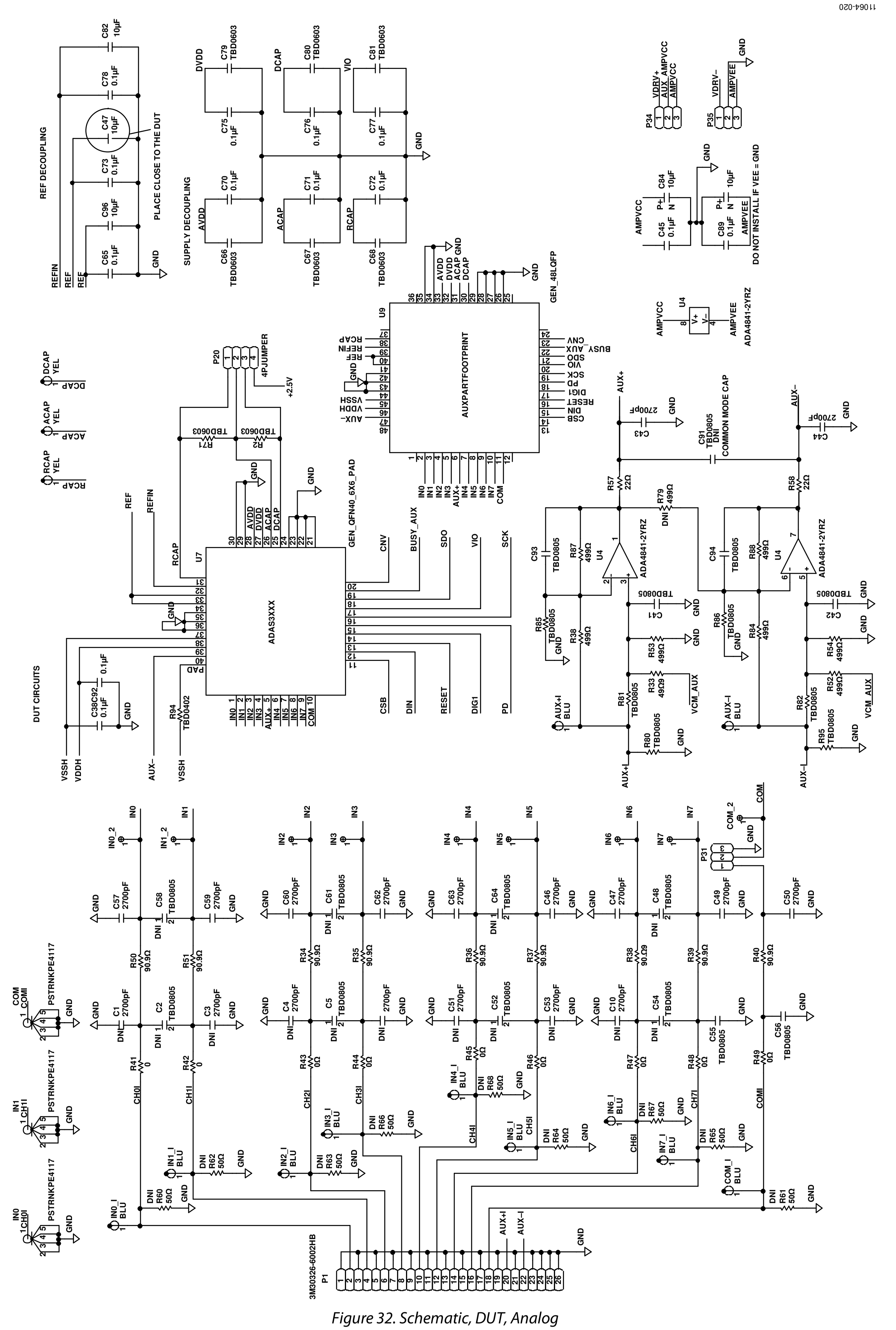


Figure 32. Schematic, DUT, Analog

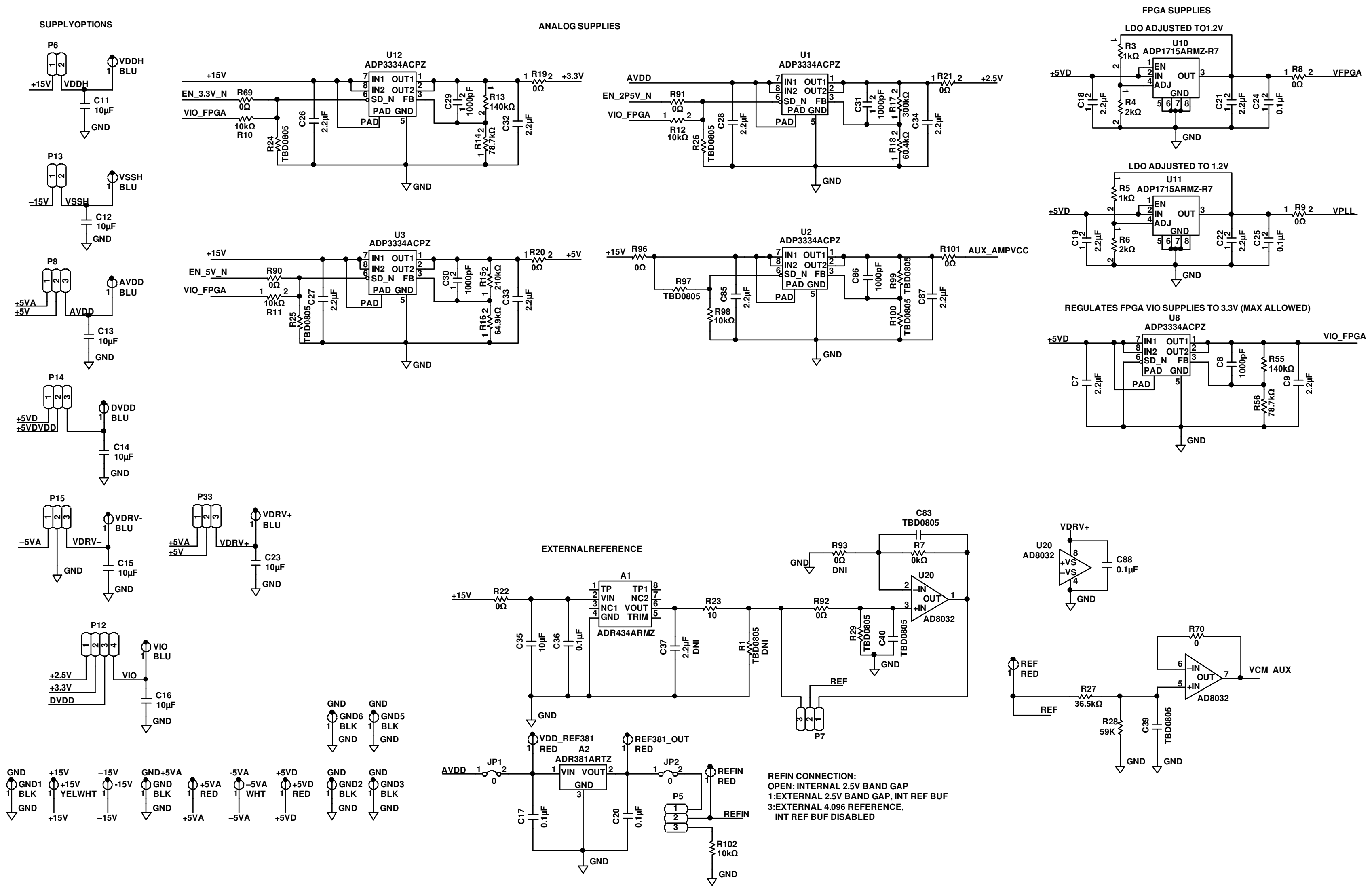


Figure 33. Schematic, Power

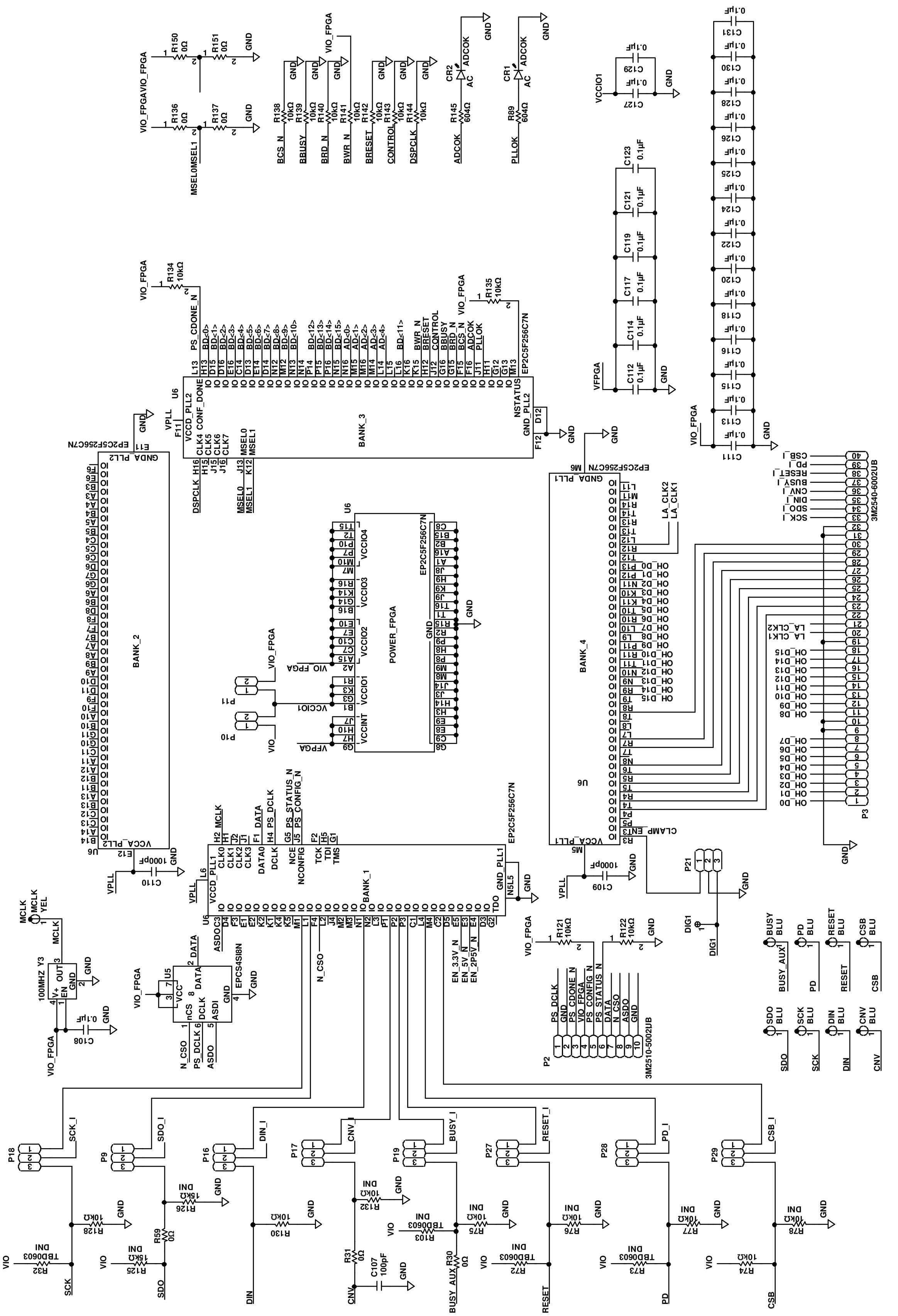


Figure 34. Schematic, FPGA

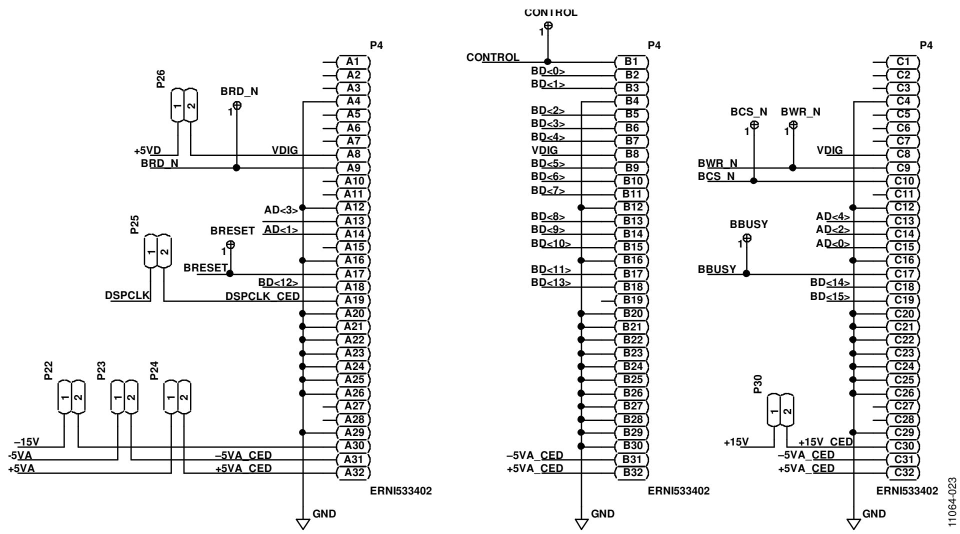


Figure 35. Schematic, 96-Pin Interface

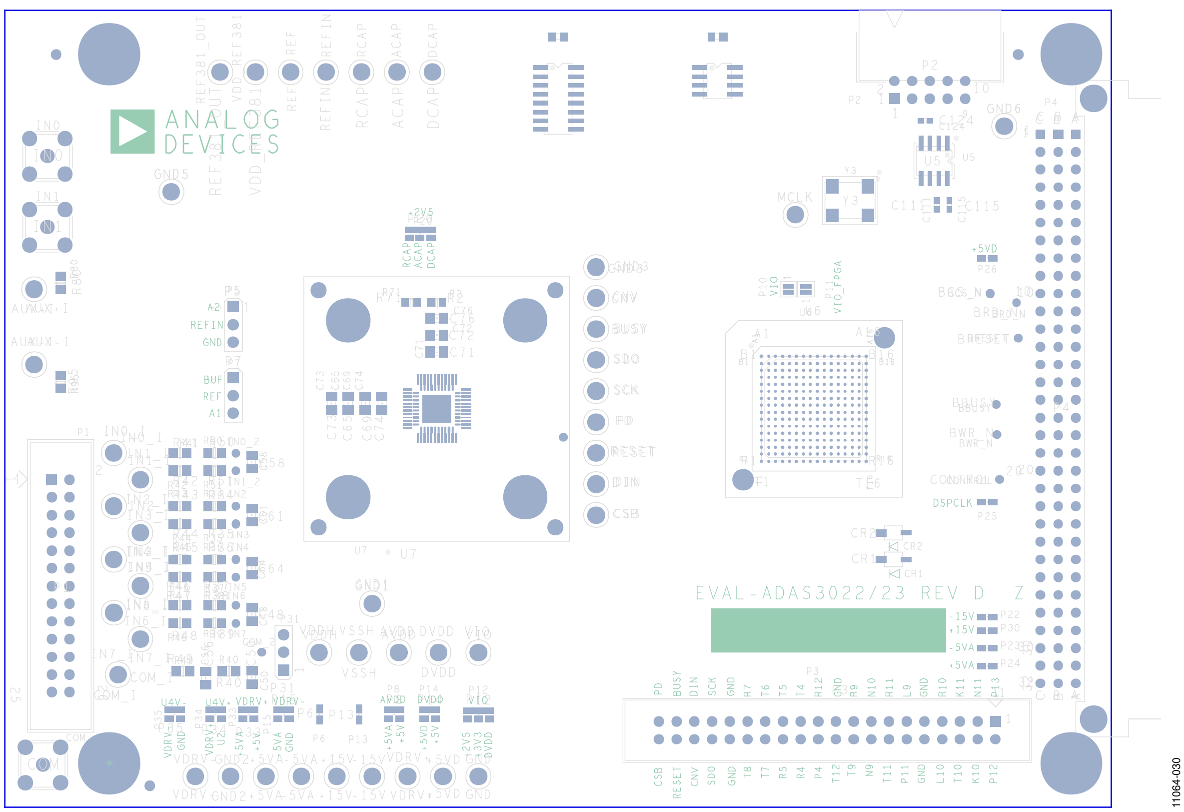


Figure 36. Silkscreen, Top

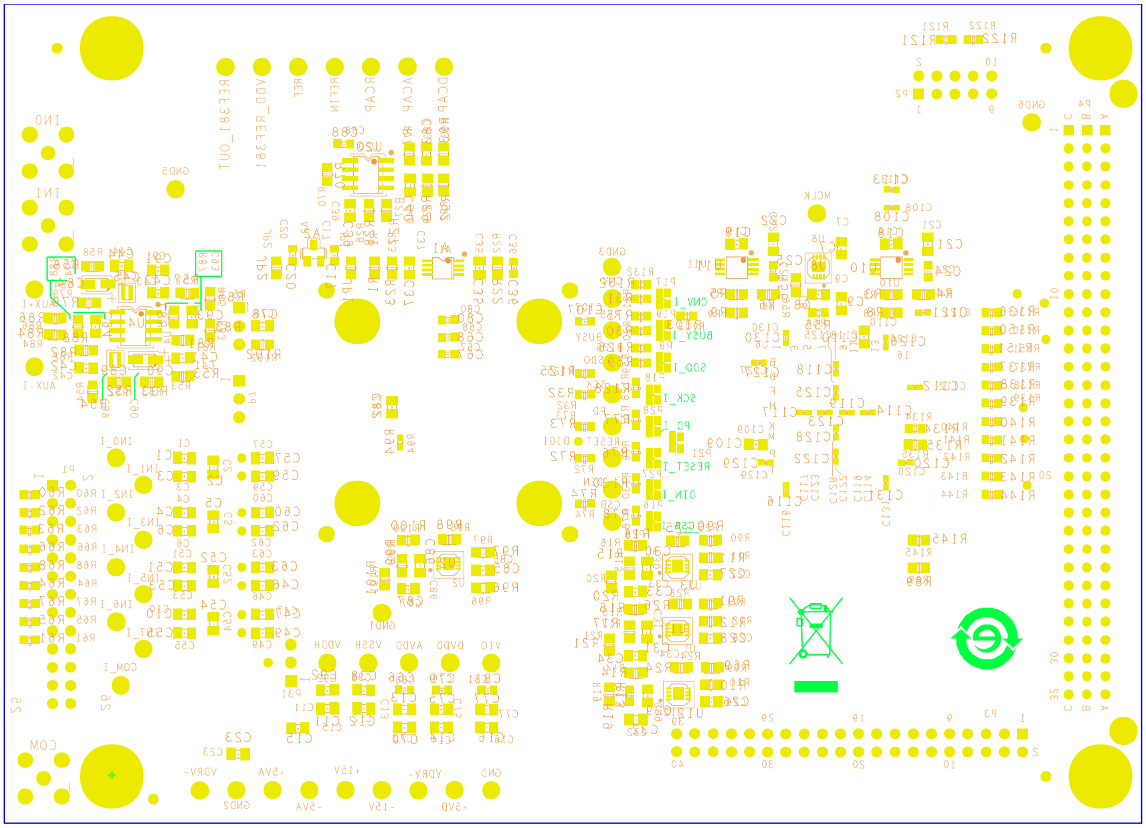
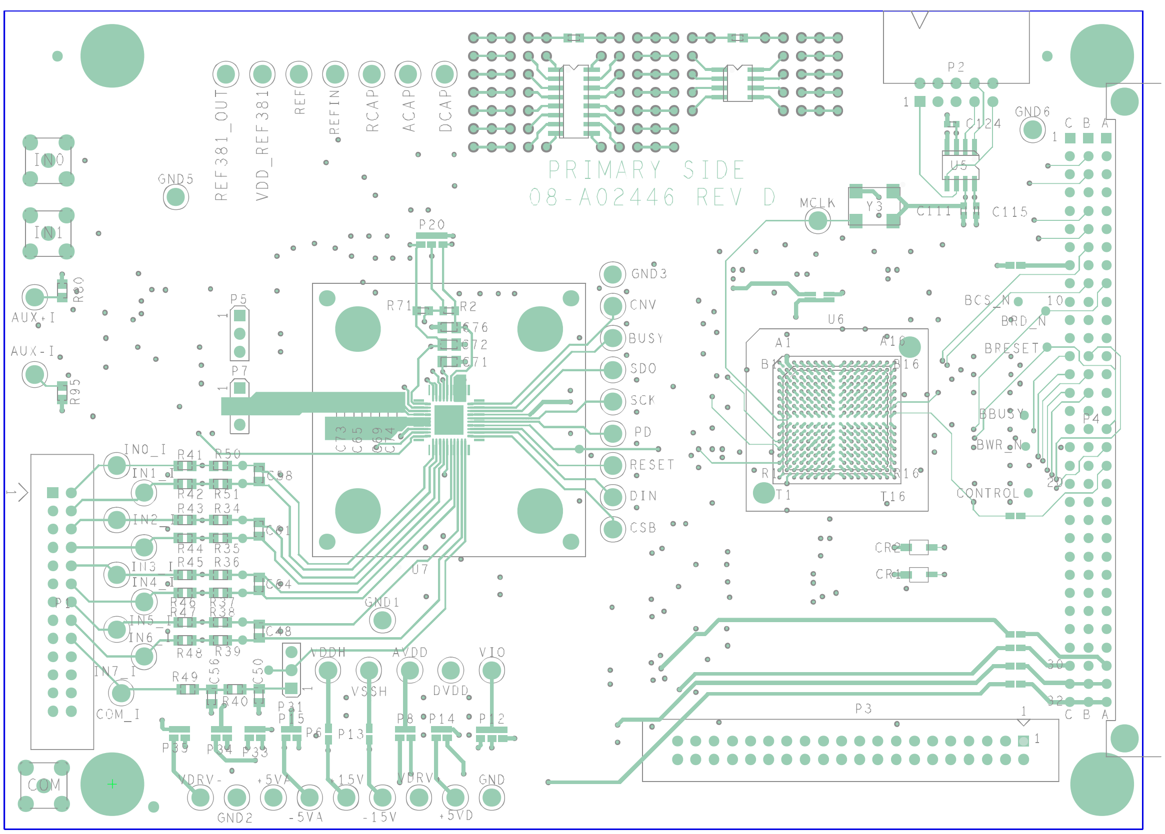

11064-031

Figure 37. Silkscreen, Bottom



11064-024

Figure 38. Top Layer 1

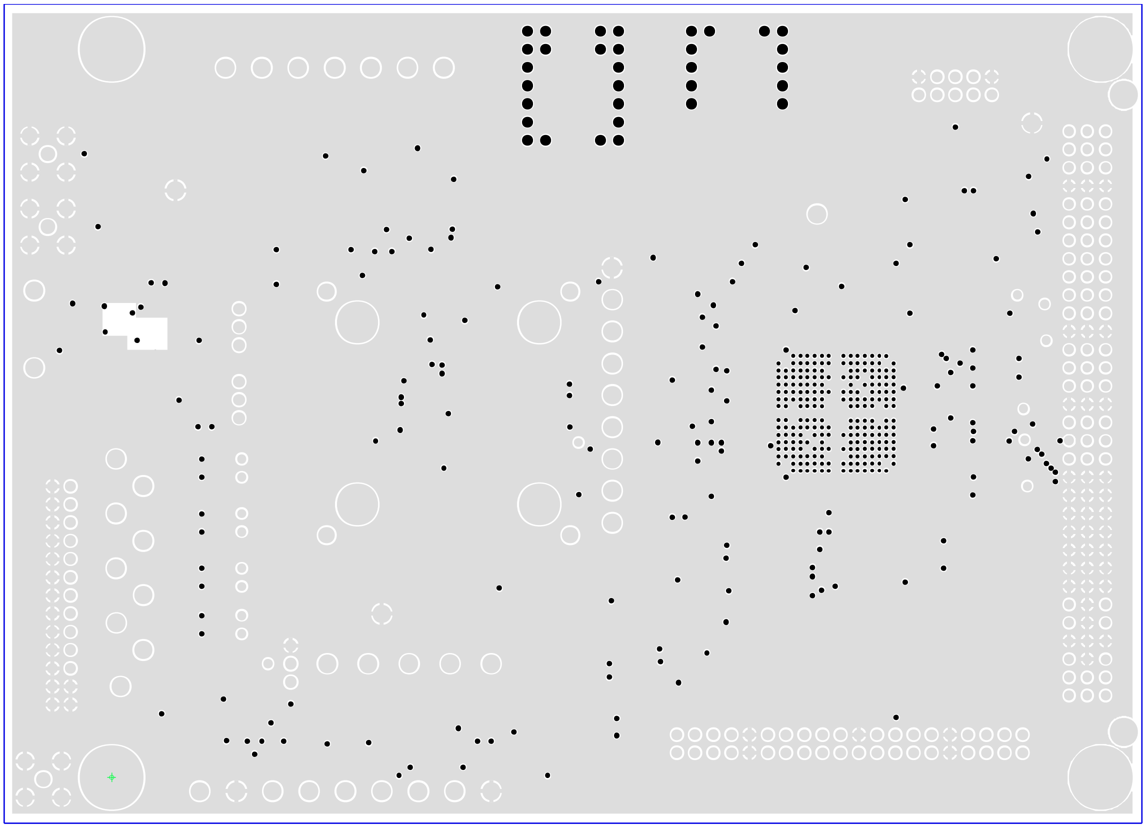


Figure 39. GND Layer 2

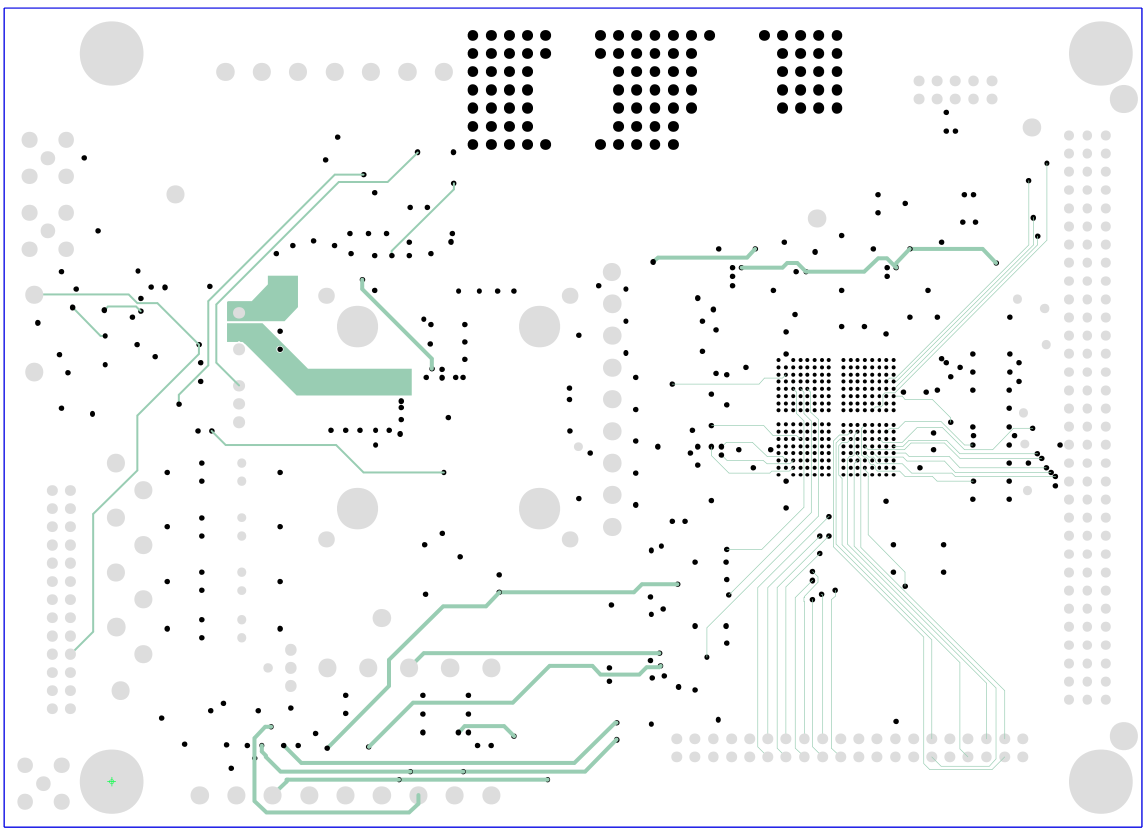


Figure 40. Signal Layer 3

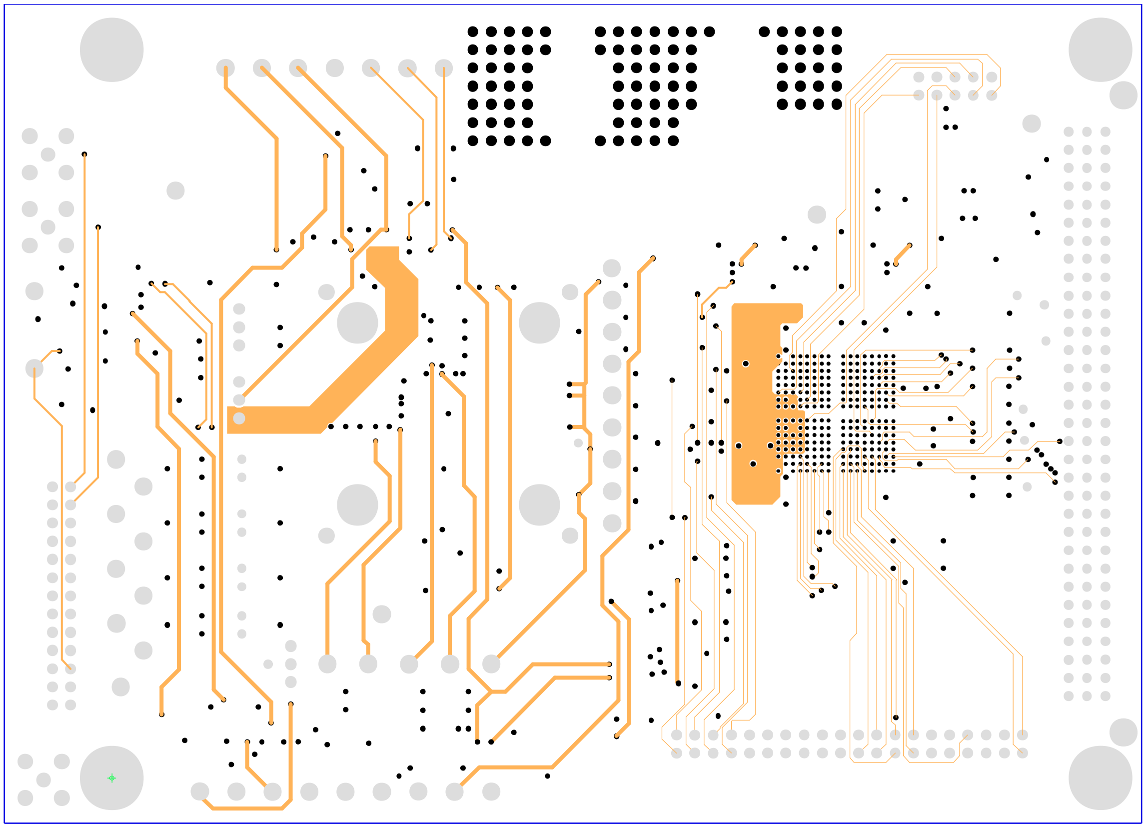


Figure 41. Signal Layer 4

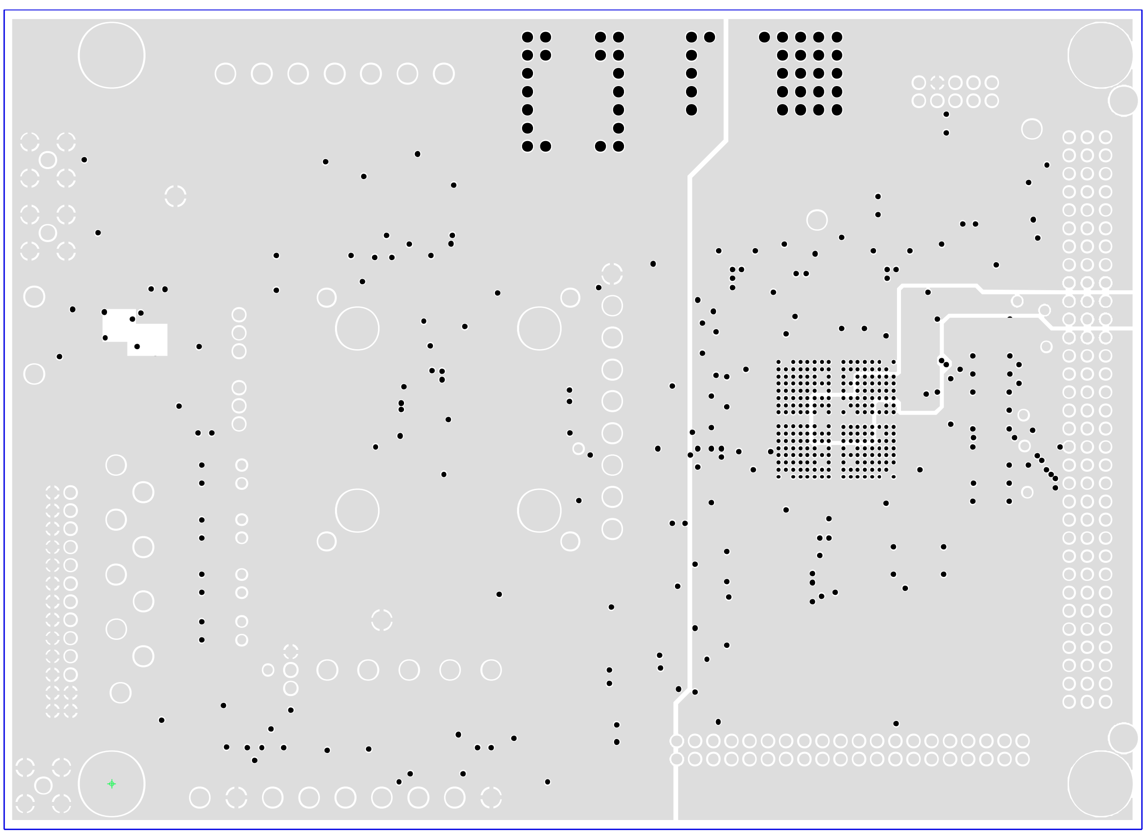


Figure 42. Power Layer 5