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Evaluation Board for the ADAS3023 16-Bit, 8-Channel, Simultaneous Sampling Data Acquisition System

FEATURES

Full-featured evaluation board for the ADAS3023
Versatile analog signal conditioning circuitry
On-board reference, clock oscillator, and buffers
Converter evaluation and development board (EVAL-CED1Z) compatible
PC software for control and data analysis (time and frequency domain)

KIT CONTENTS

EVAL-ADAS3023EDZ evaluation board

ADDITIONAL EQUIPMENT NEEDED

EVAL-CED1Z board
Precision signal source
World-compatible 7 V dc supply (enclosed with EVAL-CED1Z)
USB cable

EVALUATION BOARD DESCRIPTION

The EVAL-ADAS3023EDZ is an evaluation board for the ADAS3023 16-bit data acquisition system (DAS). This device integrates an 8-channel low leakage track and hold, a high impedance programmable gain instrumentation amplifier (PGIA) stage with high common-mode rejection, a precision 16-bit successive approximation (no latency) analog-to-digital converter, and precision 4.096 V reference. It is capable of converting two channels simultaneously up to 500,000 samples per second (500 kSPS) throughput.

The evaluation board is designed to demonstrate the performance of the ADAS3023 and to provide an easy-to-understand interface for a variety of system applications. A full description of this product is available in the product data sheet and should be consulted when utilizing this evaluation board.

The evaluation board is intended to be used with the Analog Devices, Inc., converter evaluation and development (CED) board, EVAL-CED1Z, a USB-based capture board connected to P4, the 96-pin interface.

On-board components include a high precision, buffered band gap 4.096 V reference (ADR434), a reference buffer (AD8032), passive signal conditioning circuitry, and an FPGA for deserializing the serial conversion results and configuring the ADAS3023 via a 4-wire serial interface.

The P3 connector allows users to test their own interface with or without the optional Altera FPGA, U6 (programmed using the P2 and passive serial EEPROM, U5).

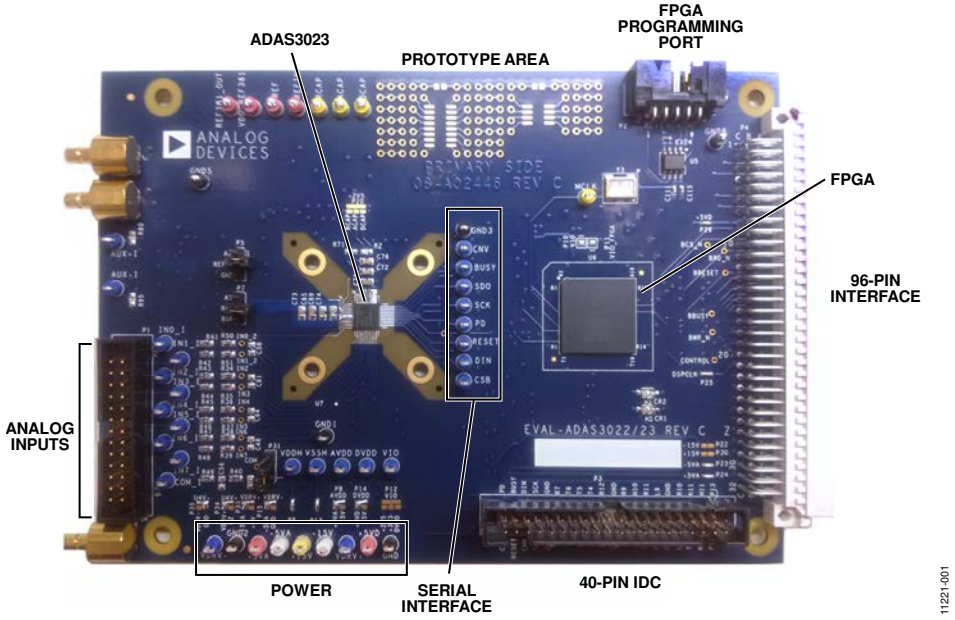

Figure 1. EVAL-ADAS3023EDZ Evaluation Board

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REVISION HISTORY

5/13—Rev. 0 to Rev. A

Changes to Title and Evaluation Board Description Section 1
Changes to Device Description Section 3
Removed CD-ROM Section 8
Changes to Running the Software with the Hardware Connected Section 10
Changes to Figure 10 and changes to Start Up Section 11
Changes to Figure 14 13
Changes to Figure 16 14
Changes to Figure 17 15
Changes to Figure 18 16
Changes to Figure 19 17

4/13—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

OVERVIEW

The EVAL-ADAS3023EDZ evaluation board is designed to offer simple evaluation of this integrated device. From a block diagram perspective, the board uses a set of analog input test points (or an IDC header), some passive footprints for RC filtering and external reference, the ADAS3023 device, a serial interface to the on-board FPGA, and power that can be supplied locally or via EVAL-CED1Z or externally. Note that the ADAS3023 device also has an on-chip reference; however, external circuitry is provided for those who need to test other suitable options.

The small prototyping area can be useful for building additional circuitry, if desired. Each block has a specific function as defined in the following sections.

DEVICE DESCRIPTION

Manufactured using the Analog Devices patented high voltage iCMOS® process, the ADAS3023 is a complete data acquisition system (DAS) on a single chip that is capable of converting two channels simultaneously up to 500 kSPS. This part allows the differential voltage range up to ±20.48 V when using ±15 V supplies. The ADAS3023 can resolve the full-scale differential voltages of ±2.56 V, ±5.12 V, ±10.24 V, and ±20.48 V, and it can be configured to sample two, four, six, or eight channels simultaneously.

The key difference between the ADAS3022 and ADAS3023 is that the ADAS3023 does not offer the AUX± channels and temperature sensor (using the CFG register) In addition, the BUSY/SDO2 (Pin 19) functionality of the ADAS3023 is different.

The ADAS3022/ADAS3023 devices become pin compatible and can be exchanged on the same footprint if the no connect (NC) pins (Pin 14/Pin 29/Pin 30 on the ADAS3022) and AUX± (Pin 5 and Pin 40 on the ADAS3022) are tied to AGND, and if the SDO2 (using the CFG register) of the ADAS3023 is not enabled, so that the user can actually work with either one of these options using the same evaluation board. Leaving these pins floating is not recommended. Note that the differential paired mode does not exist in the ADAS3023 and, therefore, its 2/4/6/8 channels are always referenced to COM.

The ADAS3023 is an ideal replacement for a typical 16-bit, simultaneous sampling precision data acquisition system that simplifies the design challenges by eliminating signal buffering, level shifting, amplification/attenuation, common-mode rejection, settling time, or any of the other analog signal conditioning challenges while allowing smaller form factor, faster time to market, and lower costs.

Data communication to and from the ADAS3023 occurs asynchronously without any pipeline delay using a common 4-wire serial interface compatible with SPI, FPGA, and DSP.

A rising edge on CNV samples the differential analog inputs of a channel or channel pair. The ADAS3023 configuration register allows the user to configure the number of enabled channels, the differential input voltage range, and the interface mode using the evaluation board and software as detailed in this user guide. Complete specifications for the ADAS3023 are provided in the product data sheet and should be consulted in conjunction with this user guide when using the evaluation board. Full details on the EVAL-CED1Z are available on the Analog Devices website.

Table 1. Typical Input Range Selection

Single-Ended Signals[1]	Input Range, VIN (V)
0 V to 1 V	±1.28 V
0 V to 2.5 V	±2.56 V
0 V to 5 V	±5.12 V
0 V to 10 V	±10.24 V

[1] See the ADAS3023 data sheet for more information

JUMPERS, SOLDER PADS, AND TEST POINTS

Numerous solder pads and test points are provided on the evaluation board and are detailed fully in Table 4, Table 5, and Table 6. Note the nomenclature for this evaluation board for a signal that is also connected to an IDC connector would be signal_I. The two 3-pin user selectable jumpers are used for the ADCs reference selection and are fully described in the Reference section.

ANALOG INTERFACE

The analog interface is provided with test points for each of the analog inputs IN[7:0] and COM (that is, IN0_I is common to both the test point and to P1). The passive device footprints can be used for filtering, if desired. A simple RC filter made up of 22 Ω and 2700 pF NPO capacitors is provided. Note that the use of stable dielectric capacitors, such as NPO or COG, is required in the analog signal path to preserve the ADAS3023 distortion. Using X5R or other capacitors in the analog signal path greatly reduces the performance of the system. Also, note that many bench top arbitrary waveform generators (AWGs) use 12-bit or 14-bit digital-to-analog converter outputs such that the 16-bit ADAS3023 devices digitize this directly resulting in erroneous looking data. If such an AWG is used, a high-order band-pass filter should be used to filter the unwanted noise from these sources.

The P31 center pin is connected to the ADAS3023 COM input, which can be routed to P1 or GND using P31. For channel to COM configuration, set the jumper across Pin 1 and Pin 2 to route to P1. For channel pairs configuration, set the jumper across Pin 2 to Pin 3 to route to GND. This is useful for single-ended applications.

For dynamic performance, an FFT test can be done by applying a very low distortion ac source, such as an Audio Precision

System 2702. This source can be set for balanced or unbalanced, and can be floated or grounded depending on the user's choice.

FPGA

The on-board FPGA performs a number of digital functions, one of them being the sample rate conversion controlled using the software. Another function is deserializing the serial conversion results as the CED data capture board uses a 16-bit parallel interface. If desired, the deserialized data can be monitored on the 96-pin edge connecter P1, BD[15:0]. The CED uses a buffered busy signal, BBUSY, as the general interrupt for the data transfer to the CED board.

The FPGA also provides the necessary ADAS3023 asynchronous control signals for RESET and power down (PD).

The signals from the FPGA to the ADAS3023 can be bypassed by modifying the default solder pad connections. As shown in Figure 2, each digital signal on the ADAS3023 is connected to the larger (top) pad of the three. The default configuration is the small pad and larger pad (no text) which connects the FPGA to the ADAS3023 (CNV, BUSY, and SDO signals shown). The labeled pads, CNV_I, BUSY_I, SDO_I, and so on, are the signals that are routed to P3. To use P3 instead of the FPGA, unsolder the default connections and resolder from the large pad to the xxx_I pads. The FPGA will remain powered; however, if all the signals are bypassed in this fashion, it will not have any influence on the ADAS3023.

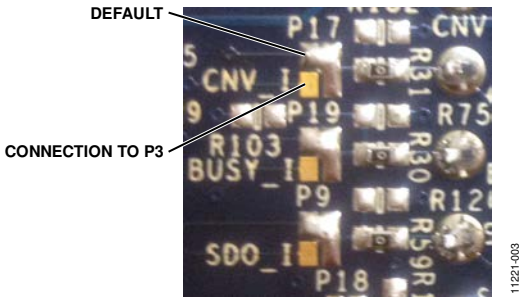

Figure 2. Digital Interface Solder Pads—Partial View

Serial Interface

The 4-wire serial interface consisting of $\overline{CS}$, DIN, SCK, and SDO is present on the digital interface test points and is controlled by the FPGA. The FPGA can be bypassed by using the solder pads.

REFERENCE

The ADAS3023 has an internal 4.096 V reference, along with an internal buffer, useful for using an external reference or one can use an external 4.096 V reference directly, such as the ADR434 provided on the evaluation board. The evaluation board can be configured to use any of these references. Two jumpers (P5 and P9) are used for setting the reference in conjunction with software control.

External Reference–Factory Configuration

The evaluation board includes the ADR434, A1, which is a 4.096 V precision voltage reference. This reference can drive the ADC REF1 or REF2 (REFx) pin directly or it can also be buffered with U20, the AD8032; both of these are set to the factory default setting.

Table 2. Factory Reference Jumper Configuration

Jumper	Setting
P5	REFIN to GND[1]
P9	REF to BUF (U20)

[1] The connection is made through R102 = 10 k to GND.

To use another reference source, there are two methods:

- For an external unbuffered reference, remove the P9 jumper and connect a source to the REF test point.
- Since the ADR434 is a standard 8-lead SOIC, it can also be removed and replaced with the user's reference. In this case, the user reference and the U20 AD8032 buffer can be used as a reference source.

Internal 4.096 V Reference

The ADC has an internal 4.096 V precision reference and can be used on most applications. When enabled, 4.096 V will be present on the ADAS3023 REFx pin and test point, REF. In addition, a voltage will also be present on the ADAS3023 REFIN pin and test point, REFIN. The voltage present on REFIN can be used for other purposes, such as to provide the bias voltage; however, it would need a suitable buffer as the output impedance of the REFIN is on the order of a few kilo ohms and loading this voltage down will degrade the internal reference's performance.

Table 3. Internal Reference Jumper Configuration

Jumper	Setting
P5	Open
P9	Open

Note that the ADAS3023 configuration register needs to be updated either using the included software or by writing the appropriate bits to enable the internal reference.

Internal Reference Buffer

The internal reference buffer is useful when using an external 2.5 V reference. When using the internal reference buffer, applying 2.5 V to REFIN, which is directly connected to the ADC's REFIN pin, produces 4.096 V at the ADCs REFx pin and REF test point.

POWER SUPPLIES AND GROUNDING

The on-board ADP3334 low dropout regulators are provided for 2.5 V, 3.3 V, and 5 V and also for the FPGA I/O supply which is user configurable and set to 3.3 V by default. The FPGA core is supplied by a pair of ADP1715 devices set for 1.2 V. Additional power is supplies via the CED board for an alternative +5 V analog and digital 3.3 V/5 V digital through P4.

The ADAS3023 requires ±15 V supplies for VDDH and VSSH. These must be supplied by the user using a standard lab supply ensuring that the return paths are at the same potential. Refer to

CN-0201 for the complete information on generating these ±15 V supplies from a +5 V single supply. The differential input common-mode voltage (VCM) range changes according to the maximum input range selected and the high voltage power supplies (VDDH and VSSH). In other words, the specified operating input voltage of any input pin requires 2.5 V of headroom from the VDDH and VSSH supplies.

The evaluation board ground plane consists of a solid plane on one PCB layer shared on another layer with the power plane. To attain high-resolution performance, the board was designed to ensure that all digital ground return paths do not cross the analog ground return paths, that is, all analog on one side and digital on the other.

EVALUATION BOARD SCHEMATICS/PCB LAYOUT

The evaluation board is a 6-layer board carefully laid out and tested to demonstrate the specific high accuracy performance of the ADAS3023 devices. The Evaluation Board Schematics and Artwork section of this user guide shows the schematics of the evaluation board.

BASIC HARDWARE SETUP

The ADAS3023 evaluation board connects to the EVAL-CED1Z converter evaluation and demonstration board. The EVAL-CED1Z board is the controller board, which is the communication link between the PC and the main evaluation board.

Figure 5 shows a photograph of the connections made between the ADAS3023 daughter board and the EVAL-CED1Z board.

1. Before connecting power, ensure that the EVAL-ADAS3023EDZ and the EVAL-CED1Z boards are connected firmly together.
2. Connect the power supplies on the EVAL-ADAS3023EDZ board. The EVAL-ADAS3023EDZ requires external power supplies of ±15 V. Connect them from a bench top power supply.
3. Before connecting the EVAL-CED1Z board to your PC, ensure that the ADAS3023 software has been installed from the Analog Devices website. The full software installation procedure is detailed in the Evaluation Board Software section.
4. Connect the EVAL-CED1Z board to the PC via the USB cable enclosed in the EVAL-SDPCB1Z kit. If using a Windows® XP platform, you may need to search for the EVAL-CED1Z drivers. Choose to automatically search for the drivers for the EVAL-CED1Z board if prompted by the operating system.
5. Proceed to the Software Installation section to install the software. Note that the EVAL-CED1Z board must not be connected to the PC's USB port until the software is installed. The 7 V dc supply should be connected to power up the board and make sure that the green LED lit.

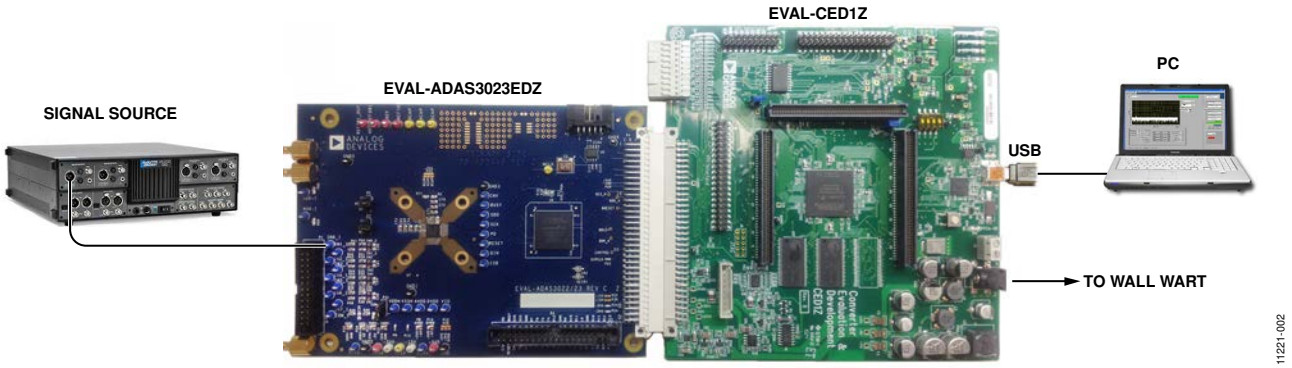

Figure 3. Hardware Configuration—Setting Up the EVAL-ADAS3023EDZ

JUMPERS AND TEST POINTS

Three-pin jumpers are used to configure the ADC reference. Refer to the Reference section for further details and settings.

Table 4. Pin Jumper Descriptions

Jumper	Default	Function
P5	REFIN to GND	REFIN Select. Buffered reference input selection. Use in conjunction with P7. Note that the ADAS3023 REFx pin and any other circuit traces/test points will produce 4.096 V when using the buffered reference configuration; P7 must be left in the open position. REFIN to A2: Uses the on-board ADR381, A2 (2.5 V) reference. The ADAS3023 must use the buffered reference configuration. REFIN to GND: Disables the ADAS3023 internal reference. The ADAS3023 must use the full external reference configuration. Open: For use either when using the ADAS3023 on-chip reference or when applying an external 2.5 V source. When using the on chip reference, a voltage is present on Pin 2 and any other circuit traces/test points. When using an external source, the ADAS3023 must use the buffered reference configuration.
P7	REF to BUF	REF Select. External 4.096 V reference input selection. Use in conjunction with P5. Note that the ADAS3023 REFIN pin and any other circuit traces/test points produce 2.5 V when using the internal or external reference configuration and P5 must be left in the open position. REF to A1: Uses the on-board ADR434, A1 (4.096 V), reference. The ADAS3023 must use the external reference configuration. REF to BUF: Uses the on-board ADR434 followed by the AD8032, U20 unity gain buffer. This allows some adjustment to the reference voltage by use of some resistors around the AD8032. The ADAS3023 must use the external reference configuration. Open: For use when using the ADAS3023 on-chip reference or an externally applied source connected directly to Pin 2 or the REF test point.
P31	COM to PIN 1	COM Input Select. Center pin connected to ADAS3023 COM pin. Center pin to PIN1 routes COM to P1. Center to PIN3 routes COM to GND.

Solder pads jumpers are factory configured and can be changed by the user.

Table 5. Analog and Digital Solder Pads Descriptions

Jumper	Name	Default	Function
P9	SDO	1 to 3	SDO Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P34.
P16	DIN	1 to 3	DIN Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P35.
P17	CNV	1 to 3	CNV Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P36.
P18	SCK	1 to 3	SCK Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P33.
P19	BUSY	1 to 3	BUSY Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P37.
P27	RESET	1 to 3	RESET Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P38.
P28	PD	1 to 3	PD Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P39.
P29	$\overline{CS}$	1 to 3	$\overline{CS}$ Interface Select. Pad 1 to Pad 3 for FPGA; Pad 2 to Pad 3 for P3 to P40.
P25	DSPCLK	Soldered	CED Clock Source.

Table 6. Power Supply Solder Pads

Jumper	Name	Default	Function
P6	VDDH	Soldered	VDDH Supply.
P13	VSSH	Soldered	VSSH Supply.
P8	AVDD	+5VA	AVDD Supply. Selection of +5 V A, analog supply from the CED board or +5 V from U3.
P10	–	Soldered	VIO Supply. This solder pad can be used to power the FPGA VIO and ADAS3023 VIO together.
P11	–	Soldered	FPGA VIO Supply. Supplied from U8, 3.3 V, dedicated digital supply.
P12	VIO	Open	VIO Supply. Selection of 2.5 V (2V5), 3.3 V (3V3), or DVDD (5V). Note that the ADAS3023 digital outputs are set to this level and are directly wired to the FPGA, U6, which is 3.3 V max. When using the 5 V setting, the ADAS3023 outputs, SDO and BUSY must be resistively divided using the 0603 pads provided on the evaluation board. For this reason, P10 is used as the default.
P14	DVDD	+5VD	DVDD Supply. Selection of +5 V digital, +5 V D, and +5 V from U3.
P15	VDRV-	−5VA	U20 V−/P34 Supply. Selection of −5 V A, analog supply from the CED board or GND.
P33	VDRV+	+5VA	U20 V+/P35 Supply. Selection of +5 V A, analog supply from the CED board or +5 V from U3.
P34	U4 V+	VDRV+	U4 V+ Supply. Selection of VDRV+ or U2.
P35	U4 V−	VDRV−	U4 V− Supply. Selection of VDRV− or GND.
P22	−15V	Soldered	−15 V CED Supply.
P23	−5VA	Soldered	−5 V A (Analog) CED Supply.
P24	+5VA	Soldered	+5 V A (Analog) CED Supply.
P26	+5VD	Soldered	+5 V D (Digital) CED Supply.
P30	+15V	Soldered	+15 V (Analog) CED Supply.

Table 7. Test Points (By Signal Type)

Test Point	Type	Description
IN0_I	Analog Input	Path for IN0 Input.
IN1_I	Analog Input	Path for IN1 Input.
IN2_I	Analog Input	Path for IN2 Input.
IN3_I	Analog Input	Path for IN3 Input.
IN4_I	Analog Input	Path for IN4 Input.
IN5_I	Analog Input	Path for IN5 Input.
IN6_I	Analog Input	Path for IN6 Input.
IN7_I	Analog Input	Path for IN7 Input.
COM_I	Analog Input	Path for COM Input.
REF	Analog Input	Direct Connection to ADAS3023 REFx Pin.
REFIN	Analog Input	Direct Connection to ADAS3023 REFIN Pin.
CNV	Digital Input	Direct Connection to ADAS3023 CNV Pin.
BUSY	Digital Output	Direct Connection to ADAS3023 BUSY Pin.
SDO	Digital Output	Direct Connection to ADAS3023 SDO Pin.
SCK	Digital Input	Direct Connection to ADAS3023 SCK Pin.
PD	Digital Input	Direct Connection to ADAS3023 PD Pin.
RESET	Digital Input	Direct Connection to ADAS3023 RESET Pin.
DIN	Digital Input	Direct Connection to ADAS3023 DIN Pin.
CSB	Digital Input	Direct Connection to ADAS3023 $\overline{CS}$ Pin.
MSCL	Digital Output	Eval Board Master Clock Form Y3, 100 MHz Oscillator.
VDDH	Power	Direct Connection to ADAS3023 VDDH Pin.
VSSH	Power	Direct Connection to ADAS3023 VSSH Pin.
AVDD	Power	Direct Connection to ADAS3023 AVDD Pin.
DVDD	Power	Direct Connection to ADAS3023 DVDD Pin.
VIO	Power	Direct Connection to ADAS3023 VIO Pin.
+5VA	Power	Connected to P24; CED +5 V A.
−5VA	Power	Connected to P23; CED −5 V A.
+15V	Power	Connected to P30; CED +5 V A.
−15V	Power	Connected to P22; CED −5 V A.
+5VD	Power	Connected to P26; CED +5 V D.
GND(s)	Power	Connected to Eval Board GND Plane.

EVALUATION BOARD SOFTWARE

SOFTWARE INSTALLATION

It is recommended that you close major Windows applications prior to installing the software.

System Requirements

- PC operating Windows XP or Vista
- USB 2.0 (for CED board)
- Administrator privileges

Website Download

The software versions are also available from the Analog Devices PulSAR Analog to Digital Converter Evaluation Kit page. After downloading the software, it is recommended to use the WinZip Extract function to extract all of the necessary components as opposed to just clicking on **setup.exe** in the zipped file.

After extracting, click on **setup.exe** in the folder created during the extraction and follow the instructions on the screen. If another version exists, it may be necessary to remove it.

USB Drivers

The software also installs the necessary USB drivers. After installing the software, power up the CED board and connect to the PC USB 2.0 port. The Windows **Found New Hardware Wizard** will display.

Click **Next** to install the drivers automatically.

Figure 4. Welcome to the Found New Hardware Wizard

When installed properly, Windows displays a completion message as shown in Figure 5.

Figure 5. Completing the Found New Hardware Wizard

On some PCs, the **Found New Hardware Wizard** may show up again and, if so, follow the same procedure to install it properly.

The Device Manager can be used to verify that the driver was installed successfully.

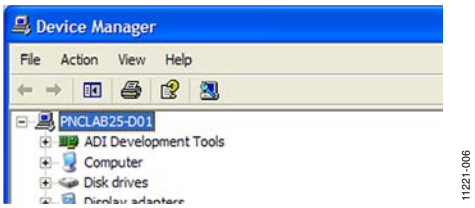

Figure 6. Device Manager

Troubleshooting the Installation

If the driver was not installed successfully, the Device Manager displays a question mark for **Other devices** because Windows does not recognize the EVAL-CED1Z board.

Figure 7. Device Manager Troubleshooting

The USB Device can be opened to view the uninstalled properties.

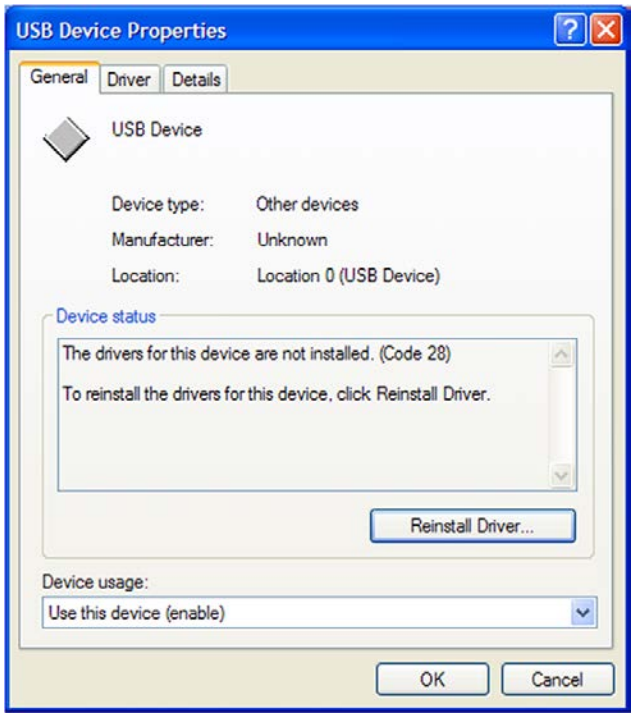

Figure 8. USB Device Properties

This is usually the case if the software and drivers were installed by a user without administrator privileges. If so, log on as an administrator with full privileges and reinstall the software.

POWERING UP THE BOARD

The evaluation board, as configured from the factory, uses the local LDOs for power where necessary. A ±15 V dc lab supply must be connected to the board. Test points (yellow and white) are provided for these external supplies.

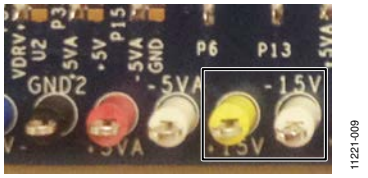

Figure 9. Test Points

RUNNING THE SOFTWARE WITH THE HARDWARE CONNECTED

The evaluation board includes software for analyzing the ADAS3023. The EVAL-CED1Z is required when using the software. The software is used to perform the following tests:

- Histogram tests for determining code transition noise (dc)
- Fast Fourier transforms (FFT) for signal-to-noise ratio (SNR), SNR and distortion (SINAD), total harmonic distortion (THD), and spurious free dynamic range (SFDR)
- Time domain analysis

This evaluation software should be located at **<local_drive>:\Program Files\Analog Devices\ADAS3023 Evaluation Software**.

In order to launch the software, click **Start>All Programs>Analog Devices\ADAS3023 Evaluation Software**. You can then apply the signal source and capture the data.

To uninstall the program, click **Start>Control Panel>Add or Remove Programs>Analog Devices ADAS3023 16-Bit, 8-Channel Simultaneous Sampling Data Acquisition System**.

Refer to Figure 10 to Figure 19 for further details and features of the software.

DC TESTING–HISTOGRAM

This tests the ADC for the code distribution for dc input and computes the mean and standard deviation, or transition noise, of the converter and displays the results. Raw data is captured and passed to the PC for statistical computations.

To perform a histogram test, select **Histogram** from the test selection window and click on **Start**. To test dc values, apply a source to any of the analog inputs IN[7:0]_I either via test points or P1. Note that 0805 and 0603 SMT pads are provided in each signal path and can be used for filtering the source, if necessary.

AC TESTING

This tests the traditional ac characteristics of the device and displays a fast Fourier transform (FFT) of the result. As in the histogram test, raw data is captured and passed to the PC where the FFT is performed displaying SNR, SINAD, THD, and SFDR. The data can also be displayed in the time domain.

To perform an ac test, apply a sinusoidal signal to the analog inputs. Low distortion, better than 97 dB, is required to allow true evaluation of the part. Note than many bench-top signal generators are at best 14-bit digital to analog converter (DAC) outputs and the ADAS3023 is 16-bits.

Simply connecting a source of this resolution results in what would appear to be incorrect displayed results (numerous harmonics and spurs). To alleviate this, one possibility is to filter the input signal from the ac source. There is no suggested band-pass filter, but consideration should be taken in the choice. Note that a passive filter also provides dc blocking and if any dc common mode is to be preserved, it would have to take place after the filtering.

SOFTWARE OPERATION

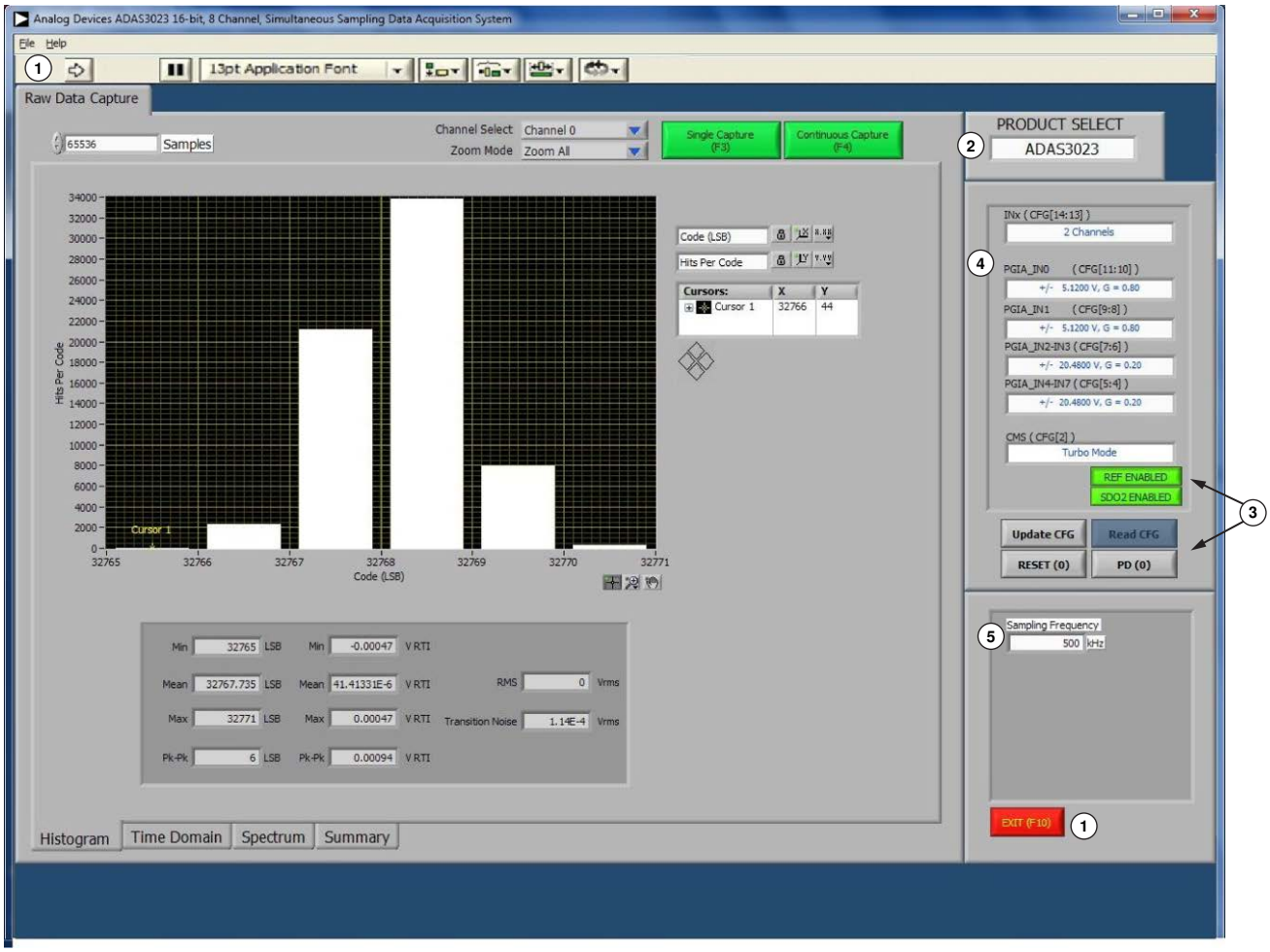

Figure 10. Setup Screen

Start Up

Refer to the numbered labels in Figure 10 which match the numbered descriptions in this section. This section details the operation of the software located in the default directory:

<local_drive>:\Program Files\Analog Devices\ADAS3023 Evaluation Software\ADAS3023 Evaluation Software.exe

1. When running the software from **Start/All Programs/ Analog Devices,** the software automatically runs. Select **EXIT (F10)** to stop the software and display the right arrow (see 1 in Figure 10).This arrow is used to start the software again. When running the software, this icon is not displayed.
2. Select the ADAS3023 from the **PRODUCT SELECT** field.
3. To begin evaluating the device, the on-board supplies must be enabled.
   - **RESET (0)** resets the ADAS3023 device to a known state. Click **RESET** twice: once to reset the ADAS3023 and again to bring it out of the reset state. Note that the CFG is also reset to the default condition.
   - **PD (0)** places the ADAS3023 device in power-down. This does not need to take place when starting the software.
   - Reference Selection: At this time, it is recommended to use the evaluation board's externally generated reference (default). To select the on-chip reference, remove the P5 and P7 jumpers and click **REF DISABLED** once to display **REF ENABLED**.
   - Serial Data Output 2 (SDO2) Option: The ADAS3023 busy signal is always output on the BUSY/SDO2 pin when $\overline{CS}$ is logic high. If SDO2 is enabled when $\overline{CS}$ is brought low after the EOC, the SDO outputs the data from Channel 0, Channel 1, Channel 2, and Channel 3 and SDO2 outputs the data from Channel 4, Channel 5, Channel 6, and Channel 7 after 16 SCK rising edges. The conversion result output on this pin synchronizes to the SCK falling edges. Click **SDO2 DISABLED** once to display **SDO2 ENABLED**.
   - **Update CFG**: If the default configuration (channel, channel configuration, reference, and so on) is acceptable, clicking **Update CFG** writes to the

ADAS3023 configuration register (CFG). Note that after changing any of the CFG register, this button must be clicked for the new setting to take effect.

4. The CFG controls (labeled 4 in Figure 10) are used to set the CFG. See the Software Controls section.
5. **Sampling Frequency** is used to set the sample frequency. Enter the sample rate in kilohertz. Units, such as .5 k (case sensitive) for 500,000 Hz (maximum 500 kSPS), can be used.

Configuring the ADAS3023 Device

The ADAS3023 device is configurable using a 16-bit on-chip register, CFG (refer to the device data sheet for more details).

Remember to select **Update CFG** after choosing CFG details for the new setting to take place. Configure all the selections and then select **Update CFG**.

Input Channel

To select the input channel, make a selection from the pull-down menu.

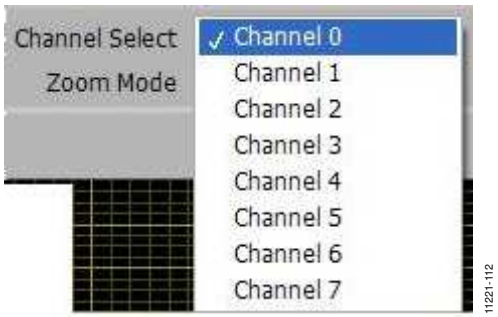

Figure 11. Input Channel

Channel Pairing

The channels can be paired (up to 4 maximum) or all channels can be referenced to the COM input. Note that any input channel including COM has an absolute input range of VDDH − 2.5 V and VSSH + 2.5 V (± high voltage supplies, usually external).

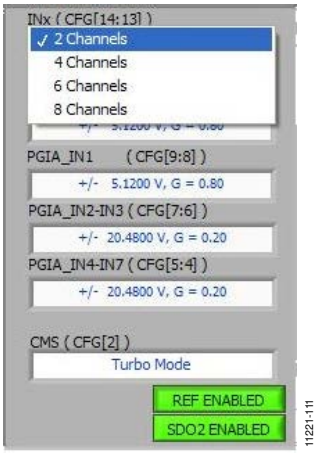

Figure 12. Channel Pairing

Programmable Gain

The most useful and innovative feature of the ADAS3023 is the on-chip programmable gain instrumentation amplifier, which allows four (±2.56 V to ±20.48 V) input ranges. Select the appropriate setting for the input voltage span. Do not include any common-mode signals, which are rejected. Note that the ADAS3023 device does not need the usual level shifting that is common in SAR ADC systems. The ADAS3023 device can accommodate any input type, fully differential, single ended, bipolar, and so on.

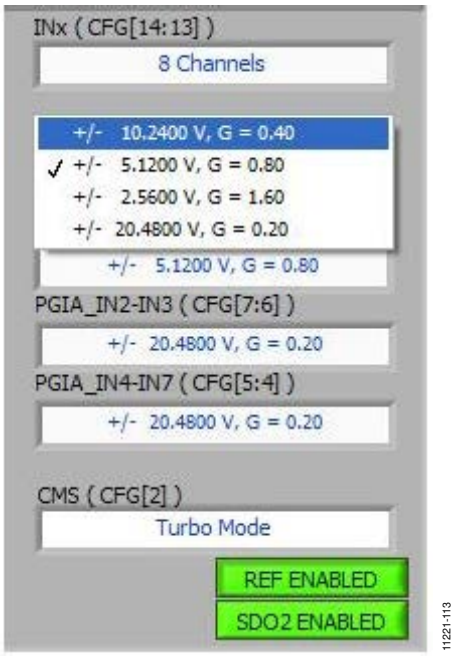

Figure 13. Programmable Gain

Software Controls

Within any of the chart panels, these controls are used to control the display.

Locks the graph axis to automatically fit the data.

Uses last axis set by user.

, Rescales the axes to the automatic values.

, Set the axes properties, such as format, precision, color, and so on.

Displays the cursor.

Is used for zooming in and out.

Is used for panning.

Is used to set various graph properties such as graph type, colors, lines, and so on.

HISTOGRAM TAB

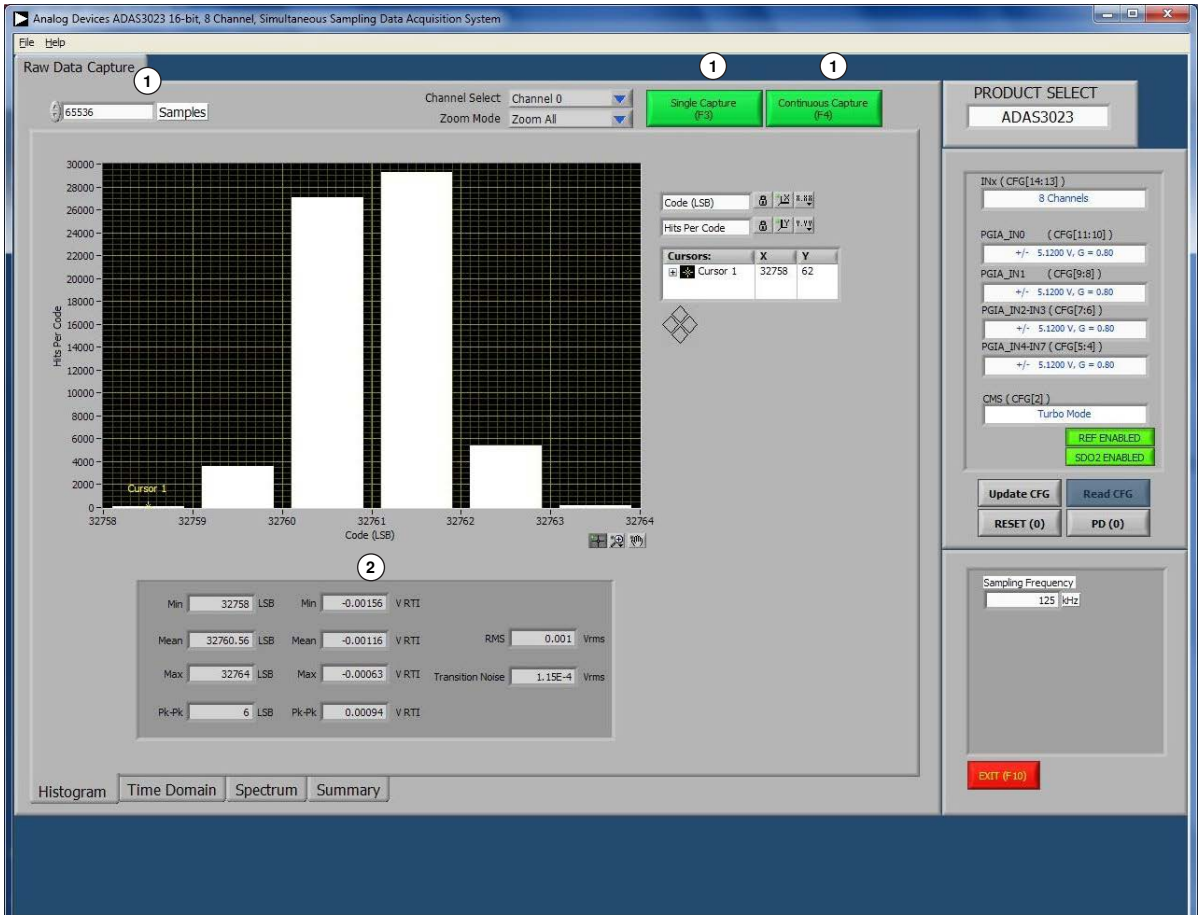

Figure 14. Histogram Screen

Single Capture (F3) and **Continuous Capture (F4)**, labeled 1 in Figure 14, are used to perform a single capture or continuous capture of data in the **Samples** field. Refer to label 2 for histogram statistics in Figure 14. The results are displayed in Figure 15. Note that the results can be displayed as a histogram, in the time domain, or in the frequency domain.

Histogram Display

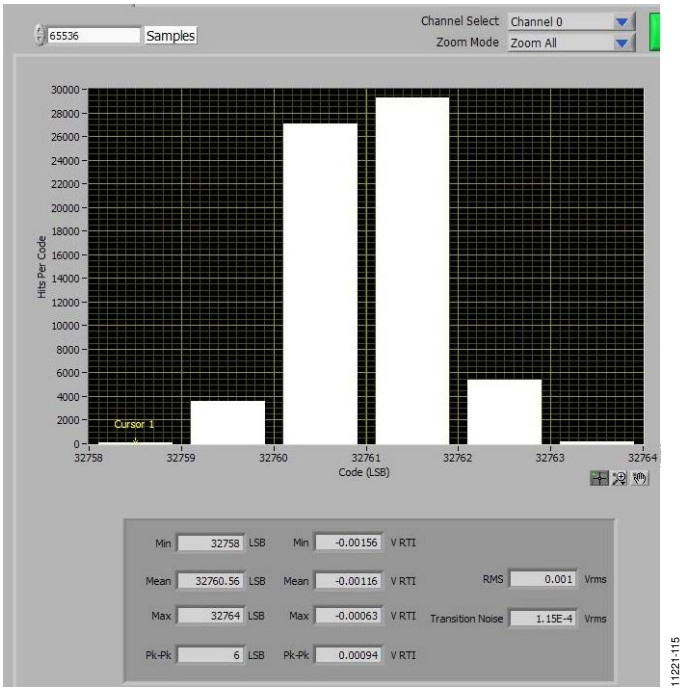

Figure 15. Histogram Display

Note that ADAS3023 output is twos complemented output; however, the software outputs the results in straight binary.

Time Domain Display

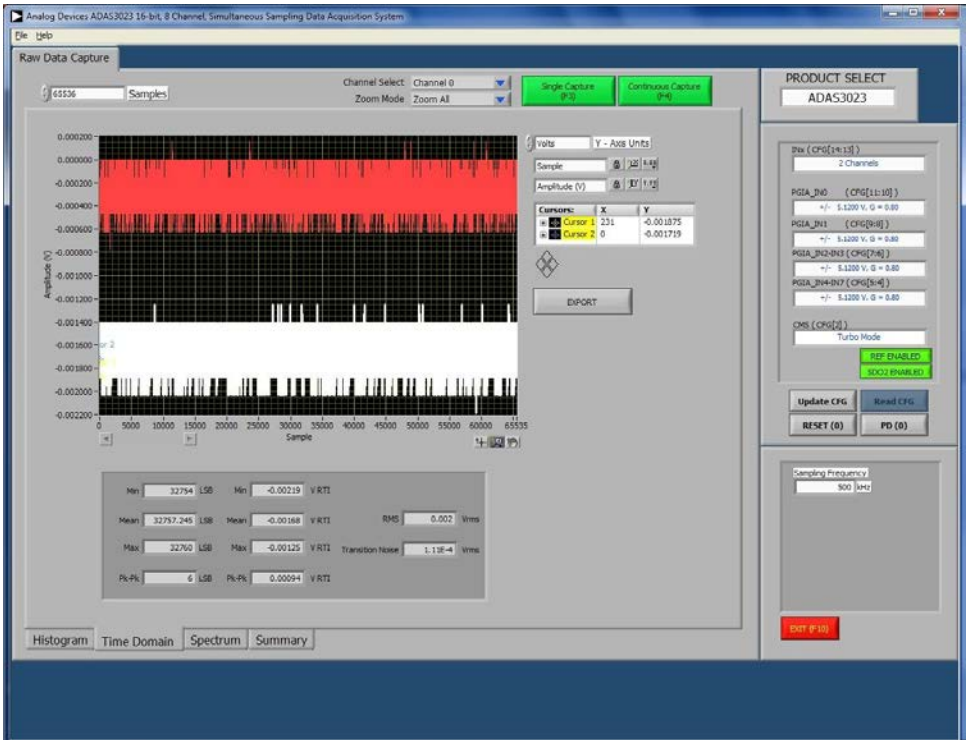

Figure 16. Time Domain Display

Figure 18 display the time domain statistics for the x-axes and y-axes, respectively.

SUMMARY TAB

The charts can be displayed together when the **Summary** tab is selected as shown in Figure 18.

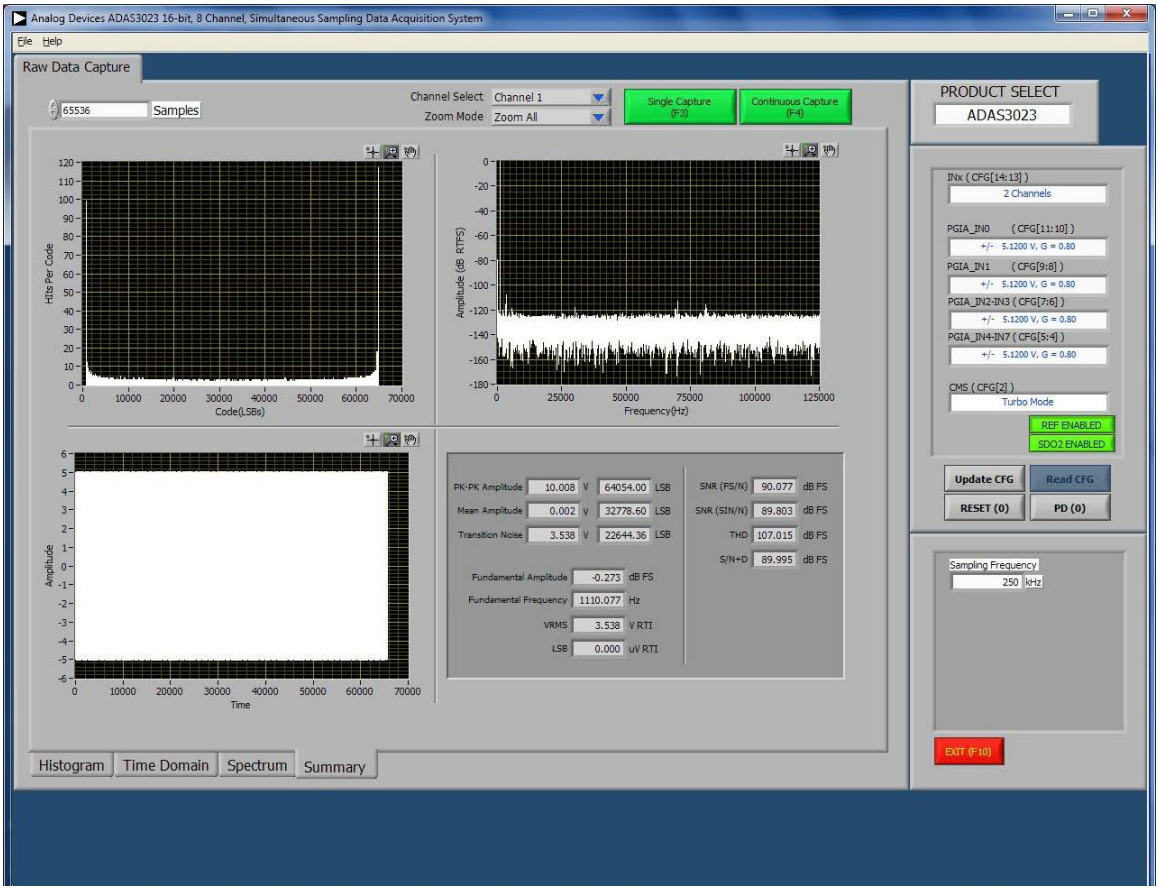

Figure 17. Summary

SPECTRUM TAB

The FFT is displayed when the **Spectrum** tab is selected and the FFT data is shown (see label 2) in Figure 18.

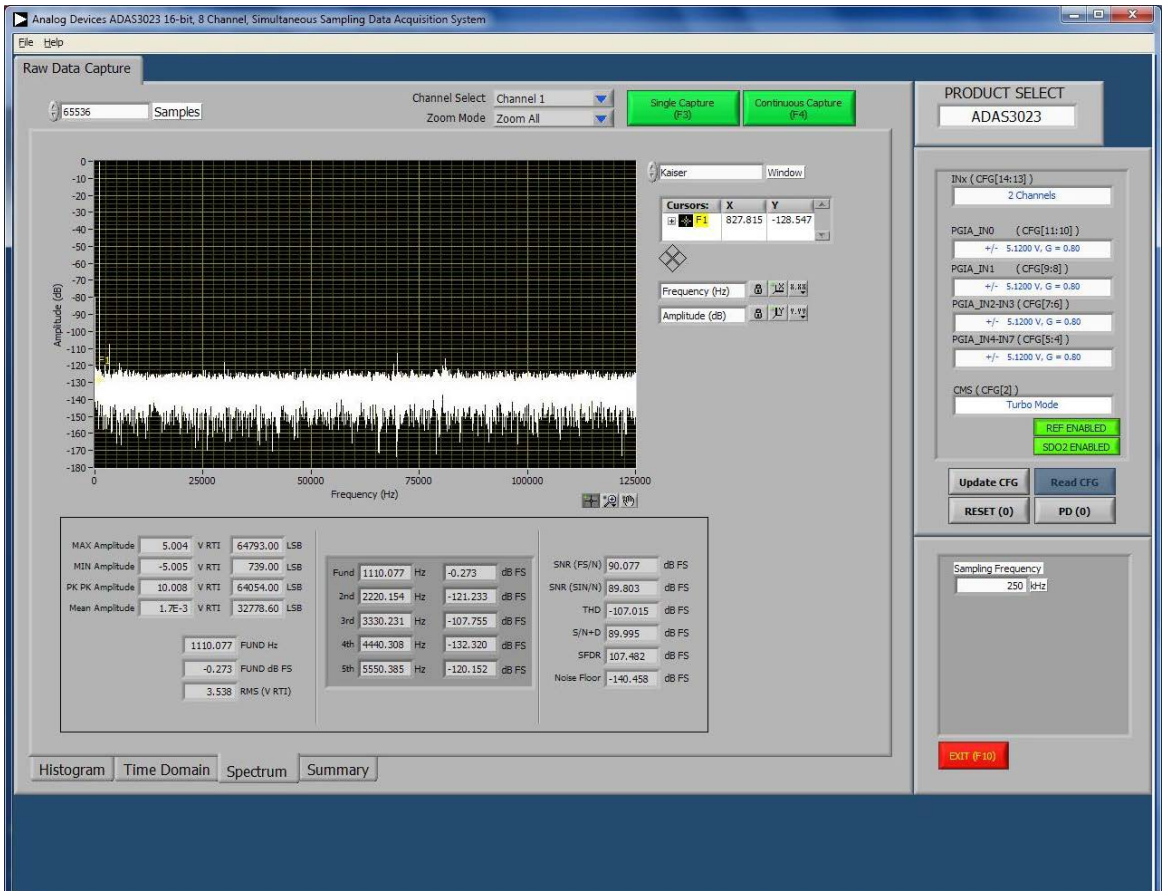

Figure 18. FFT Spectrum

TIME DOMAIN TAB

The time domain (oscilloscope) data is shown in Figure 19 (see label 1).

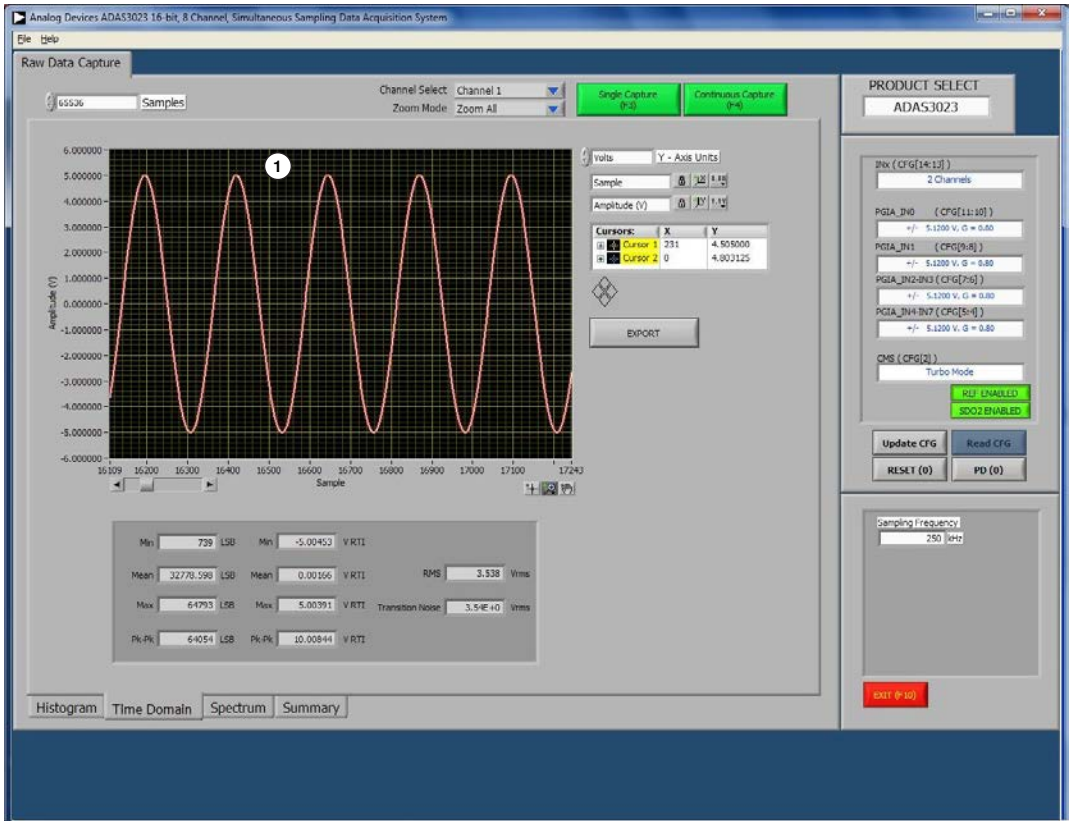

Figure 19. Time Domain

EVALUATION BOARD SCHEMATICS AND ARTWORK

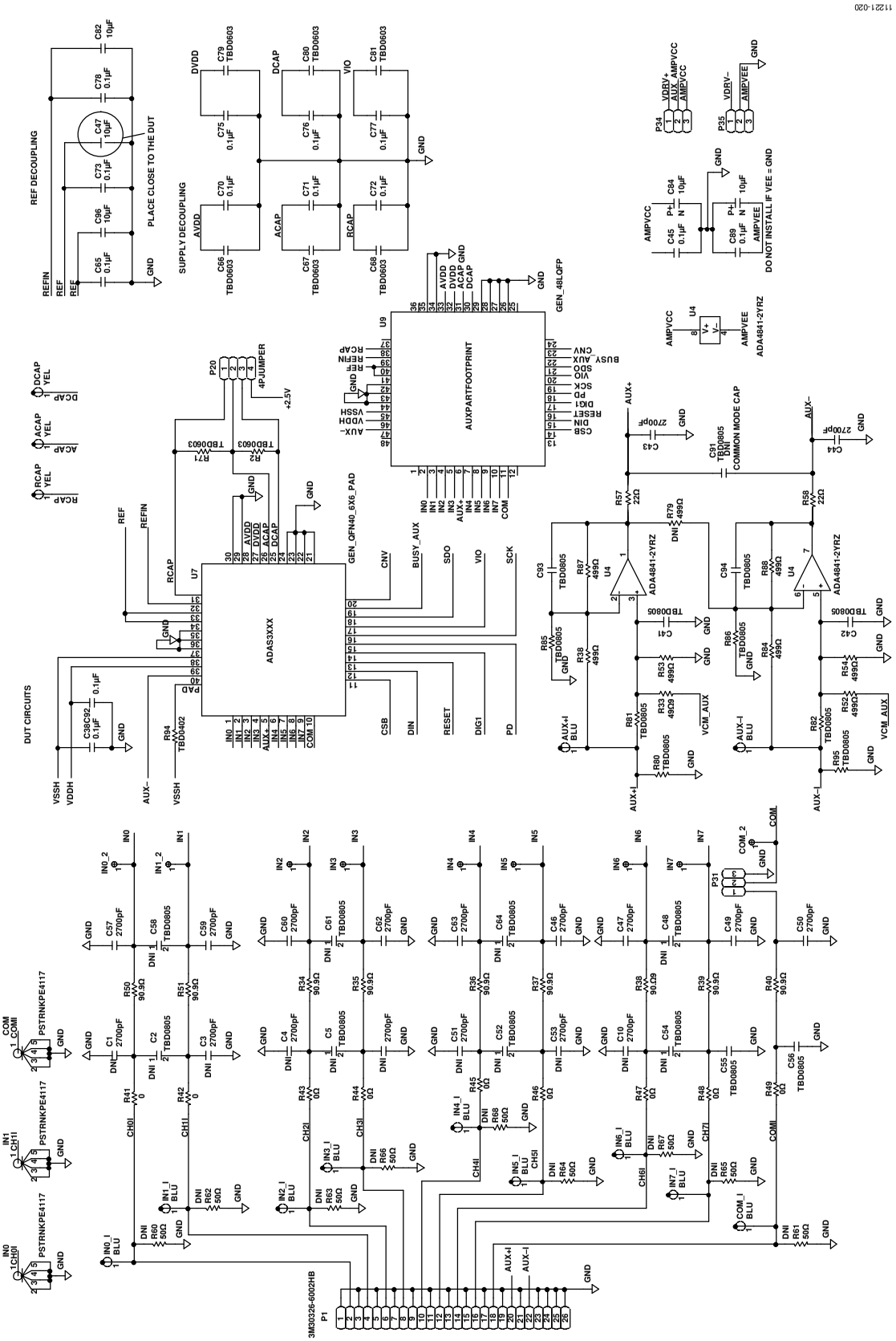

Figure 20. Schematic, DUT, Analog

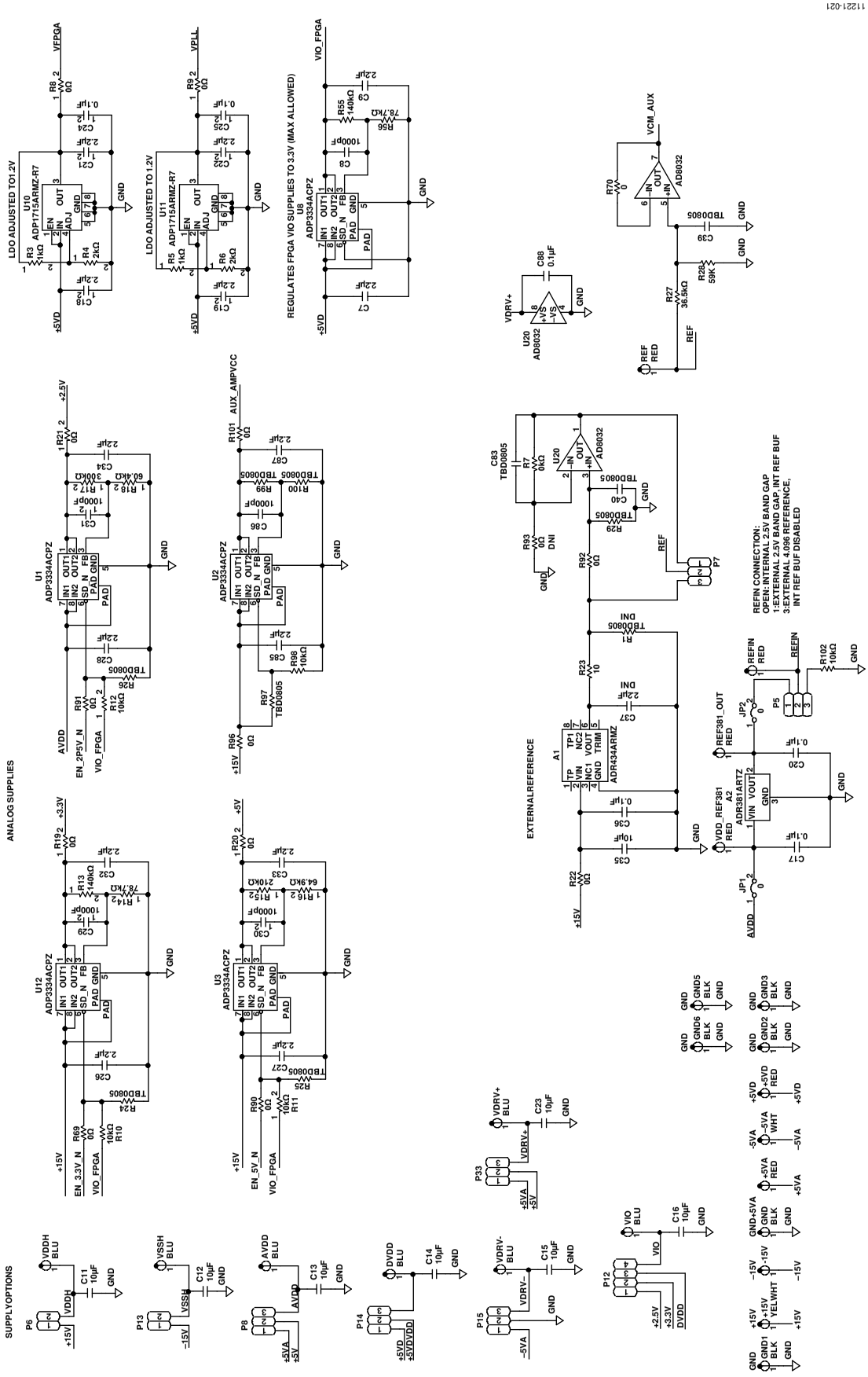

Figure 21. Schematic, Power

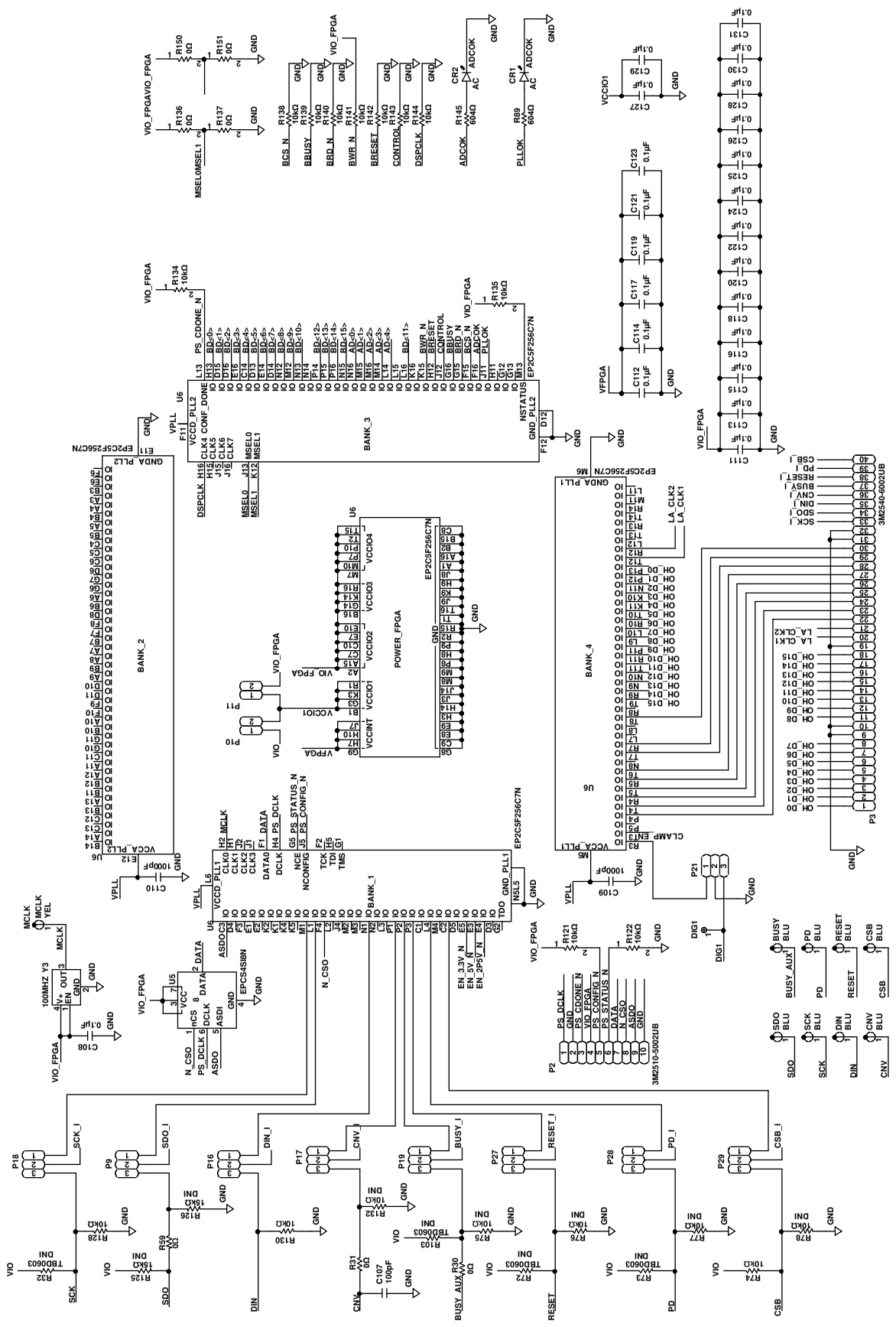

Figure 22. Schematic, FPGA

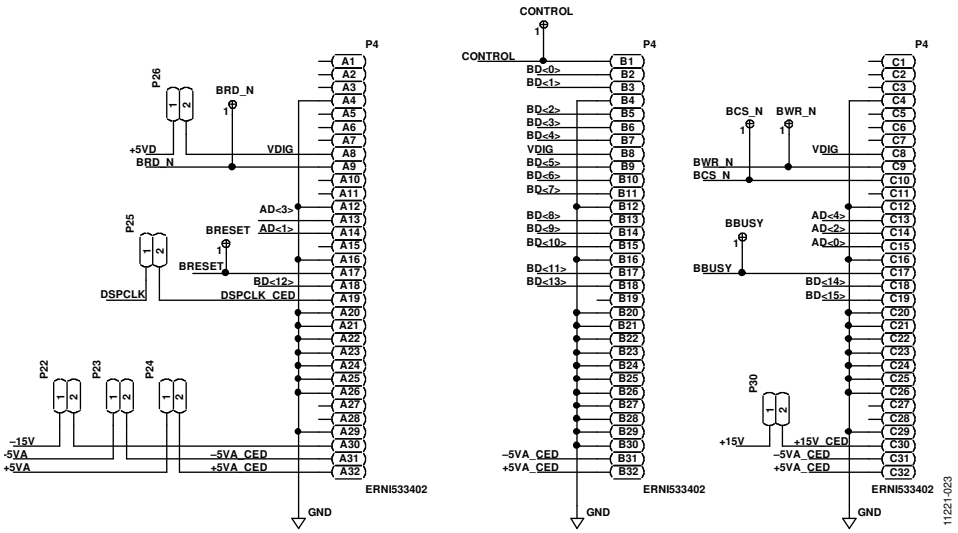

Figure 23. Schematic, 96-Pin Interface

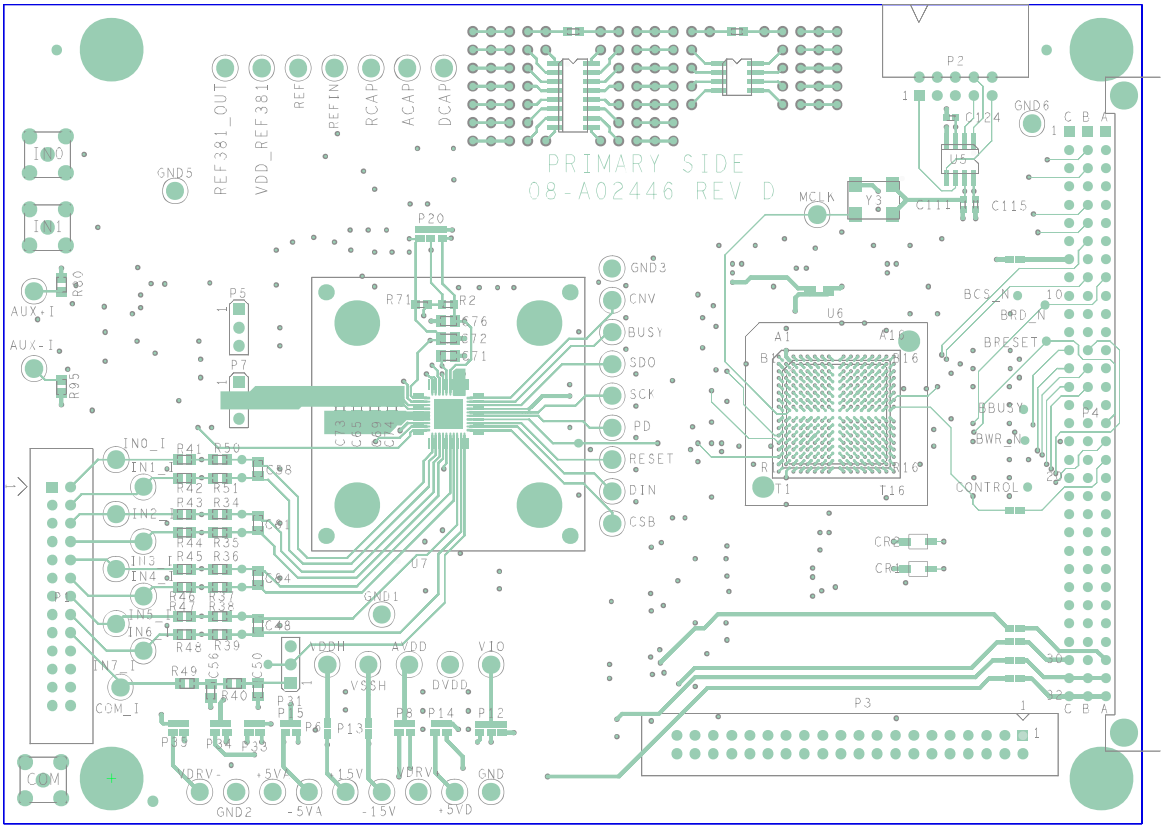

Figure 24. Silkscreen, Top

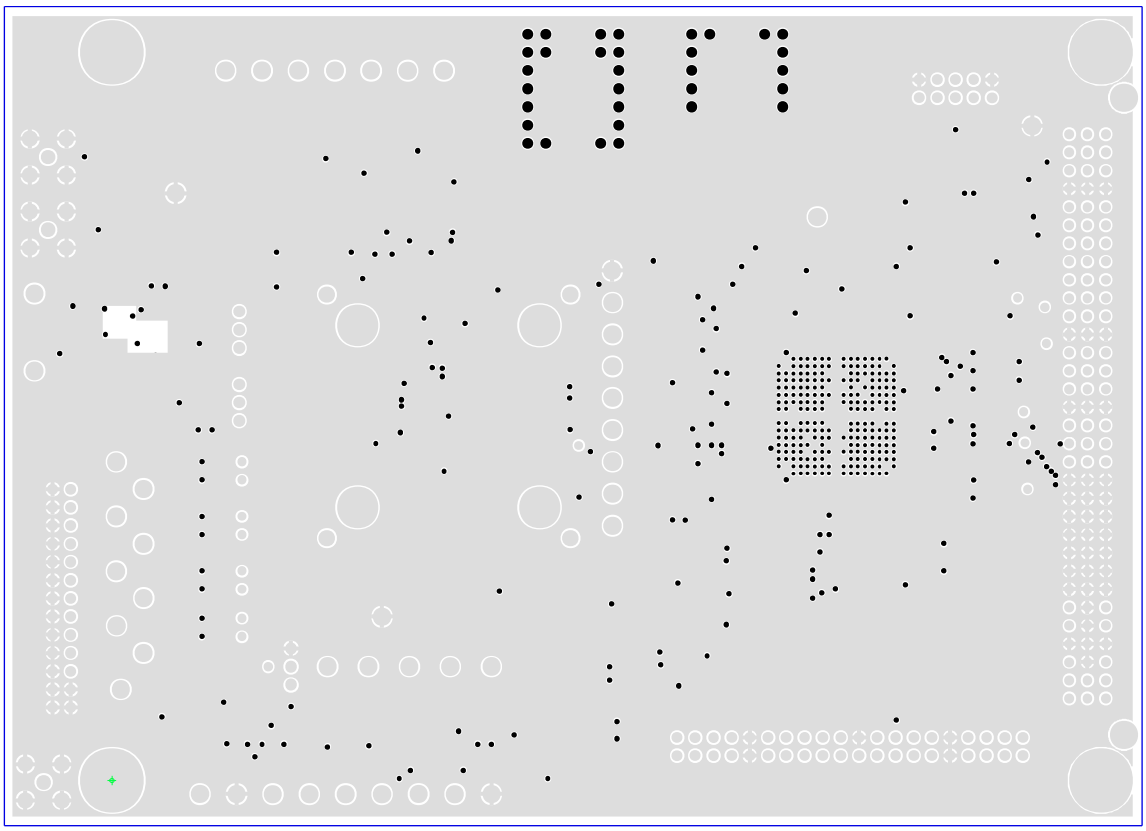

Figure 25. Silkscreen, Bottom

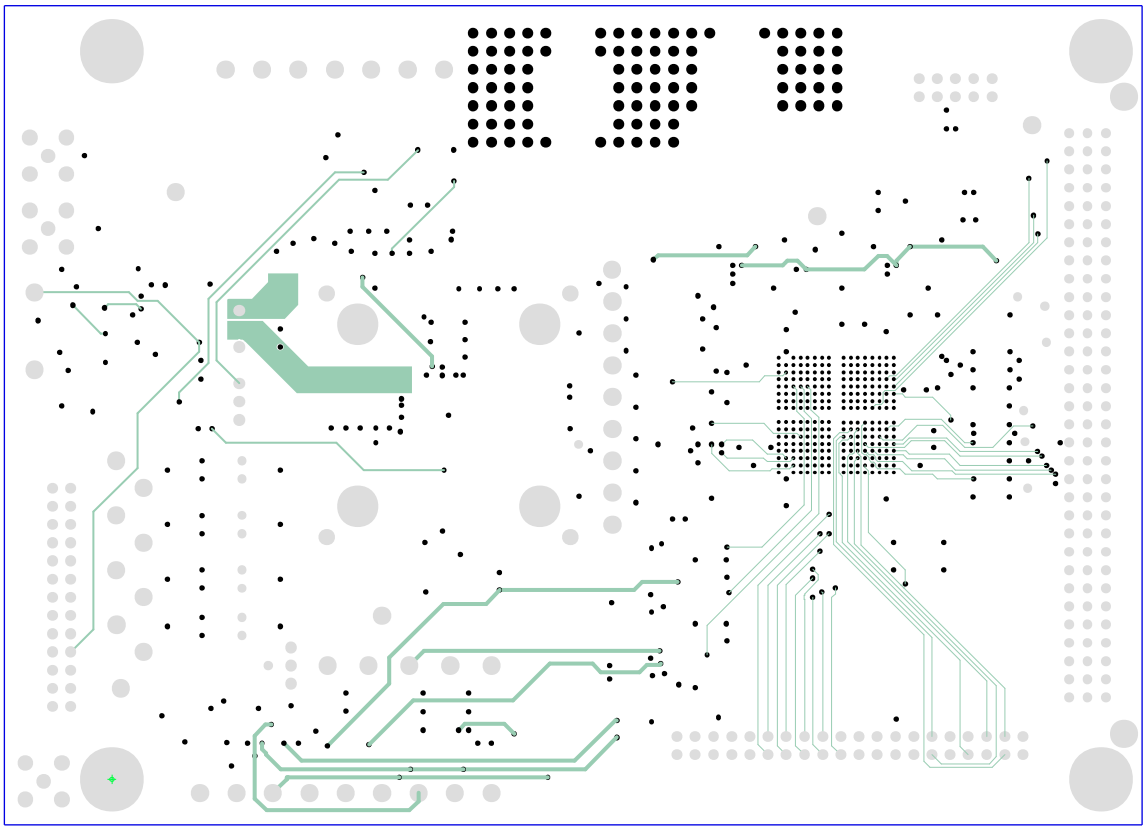

Figure 26. Top Layer 1

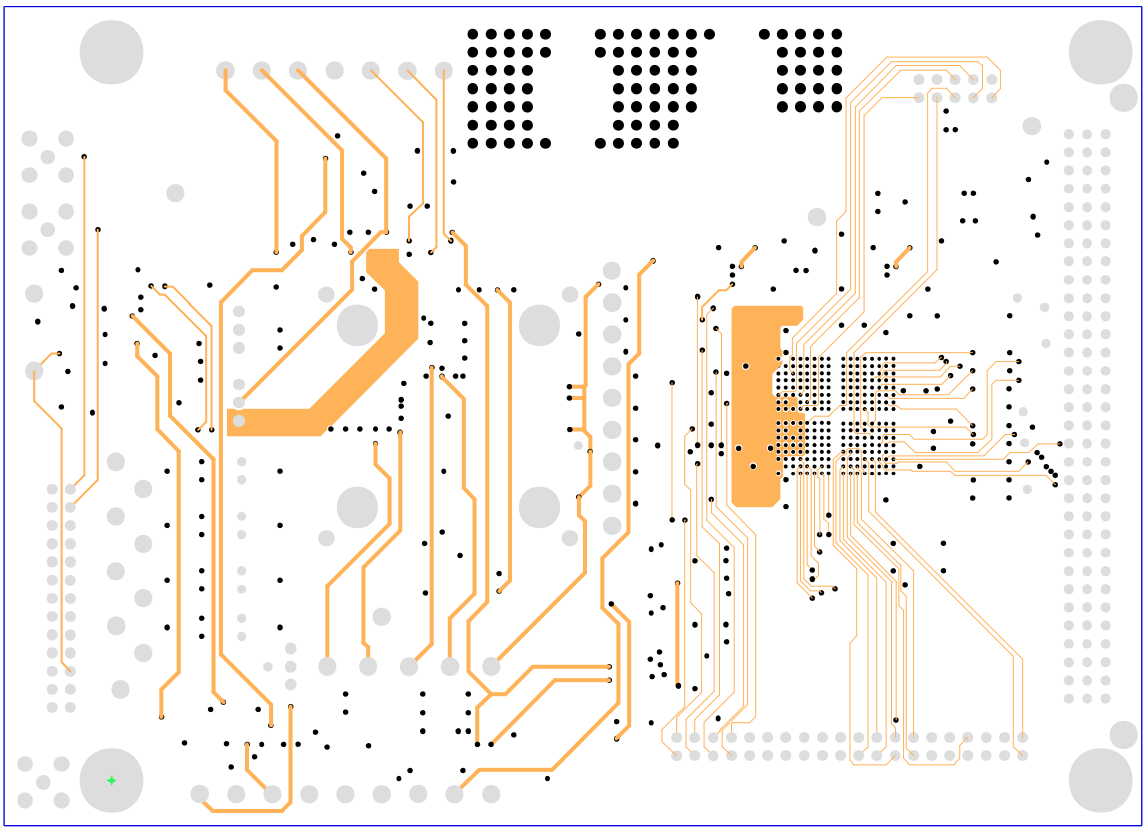

Figure 27. GND Layer 2

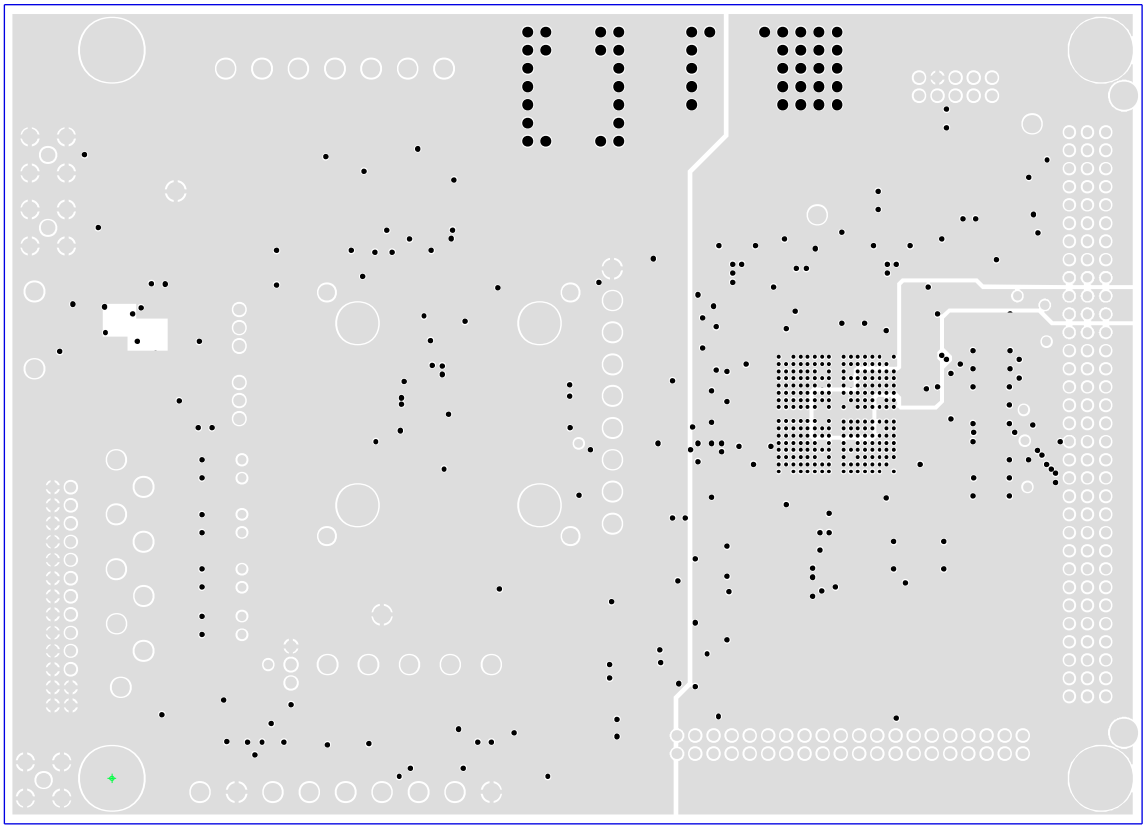

Figure 28. Signal Layer 3

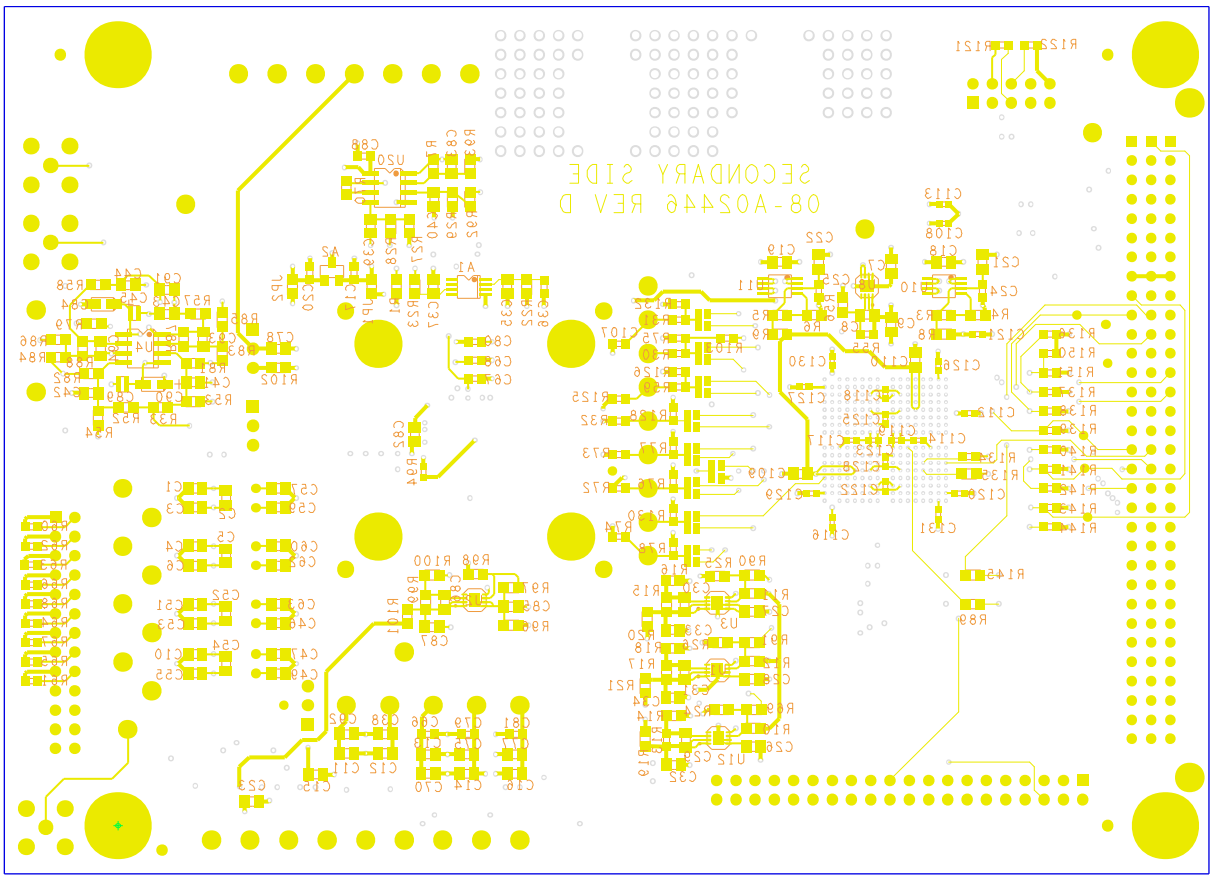

Figure 29. Signal Layer 4

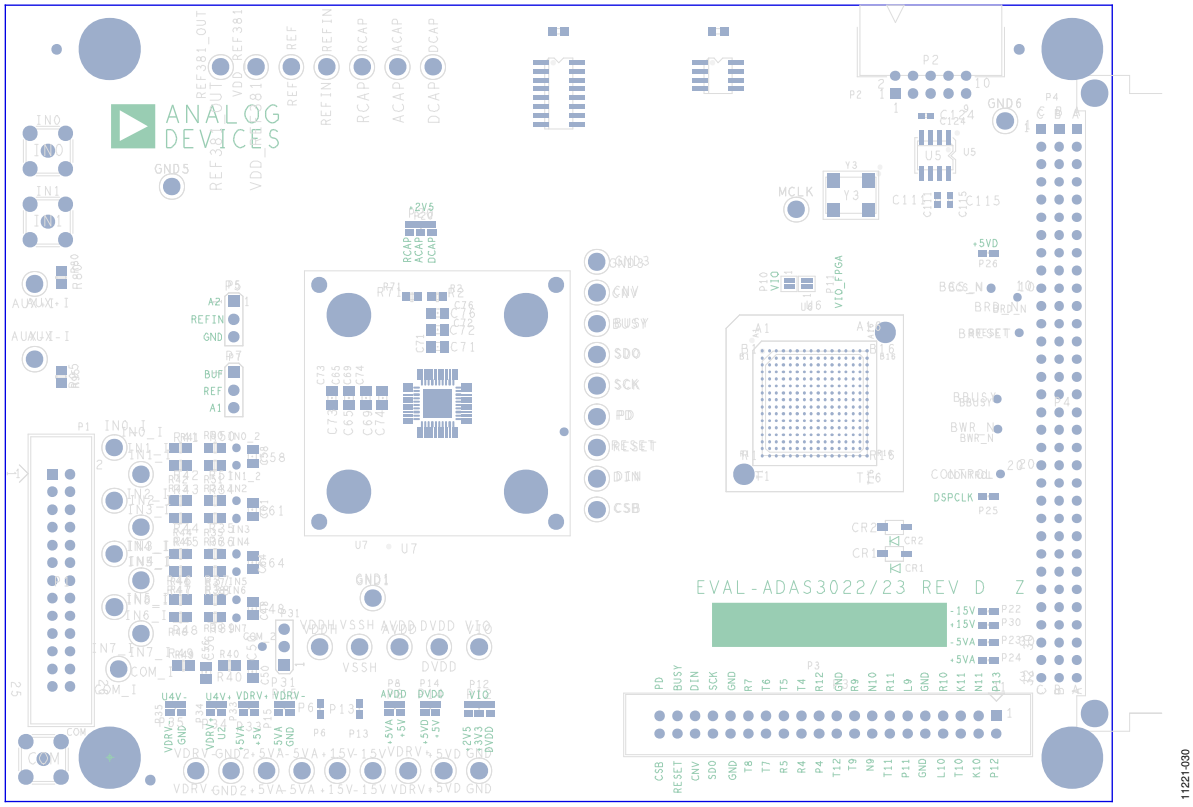

Figure 30. Power Layer 5

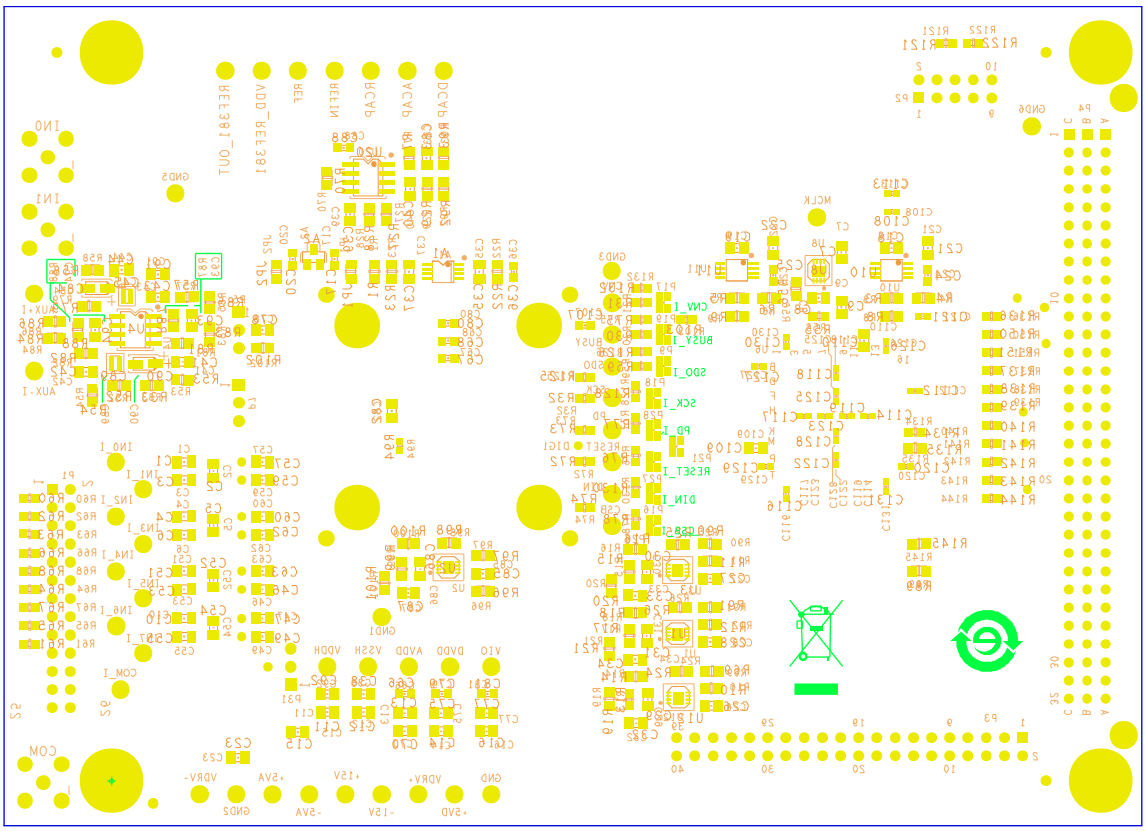

Figure 31. Bottom Layer 6