Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Evaluation Board User Guide
UG-564

One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADAU1962A/ADAU1966A High Performance, Low Power Multibit Sigma-Delta DAC

PACKAGE CONTENTS

ADAU1962A/ADAU1966A evaluation board (EVAL-ADAU1962AZ/EVAL-ADAU1966AZ)
USBi control interface board
USB cable
12 V desktop supply

OTHER SUPPORTING DOCUMENTATION

ADAU1962A data sheet
ADAU1966A data sheet

EVALUATION BOARD OVERVIEW

This user guide describes the design and setup of the evaluation board for the ADAU1962A or the ADAU1966A. This document uses ADAU196xA to refer to either the ADAU1962A or the ADAU1966A. Since the ADAU1962A is a 12-channel part and the ADAU1966A is a 16-channel part, DAC outputs 13 through 16 do not function on the ADAU1962A evaluation board. The evaluation board must be connected to an external 12 V dc power supply and ground. On-board regulators derive 5 V and 3.3 V supplies for the ADAU196xA and peripherals.

The ADAU196xA can be controlled through either an I²C or SPI interface. A small, external interface board, EVAL-ADUSB2EBZ, also called USBi, connects to a PC USB port and provides either I²C or SPI access to the evaluation board through a ribbon cable.

A graphical user interface (GUI) program, the Automated Register Window Builder, is provided for easy programming of the chip in a Windows® PC environment. The evaluation board allows demonstration and performance testing of most ADAU196xA features, including high performance DAC operation.

The board has an S/PDIF receiver with RCA and optical connectors, as well as a discrete serial audio interface. Analog outputs are accessible via eight stereo TRS mini jacks.

FUNCTIONAL BLOCK DIAGRAM

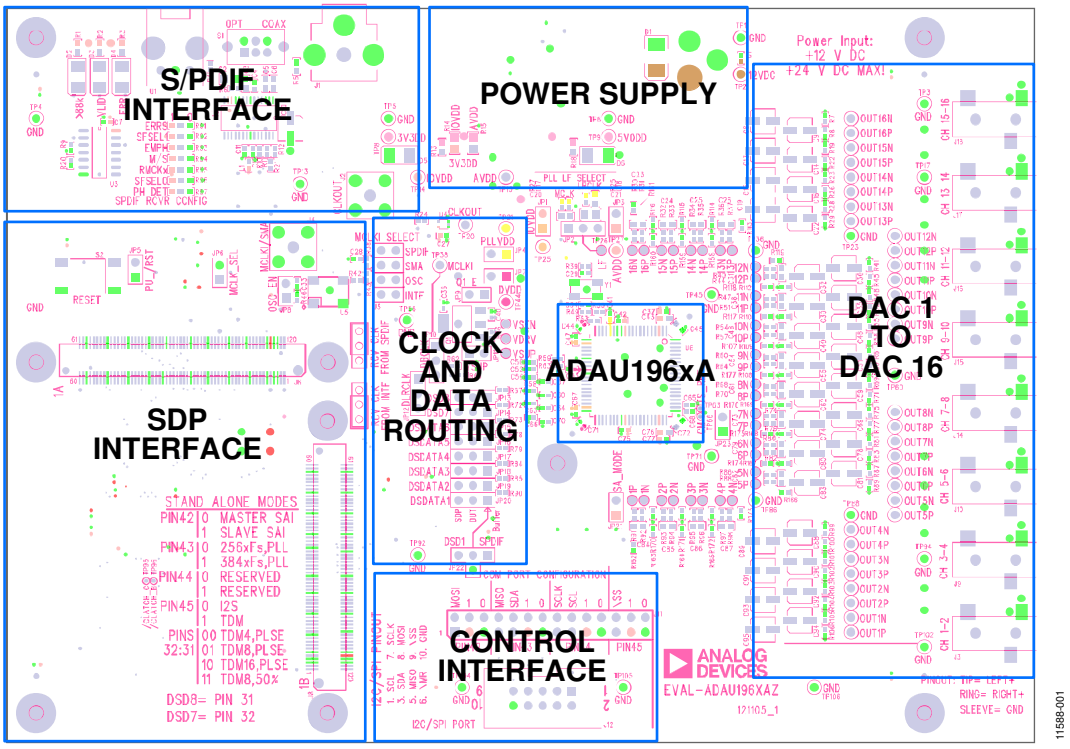


Figure 1.

TABLE OF CONTENTS

Package Contents 1
Other Supporting Documentation 1
Evaluation Board Overview 1
Functional Block Diagram 1
Revision History 2
Setting Up the Evaluation Board 3
Standalone Mode 3
I²C and SPI Control 3
Automated Register Window Builder Software Installation .. 4
Hardware Setup—USBi 4
Powering the Board 5
Resetting the Evaluation Board 5
Setting Up the Master Clock (MCLK) 6
Selecting PLL 6
Routing Digital Audio Connections 7
Connecting Analog Audio Cables 8
Modification for Differential Output 8
Modification to Use the N Output 8
Schematics and Artwork 9
Bill of Material 25

REVISION HISTORY

7/13—Revision 0: Initial Version

SETTING UP THE EVALUATION BOARD

STANDALONE MODE

The ADAU196xA has a standalone mode, which allows the user to choose between a limited number of operation modes without the need for a control interface. Applying a jumper across JP21, as shown in Figure 2, pulls SA_MODE (Pin 46) high enabling standalone mode in the ADAU196xA. The SA_MODE selections are listed in Table 1.

Table 1. Standalone Modes

Pin	Setting	Description
Pin 42	0	Master serial audio interface
	1	Slave serial audio interface
Pin 43	0	256 × f_S
	1	384 × f_S
Pin 44	0	Reserved, set to 0
Pin 45	0	I²S mode
	1	TDM mode
Pin 32 to Pin 31	00	TDM4, pulse
	01	TDM8, pulse
	10	TDM16, pulse
	11	TDM8, 50% duty

On the EVAL-ADAU196xAZ, each of the four control port pins of the ADAU196xA are brought out to a block of jumpers, allowing the user to assign each pin to either the I²C or SPI ports. In standalone mode, these jumpers can connect the individual pins to high (IOVDD) or low (GND) to put the ADAU196xA in the desired mode.

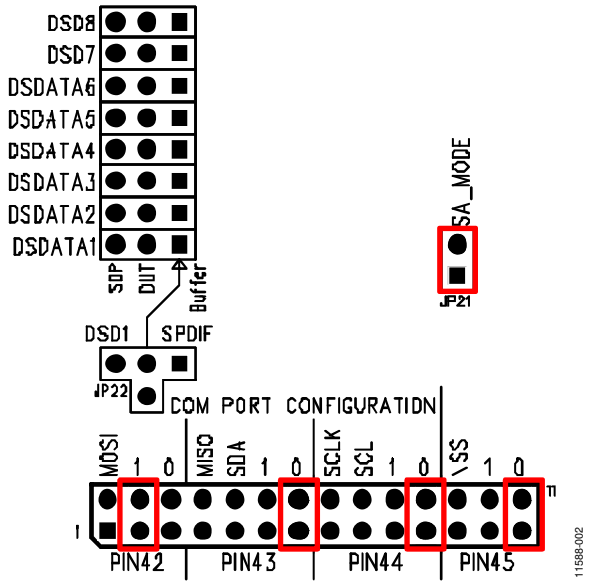


Figure 2. SA_MODE—Slave, 256 × f_S, I²S

The EVAL-ADAU196xAZ arrives configured for S/PDIF input. The S/PDIF receiver operates as a clock master, putting out an I²S stream at 256 × f_S. For quick startup, the ADAU196xA is in standalone mode with the settings shown in Figure 2.

Pin 42 is pulled high (1) and Pin 43 to Pin 45 are pulled low (0). According to Table 1, this puts the ADAU196xA in slave mode, running at 256 × f_S, and the audio serial port in I²S mode. Looking at Figure 2, notice that the jumper for Pin 42 is beneath the label for 1 and the other pins are assigned to 0.

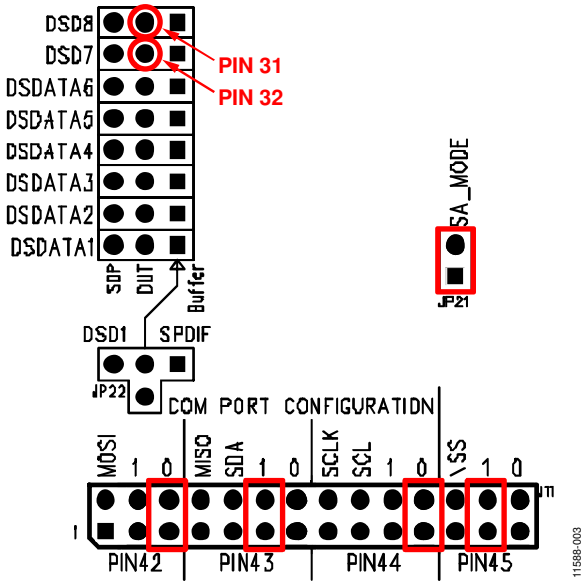


Figure 3. SA_MODE—Master, 384 × f_S, TDM

Figure 3 shows the other options for each SA_MODE configuration pin; master mode, running at 384 × f_S, and the audio serial port in TDM mode. In the case where the ADAU196xA is put in TDM mode, Pin 31 and Pin 32 can be pulled high (IOVDD) or low (GND) to achieve the modes listed in Table 1. The correct pins are located in the top left corner of Figure 3.

I²C AND SPI CONTROL

The evaluation board can be configured for live control over the registers in the ADAU196xA. When the Automated Register Window Builder software is installed and the USBi control interface is plugged into the board, the software can control the ADAU196xA. For this configuration, the ADAU196xA must be assigned to I²C mode using Address 00. See Figure 4 for the correct jumper positions.

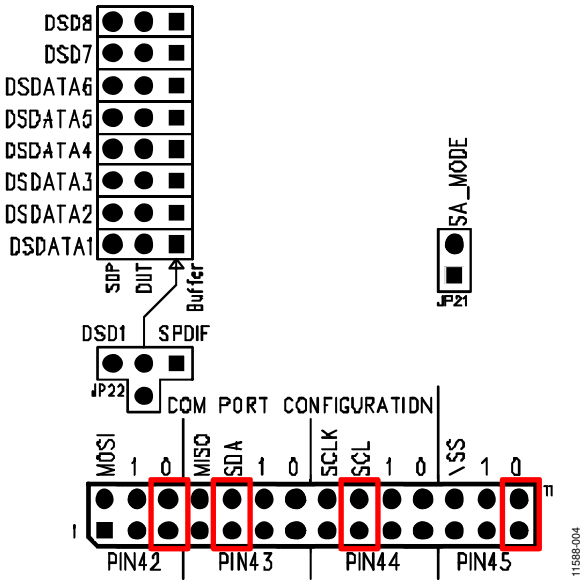


Figure 4. ADAU196xA I²C Control, Address 00

The Automated Register Window Builder controls the ADAU196xA and is available for download at **www.analog.com/ADAU1962A** or **www.analog.com/ADAU1966A**.

The ADAU196xA can also be put in SPI mode for control by other means. See Figure 5 for the correct jumper positions.

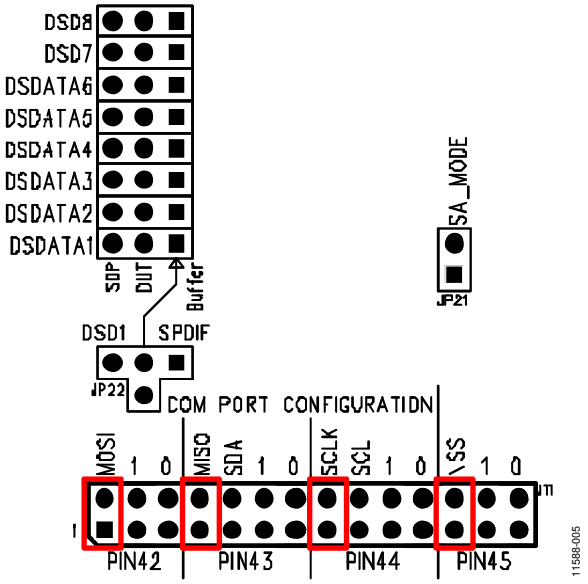


Figure 5. ADAU196xA SPI Control

AUTOMATED REGISTER WINDOW BUILDER SOFTWARE INSTALLATION

The Automated Register Window Builder is a program that launches a graphical interface for direct, live control of the ADAU196xA registers. The GUI content for a specific part is defined in a part-specific .xml file; these files are included in the software installation.

To install the Automated Register Window Builder software, follow these steps:

1. Go to **www.analog.com/ADAU1962A** or **www.analog.com/ADAU1966A** and download the **ARWBvXX.zip** file from the product page.
2. Open the downloaded **ARWBvXX.zip** file and extract the files to an empty folder on your PC.
3. Install the Automated Register Window Builder by double-clicking **setup.exe** and following the prompts. A computer restart is not required.
4. Copy the .xml file for the ADAU196xA from the extraction folder into the folder **C:\ProgramFiles\Analog Devices Inc\AutomatedRegWin**, if it is not already installed.

HARDWARE SETUP—USBi

To set up the USBi hardware, follow these steps:

1. Plug the USBi ribbon cable into the J12 I²C/SPI port.
2. Connect the USB cable to your computer and to the USBi.
3. When prompted for drivers,
   a. Choose **Install from a list or a specific location**.
   b. Choose **Search for the best driver in these locations**.
   c. Check the box for **Include this location in the search**.
   d. Find the USBi driver **C:\Program Files\Analog Devices Inc\AutomatedRegWin\USB drivers**.
   e. Click **Next**.
   f. If prompted to choose a driver, select **CyUSB.sys**.
   g. If the PC is running Windows® XP and a message appears stating that the software has not passed Windows logo testing, click **Continue Anyway**.

You can now open the Automated Register Window Builder application and load the .xml file for the part on your evaluation board. Plug the 10-way ribbon cable on the USBi into the I²C/SPI port (J12) on the evaluation board.

POWERING THE BOARD

The EVAL-ADAU196xAZ evaluation board requires a power supply input of +12 V dc and ground to the power jack; +12 V draws ~150 mA at higher sample rates with all channels running.

The on-board regulators provide 5 V and 3.3 V rails. The 5 V rail is derived from +12 V by a switching regulator; it supplies 5 V for the 3.3 V power supply and other peripherals via the SDP interface optional resistors R133 and R156. The 3.3 V rail is derived from the 5 V supply by an LDO linear regulator; it provides voltage to AVDD and IOVDD as well as other active peripherals.

AVDD and IOVDD are connected on the board using 0R00 Ω 0805 package resistors. Should a need arise to insert a different power source, or measure current draw of the entire board, it can be accomplished using these 0 Ω jumpers.

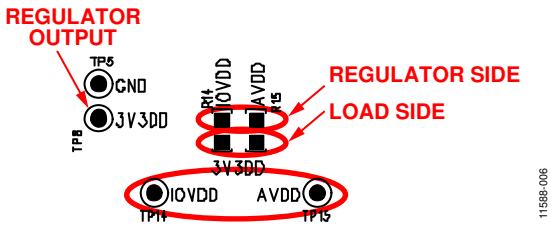


Figure 6. AVDD and IOVDD Jumper Resistors

The ADAU196xA has an internal voltage regulator that allows the user to derive DVDD and PLLVDD from the AVDD voltage source. The external PNP transistor Q1 and and the passives, C36, C40, and R56, make the regulator circuit shown in Figure 7. Both JP9 and JP11 must be shorted to activate the circuit; JP9 supplies the emitter of the PNP and JP11 powers VSUPPLY (Pin 25) on the ADAU196xA.

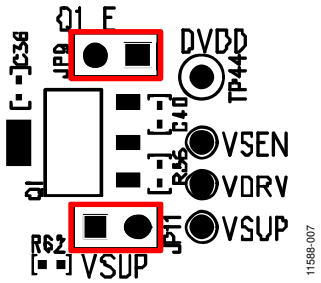


Figure 7. ADAU196xA Internal Regulator Jumpers

Links are provided along each ADAU196xA power rail to provide access for current measurement of only the ADAU196xA (see Figure 8). These links also allow the user to directly supply voltage from an outside source. The square pins and the test points are the load side. All four links must be connected for proper operation.

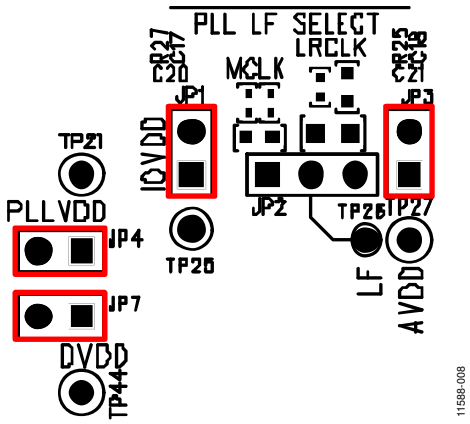


Figure 8. ADAU196xA Power Links

RESETTING THE EVALUATION BOARD

The EVAL-ADAU196xAZ has provisions for resetting and powering down the ADAU196xA. S2 on the evaluation board, shown in Figure 9, is a momentary reset switch that pulls the master reset ($\overline{MR}$) line low; this line controls the reset generator U10. $\overline{MR}$ is also connected to the USBi and the SDP interface connectors through steering diodes and protection resistors so that outside devices can control the reset state of the evaluation board as shown in Figure 25. The power-down jumper JP5 allows the $\overline{MR}$ line to be tied low. The output of the reset generator drives the PU/$\overline{RST}$ line.

The PU/$\overline{RST}$ line is directly connected to two devices: the S/PDIF receiver and the ADAU196xA. The line is held low by a pull-down resistor until the reset generator U10 asserts the line high as shown in Figure 25. The PU/$\overline{RST}$ line is also connected to a pin on the SDP interface through a steering diode and protection resistor allowing external reset control.

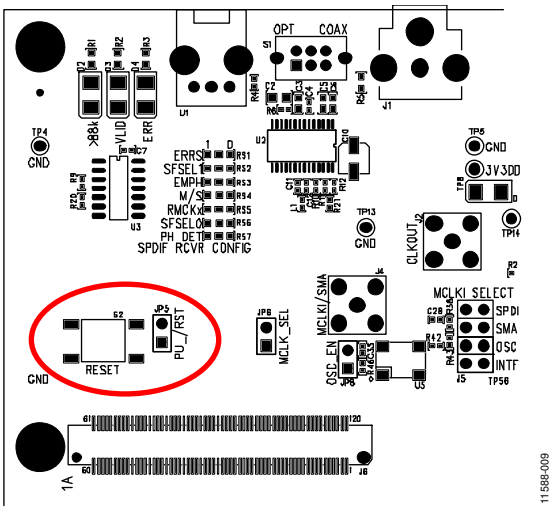


Figure 9. Reset Switch and Power-Down Jumper

SETTING UP THE MASTER CLOCK (MCLK)

The MCLK routing on the evaluation board is handled by a block of jumpers, J5, allowing any one of four sources to be selected—S/PDIF, the SMA connector, active OSC, and the INTF connector. The board arrives with S/PDIF selected as shown in Figure 10.

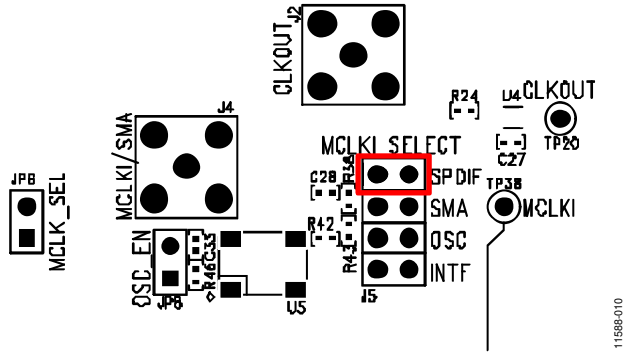


Figure 10. SPDIF Selected as MCLK Source

The evaluation board has a 12.288 MHz active oscillator that can be selected by shorting the OSC_EN jumper JP8 and selecting OSC on J5 as shown in Figure 11.

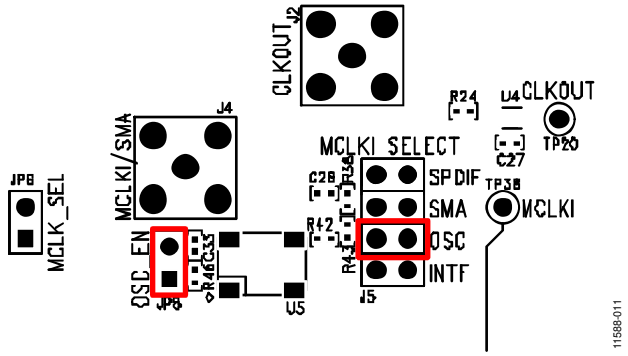


Figure 11. Active OSC Enabled and Selected as MCLK

The evaluation board can be set to receive MCLK from the SDP interface connectors. To do so, select the INTF setting on J5 and enable the MCLK buffer by shorting jumper J6, MCLK_SEL, as shown in Figure 12.

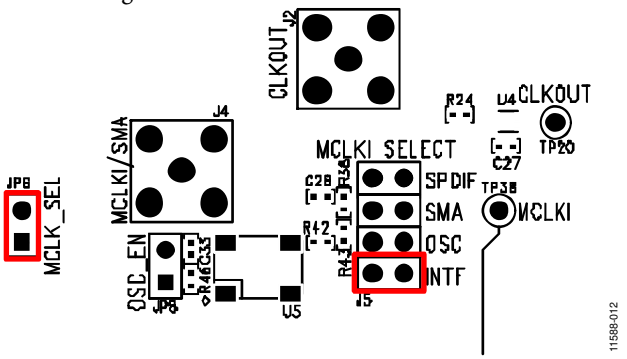


Figure 12. INTF Input Enabled and Selected

SELECTING PLL

The PLL in the ADAU196xA is very flexible, allowing the part to run from a wide range of either MCLK or LRCLK frequencies.

It is also possible to shut the PLL off altogether and use the part in direct lock mode; functionality with no PLL is limited to 256 × f_S.

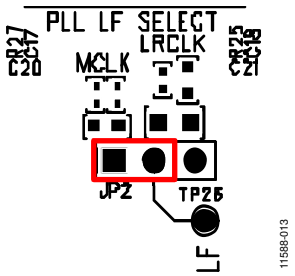


Figure 13. MCLK Selection for PLL Loop Filter

By default, the ADAU196xA runs from the PLL using MCLK as the clock source. The MCLK loop filter must be selected using JP2 as shown in Figure 13.

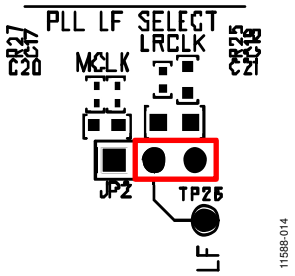


Figure 14. LRCLK Selection for PLL Loop Filter

DLRCLK can be selected as the PLL clock source using the PLL and Clock Control 0 Register [7:6]. In this case, the LRCLK loop filter must be selected as shown in Figure 14. If DLRCLK is selected as the PLL clock, there is no need for an MCLK.

ROUTING DIGITAL AUDIO CONNECTIONS

The ADAU196xA evaluation board has two separate inputs for digital audio signals: the S/PDIF and the SDP interface.

The S/PDIF receiver can handle either of two options: S/PDIF uses the RCA jack, J1, and optical uses the Toslink jack, U1. The input is selected using S1 as shown in Figure 15.

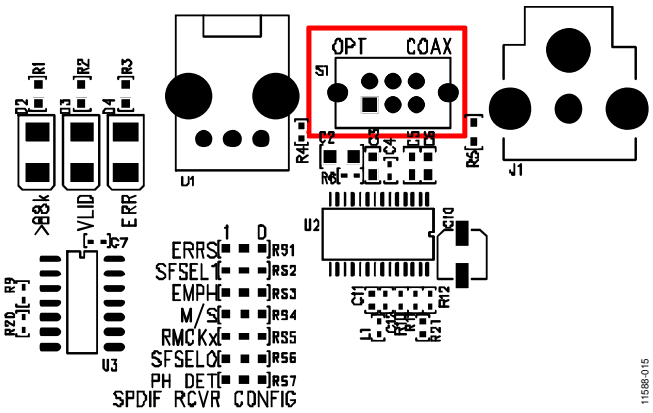


Figure 15. S/PDIF Input Selector Switch SW1

A series of resistors have been provided to set the functional mode of the S/PDIF receiver as shown in Figure 16. By default, the S/PDIF receiver runs in master mode, 256 × f_S, I²S format. Consult the data sheet for the S/PDIF receiver to make the required changes to the hardware mode.

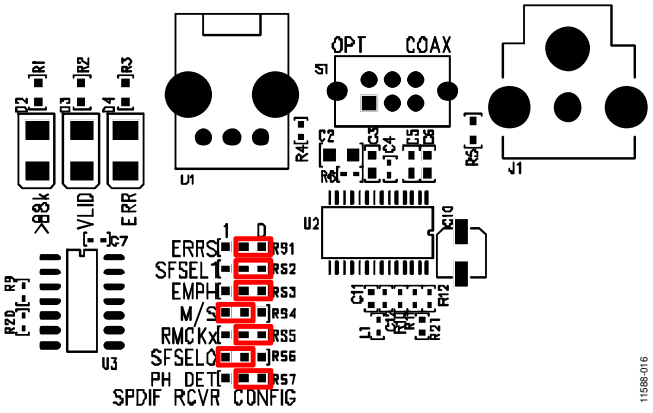


Figure 16. S/PDIF Mode Selection Resistors

The jumpers shown in Figure 17 are set for the S/PDIF receiver to drive the DBCLK and DLRCLK clock ports and the eight DSDATAx lines of the ADAU1962A/ADAU1966A. JP22 selects the input to a buffer; the output of this buffer shows up on the right-hand column of JP13 to JP20.

The pins in the middle column of these jumpers are connected to the DSDATAx pins of the ADAU196xA through the appropriate line termination. DBCLK and DLRCLK selections are made with JP10 and JP12 where the middle pins are connected to the DBCLK and DLRCLK pins of the ADAU196xA.

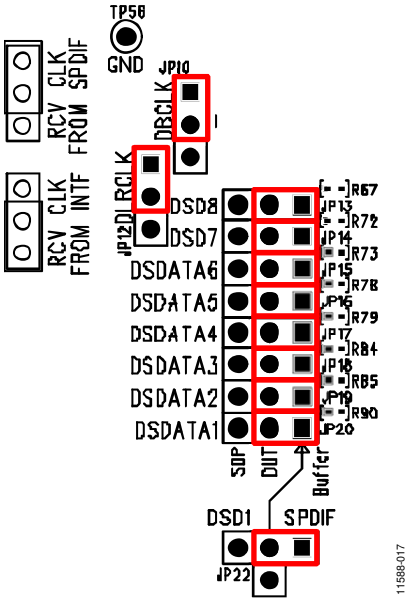


Figure 17. S/PDIF Data and Clock Routing

The system development platform (SDP) interfaces, J6 and J8, make up a standard interconnect within Analog Devices, Inc. They provide for the transfer of digital audio clocks and control between boards. See the pinout included in the schematic in Figure 27.

Figure 18 shows the jumper configuration for using the SDP interface connector as the digital audio source. JP22 is set so that the DSDATA1 source from the SDP interface is driving the buffer, and this buffer is connected to all eight DSDATA inputs of the ADAU196xA. JP10 and JP12 are set for the ADAU196xA to run in slave mode from clocks supplied by the SDP interface.

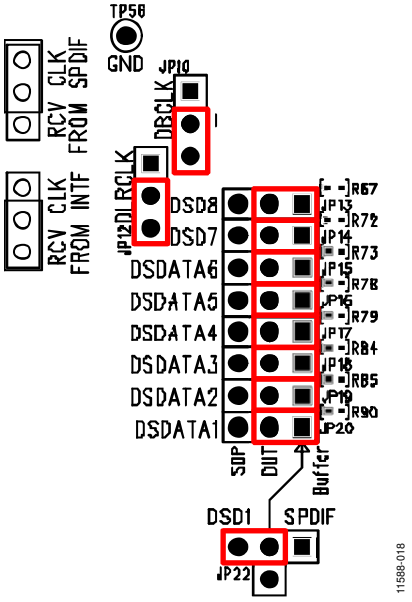


Figure 18. SDP Interface DSDATA1 Distribution

CONNECTING ANALOG AUDIO CABLES

There are two forms of the analog outputs of the ADAU196xA evaluation board: differential and single ended.

The board comes standard with the single-ended outputs appearing on through-hole test points as well as on the TRS mini connectors.

The single-ended outputs of the ADAU196xA drive the connectors directly, through a simple 1-pole RC filter with appropriate ac coupling.

To evaluate the differential outputs, one can modify the board to accomplish this with a little soldering and a few parts.

MODIFICATION FOR DIFFERENTIAL OUTPUT

The ADAU196xA evaluation board can be modified to be used differentially.

See Figure 19 for the schematic of the standard filter. To modify for balanced operation, perform the following steps for each channel:

1. Remove R6 (0 Ω jumper).
2. Change R1 from 470 Ω to 237 Ω (0402).
3. Add R2 (237 Ω, 0402).
4. Add C3 (10 µf).
5. Add R4 (49.9 kΩ, 0402).

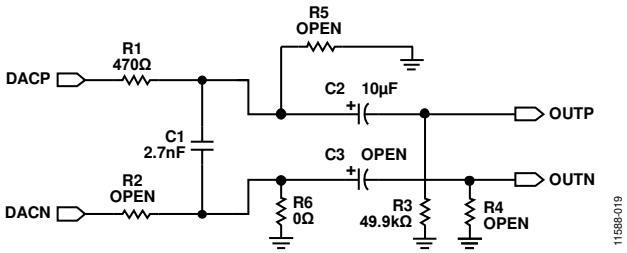


Figure 19. Typical Evaluation Board Filter

MODIFICATION TO USE THE N OUTPUT

The ADAU196xA evaluation board can be modified to use the DACN output instead of the DACP output. Should you need to invert all the channels, it is recommended to do so in the software using the DAC CONTROL 2 Register or by inverting the I^2S data stream.

See Figure 19 for the schematic of the standard filter. To modify to use the N output, perform the following steps for each channel:

1. Move R6 over to R5 (0 Ω jumper).
2. Move R1 over to R2 (470 Ω).
3. Move C2 over to C3 (10 µF).
4. Move R3 over to R4 (49.9 kΩ).
5. Install a jumper between the N and P output test points.

Note that if new parts are to be used for R2, R4, R5, and C3, then R1, R3, R6, and C2 must be removed.

SCHEMATICS AND ARTWORK

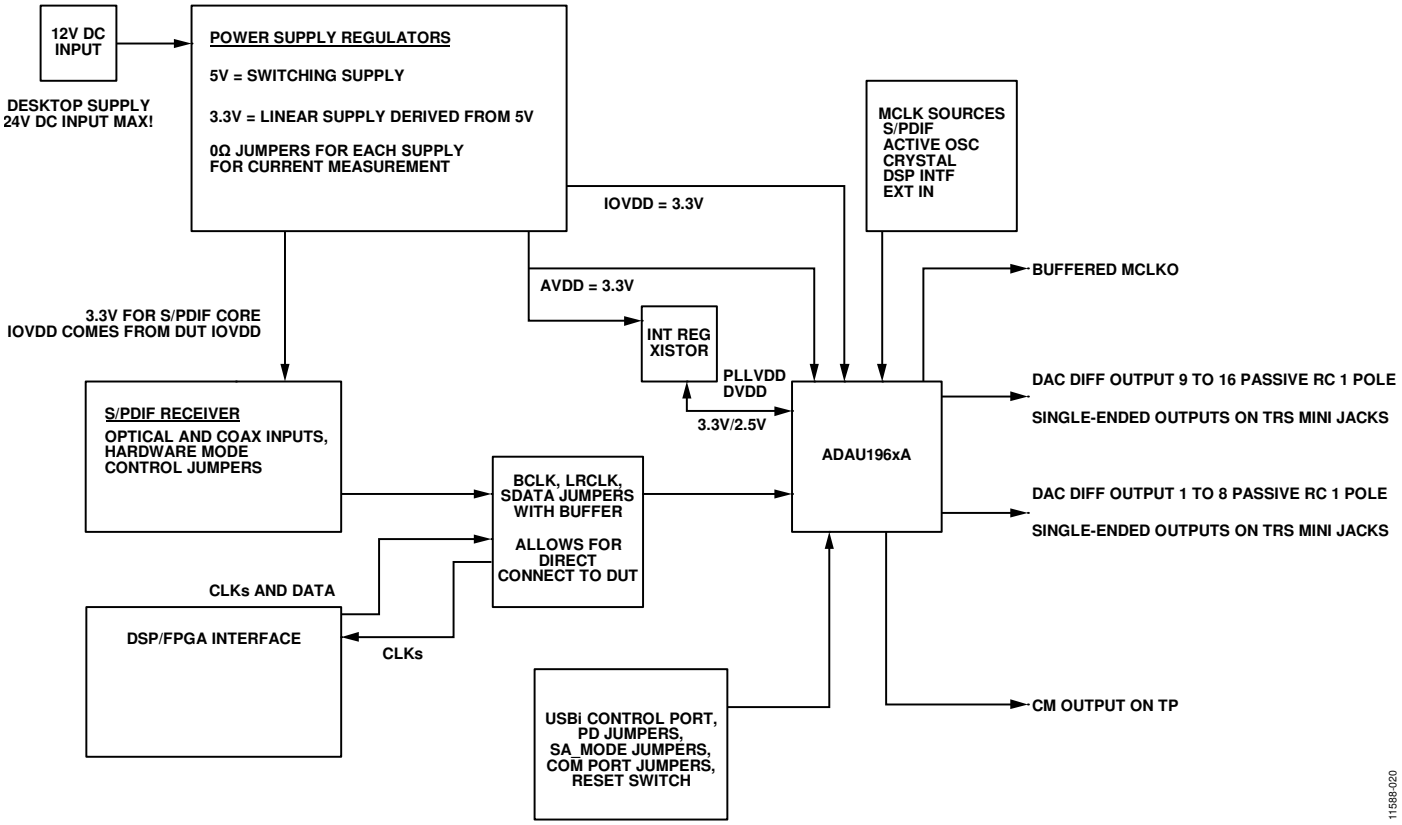


Figure 20. Schematic, Page 1—EVAL-ADAU196xAZ Block Diagram

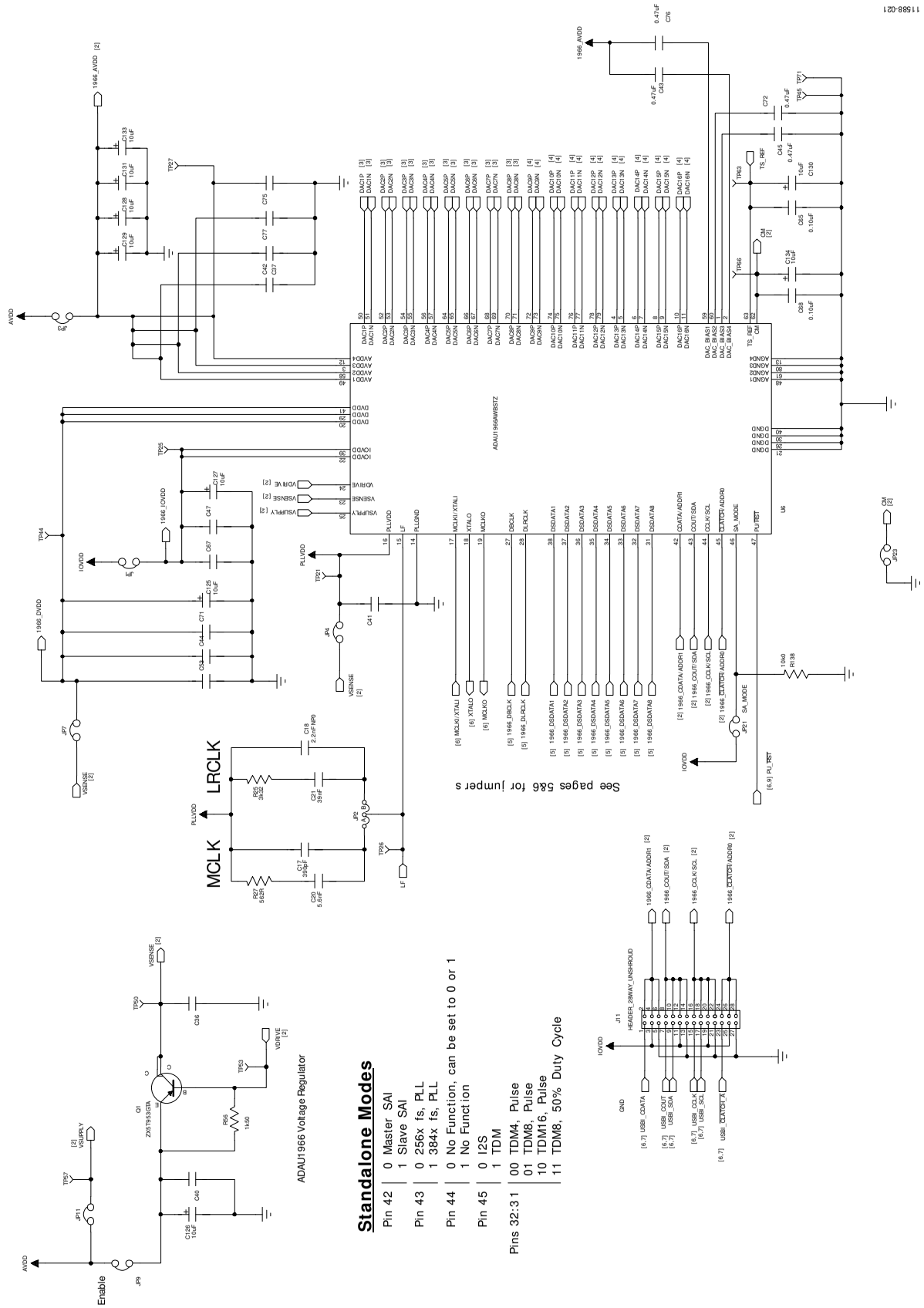


Figure 21. Schematic, Page 2—ADAU196xA, PLL Loop Filter (LF) Selection and Internal Regulator

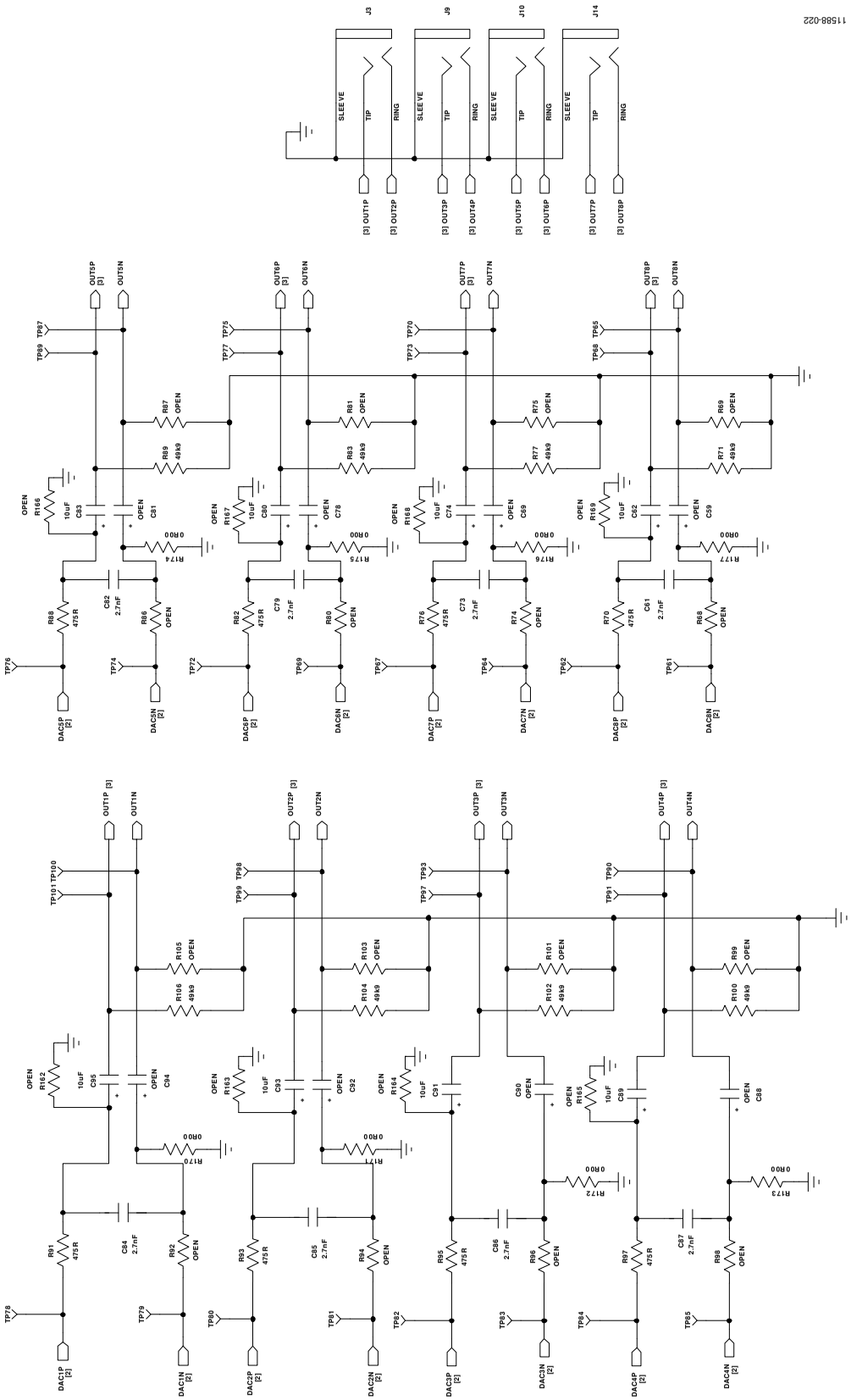


Figure 22. Schematic, Page 3—ADAU196xA DAC Output 1 to Output 8

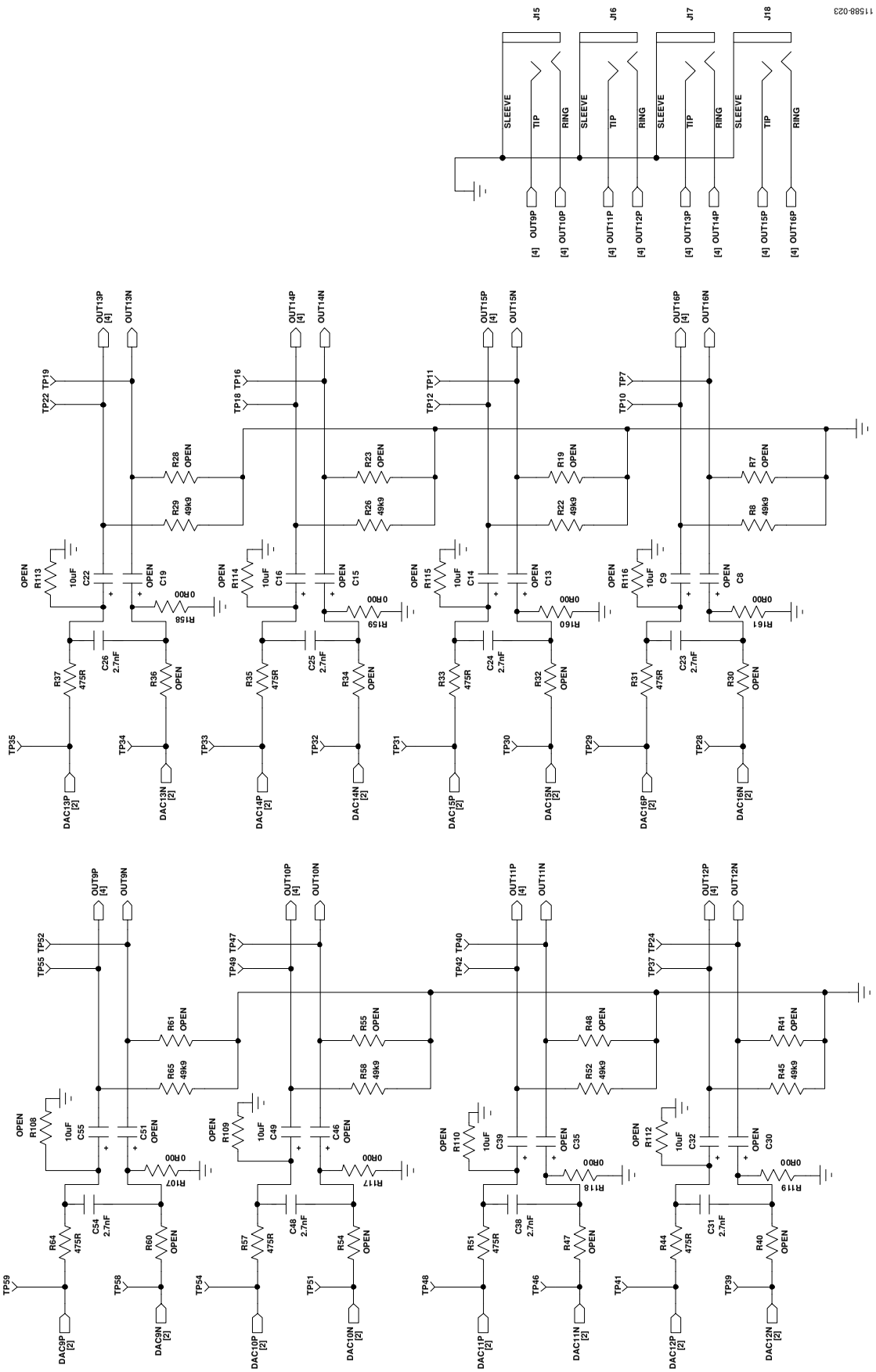


Figure 23. Schematic, Page 4—ADAU196xA DAC Output 9 to Output 12

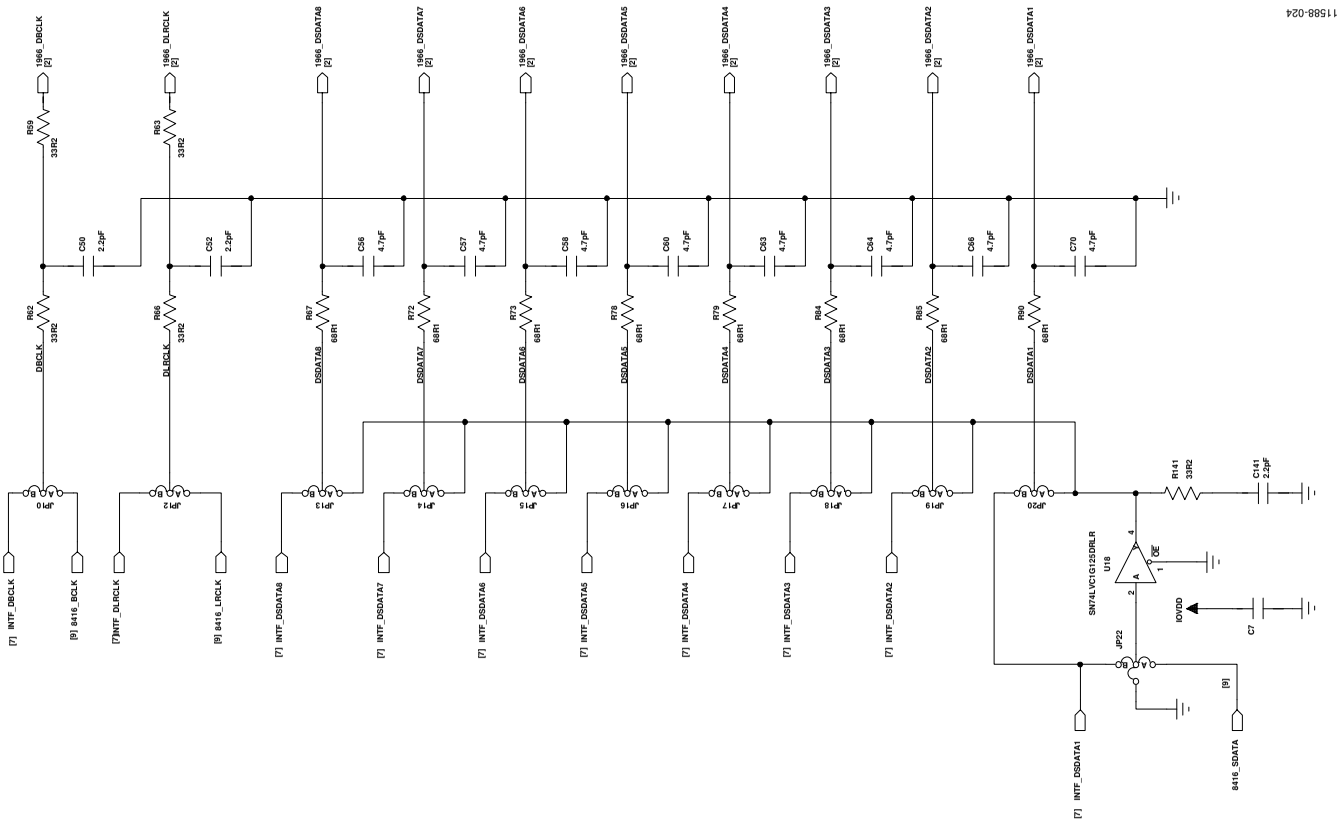
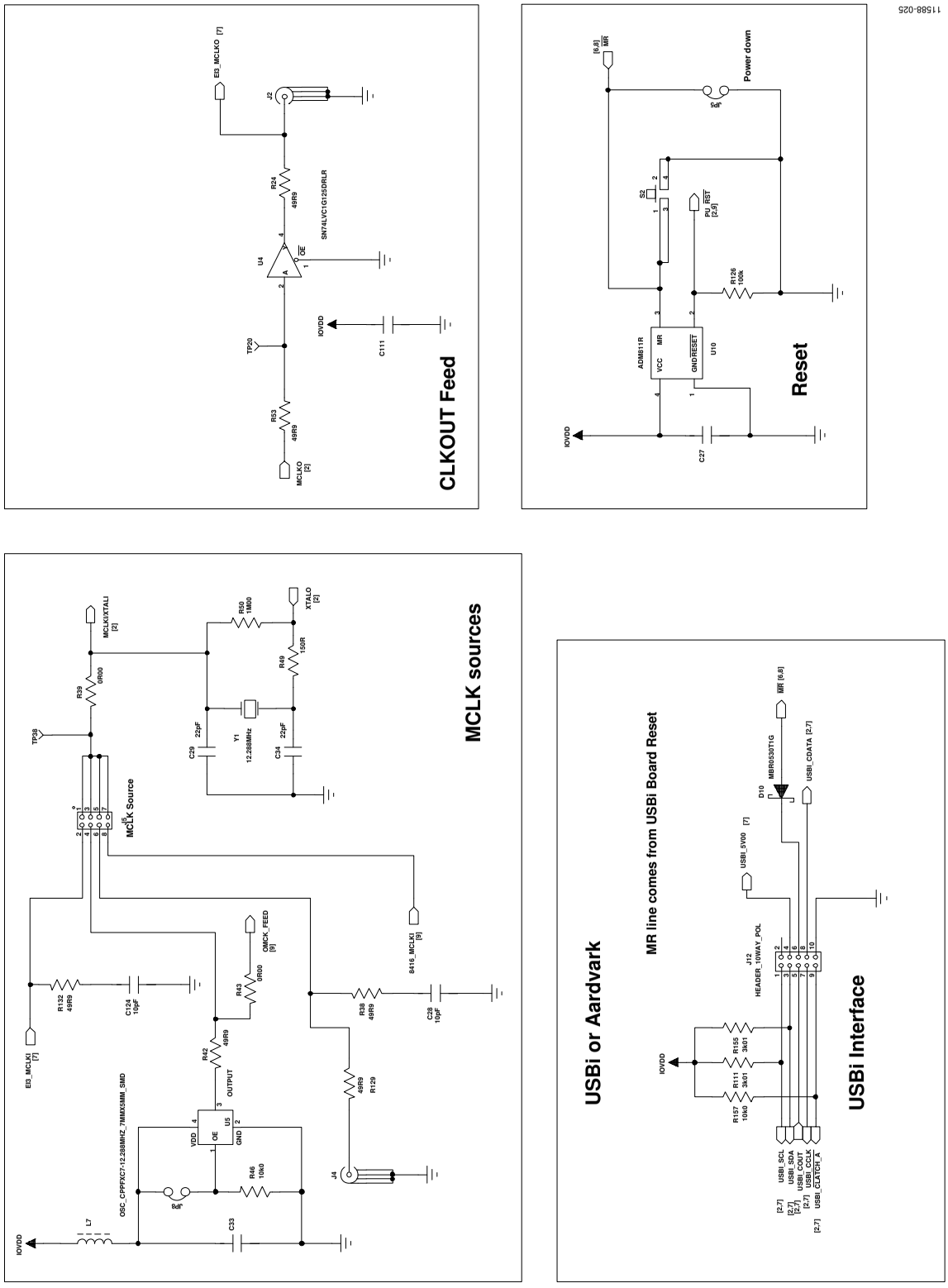


Figure 24. Schematic, Page 5—BCLK, LRCLK, and SDATA Jumpers and Routing



11588-025

Figure 25. Schematic, Page 6—MCLK Selection, USBi Interface, CLKOUT Feed, and Reset Generator

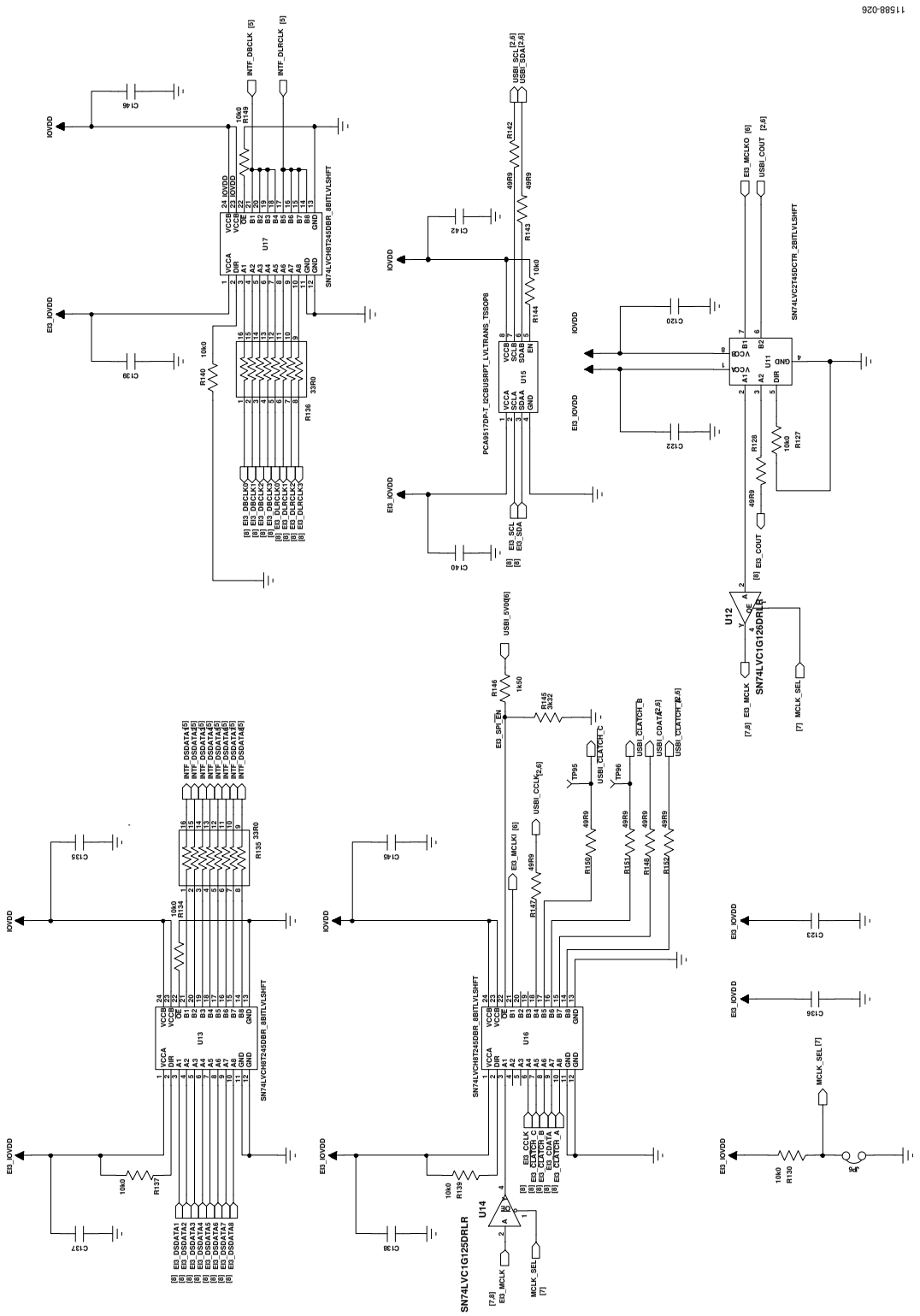


Figure 26. Schematic, Page 7—Level Shift and Clock Direction Control

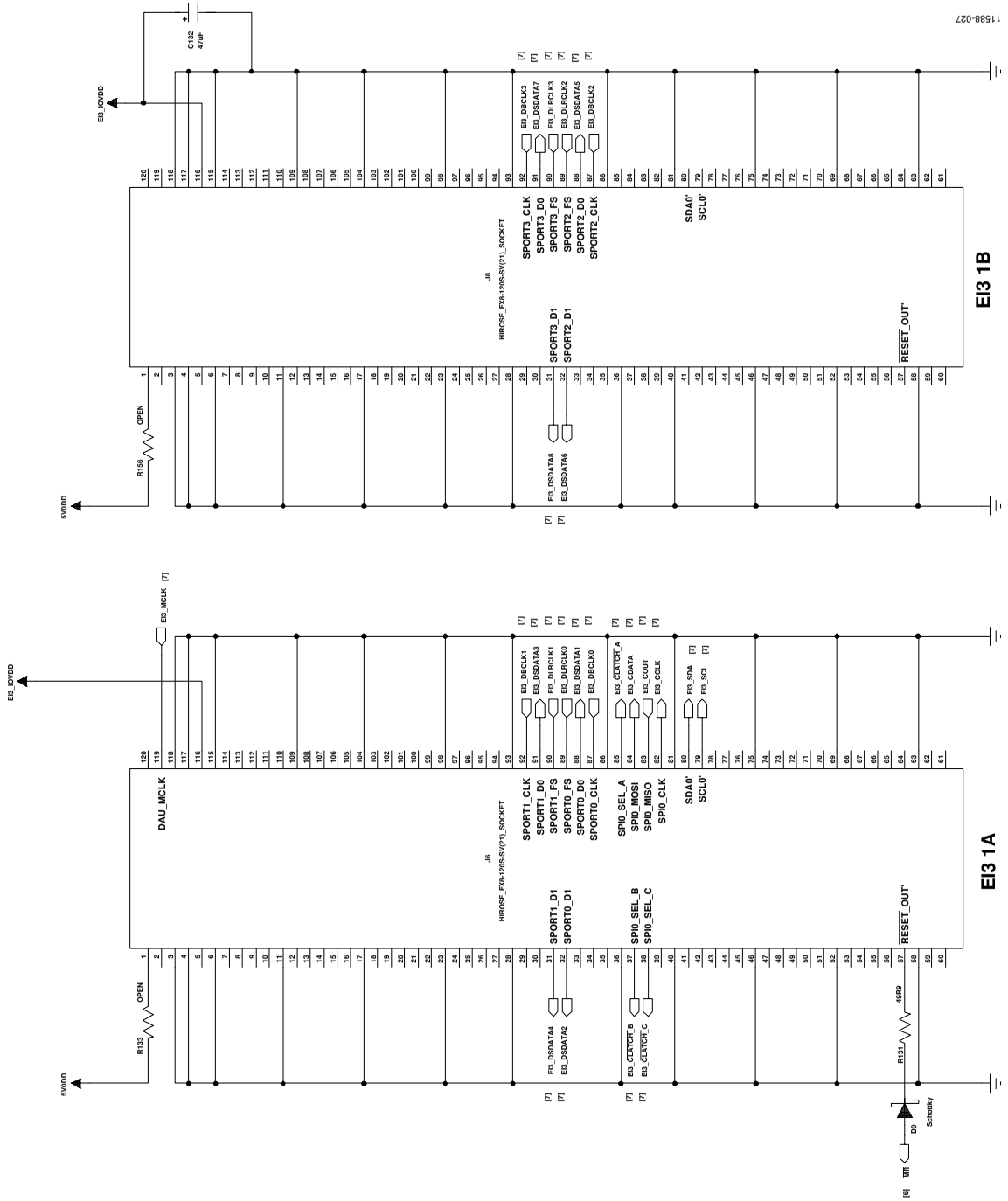


Figure 27. Schematic, Page 8—SDP Interface Connectors

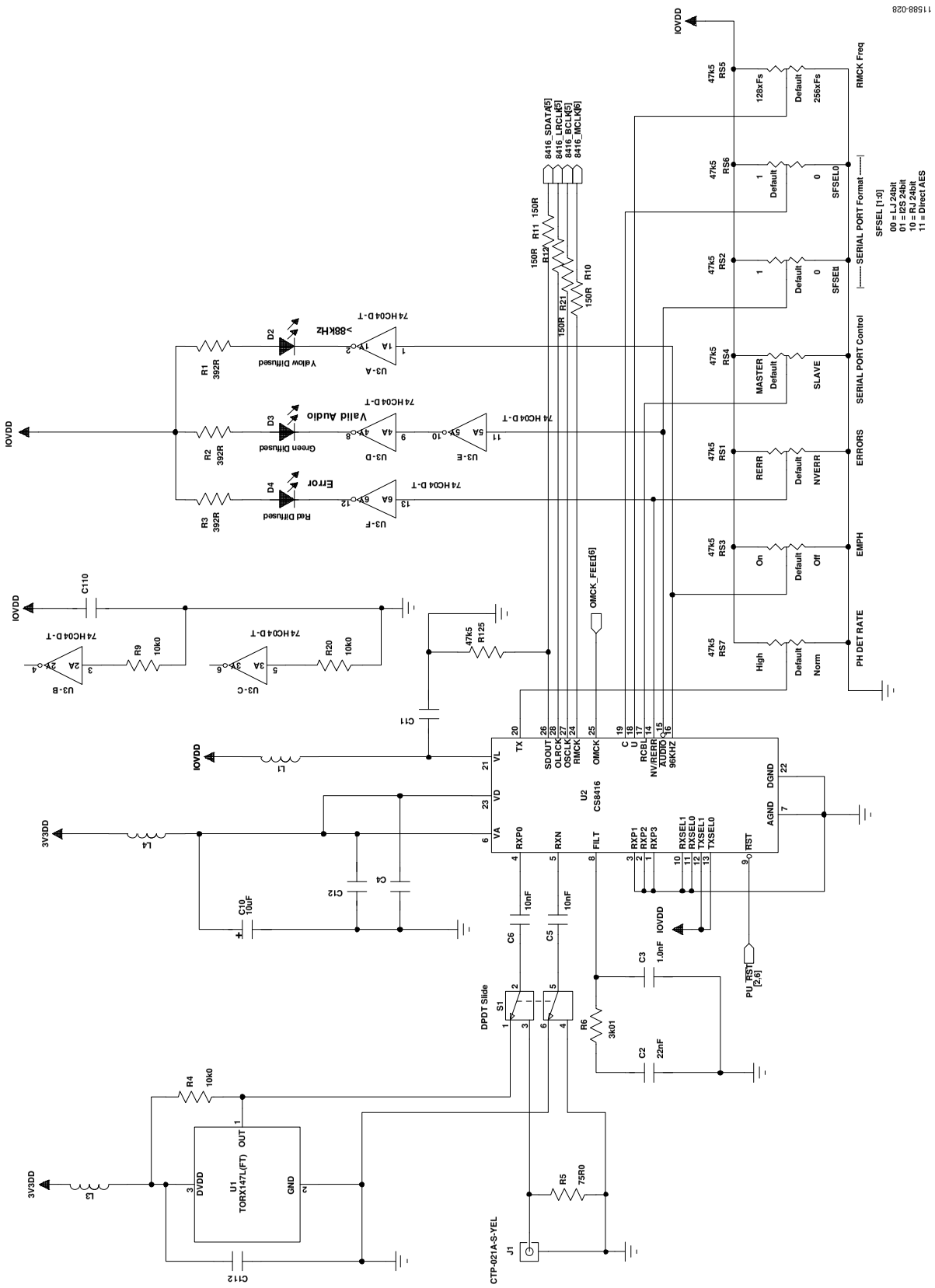


Figure 28. Schematic, Page 9—S/PDIF Receiver

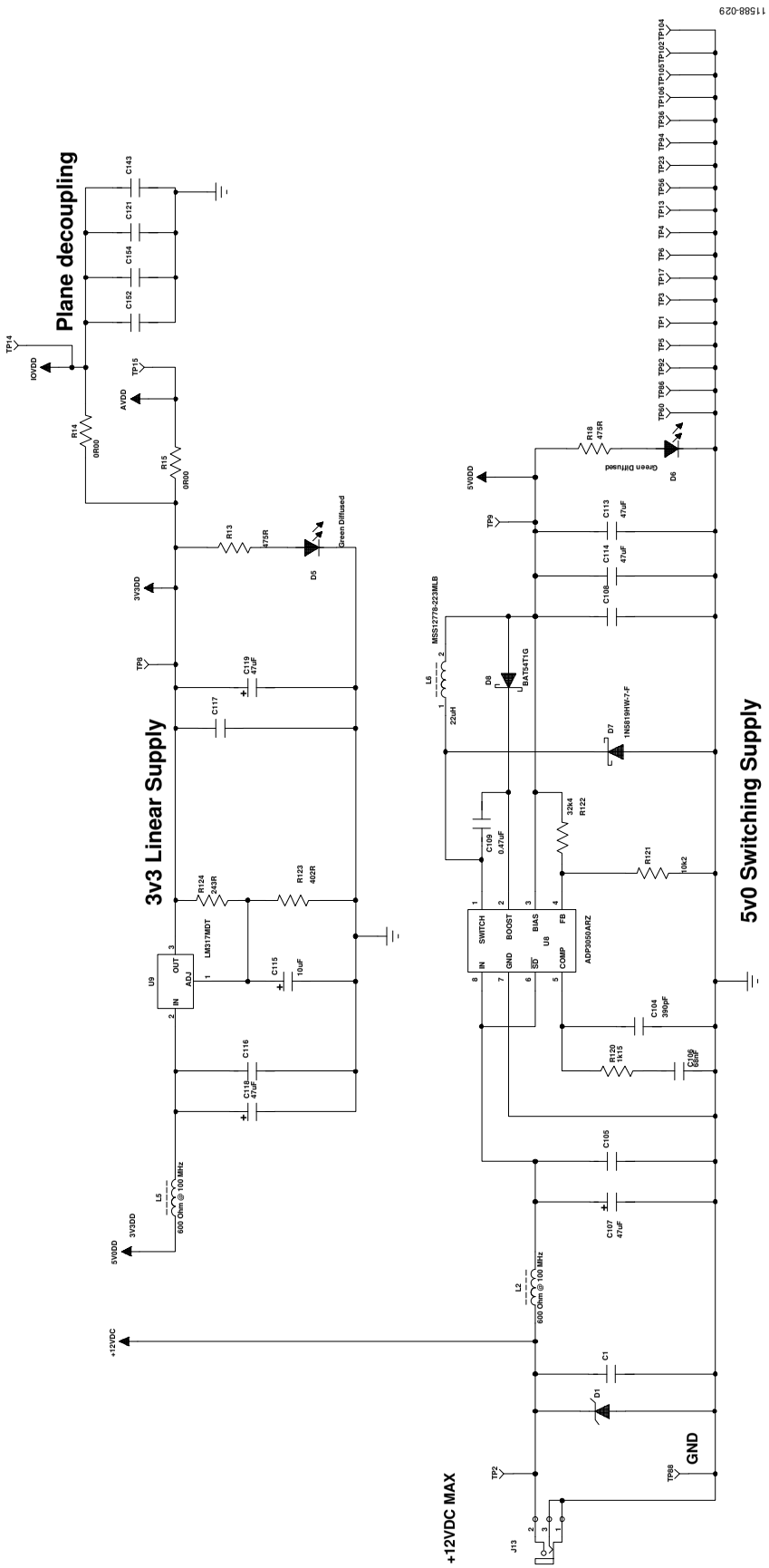


Figure 29. Schematic, Page 10—Power Supply

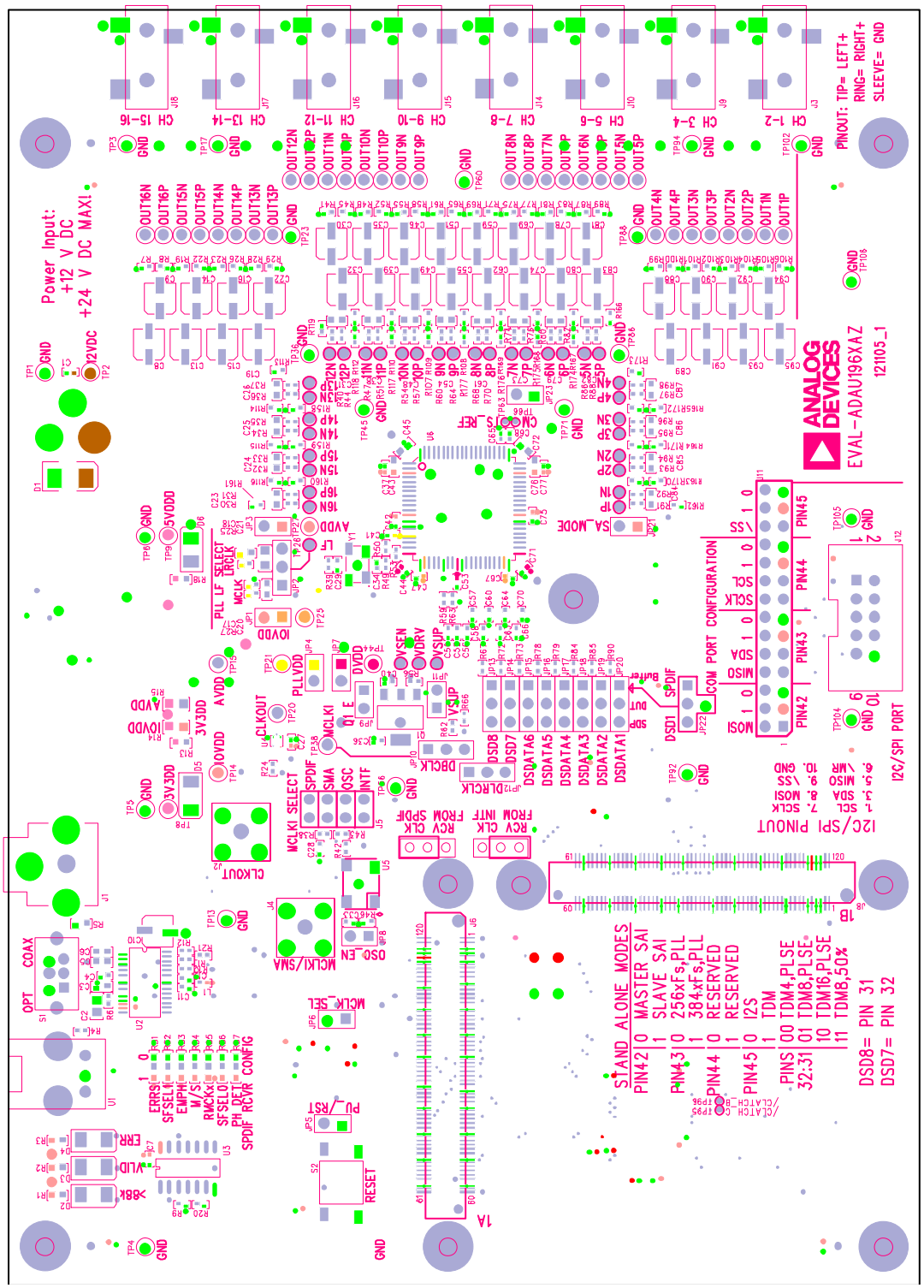


Figure 30. Top Assembly

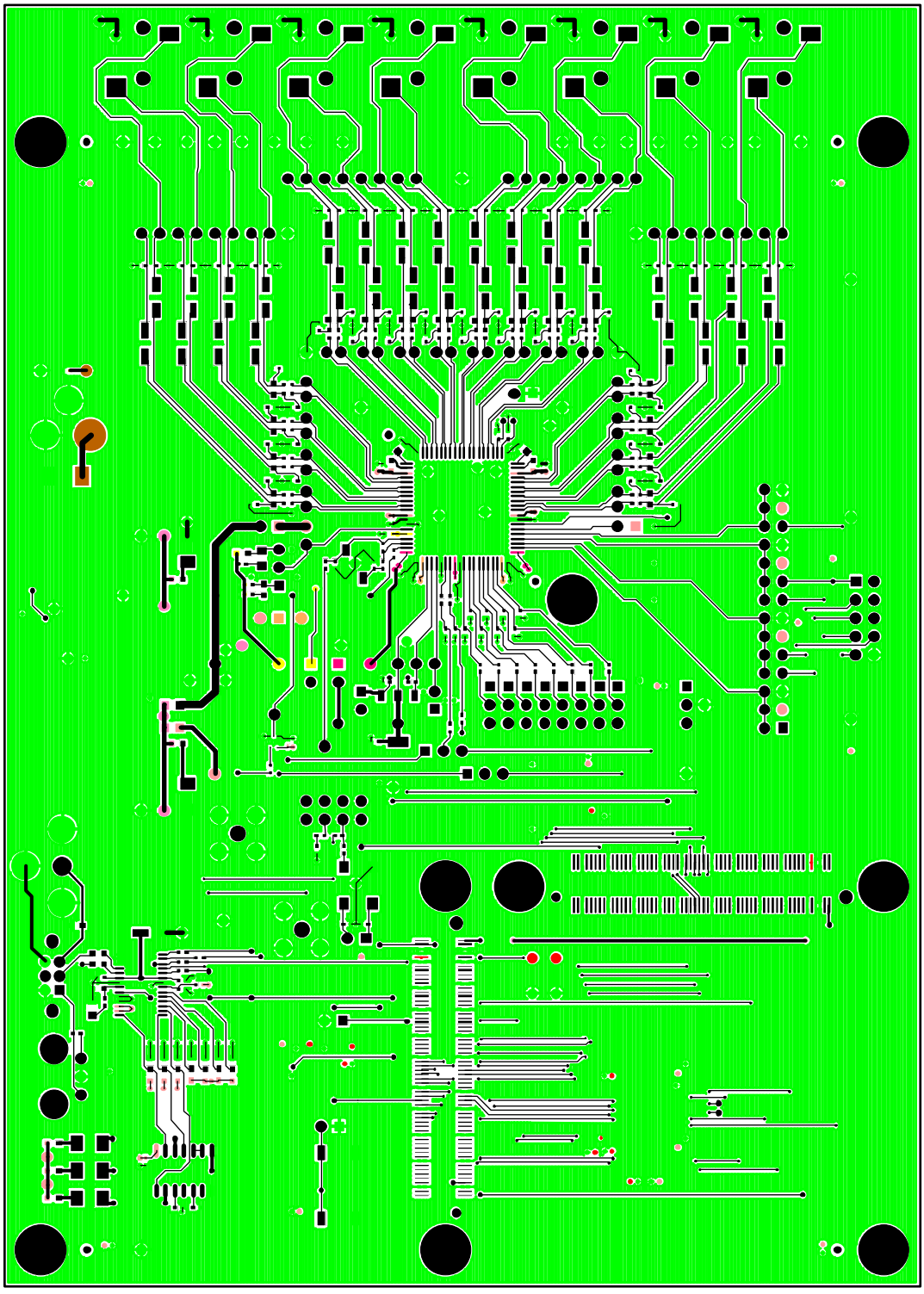


Figure 31. Top Layer Copper

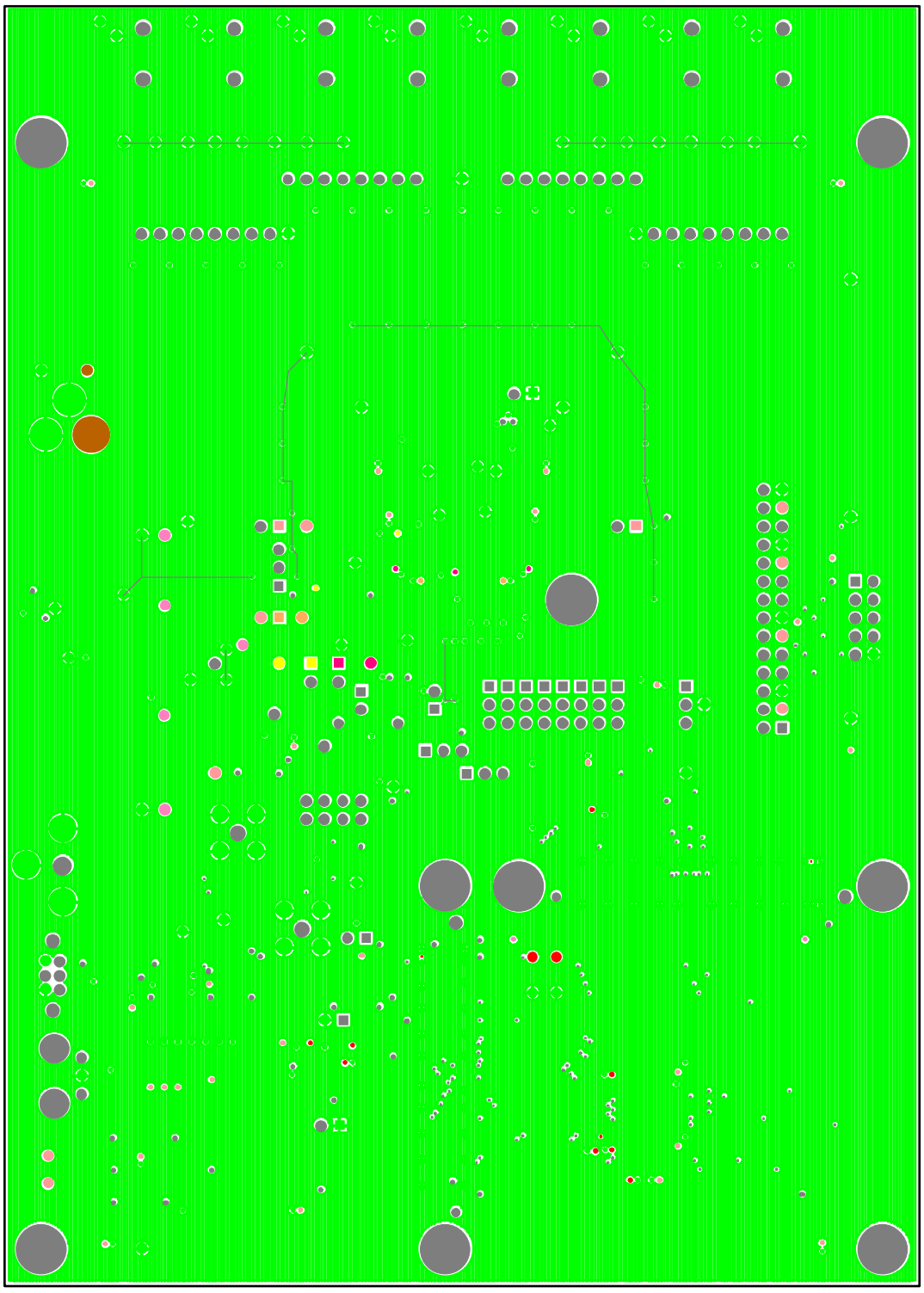


Figure 32. L2 Ground

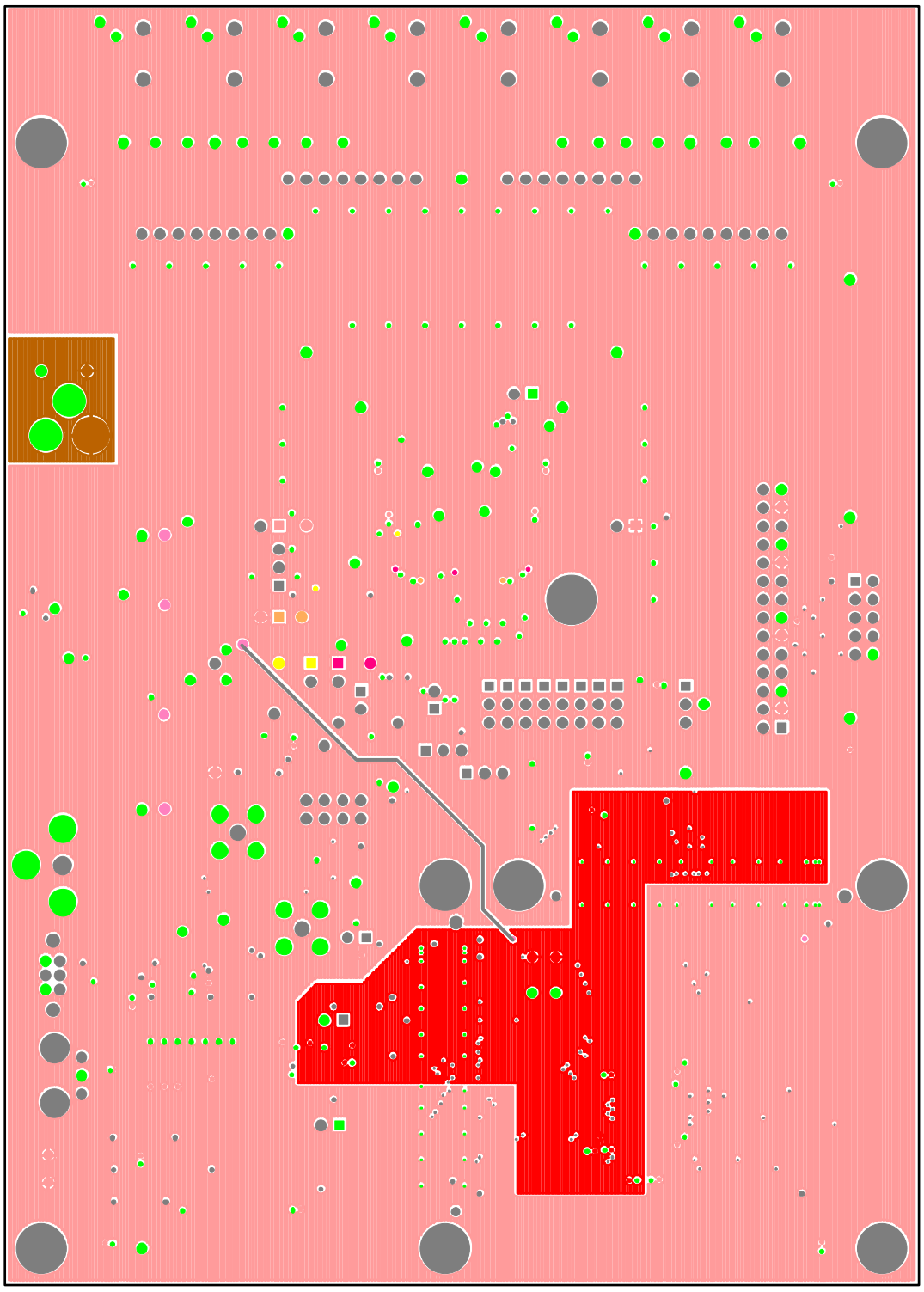


Figure 33. L3 Power

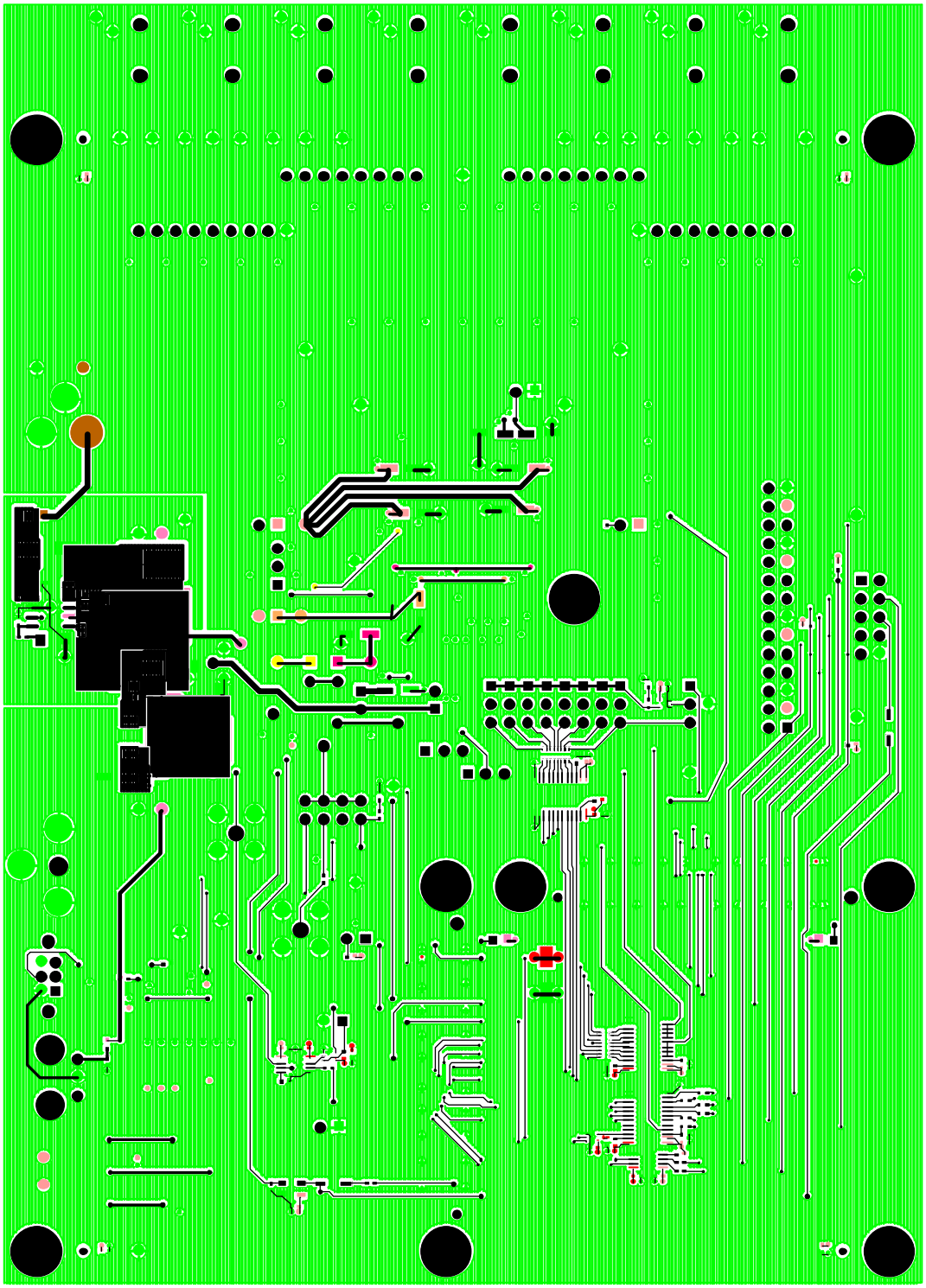


Figure 34. Bottom Copper

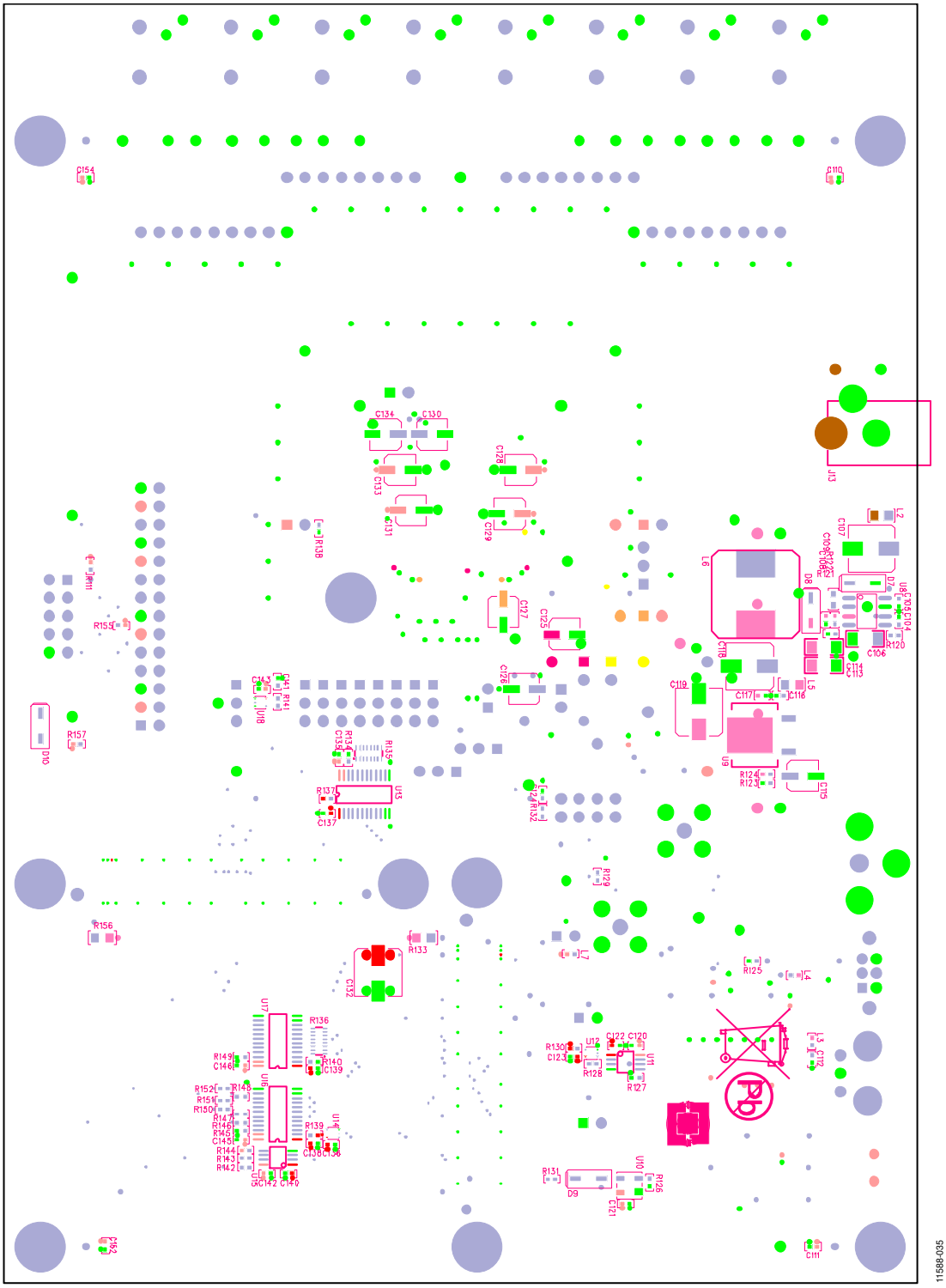


Figure 35. Bottom Assembly

BILL OF MATERIAL

Table 2.

Qty	Reference	Description	Manufacturer	Part Number	Vendor	Vendor Order #
1	U6	Multibit Sigma-Delta DAC	Analog Devices	ADAU1962AWBSTZ or ADAU1966AWBSTZ	Analog Devices	ADAU1962AWBSTZ or ADAU1966AWBSTZ
1	J12	10-way shroud, polarized header	3M	N2510-6002RB	Digi-Key	MHC10K-ND
1	U5	12.288 MHz, fixed SMD oscillator, 3.3 V to 5 V dc	Cardinal Components	CPPFX C 7 L T-A7 BR-12.288MHz TS	Cardinal Components	CPPFX C 7 L T-A7 BR-12.288MHz TS
2	J6, J8	120-pin socket, 0.6 mm	Hirose Electric	FX8-120S-SV(21)	Digi-Key	H1219-ND
1	U1	15 Mbps fiber optic receiving module with shutter	Toshiba	TORX147L(FT)	Digi-Key	TORX147LFT-ND
1	U2	192 kHz dgtl rcvr, 28-TSSOP	Cirrus Logic	CS8416-CZZ	Digi-Key	598-1124-5-ND
10	JP1, JP3 to JP9, JP11, JP21	2-pin header, unshrouded, jumper ,0.10"; use Tyco 881545-2 shunt	Sullins Electronics Corp	PBC02SAAN or cut down PBC36SAAN	Digi-Key	S1011E-02-ND
1	U8	200 kHz, 1A, buck regulator	Analog Devices	ADP3050ARZ	Digi-Key	ADP3050ARZ-R7CT-ND
1	J11	28-way, unshrouded	3M	PBC14DAAN, or cut down PBC36DAAN	Digi-Key	S2011E-14-ND
1	U9	3-term adj voltage regulator DPAK	ST Microelectronics	LM317MDT-TR	Digi-Key	497-1574-1-ND
11	JP2, JP10, JP12 to JP20	3-pos SIP header	Sullins	PBC03SAAN or cut down PBC36SAAN	Digi-Key	S1011E-03-ND
1	JP22	3-pos T-header	Sullins	PBC03SAAN or cut down PBC36SAAN	Digi-Key	S1011E-03-ND plus single pin
1	J5	8-way, unshrouded, header dual row	Sullins Electronics Corp	PBC04DAAN or cut down PBC36DAAN	Digi-Key	S2011E-04-ND or cut down S2011E-36-ND
27	C9 to C10, C14, C16, C22, C32, C39,C49, C55, C62, C74, C80, C83, C89, C91, C93, C95, C11, C125 to C131, C133 to C134	Alum electrolytic capacitor, FC 105°, SMD_B, 10 µF	Panasonic EC	EEE-FC1C100R	Digi-Key	PCE3995CT-ND
4	C107, C118 to C119, C132	Alum electrolytic capacitor, FC 105°, 47 µF, SMD_D	Panasonic EC	EEE-FC1C470P	Digi-Key	PCE4000CT-ND
3	U4, U14, U18	Buffer 3-state, single gate	Texas Instruments	SN74LVC1G125DRLR	Digi-Key	296-18012-1-ND
1	Y1	Crystal, 12.288 MHz, SMT, 18 pF	Abracon Corp	ABM3B-12.288MHZ-10-1-U-T	Digi-Key	300-8198-1-ND
4	L1, L3 to L4, L7	Chip ferrite bead, 600 Ω @ 100 MHz	TDK Corp	MMZ1005S601C	Digi-Key	445-2162-1-ND
2	L2, L5	Chip ferrite bead, 600 Ω @ 100 MHz	Steward	HZ0805E601R-10	Digi-Key	240-2399-1-ND
3	R1 to R3	Chip resistor, 1%, 100 mW, thick film, 0603, 392R	Rohm	MCR03EZPFX3920	Digi-Key	RHM392HCT-ND
1	R5	Chip resistor, 1%, 100 mW thick film, 0603, 75R0	Panasonic EC	ERJ-3EKF75R0V	Digi-Key	P75.0HCT-ND