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3-Axis, ±2 *g*/±4 *g*/±8 *g*/±16 *g* Ultralow Power Digital MEMS Accelerometer

Data Sheet

ADXL344

FEATURES

Multipurpose accelerometer with 10- to 13-bit resolution for use in a wide variety of applications
Digital output accessible via SPI (3- and 4-wire) and I²C
Built-in motion detection features make tap, double-tap, activity, inactivity, orientation, and free-fall detection trivial
User-adjustable thresholds
Interrupts independently mappable to two interrupt pins
Low power operation down to 23 µA and embedded FIFO for reducing overall system power
Wide supply and I/O voltage range: 1.7 V to 2.75 V
Wide operating temperature range (−40°C to +85°C)
10,000 *g* shock survival
Small, thin Pb free, RoHS compliant 3 mm × 3 mm × 0.95 mm LGA package

APPLICATIONS

Handsets
Gaming and pointing devices
Hard disk drive (HDD) protection

GENERAL DESCRIPTION

The ADXL344 is a versatile 3-axis, digital-output, low *g* MEMS accelerometer. Selectable measurement range and bandwidth and configurable, built-in motion detection make it suitable for sensing acceleration in a wide variety of applications. Robustness to 10,000 *g* of shock and a wide temperature range (−40°C to +85°C) enable use of the accelerometer even in harsh environments.

The ADXL344 measures acceleration with high resolution (13-bit) measurement at up to ±16 *g*. Digital output data is formatted as 16-bit twos complement and is accessible through either a SPI (3- or 4-wire) or I²C digital interface. The ADXL344 can measure the static acceleration of gravity in tilt-sensing applications, as well as dynamic acceleration resulting from motion or shock. Its high resolution (3.9 mg/LSB) enables measurement of inclination changes less than 1.0°.

Several special sensing functions are provided. Activity and inactivity sensing detect the presence or lack of motion. Tap sensing detects single and double taps in any direction. Free-fall sensing detects if the device is falling. Orientation detection reports four- and six-position orientation and can trigger an interrupt upon change in orientation. These functions can be mapped individually to either of two interrupt output pins.

An integrated memory management system with a 32-level first in, first out (FIFO) buffer can be used to store data to minimize host processor activity and lower overall system power consumption.

The ADXL344 is supplied in a small, thin, 3 mm × 3 mm × 0.95 mm, 16-terminal, plastic package.

FUNCTIONAL BLOCK DIAGRAM

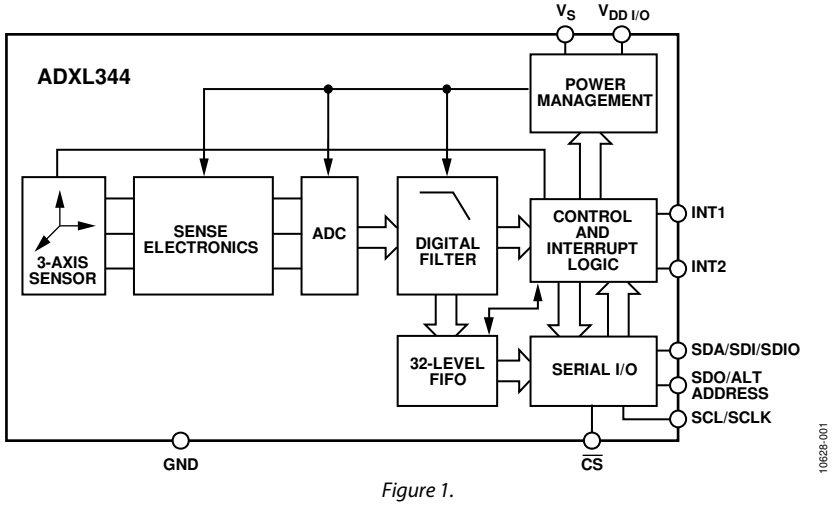

Figure 1.

Rev. 0

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ADXL344* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

EVALUATION KITS

- ADXL344 Datalogger / Development Board
- ADXL344Z Breakout Board
- Real Time Eval System for Digital Output Sensor

DOCUMENTATION

Data Sheet

- ADXL344: 3-Axis, ±2 g/±4 g/±8 g/±16 g Ultralow Power Digital MEMS Accelerometer Datasheet

DESIGN RESOURCES

- ADXL344 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL344 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

4/12—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V, acceleration = 0 *g*, C_S = 10 µF tantalum, $C_{I/O}$ = 0.1 µF, output data rate (ODR) = 800 Hz, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min[1]	Typ[2]	Max[1]	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8, ±16		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Inter-Axis Alignment Error			±0.1		Degrees
Cross-Axis Sensitivity[3]			±1		%
OUTPUT RESOLUTION	Each axis				
All *g* Ranges	10-bit resolution		10		Bits
±2 *g* Range	Full resolution		10		Bits
±4 *g* Range	Full resolution		11		Bits
±8 *g* Range	Full resolution		12		Bits
±16 *g* Range	Full resolution		13		Bits
SENSITIVITY	Each axis				
Sensitivity at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g* ranges, full resolution		256		LSB/*g*
	±2 *g*, 10-bit resolution		256		LSB/*g*
	±4 *g*, 10-bit resolution		128		LSB/*g*
	±8 *g*, 10-bit resolution		64		LSB/*g*
	±16 *g*, 10-bit resolution		32		LSB/*g*
Sensitivity Deviation from Ideal	All *g* ranges		±1.0		%
Scale Factor at X_{OUT}, Y_{OUT}, Z_{OUT}	All *g* ranges, full resolution		3.9		mg/LSB
	±2 *g*, 10-bit resolution		3.9		mg/LSB
	±4 *g*, 10-bit resolution		7.8		mg/LSB
	±8 *g*, 10-bit resolution		15.6		mg/LSB
	±16 *g*, 10-bit resolution		31.2		mg/LSB
Sensitivity Change Due to Temperature			±0.02		%/°C
0 *g* OFFSET	Each axis				
0 *g* Output Deviation from Ideal for X-, Y-, Z-Axes			±35		m*g*
0 *g* Offset vs. Temperature for X-, Y-, Z-Axes			±1.0		m*g*/°C
NOISE					
X-, Y-, Z-Axes	ODR = 100 Hz for ±2 *g*, 10-bit resolution or all *g* ranges, full resolution		1.5		LSB rms
OUTPUT DATA RATE AND BANDWIDTH	User selectable				
Output Data Rate (ODR)[4, 5, 6, 7]		0.10		3200	Hz
SELF-TEST[8]					
Output Change in X-Axis		0.27		1.55	*g*
Output Change in Y-Axis		−1.55		−0.27	*g*
Output Change in Z-Axis		0.40		1.95	*g*
POWER SUPPLY					
Operating Voltage Range (V_S)		1.7	2.6	2.75	V
Interface Voltage Range ($V_{DD\ I/O}$)		1.7	1.8	V_S	V
Measurement Mode Supply Current	ODR ≥ 100 Hz		140		µA
	ODR < 10 Hz		30		µA
Standby Mode Supply Current			0.2		µA
Turn-On and Wake-Up Time[9]	ODR = 3200 Hz		1.4		ms

Parameter	Test Conditions/Comments	Min[1]	Typ[2]	Max[1]	Unit
TEMPERATURE					
Operating Temperature Range		−40		+85	°C
WEIGHT					
Device Weight			18		mg

[1] All minimum and maximum specifications are guaranteed. Typical specifications are not guaranteed.
[2] The typical specifications shown are for at least 68% of the population of parts and are based on the worst case of mean ±1 σ except for 0 *g* output and sensitivity, which represents the target value. For 0 *g* offset and sensitivity, the deviation from the ideal describes the worst case of mean ±1 σ.
[3] Cross-axis sensitivity is defined as coupling between any two axes.
[4] Bandwidth is the −3 dB frequency and is half the output data rate bandwidth = ODR/2.
[5] The output format for the 3200 Hz and 1600 Hz ODRs is different from the output format for the remaining ODRs. This difference is described in the Data Formatting of Upper Data Rates section.
[6] Output data rates below 6.25 Hz exhibit additional offset shift with increased temperature, depending on selected output data rate. Refer to the Offset Performance at Lowest Data Rates section for details.
[7] These are typical values for the lowest and highest output data rate settings.
[8] Self-test change is defined as the output (*g*) when the SELF_TEST bit = 1 (in the DATA_FORMAT register, Address 0x31) minus the output (*g*) when the SELF_TEST bit = 0. Due to device filtering, the output reaches its final value after 4 × τ when enabling or disabling self-test, where τ = 1/(data rate). The part must be in normal power operation (LOW_POWER bit = 0 in the BW_RATE register, Address 0x2C) for self-test to operate correctly.
[9] Turn-on and wake-up times are determined by the user-defined bandwidth. At a 100 Hz data rate, the turn-on and wake-up times are each approximately 11.1 ms. For other data rates, the turn-on and wake-up times are each approximately τ + 1.1 in milliseconds, where τ = 1/(data rate).

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	10,000 *g*
Any Axis, Powered	10,000 *g*
V_S	−0.3 V to +3.0 V
$V_{DD\ I/O}$	−0.3 V to +3.0 V
Digital Pins	−0.3 V to $V_{DD\ I/O}$ + 0.3 V or 3.0 V, whichever is less
All Other Pins	−0.3 V to +3.0 V
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
Temperature Range	
Powered	−40°C to +105°C
Storage	−40°C to +105°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 3. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	150°C/W	85°C/W	18 mg

PACKAGE INFORMATION

The information in Figure 2 and Table 4 provide details about the package branding for the ADXL344. For a complete listing of product availability, see the Ordering Guide section.

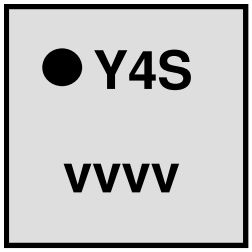


Figure 2. Product Information on Package (Top View)

Table 4. Package Branding Information

Branding Key	Field Description
Y4S	Part identifier for the ADXL344
vvvv	Factory lot code

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

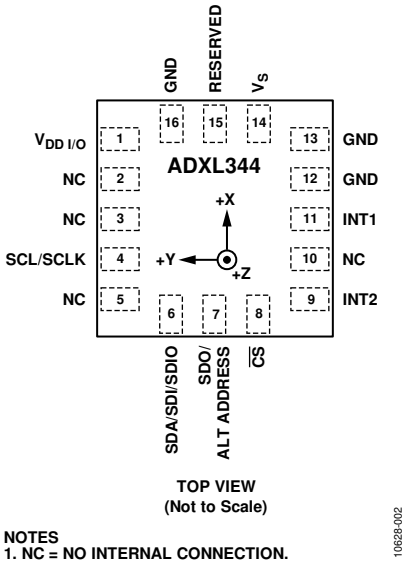


Figure 3. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Digital Interface Supply Voltage.
2	NC	Not Internally Connected.
3	NC	Not Internally Connected.
4	SCL/SCLK	Serial Communications Clock.
5	NC	Not Internally Connected.
6	SDA/SDI/SDIO	Serial Data (I^2C)/Serial Data Input (SPI 4-Wire)/Serial Data Input and Output (SPI 3-Wire).
7	SDO/ALT ADDRESS	Serial Data Output (SPI 4-Wire)/Alternate I^2C Address Select (I^2C).
8	$\overline{CS}$	Chip Select.
9	INT2	Interrupt 2 Output.
10	NC	Not Internally Connected.
11	INT1	Interrupt 1 Output.
12	GND	Must be connected to ground.
13	GND	Must be connected to ground.
14	V_S	Supply Voltage.
15	RESERVED	Reserved. This pin must be connected to V_S.
16	GND	Must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

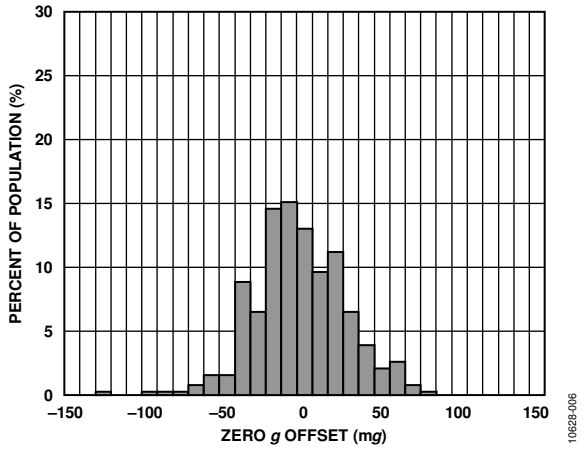


Figure 4. Zero g Offset at 25°C, V_S = 2.6 V, All Axes

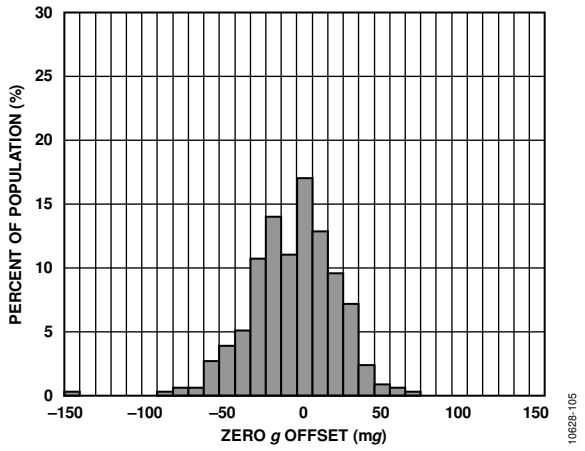


Figure 5. Zero g Offset at 25°C, V_S = 1.8 V, All Axes

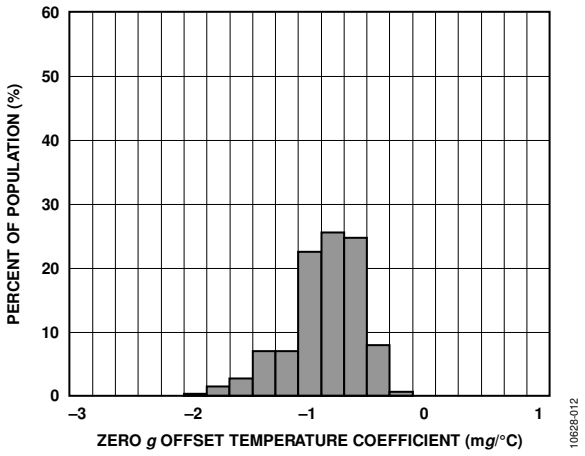


Figure 6. Zero g Offset Temperature Coefficient, V_S = 2.6 V, All Axes

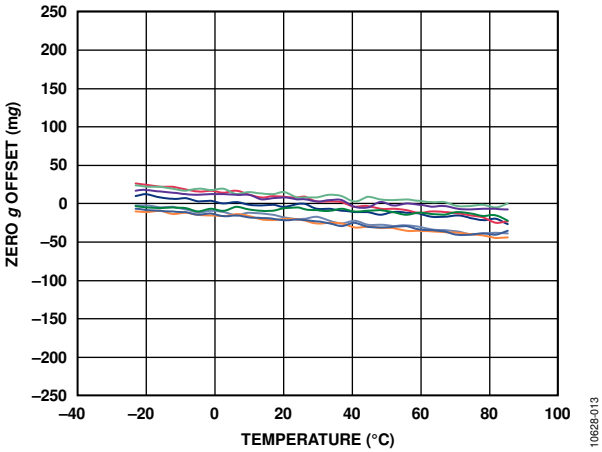


Figure 7. X-Axis Zero g Offset vs. Temperature—Eight Parts Soldered to PCB, V_S = 2.6 V

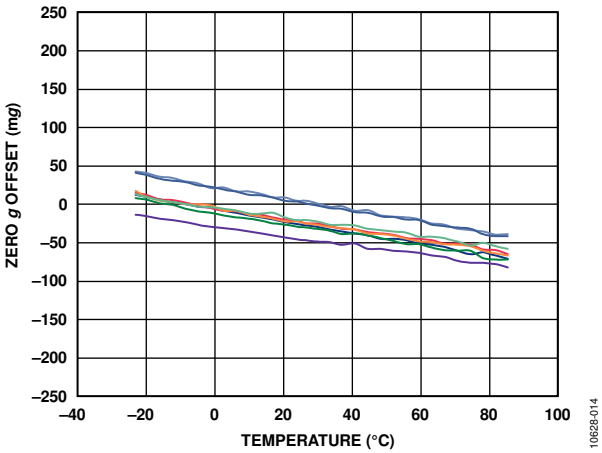


Figure 8. Y-Axis Zero g Offset vs. Temperature—Eight Parts Soldered to PCB, V_S = 2.6 V

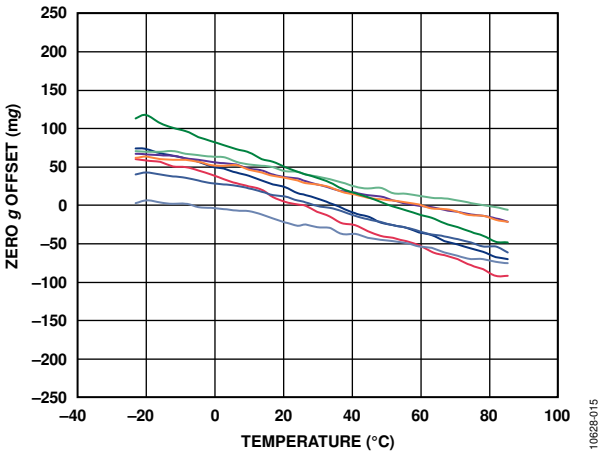


Figure 9. Z-Axis Zero g Offset vs. Temperature—Eight Parts Soldered to PCB, V_S = 2.6 V

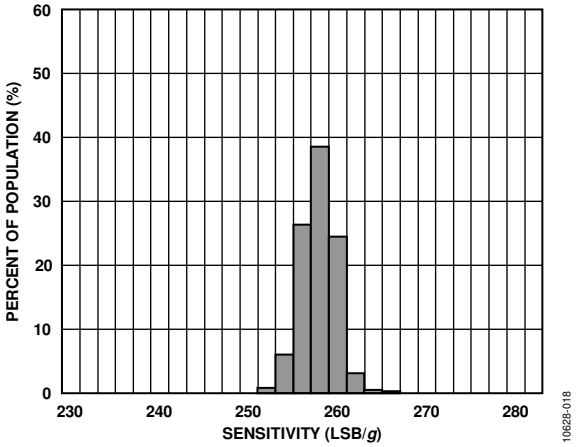


Figure 10. Sensitivity at 25°C, V_S = 2.6 V, Full Resolution, All Axes

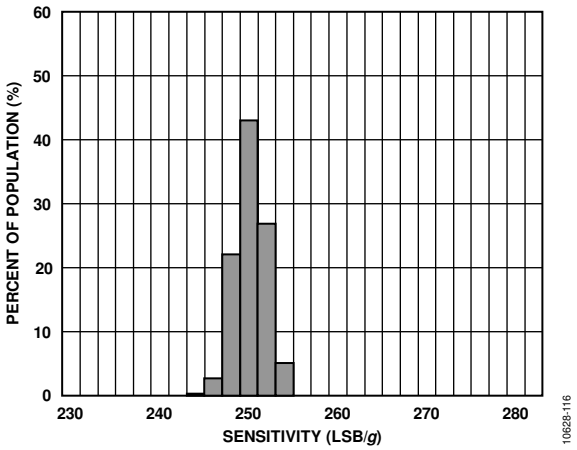


Figure 11. Sensitivity at 25°C, V_S = 1.8 V, Full Resolution, All Axes

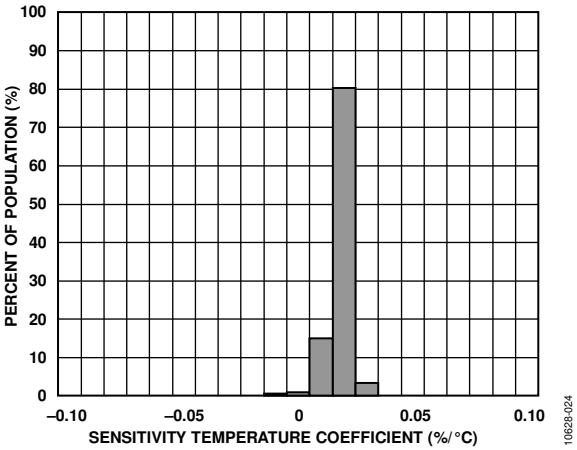


Figure 12. Sensitivity Temperature Coefficient, V_S = 2.6 V, All Axes

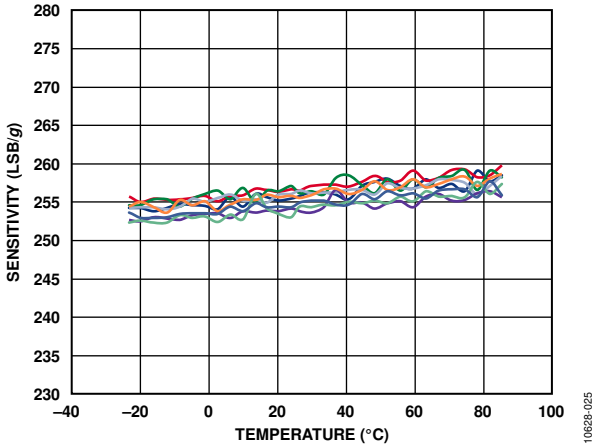


Figure 13. X-Axis Sensitivity vs. Temperature—
Eight Parts Soldered to PCB, V_S = 2.6 V, Full Resolution

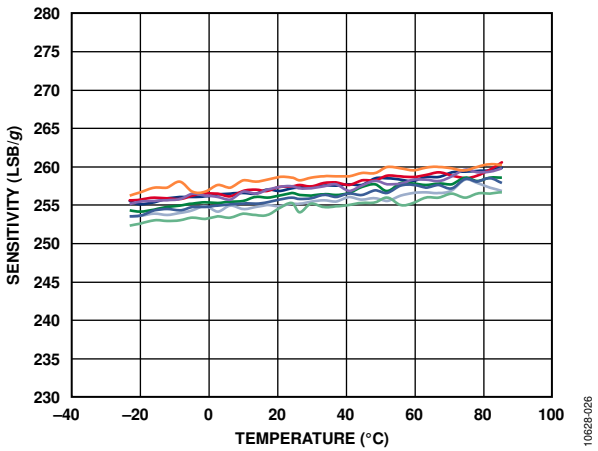


Figure 14. Y-Axis Sensitivity vs. Temperature—
Eight Parts Soldered to PCB, V_S = 2.6 V, Full Resolution

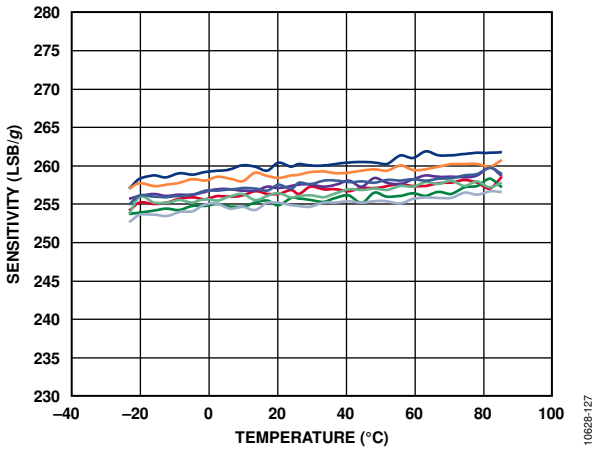


Figure 15. Z-Axis Sensitivity vs. Temperature—
Eight Parts Soldered to PCB, V_S = 2.6 V, Full Resolution

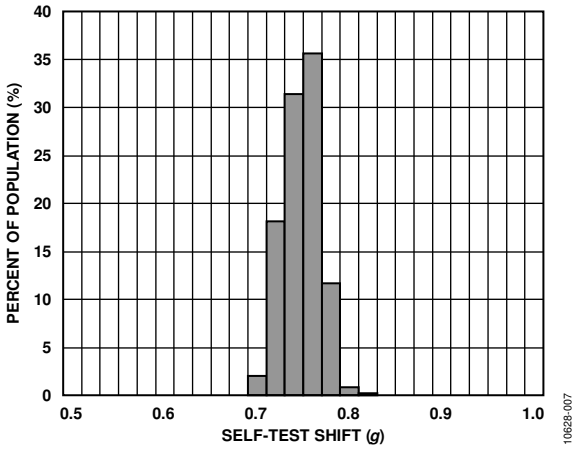


Figure 16. X-Axis Self-Test Response at 25°C, V_S = 2.6 V

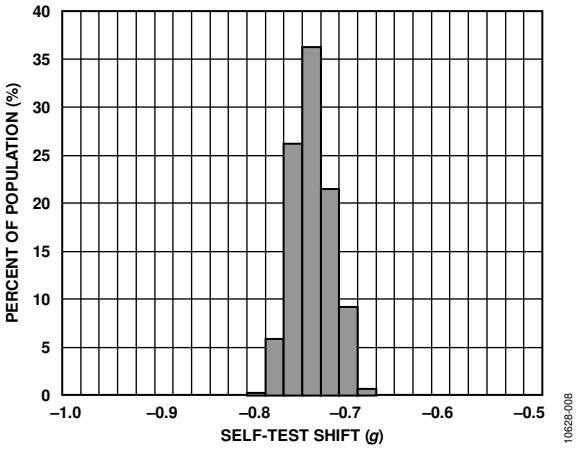


Figure 17. Y-Axis Self-Test Response at 25°C, V_S = 2.6 V

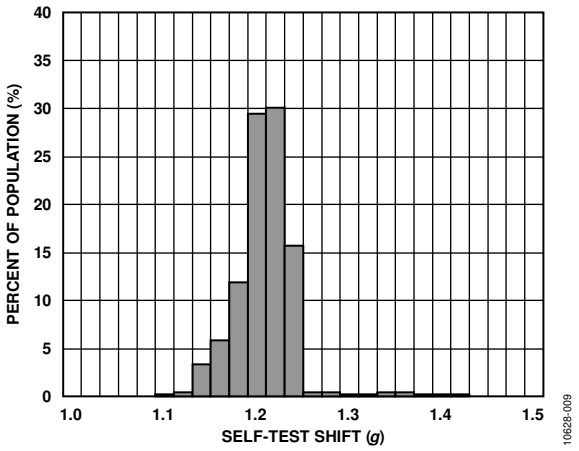


Figure 18. Z-Axis Self-Test Response at 25°C, V_S = 2.6 V

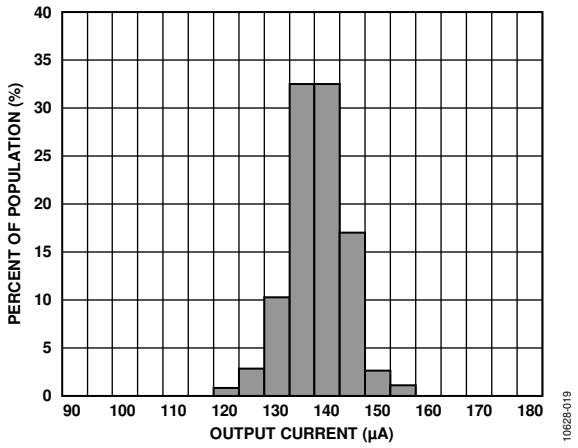


Figure 19. Supply Current at 25°C, 100 Hz Output Data Rate, V_S = 2.6 V

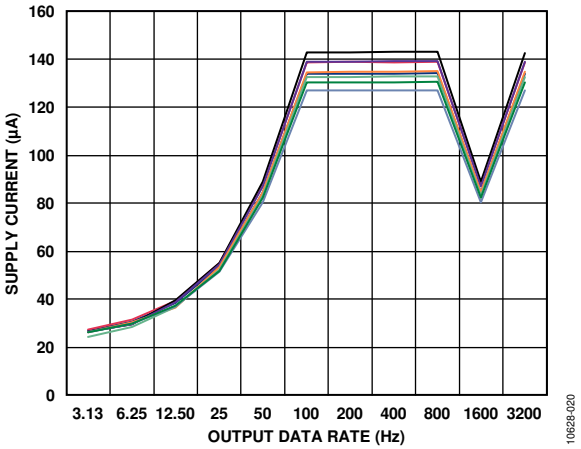


Figure 20. Supply Current vs. Output Data Rate at 25°C—10 Parts, V_S = 2.6 V

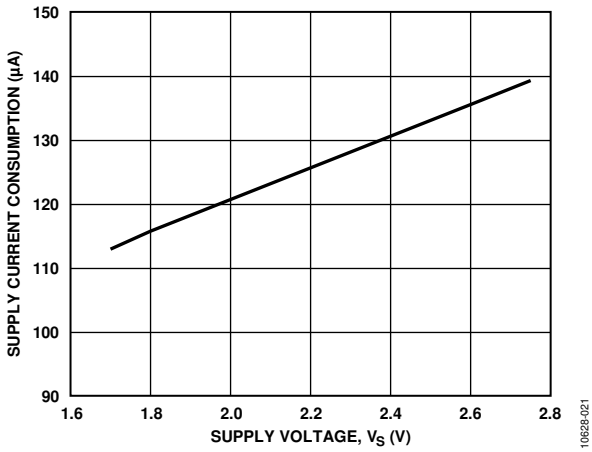


Figure 21. Supply Current vs. Supply Voltage at 25°C

THEORY OF OPERATION

The ADXL344 is a complete 3-axis acceleration measurement system with a selectable measurement range of ±2 *g*, ±4 *g*, ±8 *g*, or ±16 *g*. It measures both dynamic acceleration resulting from motion or shock and static acceleration, such as gravity, which allows the device to be used as a tilt sensor.

The sensor is a polysilicon surface-micromachined structure built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against forces due to applied acceleration.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the proof mass and unbalances the differential capacitor, resulting in a sensor output with an amplitude proportional to acceleration. Phase-sensitive demodulation is used to determine the magnitude and polarity of the acceleration.

POWER SEQUENCING

Power can be applied to V_S or $V_{DD\ I/O}$ in any sequence without damaging the ADXL344. All possible power-on modes are summarized in Table 6. The interface voltage level is set with the interface supply voltage, $V_{DD\ I/O}$, which must be present to ensure that the ADXL344 does not create a conflict on the communication bus. For single-supply operation, $V_{DD\ I/O}$ can be the same as the main supply, V_S. In a dual-supply application, however, $V_{DD\ I/O}$ can differ from V_S to accommodate the desired interface voltage, as long as V_S is greater than or equal to $V_{DD\ I/O}$.

After V_S is applied, the device enters standby mode, where power consumption is minimized and the device waits for $V_{DD\ I/O}$ to be applied and for the command to enter measurement mode to be received. (This command can be initiated by setting the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D).) In addition, any register can be written to or read from to configure the part while the device is in standby mode. It is recommended to configure the device in standby mode and then to enable measurement mode. Clearing the measure bit returns the device to the standby mode.

Table 6. Power Sequencing

Condition	V_S	$V_{DD\ I/O}$	Description
Power Off	Off	Off	The device is completely off, but there is a potential for a communication bus conflict.
Bus Disabled	On	Off	The device is on in standby mode, but communication is unavailable and will create a conflict on the communication bus. The duration of this state should be minimized during power-up to prevent a conflict.
Bus Enabled	Off	On	No functions are available, but the device will not create a conflict on the communication bus.
Standby or Measurement Mode	On	On	At power-up, the device is in standby mode, awaiting a command to enter measurement mode, and all sensor functions are off. After the device is instructed to enter measurement mode, all sensor functions are available.

POWER SAVINGS

Power Modes

The ADXL344 automatically modulates its power consumption in proportion to its output data rate, as outlined in Table 7. If additional power savings is desired, a lower power mode is available. In this mode, the internal sampling rate is reduced, allowing for power savings in the 12.5 Hz to 400 Hz data rate range at the expense of slightly greater noise. To enter low power mode, set the LOW_POWER bit (Bit D4) in the BW_RATE register (Address 0x2C). The current consumption in low power mode is shown in Table 8 for cases where there is an advantage to using low power mode. Use of low power mode for a data rate not shown in Table 8 does not provide any advantage over the same data rate in normal power mode. Therefore, it is recommended that only data rates listed in Table 8 be used in low power mode. The current consumption values shown in Table 7 and Table 8 are for a V_S of 2.6 V.

Table 7. Typical Current Consumption vs. Data Rate (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
3200	1600	1111	140
1600	800	1110	90
800	400	1101	140
400	200	1100	140
200	100	1011	140
100	50	1010	140
50	25	1001	90
25	12.5	1000	55
12.5	6.25	0111	40
6.25	3.13	0110	31
3.13	1.56	0101	27
1.56	0.78	0100	23
0.78	0.39	0011	23
0.39	0.20	0010	23
0.20	0.10	0001	23
0.10	0.05	0000	23

Table 8. Typical Current Consumption vs. Data Rate, Low Power Mode (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Output Data Rate (Hz)	Bandwidth (Hz)	Rate Code	I_{DD} (μA)
400	200	1100	90
200	100	1011	55
100	50	1010	40
50	25	1001	31
25	12.5	1000	27
12.5	6.25	0111	23

Autosleep Mode

Additional power can be saved if the ADXL344 automatically switches to sleep mode during periods of inactivity. To enable this feature, set the THRESH_INACT register (Address 0x25) and the TIME_INACT register (Address 0x26) each to a value that signifies inactivity (the appropriate value depends on the application), and then set the AUTO_SLEEP bit (Bit D4) and the link bit (Bit D5) in the POWER_CTL register (Address 0x2D). Current consumption at the sub-8 Hz data rates used in this mode is typically 23 μA for a V_S of 2.6 V.

Standby Mode

For even lower power operation, standby mode can be used. In standby mode, current consumption is reduced to 0.2 μA (typical). In this mode, no measurements are made. Standby mode is entered by clearing the measure bit (Bit D3) in the POWER_CTL register (Address 0x2D). Placing the device into standby mode preserves the contents of FIFO.

SERIAL COMMUNICATIONS

I²C and SPI digital communications are available. In both cases, the ADXL344 operates as a slave. I²C mode is enabled if the $\overline{CS}$ pin is tied high to $V_{DD\ I/O}$. The $\overline{CS}$ pin should always be tied high to $V_{DD\ I/O}$ or be driven by an external controller because there is no default mode if the $\overline{CS}$ pin is left unconnected. Therefore, not taking these precautions may result in an inability to communicate with the part. In SPI mode, the $\overline{CS}$ pin is controlled by the bus master. In both SPI and I²C modes of operation, data transmitted from the ADXL344 to the master device should be ignored during writes to the ADXL344.

SPI

For SPI, either 3- or 4-wire configuration is possible, as shown in the connection diagrams in Figure 22 and Figure 23. Clearing the SPI bit (Bit D6) in the DATA_FORMAT register (Address 0x31) selects 4-wire mode, whereas setting the SPI bit selects 3-wire mode. The maximum SPI clock speed is 5 MHz with 100 pF maximum loading, and the timing scheme follows clock polarity (CPOL) = 1 and clock phase (CPHA) = 1. If power is applied to the ADXL344 before the clock polarity and phase of the host processor are configured, the $\overline{CS}$ pin should be brought high before changing the clock polarity and phase. When using 3-wire SPI, it is recommended that the SDO pin be either pulled up to $V_{DD\ I/O}$ or pulled down to GND via a 10 kΩ resistor.

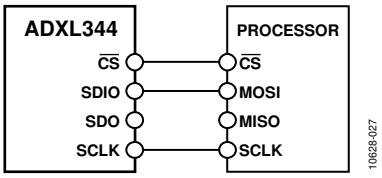


Figure 22. 3-Wire SPI Connection Diagram

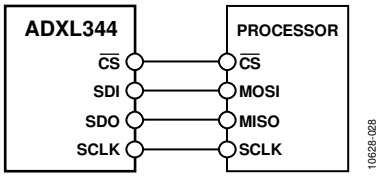


Figure 23. 4-Wire SPI Connection Diagram

$\overline{CS}$ is the serial port enable line and is controlled by the SPI master. This line must go low at the start of a transmission and high at the end of a transmission, as shown in Figure 25. SCLK is the serial port clock and is supplied by the SPI master. SCLK should idle high during a period of no transmission. SDI and SDO are the serial data input and output, respectively. Data is updated on the falling edge of SCLK and should be sampled on the rising edge of SCLK.

To read or write multiple bytes in a single transmission, the multiple-byte bit, located after the R/$\overline{W}$ bit in the first byte transfer (MB in Figure 25 to Figure 27), must be set. After the register addressing and the first byte of data, each subsequent set of clock pulses (eight clock pulses) causes the ADXL344 to point to the next register for a read or write. This shifting continues until the clock pulses cease and $\overline{CS}$ is deasserted. To perform reads or writes on different, nonsequential registers, $\overline{CS}$ must be deasserted between transmissions and the new register must be addressed separately.

The timing diagram for 3-wire SPI reads or writes is shown in Figure 27. The 4-wire equivalents for SPI writes and reads are shown in Figure 25 and Figure 26, respectively. For correct operation of the part, the logic thresholds and timing parameters in Table 9 and Table 10 must be met at all times.

Use of the 3200 Hz and 1600 Hz output data rates is only recommended with SPI communication rates greater than or equal to 2 MHz. The 800 Hz output data rate is recommended only for communication speeds greater than or equal to 400 kHz, and the remaining data rates scale proportionally. For example, the minimum recommended communication speed for a 200 Hz output data rate is 100 kHz. Operation at an output data rate above the recommended maximum may result in undesirable effects on the acceleration data, including missing samples or additional noise.

Preventing Bus Traffic Errors

The ADXL344 $\overline{CS}$ pin is used both for initiating SPI transactions and for enabling I²C mode. When the ADXL344 is used on a SPI bus with multiple devices, its $\overline{CS}$ pin is held high while the master communicates with the other devices. There may be conditions where a SPI command transmitted to another device looks like a valid I²C command. In this case, the ADXL344 interprets this as an attempt to communicate in I²C mode, and may interfere with other bus traffic. Unless bus traffic can be adequately controlled to assure such a condition never occurs, it is recommended to add a logic gate in front of the SDI pin as shown in Figure 24. This OR gate holds the SDI line high when $\overline{CS}$ is high to prevent SPI bus traffic at the ADXL344 from appearing as an I²C start command. Note that this recommendation applies only in cases where the ADXL344 is used on a SPI bus with multiple devices.

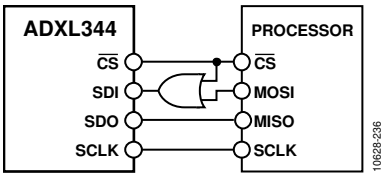


Figure 24. Recommended SPI Connection Diagram when Using Multiple SPI Devices on a Single Bus

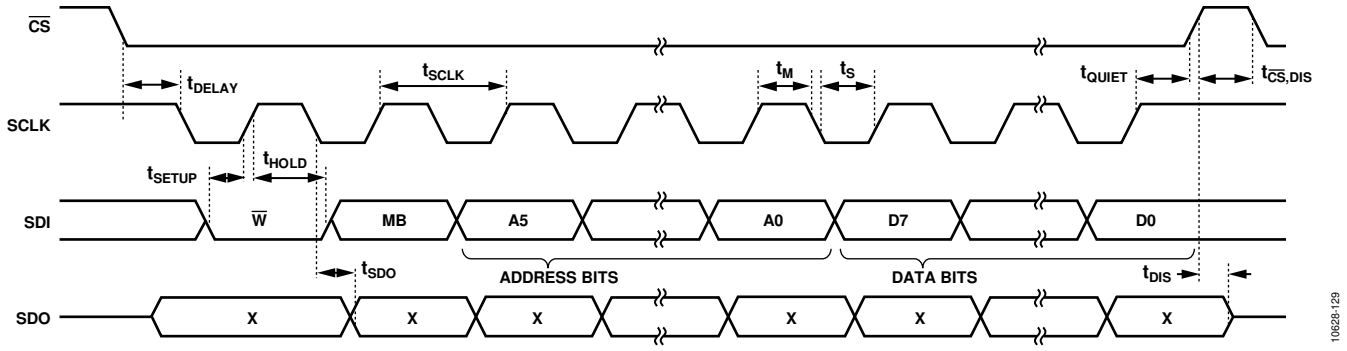


Figure 25. SPI 4-Wire Write

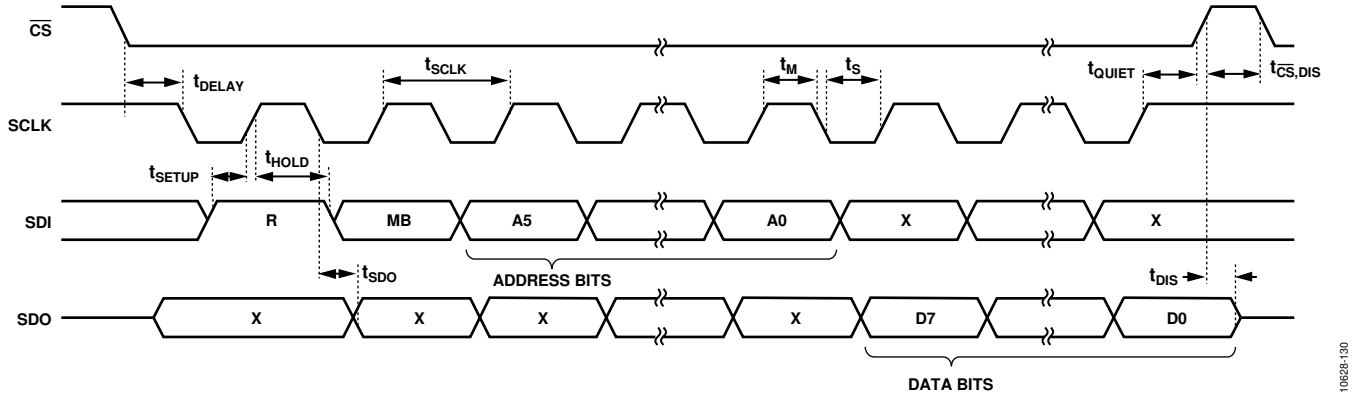
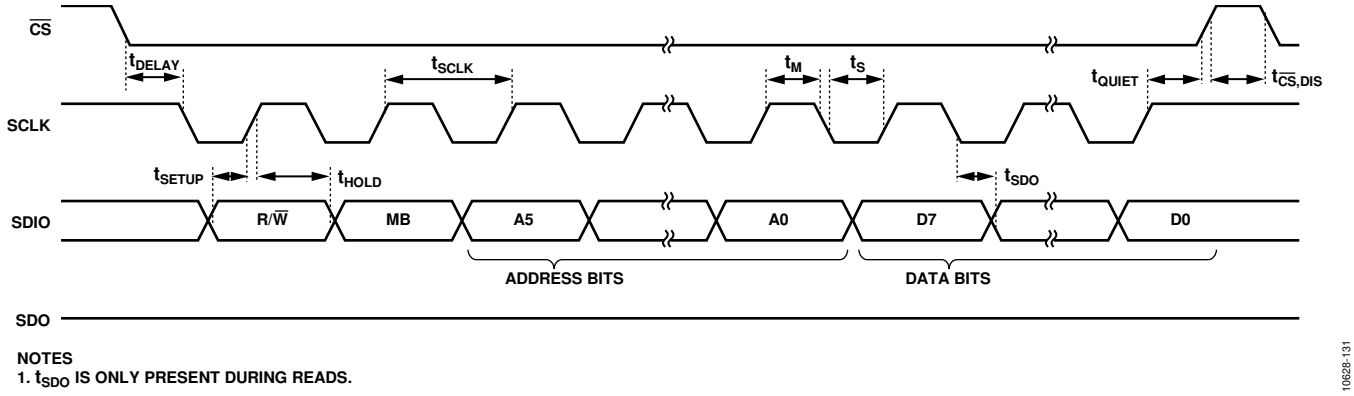


Figure 26. SPI 4-Wire Read



NOTES
1. t_{SDO} IS ONLY PRESENT DURING READS.

Figure 27. SPI 3-Wire Read/Write

Table 9. SPI Digital Input/Output

Parameter	Test Conditions	Limit[1]		Unit
		Min	Max	
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	μA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		μA
Digital Output				
Low Level Output Voltage (V_{OL})	$I_{OL} = 10$ mA		$0.2 \times V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	$I_{OH} = -4$ mA	$0.8 \times V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	10		mA
High Level Output Current (I_{OH})	$V_{OH} = V_{OH,\ min}$		−4	mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.6$ V		8	pF

[1] Limits are based on characterization results; not production tested.

Table 10. SPI Timing (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)[1]

Parameter	Limit[2, 3]		Unit	Description
	Min	Max		
f_{SCLK}		5	MHz	SPI clock frequency
t_{SCLK}	200		ns	1/(SPI clock frequency) mark-space ratio for the SCLK input is 40/60 to 60/40
t_{DELAY}	5		ns	$\overline{CS}$ falling edge to SCLK falling edge
t_{QUIET}	5		ns	SCLK rising edge to $\overline{CS}$ rising edge
t_{DIS}		10	ns	$\overline{CS}$ rising edge to SDO disabled
$t_{\overline{CS},DIS}$	150		ns	$\overline{CS}$ deassertion between SPI communications
t_S	$0.3 \times t_{SCLK}$		ns	SCLK low pulse width (space)
t_M	$0.3 \times t_{SCLK}$		ns	SCLK high pulse width (mark)
t_{SETUP}	5		ns	SDI valid before SCLK rising edge
t_{HOLD}	5		ns	SDI valid after SCLK rising edge
t_{SDO}		40	ns	SCLK falling edge to SDO/SDIO output transition
t_R[4]		20	ns	SDO/SDIO output low to output high transition
t_F[4]		20	ns	SDO/SDIO output high to output low transition

[1] The $\overline{CS}$, SCLK, SDI, and SDO pins are not internally pulled up or down; they must be driven for proper operation.
[2] Limits are based on characterization results; not production tested.
[3] The timing values are measured corresponding to the input thresholds (V_{IL} and V_{IH}) given in Table 9.
[4] Output rise and fall times are measured with a capacitive load of 150 pF.

I²C

With $\overline{CS}$ tied high to $V_{DD\ I/O}$, the ADXL344 is in I²C mode, requiring a simple 2-wire connection as shown in Figure 28. The ADXL344 conforms to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, available from NXP Semiconductor. It supports standard (100 kHz) and fast (400 kHz) data transfer modes if the bus parameters given in Table 11 and Table 12 are met. Single- or multiple-byte reads/writes are supported, as shown in Figure 29. With the ALT ADDRESS pin (Pin 7) high, the 7-bit I²C address for the device is 0x1D, followed by the R/$\overline{W}$ bit. This translates to 0x3A for a write and 0x3B for a read. An alternate I²C address of 0x53 (followed by the R/$\overline{W}$ bit) can be chosen by grounding the ALT ADDRESS pin. This translates to 0xA6 for a write and 0xA7 for a read.

There are no internal pull-up or pull-down resistors for any unused pins; therefore, there is no known state or default state for the $\overline{CS}$ or ALT ADDRESS pin if left floating or unconnected. It is required that the $\overline{CS}$ pin be connected to $V_{DD\ I/O}$ and that the ALT ADDRESS pin be connected to either $V_{DD\ I/O}$ or GND when using I²C.

Due to communication speed limitations, the maximum output data rate when using 400 kHz I²C is 800 Hz and scales linearly with a change in the I²C communication speed. For example, using I²C at 100 kHz limits the maximum ODR to 200 Hz. Operation at an output data rate above the recommended maximum may result in an undesirable effect on the acceleration data, including missing samples or additional noise.

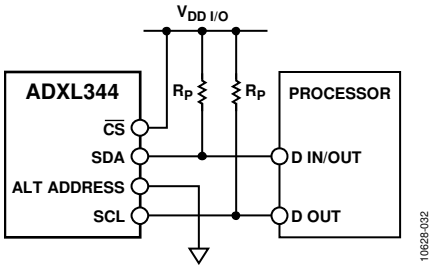


Figure 28. I²C Connection Diagram (Address 0x53)

If other devices are connected to the same I²C bus, the nominal operating voltage level of these other devices cannot exceed $V_{DD\ I/O}$ by more than 0.3 V. External pull-up resistors, R_P, are necessary for proper I²C operation. Refer to the *UM10204 I²C-Bus Specification and User Manual*, Rev. 03—19 June 2007, when selecting pull-up resistor values to ensure proper operation.

Table 11. I²C Digital Input/Output

Parameter	Test Conditions	Limit[1]		Unit
		Min	Max	
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	μA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		μA
Digital Output				
Low Level Output Voltage (V_{OL})	$V_{DD\ I/O} < 2$ V, $I_{OL} = 3$ mA		$0.2 \times V_{DD\ I/O}$	V
	$V_{DD\ I/O} \geq 2$ V, $I_{OL} = 3$ mA		400	mV
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	3		mA
Pin Capacitance	$f_{IN} = 1$ MHz, $V_{IN} = 2.6$ V		8	pF

[1] Limits are based on characterization results; not production tested.

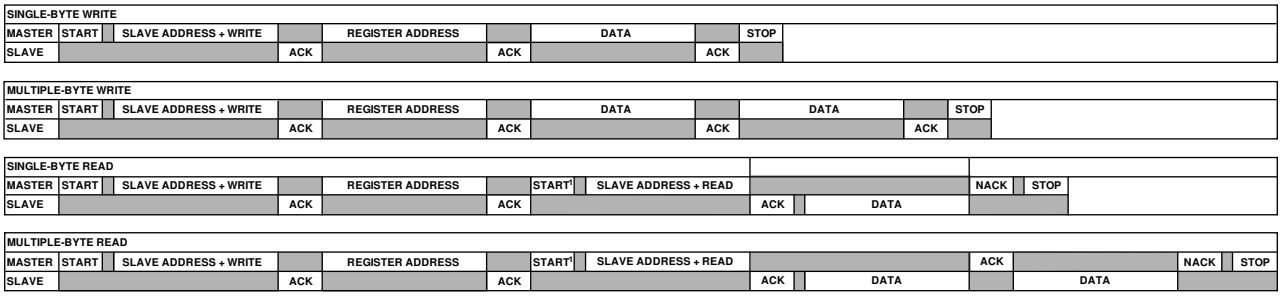


Figure 29. I²C Device Addressing

Table 12. I²C Timing (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

	Limit[1, 2]			
Parameter	**Min**	**Max**	**Unit**	**Description**
f_{SCL}		400	kHz	SCL clock frequency
t_1	2.5		µs	SCL cycle time
t_2	0.6		µs	t_{HIGH}, SCL high time
t_3	1.3		µs	t_{LOW}, SCL low time
t_4	0.6		µs	$t_{HD, STA}$, start/repeated start condition hold time
t_5	100		ns	$t_{SU, DAT}$, data setup time
t_6[3, 4, 5, 6]	0	0.9	µs	$t_{HD, DAT}$, data hold time
t_7	0.6		µs	$t_{SU, STA}$, setup time for repeated start
t_8	0.6		µs	$t_{SU, STO}$, stop condition setup time
t_9	1.3		µs	t_{BUF}, bus-free time between a stop condition and a start condition
t_{10}		300	ns	t_R, rise time of both SCL and SDA when receiving
	0		ns	t_R, rise time of both SCL and SDA when receiving or transmitting
t_{11}		300	ns	t_F, fall time of SDA when receiving
		250	ns	t_F, fall time of both SCL and SDA when transmitting
C_B		400	pF	Capacitive load for each bus line

[1] Limits are based on characterization results, with f_{SCL} = 400 kHz and a 3 mA sink current; not production tested.
[2] All values referred to the V_{IH} and the V_{IL} levels given in Table 11.
[3] t_6 is the data hold time that is measured from the falling edge of SCL. It applies to data in transmission and acknowledge.
[4] A transmitting device must internally provide an output hold time of at least 300 ns for the SDA signal (with respect to $V_{IH,min}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.
[5] The maximum t_6 value must be met only if the device does not stretch the low period (t_3) of the SCL signal.
[6] The maximum value for t_6 is a function of the clock low time (t_3), the clock rise time (t_{10}), and the minimum data setup time ($t_{5(min)}$). This value is calculated as $t_{6(max)} = t_3 - t_{10} - t_{5(min)}$.

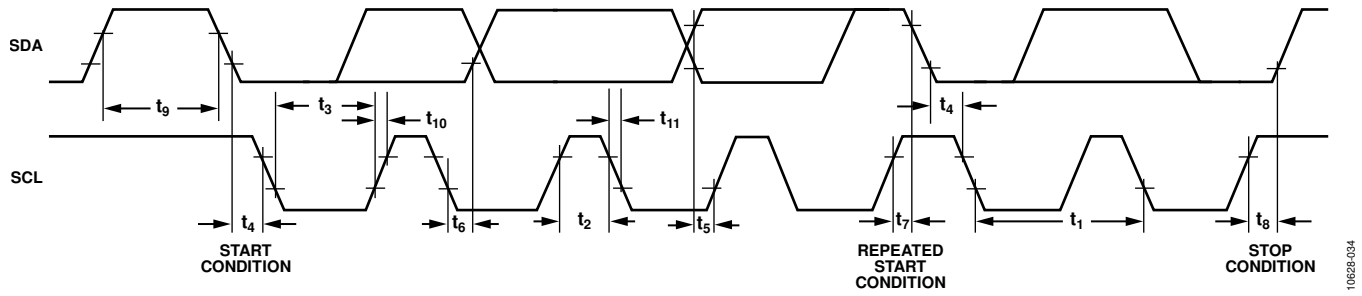


Figure 30. I²C Timing Diagram

INTERRUPTS

The ADXL344 provides two output pins for driving interrupts: INT1 and INT2. Both interrupt pins are push-pull, low impedance pins with the output specifications listed in Table 13. The default configuration of the interrupt pins is active high. This can be changed to active low by setting the INT_INVERT bit (Bit D5) in the DATA_FORMAT (Address 0x31) register. All functions can be used simultaneously, with the only limiting feature being that some functions may need to share interrupt pins.

Interrupts are enabled by setting the appropriate bit in the INT_ENABLE register (Address 0x2E) and are mapped to either the INT1 or INT2 pin based on the contents of the INT_MAP register (Address 0x2F). When initially configuring the interrupt pins, it is recommended that the functions and interrupt mapping be done before enabling the interrupts. When changing the configuration of an interrupt, it is recommended that the interrupt be disabled first, by clearing the bit corresponding to that function in the INT_ENABLE register, and then the function be reconfigured before enabling the interrupt again. Configuration of the functions while the interrupts are disabled helps to prevent the accidental generation of an interrupt before it is desired.

The interrupt functions are latched and cleared by either reading the DATAX, DATAY, and DATAZ registers (Address 0x32 to Address 0x37) until the interrupt condition is no longer valid for the data-related interrupts or by reading the INT_SOURCE register (Address 0x30) for the remaining interrupts. This section describes the interrupts that can be set in the INT_ENABLE register and monitored in the INT_SOURCE register.

DATA_READY Bit

The DATA_READY bit is set when new data is available and is cleared when no new data is available.

SINGLE_TAP Bit

The SINGLE_TAP bit is set when a single acceleration event that is greater than the value in the THRESH_TAP register (Address 0x1D) occurs for less time than is specified in the DUR register (Address 0x21).

DOUBLE_TAP Bit

The DOUBLE_TAP bit is set when two acceleration events that are greater than the value in the THRESH_TAP register (Address 0x1D) occur for less time than is specified in the DUR register (Address 0x21). The second tap starts after the time specified by the latent register (Address 0x22) but within the time specified in the window register (Address 0x23). See the Tap Detection section for more details.

Activity Bit

The activity bit is set when acceleration greater than the value stored in the THRESH_ACT register (Address 0x24) is experienced on any participating axis, as set by the ACT_INACT_CTL register (Address 0x27).

Inactivity Bit

The inactivity bit is set when acceleration of less than the value stored in the THRESH_INACT register (Address 0x25) is experienced for more time than is specified in the TIME_INACT register (Address 0x26) on all participating axes, as set by the ACT_INACT_CTL register (Address 0x27). The maximum value for TIME_INACT is 255 sec.

FREE_FALL Bit

The FREE_FALL bit is set when acceleration of less than the value stored in the THRESH_FF register (Address 0x28) is experienced for more time than is specified in the TIME_FF register (Address 0x29) on all axes (logical AND). The FREE_FALL interrupt differs from the inactivity interrupt as follows: all axes always participate and are logically AND'ed, the timer period is much smaller (1.28 sec maximum), and the mode of operation is always dc-coupled.

Watermark Bit

The watermark bit is set when the number of samples in FIFO equals the value stored in the samples bits (Register FIFO_CTL, Address 0x38). The watermark bit is cleared automatically when FIFO is read, and the content returns to a value below the value stored in the samples bits.

Table 13. Interrupt Pin Digital Output

Parameter	Test Conditions	Limit[1]		Unit
		Min	Max	
Digital Output				
Low Level Output Voltage (V_{OL})	I_{OL} = 300 µA		0.2 × $V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	I_{OH} = −150 µA	0.8 × $V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	V_{OL} = $V_{OL,\ max}$	300		µA
High Level Output Current (I_{OH})	V_{OH} = $V_{OH,\ min}$		−150	µA
Pin Capacitance	f_{IN} = 1 MHz, V_{IN} = 2.6 V		8	pF
Rise/Fall Time				
Rise Time (t_R)[2]	C_{LOAD} = 150 pF		210	ns
Fall Time (t_F)[3]	C_{LOAD} = 150 pF		150	ns

[1] Limits are based on characterization results; not production tested.
[2] Rise time is measured as the transition time from $V_{OL,\ max}$ to $V_{OH,\ min}$ of the interrupt pin.
[3] Fall time is measured as the transition time from $V_{OH,\ min}$ to $V_{OL,\ max}$ of the interrupt pin.

Overrun Bit

The overrun bit is set when new data replaces unread data. The precise operation of the overrun function depends on the FIFO mode. In bypass mode, the overrun bit is set when new data replaces unread data in the DATAX, DATAY, and DATAZ registers (Address 0x32 to Address 0x37). In all other modes, the overrun bit is set when FIFO is filled. The overrun bit is automatically cleared when the contents of FIFO are read.

Orientation Bit

The orientation bit is set when the orientation of the accelerometer changes from a valid orientation to a different valid orientation. An interrupt is not generated, however, if the orientation of the accelerometer changes from a valid orientation to an invalid orientation, or from a valid orientation to an invalid orientation and then back to the same valid orientation. An invalid orientation is defined as an orientation within the dead zone, or the region of hysteresis. This region helps to prevent rapid orientation change due to noise when the accelerometer orientation is close to the boundary between two valid orientations.

The orientations that are valid for the interrupt depend on which mode, 2D or 3D, is linked to the orientation interrupt. The mode is selected with the INT_3D bit (Bit D3) in the ORIENT_CONF register (Address 0x3B). See the Register 0x3B—ORIENT_CONF (Read/Write) section for more details on how to enable the orientation interrupt.

FIFO

The ADXL344 contains an embedded memory management system with a 32-level FIFO memory buffer that can be used to minimize host processor burden. This buffer has four modes: bypass, FIFO, stream, and trigger (see Table 22). Each mode is selected by the settings of the FIFO_MODE bits (Bits[D7:D6]) in the FIFO_CTL register (Address 0x38).

If use of the FIFO is not desired, the FIFO should be placed in bypass mode.

Bypass Mode

In bypass mode, FIFO is not operational and, therefore, remains empty.

FIFO Mode

In FIFO mode, data from measurements of the x-, y-, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set. FIFO continues accumulating samples until it is full (32 samples from measurements of the x-, y-, and z-axes) and then stops collecting data. After FIFO stops collecting data, the device continues to operate; therefore, features such as tap detection can be used after FIFO is full. The watermark interrupt continues to occur until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Stream Mode

In stream mode, data from measurements of the x-, y-, and z-axes are stored in FIFO. When the number of samples in FIFO equals the level specified in the samples bits of the FIFO_CTL register (Address 0x38), the watermark interrupt is set. FIFO continues accumulating samples and holds the latest 32 samples from measurements of the x-, y-, and z-axes, discarding older data as new data arrives. The watermark interrupt continues occurring until the number of samples in FIFO is less than the value stored in the samples bits of the FIFO_CTL register.

Trigger Mode

In trigger mode, FIFO accumulates samples, holding the latest 32 samples from measurements of the x-, y-, and z-axes. After a trigger event occurs and an interrupt is sent to the INT1 or INT2 pin (determined by the trigger bit in the FIFO_CTL register), FIFO keeps the last n samples (where n is the value specified by the samples bits in the FIFO_CTL register) and then operates in FIFO mode, collecting new samples only when FIFO is not full. A delay of at least 5 µs should be present between the trigger event occurring and the start of reading data from the FIFO to allow the FIFO to discard and retain the necessary samples. Additional trigger events cannot be recognized until the trigger mode is reset. To reset the trigger mode, set the device to bypass mode and then set the device back to trigger mode. Note that the FIFO data should be read first because placing the device into bypass mode clears FIFO.

Retrieving Data from FIFO

The FIFO data is read through the DATAX, DATAY, and DATAZ registers (Address 0x32 to Address 0x37). When the FIFO is in FIFO, stream, or trigger mode, reads to the DATAX, DATAY, and DATAZ registers read data stored in the FIFO. Each time data is read from the FIFO, the oldest x-, y-, and z-axes data are placed into the DATAX, DATAY, and DATAZ registers.

If a single-byte read operation is performed, the remaining bytes of data for the current FIFO sample are lost. Therefore, all axes of interest should be read in a burst (or multiple-byte) read operation. To ensure that the FIFO has completely popped (that is, that new data has completely moved into the DATAX, DATAY, and DATAZ registers), there must be at least 5 µs between the end of reading the data registers and the start of a new read of the FIFO or a read of the FIFO_STATUS register (Address 0x39). The end of reading a data register is signified by the transition of data from Register 0x37 to Register 0x38 or by the $\overline{CS}$ pin going high.

For SPI operation at 1.6 MHz or less, the register addressing portion of the transmission is a sufficient delay to ensure that the FIFO has completely popped. For SPI operation greater than 1.6 MHz, it is necessary to deassert the $\overline{CS}$ pin to ensure a total delay of 5 µs; otherwise, the delay is not be sufficient. The total delay necessary for 5 MHz operation is at most 3.4 µs. This is not a concern when using I^2C mode because the communication rate is low enough to ensure a sufficient delay between FIFO reads.

SELF-TEST

The ADXL344 incorporates a self-test feature that effectively tests its mechanical and electronic systems simultaneously. When the self-test function is enabled (via the SELF_TEST bit (Bit D7 in the DATA_FORMAT register, Address 0x31), an electrostatic force is exerted on the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration would, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change in the x-, y-, and z-axes. Because the electrostatic force is proportional to V_S^2, the output change varies with V_S. This effect is shown in Figure 31.

The scale factors listed in Table 14 can be used to adjust the expected self-test output limits for different supply voltages, V_S. The self-test feature of the ADXL344 also exhibits a bimodal behavior. However, the limits listed in Table 1 and Table 15 to Table 18 are valid for both potential self-test values due to bimodality. Use of the self-test feature at data rates less than 100 Hz or at 1600 Hz may yield values outside these limits. Therefore, the part must be in normal power operation (LOW_POWER bit = 0 in the BW_RATE register, Address 0x2C) and be placed into a data rate of 100 Hz through 800 Hz or 3200 Hz for the self-test function to operate correctly.

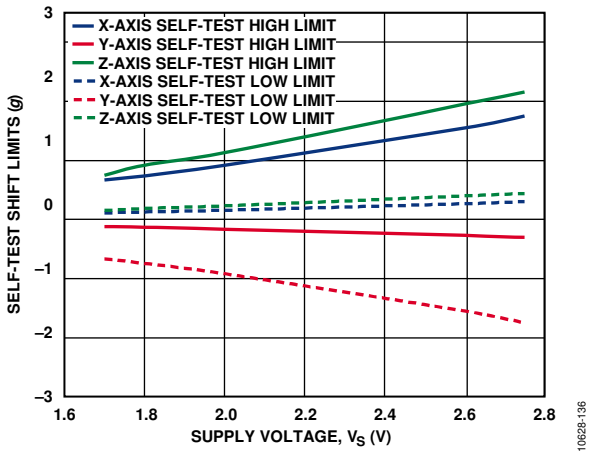


Figure 31. Self-Test Output Change Limits vs. Supply Voltage

Table 14. Self-Test Output Scale Factors for Different Supply Voltages, V_S

Supply Voltage, V_S	X-, Y-Axes	Z-Axis
1.70 V	0.43	0.38
1.80 V	0.48	0.47
2.00 V	0.59	0.58
2.60 V	1.00	1.00
2.75 V	1.13	1.11

Table 15. Self-Test Output in LSB for ±2 *g*, 10-Bit or Full Resolution (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Axis	Min	Max	Unit
X	70	400	LSB
Y	−400	−70	LSB
Z	100	500	LSB

Table 16. Self-Test Output in LSB for ±4 *g*, 10-Bit Resolution (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Axis	Min	Max	Unit
X	35	200	LSB
Y	−200	−35	LSB
Z	50	250	LSB

Table 17. Self-Test Output in LSB for ±8 *g*, 10-Bit Resolution (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Axis	Min	Max	Unit
X	17	100	LSB
Y	−100	−17	LSB
Z	25	125	LSB

Table 18. Self-Test Output in LSB for ±16 *g*, 10-Bit Resolution (T_A = 25°C, V_S = 2.6 V, $V_{DD\ I/O}$ = 1.8 V)

Axis	Min	Max	Unit
X	8	50	LSB
Y	−50	−8	LSB
Z	12	63	LSB

REGISTER MAP

Table 19. Register Map

Address					
Hex	**Dec**	**Name**	**Type**	**Reset Value**	**Description**
0x00	0	DEVID	R	11100110	Device ID.
0x01 to 0x1C	1 to 28	Reserved			Reserved. Do not access.
0x1D	29	THRESH_TAP	R/$\overline{W}$	00000000	Tap threshold.
0x1E	30	OFSX	R/$\overline{W}$	00000000	X-axis offset.
0x1F	31	OFSY	R/$\overline{W}$	00000000	Y-axis offset.
0x20	32	OFSZ	R/$\overline{W}$	00000000	Z-axis offset.
0x21	33	DUR	R/$\overline{W}$	00000000	Tap duration.
0x22	34	Latent	R/$\overline{W}$	00000000	Tap latency.
0x23	35	Window	R/$\overline{W}$	00000000	Tap window.
0x24	36	THRESH_ACT	R/$\overline{W}$	00000000	Activity threshold.
0x25	37	THRESH_INACT	R/$\overline{W}$	00000000	Inactivity threshold.
0x26	38	TIME_INACT	R/$\overline{W}$	00000000	Inactivity time.
0x27	39	ACT_INACT_CTL	R/$\overline{W}$	00000000	Axis enable control for activity and inactivity detection.
0x28	40	THRESH_FF	R/$\overline{W}$	00000000	Free-fall threshold.
0x29	41	TIME_FF	R/$\overline{W}$	00000000	Free-fall time.
0x2A	42	TAP_AXES	R/$\overline{W}$	00000000	Axis control for single tap/double tap.
0x2B	43	ACT_TAP_STATUS	R	00000000	Source of single tap/double tap.
0x2C	44	BW_RATE	R/$\overline{W}$	00001010	Data rate and power mode control.
0x2D	45	POWER_CTL	R/$\overline{W}$	00000000	Power-saving features control.
0x2E	46	INT_ENABLE	R/$\overline{W}$	00000000	Interrupt enable control.
0x2F	47	INT_MAP	R/$\overline{W}$	00000000	Interrupt mapping control.
0x30	48	INT_SOURCE	R	00000010	Source of interrupts.
0x31	49	DATA_FORMAT	R/$\overline{W}$	00000000	Data format control.
0x32	50	DATAX0	R	00000000	X-Axis Data 0.
0x33	51	DATAX1	R	00000000	X-Axis Data 1.
0x34	52	DATAY0	R	00000000	Y-Axis Data 0.
0x35	53	DATAY1	R	00000000	Y-Axis Data 1.
0x36	54	DATAZ0	R	00000000	Z-Axis Data 0.
0x37	55	DATAZ1	R	00000000	Z-Axis Data 1.
0x38	56	FIFO_CTL	R/$\overline{W}$	00000000	FIFO control.
0x39	57	FIFO_STATUS	R	00000000	FIFO status.
0x3A	58	TAP_SIGN	R	00000000	Sign and source for single tap/double tap.
0x3B	59	ORIENT_CONF	R/$\overline{W}$	00100101	Orientation configuration.
0x3C	60	Orient	R	00000000	Orientation status.

REGISTER DEFINITIONS

Register 0x00—DEVID (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	0	1	1	0

The DEVID register holds a fixed device ID code of 0xE6 (346 octal).

Register 0x1D—THRESH_TAP (Read/Write)

The THRESH_TAP register is eight bits and holds the threshold value for tap interrupts. The data format is unsigned, therefore, the magnitude of the tap event is compared with the value in THRESH_TAP for normal tap detection. For information on improved tap detection, refer to the Improved Tap Detection section. The scale factor is 62.5 m*g*/LSB (that is, 0xFF = +16 *g*). A value of 0 may result in undesirable behavior if single-tap/double-tap interrupts are enabled.

Register 0x1E, Register 0x1F, Register 0x20—OFSX, OFSY, OFSZ (Read/Write)

The OFSX, OFSY, and OFSZ registers are each eight bits and offer user-set offset adjustments in twos complement format with a scale factor of 15.6 m*g*/LSB (that is, 0x7F = 2 *g*). The values stored in the offset registers are automatically added to the acceleration data, and the resulting value is stored in the output data registers. For additional information regarding offset calibration and the use of the offset registers, refer to the Offset Calibration section.

Register 0x21—DUR (Read/Write)

The DUR register is eight bits and contains an unsigned time value representing the maximum time that an event must be above the THRESH_TAP threshold to qualify as a tap event. For information on improved tap detection, refer to the Improved Tap Detection section. The scale factor is 625 µs/LSB. A value of 0 disables the single-tap/double-tap functions.

Register 0x22—Latent (Read/Write)

The latent register is eight bits and contains an unsigned time value representing the wait time from the detection of a tap event to the start of the time window (defined by the window register) during which a possible second tap event can be detected. For information on improved tap detection, refer to the Improved Tap Detection section. The scale factor is 1.25 ms/LSB. A value of 0 disables the double-tap function.

Register 0x23—Window (Read/Write)

The window register is eight bits and contains an unsigned time value representing the amount of time after the expiration of the latency time (determined by the latent register) during which a second valid tap can begin. For information on improved tap detection, refer to the Improved Tap Detection section. The scale factor is 1.25 ms/LSB. A value of 0 disables the double-tap function.

Register 0x24—THRESH_ACT (Read/Write)

The THRESH_ACT register is eight bits and holds the threshold value for detecting activity. The data format is unsigned, therefore, the magnitude of the activity event is compared with the value in the THRESH_ACT register. The scale factor is 62.5 m*g*/LSB. A value of 0 may result in undesirable behavior if the activity interrupt is enabled.

Register 0x25—THRESH_INACT (Read/Write)

The THRESH_INACT register is eight bits and holds the threshold value for detecting inactivity. The data format is unsigned, therefore, the magnitude of the inactivity event is compared with the value in the THRESH_INACT register. The scale factor is 62.5 m*g*/LSB. A value of 0 may result in undesirable behavior if the inactivity interrupt is enabled.

Register 0x26—TIME_INACT (Read/Write)

The TIME_INACT register is eight bits and contains an unsigned time value representing the amount of time that acceleration must be less than the value in the THRESH_INACT register for inactivity to be declared. The scale factor is 1 sec/LSB. Unlike the other interrupt functions, which use unfiltered data (see the Threshold section), the inactivity function uses filtered output data. At least one output sample must be generated for the inactivity interrupt to be triggered. This results in the function appearing unresponsive if the TIME_INACT register is set to a value less than the time constant of the output data rate. A value of 0 results in an interrupt when the output data is less than the value in the THRESH_INACT register.

Register 0x27—ACT_INACT_CTL (Read/Write)

D7	D6	D5	D4
ACT ac/dc	ACT_X enable	ACT_Y enable	ACT_Z enable
D3	**D2**	**D1**	**D0**
INACT ac/dc	INACT_X enable	INACT_Y enable	INACT_Z enable

ACT AC/DC and INACT AC/DC Bits

A setting of 0 selects dc-coupled operation, and a setting of 1 enables ac-coupled operation. In dc-coupled operation, the current acceleration magnitude is compared directly with THRESH_ACT and THRESH_INACT to determine whether activity or inactivity is detected.

In ac-coupled operation for activity detection, the acceleration value at the start of activity detection is taken as a reference value. New samples of acceleration are then compared to this reference value, and if the magnitude of the difference exceeds the THRESH_ACT value, the device triggers an activity interrupt.

Similarly, in ac-coupled operation for inactivity detection, a reference value is used for comparison and is updated whenever the device exceeds the inactivity threshold. After the reference value is selected, the device compares the magnitude of the difference between the reference value and the current acceleration with THRESH_INACT. If the difference is less than the value in THRESH_INACT for the time in TIME_INACT, the device is considered inactive and the inactivity interrupt is triggered.

ACT_x Enable Bits and INACT_x Enable Bits

A setting of 1 enables x-, y-, or z-axis participation in detecting activity or inactivity. A setting of 0 excludes the selected axis from participation. If all axes are excluded, the function is disabled. For activity detection, all participating axes are logically OR'ed, causing the activity function to trigger when any of the participating axes exceeds the threshold. For inactivity detection, all participating axes are logically AND'ed, causing the inactivity function to trigger only if all participating axes are below the threshold for the specified period of time.

Register 0x28—THRESH_FF (Read/Write)

The THRESH_FF register is eight bits and holds the threshold value, in unsigned format, for free-fall detection. The acceleration on all axes is compared with the value in THRESH_FF to determine if a free-fall event occurred. The scale factor is 62.5 mg/LSB. Note that a value of 0 mg may result in undesirable behavior if the free-fall interrupt is enabled. Values between 300 mg and 600 mg (0x05 to 0x09) are recommended.

Register 0x29—TIME_FF (Read/Write)

The TIME_FF register is eight bits and stores an unsigned time value representing the minimum time that the value of all axes must be less than THRESH_FF to generate a free-fall interrupt. The scale factor is 5 ms/LSB. A value of 0 may result in undesirable behavior if the free-fall interrupt is enabled. Values between 100 ms and 350 ms (0x14 to 0x46) are recommended.

Register 0x2A—TAP_AXES (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Improved tap	Suppress	TAP_X enable	TAP_Y enable	TAP_Z enable

Improved Tap Bit

The improved tap bit is used to enable improved tap detection. This mode of operation improves tap detection by performing an ac-coupled differential comparison of the output acceleration data. The improved tap detection is performed on the same output data available in the DATAX, DATAY, and DATAZ registers. Due to the dependency on the output data rate and the ac-coupled differential measurement, the threshold and timing values for single taps and double taps must be adjusted for improved tap detection. For further explanation of improved tap detection, see the Improved Tap Detection section. Improved tap is enabled by setting the improved tap bit to a value of 1 and is disabled by clearing the bit to a value of 0.

Suppress Bit

Setting the suppress bit suppresses double-tap detection if acceleration greater than the value in THRESH_TAP is present between taps. See the Tap Detection section for more details.

TAP_x Enable Bits

A setting of 1 in the TAP_X enable, TAP_Y enable, or TAP_Z enable bit enables x-, y-, or z-axis participation in tap detection. A setting of 0 excludes the selected axis from participation in tap detection.

Register 0x2B—ACT_TAP_STATUS (Read Only)

D7	D6	D5	D4	D3	D2	D1	D0
0	ACT_X source	ACT_Y source	ACT_Z source	Asleep	TAP_X source	TAP_Y source	TAP_Z source

ACT_x Source and TAP_x Source Bits

These bits indicate the first axis involved in a tap or activity event. A setting of 1 corresponds to involvement in the event, and a setting of 0 corresponds to no involvement. When new data is available, these bits are not cleared but are overwritten by the new data. The ACT_TAP_STATUS register should be read before clearing the interrupt. Disabling an axis from participation clears the corresponding source bit when the next activity or single-tap/double-tap event occurs.

Asleep Bit

A setting of 1 in the asleep bit indicates that the part is asleep, and a setting of 0 indicates that the part is not asleep. This bit toggles only if the device is configured for autosleep. See the Register 0x2D—POWER_CTL (Read/Write) section for more information on autosleep mode.

Register 0x2C—BW_RATE (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	LOW_POWER	Rate			

LOW_POWER Bit

A setting of 0 in the LOW_POWER bit selects normal operation, and a setting of 1 selects reduced power operation, which is associated with somewhat higher noise (see the Power Modes section for details).

Rate Bits

These bits select the device bandwidth and output data rate (see Table 7 and Table 8 for details). The default value is 0x0A, which translates to a 100 Hz output data rate. An output data rate should be selected that is appropriate for the communication protocol and frequency selected. Selecting too high of an output data rate with a low communication speed results in samples being discarded.

Register 0x2D—POWER_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	Link	AUTO_SLEEP	Measure	Sleep	Wakeup	

Link Bit

A setting of 1 in the link bit with both the activity and inactivity functions enabled delays the start of the activity function until inactivity is detected. After activity is detected, inactivity detection begins, preventing the detection of activity. This bit serially links the activity and inactivity functions. When this bit is set to 0, the inactivity and activity functions are concurrent. Additional information can be found in the Link Mode section.

When clearing the link bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the link bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

AUTO_SLEEP Bit

If the link bit is set, a setting of 1 in the AUTO_SLEEP bit enables the autosleep functionality. In this mode, the ADXL344 automatically switches to sleep mode if the inactivity function is enabled and inactivity is detected (that is, when acceleration is below the THRESH_INACT value for at least the time indicated by TIME_INACT). If activity is also enabled, the ADXL344 automatically wakes up from sleep after detecting activity and returns to operation at the output data rate set in the BW_RATE register. A setting of 0 in the AUTO_SLEEP bit disables automatic switching to sleep mode. See the description of the sleep bit in this section for more information on sleep mode.

If the link bit is not set, the AUTO_SLEEP feature is disabled, and setting the AUTO_SLEEP bit does not have any impact on device operation. Refer to the Link Bit section or the Link Mode section for more information about using the link feature.

When clearing the AUTO_SLEEP bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the AUTO_SLEEP bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Measure Bit

A setting of 0 in the measure bit places the part into standby mode, and a setting of 1 places the part into measurement mode. The ADXL344 powers up in standby mode with minimum power consumption.

Sleep Bit

A setting of 0 in the sleep bit puts the part into the normal mode of operation, and a setting of 1 places the part into sleep mode. Sleep mode suppresses DATA_READY, stops transmission of data to FIFO, and switches the sampling rate to one specified by the wakeup bits. In sleep mode, only the activity function can be used. While the DATA_READY interrupt is suppressed, the output data registers are still updated at the sampling rate set by the wakeup bits.

When clearing the sleep bit, it is recommended that the part be placed into standby mode and then set back to measurement mode with a subsequent write. This is done to ensure that the device is properly biased if sleep mode is manually disabled; otherwise, the first few samples of data after the sleep bit is cleared may have additional noise, especially if the device was asleep when the bit was cleared.

Wakeup Bits

These bits control the frequency of readings in sleep mode as described in Table 20.

Table 20. Frequency of Readings in Sleep Mode

Setting		
D1	**D0**	**Frequency (Hz)**
0	0	8
0	1	4
1	0	2
1	1	1

Register 0x2E—INT_ENABLE (Read/Write)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun/ orientation

Setting bits in this register to a value of 1 enables their respective functions to generate interrupts, whereas a value of 0 prevents the functions from generating interrupts. The DATA_READY, watermark, and overrun/orientation bits enable only the interrupt output; the functions are always enabled. It is recommended that interrupts be configured before enabling their outputs.

Register 0x2F—INT_MAP (Read/Write)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun/ orientation

Bits set to 0 in this register send their respective interrupts to the INT1 pin, whereas bits set to 1 send their respective interrupts to the INT2 pin. All selected interrupts for a given pin are ORed.

Register 0x30—INT_SOURCE (Read Only)

D7	**D6**	**D5**	**D4**
DATA_READY	SINGLE_TAP	DOUBLE_TAP	Activity
D3	**D2**	**D1**	**D0**
Inactivity	FREE_FALL	Watermark	Overrun/ orientation

Bits set to 1 in this register indicate that their respective functions have triggered an event, whereas bits set to 0 indicate that the corresponding events have not occurred. The DATA_READY, watermark, and overrun/orientation bits are always set if the corresponding events occur, regardless of the INT_ENABLE register settings, and are cleared by reading data from the DATAX, DATAY, and DATAZ registers. The DATA_READY and watermark bits may require multiple reads, as indicated in the FIFO mode descriptions in the FIFO section. Other bits, and the corresponding interrupts, including orientation if enabled, are cleared by reading the INT_SOURCE register.

Register 0x31—DATA_FORMAT (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
SELF_TEST	SPI	INT_INVERT	0	FULL_RES	Justify	Range	

The DATA_FORMAT register controls the presentation of data to Register 0x32 through Register 0x37. All data, except that for the ±16 *g* range, must be clipped to avoid rollover.

SELF_TEST Bit

A setting of 1 in the SELF_TEST bit applies a self-test force to the sensor, causing a shift in the output data. A value of 0 disables the self-test force.

SPI Bit

A value of 1 in the SPI bit sets the device to 3-wire SPI mode, and a value of 0 sets the device to 4-wire SPI mode.

INT_INVERT Bit

A value of 0 in the INT_INVERT bit sets the interrupts to active high, and a value of 1 sets the interrupts to active low.

FULL_RES Bit

When this bit is set to a value of 1, the device is in full resolution mode, where the output resolution increases with the *g* range set by the range bits to maintain a 4 mg/LSB scale factor. When the FULL_RES bit is set to 0, the device is in 10-bit mode, and the range bits determine the maximum *g* range and scale factor.

Justify Bit

A setting of 1 in the justify bit selects left-justified (MSB) mode, and a setting of 0 selects right-justified mode with sign extension.

Range Bits

These bits set the *g* range as described in Table 21.

Table 21. *g* Range Setting

Setting		
D1	D0	*g* Range
0	0	±2 *g*
0	1	±4 *g*
1	0	±8 *g*
1	1	±16 *g*

Register 0x32 to Register 0x37—DATAX0, DATAX1, DATAY0, DATAY1, DATAZ0, DATAZ1 (Read Only)

These six bytes (Register 0x32 to Register 0x37) are eight bits each and hold the output data for each axis. Register 0x32 and Register 0x33 hold the output data for the x-axis, Register 0x34 and Register 0x35 hold the output data for the y-axis, and Register 0x36 and Register 0x37 hold the output data for the z-axis. The output data is twos complement, with DATAx0 as the least significant byte and DATAx1 as the most significant byte, where x represents X, Y, or Z. The DATA_FORMAT register (Address 0x31) controls the format of the data. It is recommended that a multiple-byte read of all registers be performed to prevent a change in data between reads of sequential registers.

Register 0x38—FIFO_CTL (Read/Write)

D7	D6	D5	D4	D3	D2	D1	D0
FIFO_MODE		Trigger	Samples				

FIFO_MODE Bits

These bits set the FIFO mode, as described in Table 22.

Table 22. FIFO Modes

Setting			
D7	D6	Mode	Function
0	0	Bypass	FIFO is bypassed.
0	1	FIFO	FIFO collects up to 32 values and then stops collecting data, collecting new data only when FIFO is not full.
1	0	Stream	FIFO holds the last 32 data values. When FIFO is full, the oldest data is overwritten with newer data.
1	1	Trigger	When triggered by the trigger bit, FIFO holds the last data samples before the trigger event and then continues to collect data until FIFO is full. New data is collected only when FIFO is not full.

Trigger Bit

A value of 0 in the trigger bit links the trigger event of trigger mode to INT1, and a value of 1 links the trigger event to INT2.

Samples Bits

The function of these bits depends on the FIFO mode selected (see Table 23). Entering a value of 0 in the samples bits immediately sets the watermark bit in the INT_SOURCE register (Address 0x30), regardless of which FIFO mode is selected. Undesirable operation may occur if a value of 0 is used for the samples bits when trigger mode is used.

Table 23. Samples Bits Functions

FIFO Mode	Samples Bits Function
Bypass	None.
FIFO	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Stream	Specifies how many FIFO entries are needed to trigger a watermark interrupt.
Trigger	Specifies how many FIFO samples are retained in the FIFO buffer before a trigger event.