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Micropower 3-Sensor Combination Including Acceleration and Temperature

Data Sheet **ADXL363**

FEATURES

- **Accelerometer, temperature sensor, and provision for 3rd analog sensor input**
- **All sensors sampled synchronously**
  - **Up to 400 Hz output data rate (ODR)**
  - **Samples can be synchronized to external trigger**
- **Ultralow power**
  - **1.95 μA at 100 Hz ODR, 2.0 V supply, all sensors on**
  - **270 nA at 6 Hz motion activated wake-up mode**
  - **10 nA standby current**
- **12-bit resolution for all sensors**
  - **Acceleration scale factor down to 1 m*g*/LSB**
  - **Temperature scale factor: 0.065°C/LSB (average)**
- **Built-in features for motion-based system level power savings**
  - **Adjustable threshold sleep/wake modes for motion activation**
  - **Autonomous interrupt processing, without need for microcontroller intervention, to allow the rest of the system to be turned off completely**
  - **Deep embedded FIFO minimizes host processor load**
  - **Awake state output enables implementation of standalone, motion activated switch**
- **Wide supply and I/O voltage ranges: 1.6 V to 3.5 V**
  - **Operates off 1.8 V to 3.3 V rails**
  - **Power can be derived from coin cell battery**
- **SPI digital interface**
- **Small and thin 3 mm × 3.25 mm × 1.06 mm package**

APPLICATIONS

- **Home healthcare devices**
- **Wireless sensors**
- **Motion enabled metering devices**

GENERAL DESCRIPTION

The ADXL363 is an ultralow power, three-sensor combination consisting of a 3-axis MEMS accelerometer, a temperature sensor, and an on-board ADC input for synchronous conversion of an external signal. The entire system consumes less than 2 μA at a 100 Hz output data rate and 270 nA when in motion triggered wake-up mode.

The ADXL363 communicates via a serial port interface (SPI) and always provides 12-bit output resolution for all three sensors.

The ADXL363 accelerometer provides selectable measurement ranges of ±2 *g*, ±4 *g*, and ±8 *g*, with a resolution of 1 m*g*/LSB on the ±2 *g* range. Unlike accelerometers that use power duty cycling to achieve low power consumption, the ADXL363 does not alias input signals by undersampling; it samples the full bandwidth of the sensor at all data rates.

The ADXL363 temperature sensor operates with a scale factor of 0.065°C (typical). Acceleration and temperature data can be stored in a 512-sample multimode FIFO buffer, allowing up to 13 sec of data to be stored.

In addition to the accelerometer and temperature sensor, the ADXL363 also provides access to an internal ADC for synchronous conversion of an additional analog input.

The ADXL363 operates on a wide 1.6 V to 3.5 V supply range, and can interface, if necessary, to a host operating on a separate, lower supply voltage. The ADXL363 is available in a 3 mm × 3.25 mm × 1.06 mm package.

FUNCTIONAL BLOCK DIAGRAM

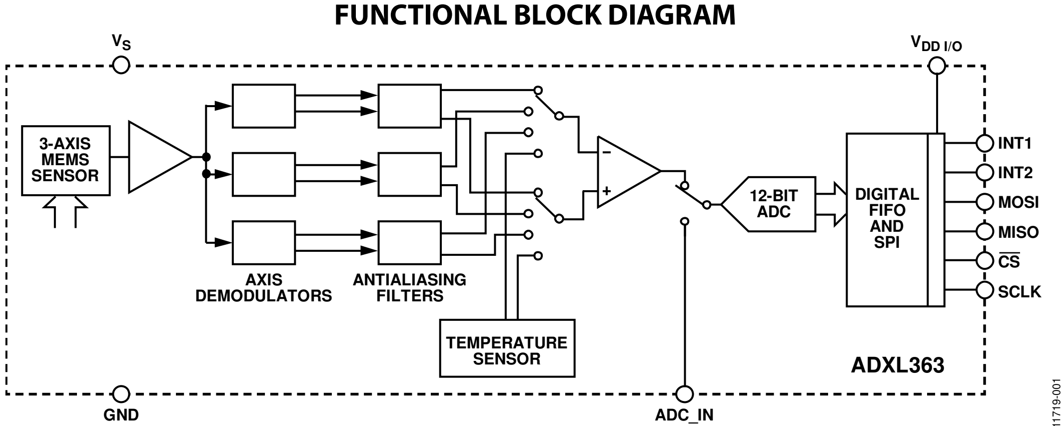

Figure 1.

Rev. 0 **Document Feedback**

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ADXL363* PRODUCT PAGE QUICK LINKS

Last Content Update: 02/23/2017

COMPARABLE PARTS

View a parametric search of comparable parts.

DOCUMENTATION

Data Sheet

- ADXL363: Micropower 3-Sensor Combination Including Acceleration and Temperature Data Sheet

DESIGN RESOURCES

- ADXL363 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

DISCUSSIONS

View all ADXL363 EngineerZone Discussions.

SAMPLE AND BUY

Visit the product page to see pricing options.

TECHNICAL SUPPORT

Submit a technical question or find your regional support number.

DOCUMENT FEEDBACK

Submit feedback for this data sheet.

TABLE OF CONTENTS

REVISION HISTORY

1//13—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 2.0 V, $V_{DD\ I/O}$ = 2.0 V, 100 Hz ODR, acceleration = 0 *g*, default register settings, unless otherwise noted. All minimum and maximum specifications are guaranteed. Typical specifications may not be guaranteed.

ADXL363 SPECIFICATIONS

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
OUTPUT RESOLUTION					
All Sensors			12		Bits
SUPPLY CURRENT					
Measurement Mode	All sensors on (ADC_EN = 1)		1.95		µA
Standby			10		nA
OUTPUT DATA RATE (ODR)	User selectable in eight steps	12.5		400	Hz
POWER SUPPLY REJECTION (PSRR)	C_S = 1.0 µF, R_S = 100 Ω, C_{IO} = 1.1 µF, input is 100 mV sine wave on V_S				
Input Frequency 100 Hz to 1 kHz			−13		dB
Input Frequency 1 kHz to 250 kHz			−20		dB
TURN-ON TIME	50 Hz bandwidth				
Power-Up to Standby			5		ms
Measurement Mode Instruction to Valid Data			4/ODR		
POWER SUPPLY REQUIREMENTS					
Operating Voltage Range (V_S)		1.6	2.0	3.5	V
I/O Voltage Range ($V_{DD\ I/O}$)		1.6	2.0	V_S	V
ENVIRONMENTAL					
Operating Temperature Range		−40		+85	°C

ACCELEROMETER SPECIFICATIONS

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SENSOR INPUT	Each axis				
Measurement Range	User selectable		±2, ±4, ±8		*g*
Nonlinearity	Percentage of full scale		±0.5		%
Sensor Resonant Frequency			3500		Hz
Cross Axis Sensitivity[1]			±1.5		%
SUPPLY CURRENT	100 Hz ODR (50 Hz bandwidth)[2], ADC_EN = 0				
Measurement Mode					
Normal Operation			1.8		µA
Accelerometer Low Noise Mode			3.3		µA
Accelerometer Ultralow Noise Mode			13		µA
Wake-Up Mode			270		nA
SCALE FACTOR	Each axis				
Scale Factor Calibration Error				±10	%
Scale Factor	Measured in m*g*/LSB				
	±2 *g* range		1		m*g*/LSB
	±4 *g* range		2		m*g*/LSB
	±8 *g* range		4		m*g*/LSB

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	Measured in LSB/*g*				
	±2 *g* range		1000		LSB/*g*
	±4 *g* range		500		LSB/*g*
	±8 *g* range		250		LSB/*g*
Scale Factor Change Due to Temperature[3]	−40°C to +85°C		0.05		%/°C
0 *g* OFFSET					
0 *g* Output	X_{OUT}, Y_{OUT}	−150	±35	+150	m*g*
	Z_{OUT}	−250	±50	+250	m*g*
0 *g* Offset vs. Temperature[3]					
Normal Operation	X_{OUT}, Y_{OUT}		±0.5		m*g*/°C
	Z_{OUT}		±0.6		m*g*/°C
Low Noise Mode and Ultralow Noise Mode	X_{OUT}, Y_{OUT}, Z_{OUT}		±0.35		m*g*/°C
NOISE PERFORMANCE					
Noise Density					
Normal Operation	X_{OUT}, Y_{OUT}		550		μ*g*/√Hz
	Z_{OUT}		920		μ*g*/√Hz
Low Noise Mode	X_{OUT}, Y_{OUT}		400		μ*g*/√Hz
	Z_{OUT}		550		μ*g*/√Hz
Ultralow Noise Mode	X_{OUT}, Y_{OUT}		250		μ*g*/√Hz
	Z_{OUT}		350		μ*g*/√Hz
	V_S = 3.5 V; X_{OUT}, Y_{OUT}		175		μ*g*/√Hz
	V_S = 3.5 V; Z_{OUT}		250		μ*g*/√Hz
BANDWIDTH					
Low-Pass (Antialiasing) Filter, −3 dB Corner	HALF_BW = 0		ODR/2		Hz
	HALF_BW = 1		ODR/4		Hz
Output Data Rate (ODR)	User selectable in eight steps	12.5		400	Hz
SELF TEST					
Output Change[4]	X_{OUT}	450	580	710	m*g*
	Y_{OUT}	−710	−580	−450	m*g*
	Z_{OUT}	350	500	650	m*g*

[1] Cross axis sensitivity is defined as coupling between any two axes.
[2] Refer to Figure 29 for current consumption at other bandwidth settings.
[3] −40°C to +25°C or +25°C to +85°C.
[4] Self test change is defined as the output change in *g* when self test is asserted.

TEMPERATURE SENSOR SPECIFICATIONS

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
BIAS	At 25°C				
Average			350		LSB
Standard Deviation			290		LSB
SCALE FACTOR					
Average			0.065		°C/LSB
Standard Deviation			0.0025		°C/LSB
Repeatability			±0.5		°C
OUTPUT RESOLUTION			12		Bits

12-BIT ADC SPECIFICATIONS

Table 4.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
ANALOG-TO-DIGITAL CONVERTER					
Input Voltage Range		$0.1 \times V_S$		$0.9 \times V_S$	
Integral Nonlinearity (INL)	V_S = 1.6 V		±1.0		LSB
	V_S = 2.0 V		±0.8		LSB
	V_S = 3.5 V		±1.1		LSB
Differential Nonlinearity (DNL)	V_S = 1.6 V		±1.8		LSB
	V_S = 2.0 V		±1.6		LSB
	V_S = 3.5 V		±2.1		LSB
Offset Error	V_S = 1.6 V		1.6		LSB
	V_S = 2.0 V		3.4		LSB
	V_S = 3.5 V		9.1		LSB
Gain Error	V_S = 1.6 V		−4.3		LSB
	V_S = 2.0 V		−5.3		LSB
	V_S = 3.5 V		−11.8		LSB
Throughput (ODR)	User selectable in eight steps		ODR		

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Acceleration (Any Axis, Unpowered)	5000 *g*
Acceleration (Any Axis, Powered)	5000 *g*
V_S	−0.3 V to +3.6 V
$V_{DD\ I/O}$	−0.3 V to +3.6 V
All Other Pins	−0.3 V to V_S
Output Short-Circuit Duration (Any Pin to Ground)	Indefinite
ESD, Human Body Model (HBM)	2000 V
Short Term Maximum Temperature	
Four Hours	150°C
One Minute	260°C
Temperature Range (Powered)	−50°C to +150°C
Temperature Range (Storage)	−50°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 6. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	150°C/W	85°C/W	18 mg

RECOMMENDED SOLDERING PROFILE

Figure 2 and Table 7 provide details about the recommended soldering profile.

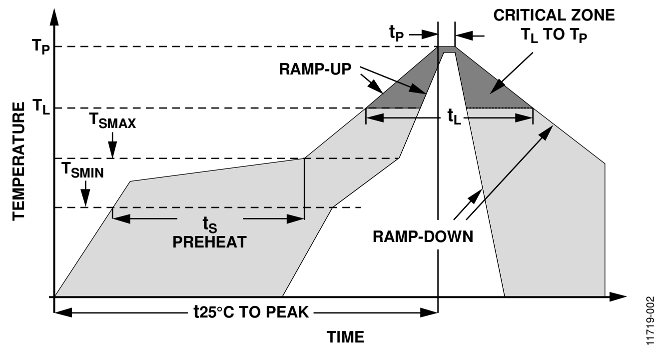

Figure 2. Recommended Soldering Profile

Table 7. Recommended Soldering Profile

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX})(t_S)	60 sec to 120 sec	60 sec to 180 sec
T_{SMAX} to T_L Ramp-Up Rate	3°C/sec max	3°C/sec max
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240 + 0/−5°C	260 + 0/−5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time ($t_{25°C}$) to Peak Temperature	6 minutes max	8 minutes max

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

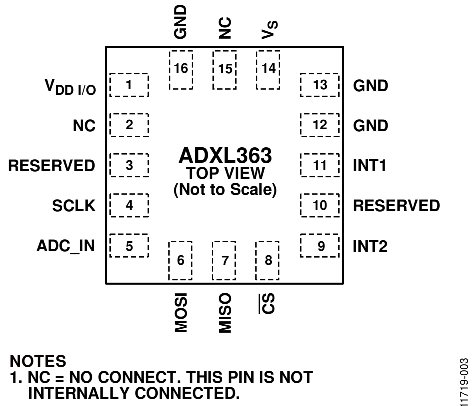

Figure 3. Pin Configuration (Top View)

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$V_{DD\ I/O}$	Supply Voltage for Digital I/O.
2	NC	No Connect. This pin is not internally connected.
3	RESERVED	Reserved. Leave this pin unconnected, or connect it to GND.
4	SCLK	SPI Communications Clock.
5	ADC_IN	Input to Auxiliary ADC.
6	MOSI	Master Output, Slave Input. SPI serial data input.
7	MISO	Master Input, Slave Output. SPI serial data output.
8	$\overline{CS}$	SPI Chip Select, Active Low. Must be low during SPI communications.
9	INT2	Interrupt 2 Output. INT2 also serves as an input for synchronized sampling.
10	RESERVED	Reserved. Leave this pin unconnected, or connect it to GND.
11	INT1	Interrupt 1 Output. INT1 also serves as an input for external clocking.
12	GND	Ground. Ground this pin.
13	GND	Ground. Ground this pin.
14	V_S	Supply Voltage.
15	NC	No Connect. This pin is not internally connected.
16	GND	Ground. Ground this pin.

TYPICAL PERFORMANCE CHARACTERISTICS

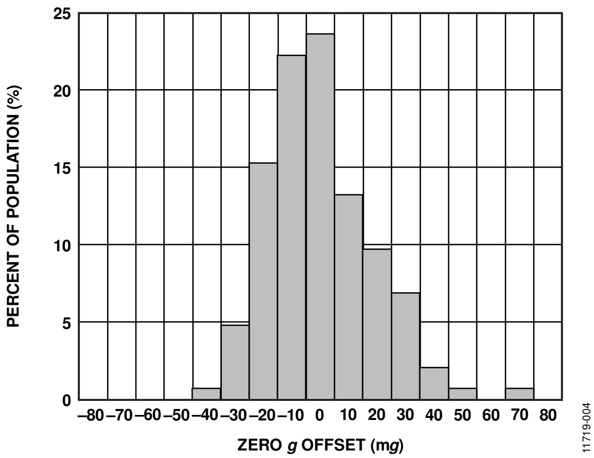

Figure 4. Accelerometer X-Axis Zero g Offset at 25°C, V_S = 2 V

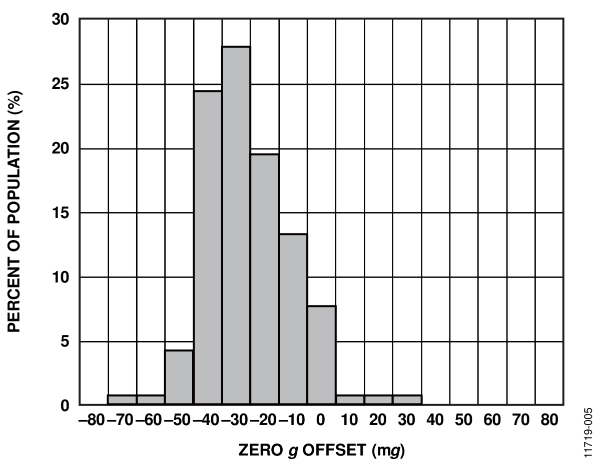

Figure 5. Accelerometer Y-Axis Zero g Offset at 25°C, V_S = 2 V

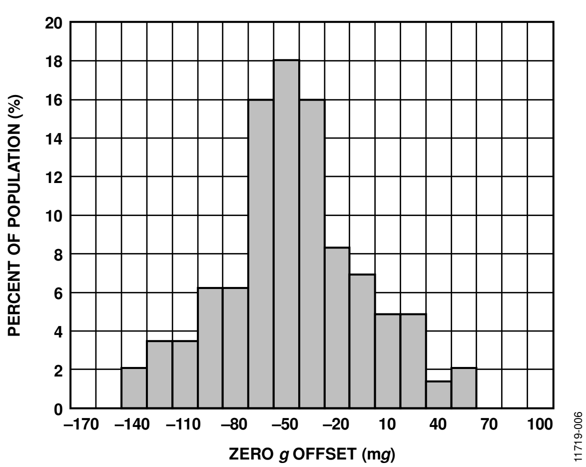

Figure 6. Accelerometer Z-Axis Zero g Offset at 25°C, V_S = 2 V

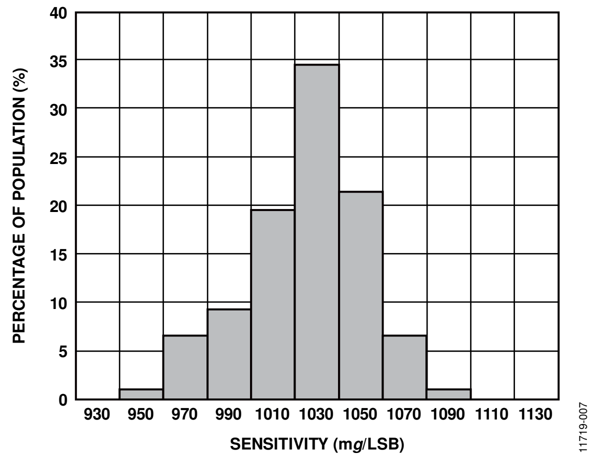

Figure 7. Accelerometer X-Axis Scale Factor at 25°C, V_S = 2 V, ±2 g Range

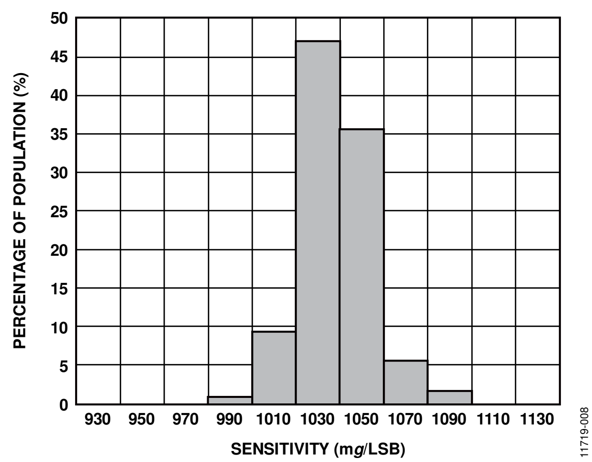

Figure 8. Accelerometer Y-Axis Scale Factor at 25°C, V_S = 2 V, ±2 g Range

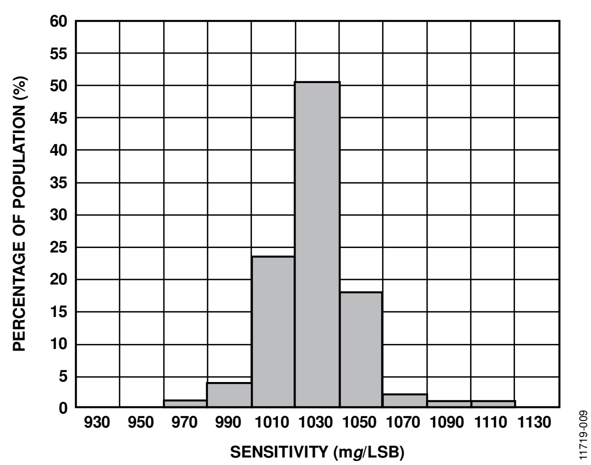

Figure 9. Accelerometer Z-Axis Scale Factor at 25°C, V_S = 2 V, ±2 g Range

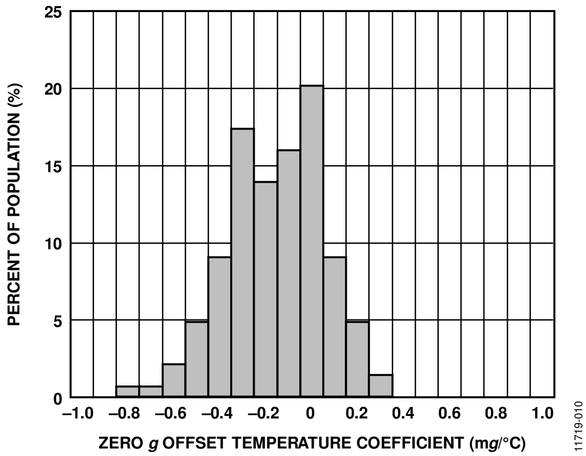

Figure 10. Accelerometer X-Axis Zero g Offset Temperature Coefficient, $V_S = 2$ V

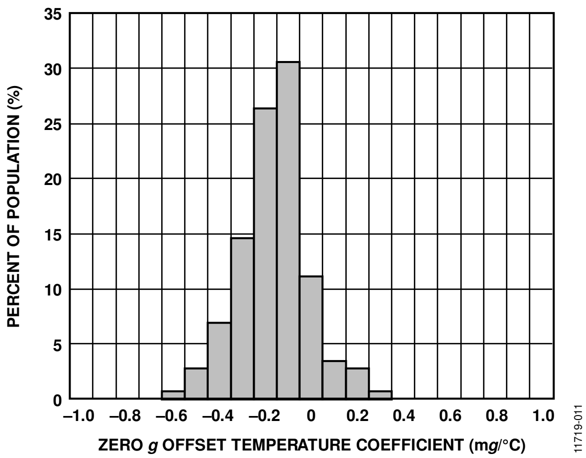

Figure 11. Accelerometer Y-Axis Zero g Offset Temperature Coefficient, $V_S = 2$ V

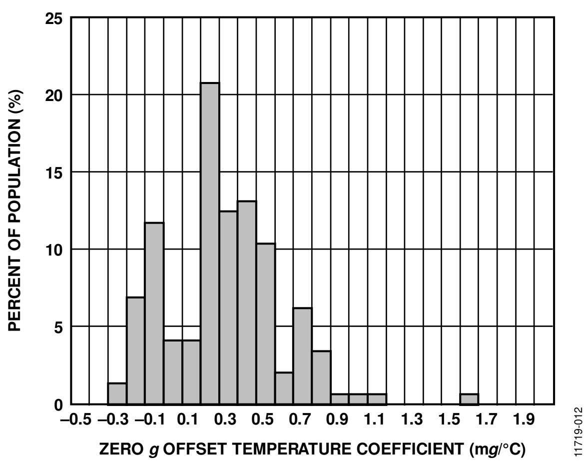

Figure 12. Accelerometer Z-Axis Zero g Offset Temperature Coefficient, $V_S = 2$ V

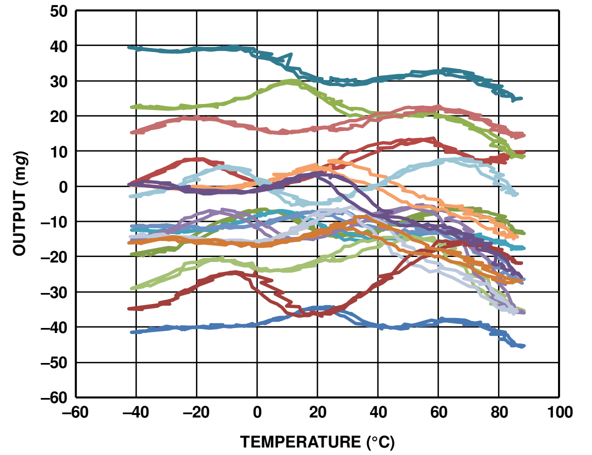

Figure 13. Accelerometer X-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, $V_S = 2$ V

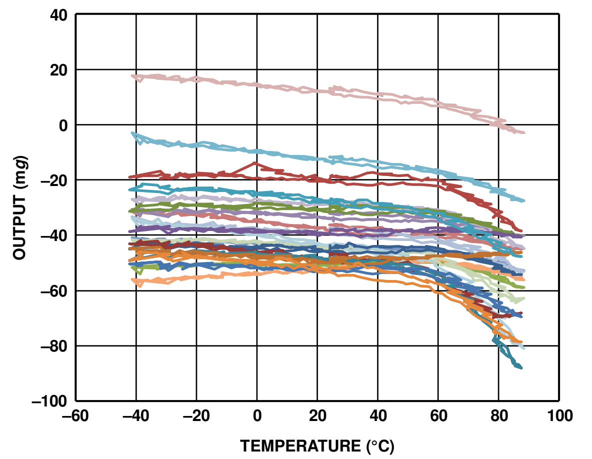

Figure 14. Accelerometer Y-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, $V_S = 2$ V

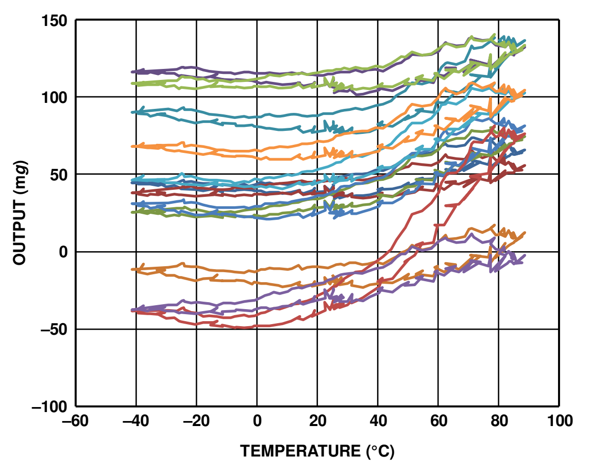

Figure 15. Accelerometer Z-Axis Zero g Offset vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, $V_S = 2$ V

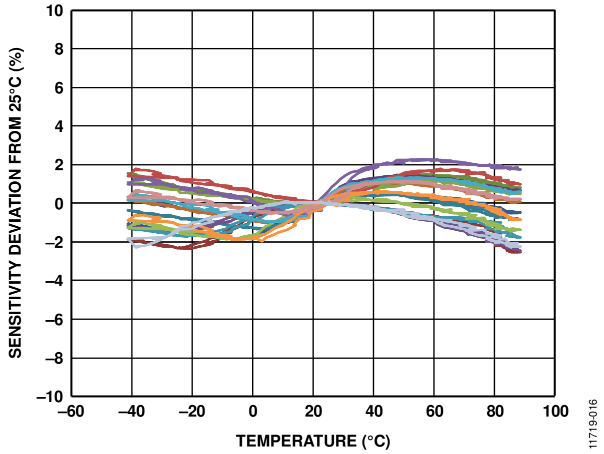

Figure 16. Accelerometer X-Axis Scale Factor Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

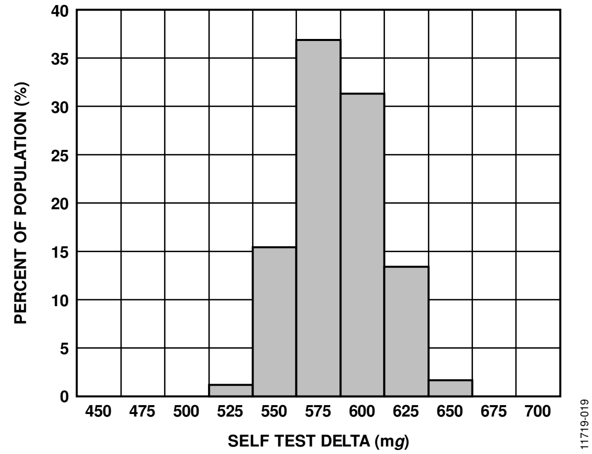

Figure 19. Accelerometer X-Axis Self Test Response at 25°C, V_S = 2 V

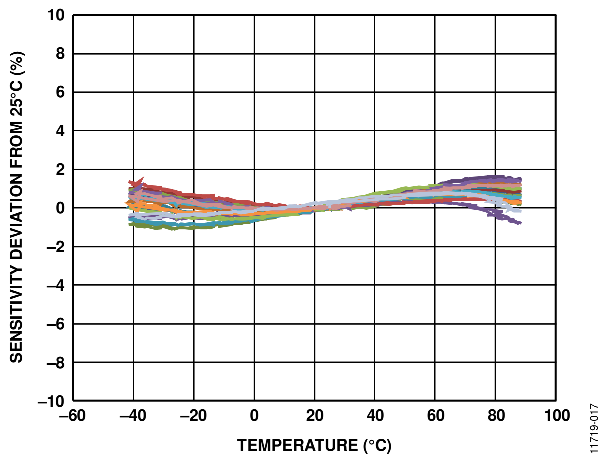

Figure 17. Accelerometer Y-Axis Scale Factor Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

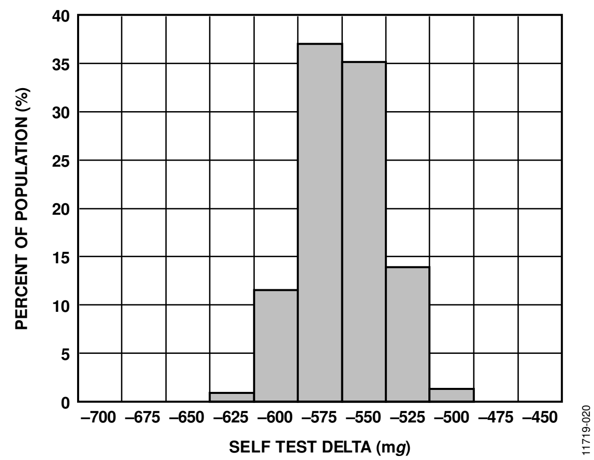

Figure 20. Accelerometer Y-Axis Self Test Response at 25°C, V_S = 2 V

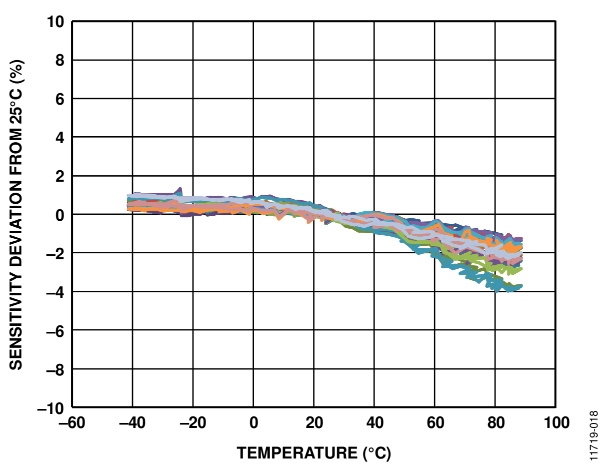

Figure 18. Accelerometer Z-Axis Scale Factor Deviation from 25°C vs. Temperature—16 Parts Soldered to PCB, ODR = 100 Hz, V_S = 2 V

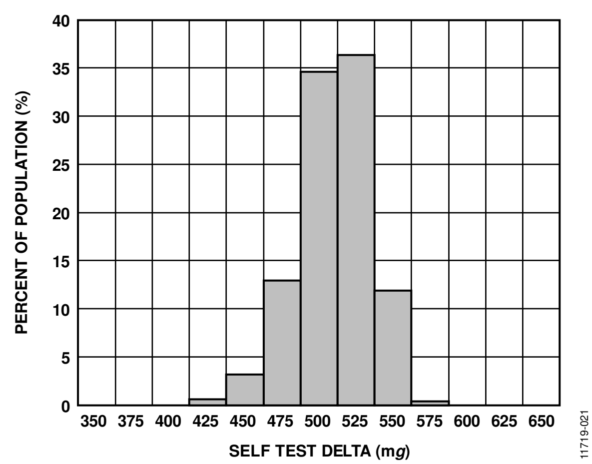

Figure 21. Accelerometer Z-Axis Self Test Response at 25°C, V_S = 2 V

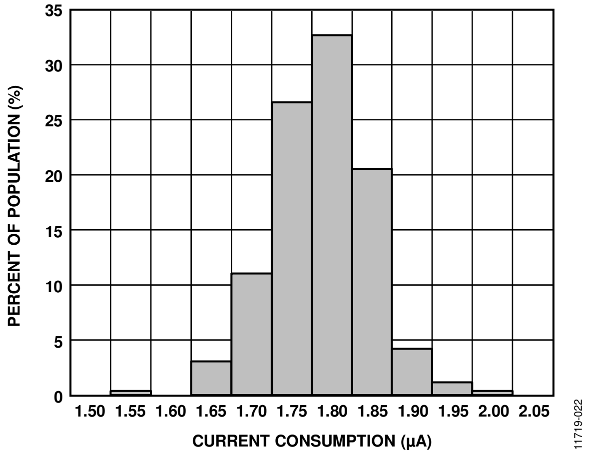

Figure 22. Current Consumption at 25°C, Normal Mode, ADC Disabled, ODR = 100 Hz, V_S = 2 V

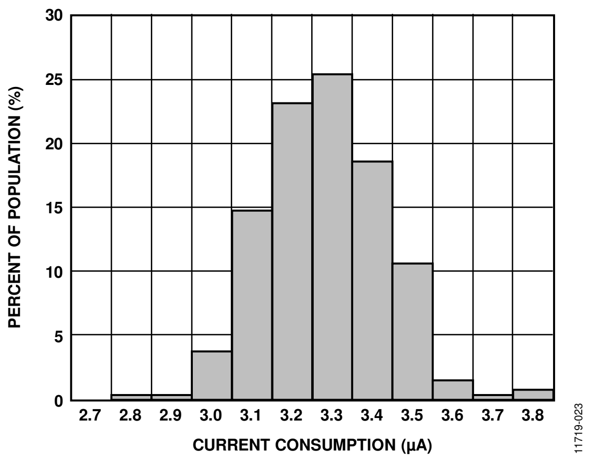

Figure 23. Current Consumption at 25°C, Low Noise Mode, ADC Disabled, ODR = 100 Hz, V_S = 2 V

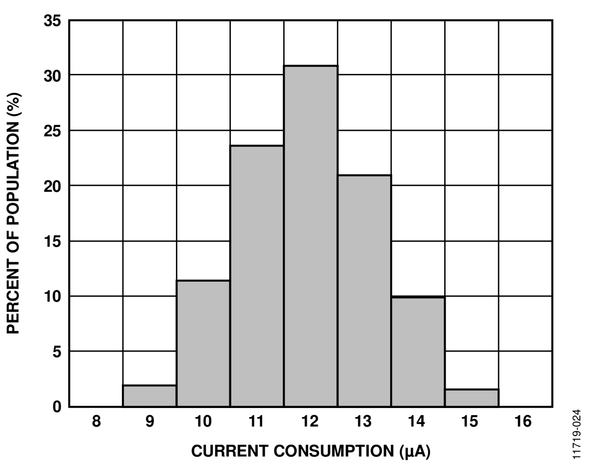

Figure 24. Current Consumption at 25°C, Ultralow Noise Mode, ADC Disabled, ODR = 100 Hz, V_S = 2 V

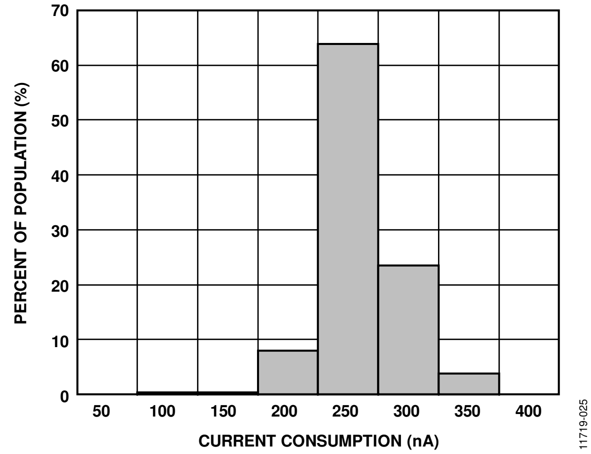

Figure 25. Current Consumption at 25°C, Wake-Up Mode, ADC Disabled, V_S = 2 V

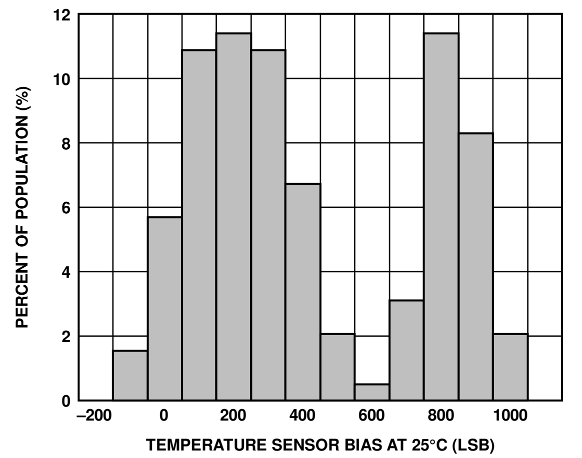

Figure 26. Temperature Sensor Response at 25°C, V_S = 2 V

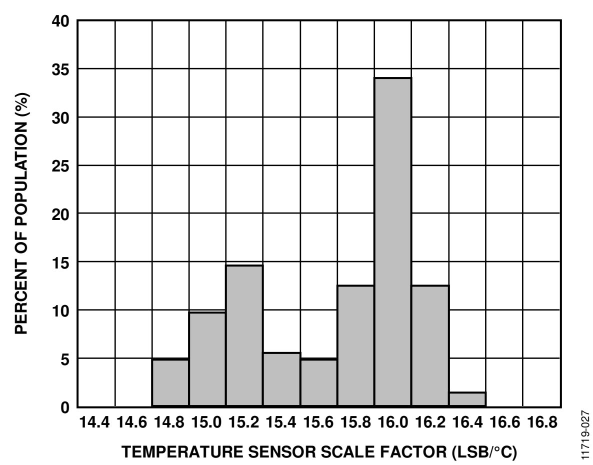

Figure 27. Temperature Sensor Scale Factor, V_S = 2 V

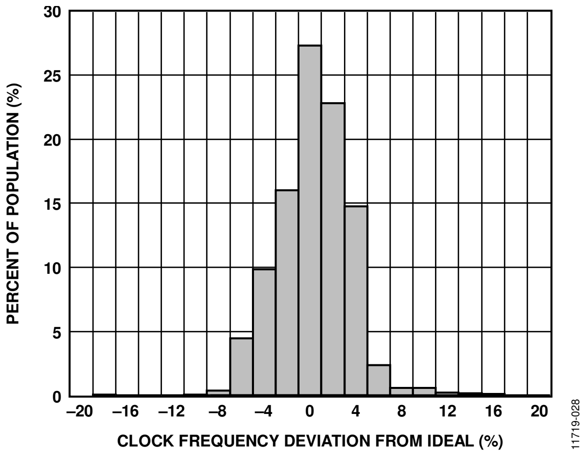

Figure 28. Clock Frequency Deviation from Ideal at 25°C, V_S = 2 V

THEORY OF OPERATION

The ADXL363 is a complete sensor suite consisting of an accelerometer, an ADC for synchronous conversion of input from a third sensor, and a temperature sensor. The entire system operates at extremely low power consumption levels.

ACCELEROMETER

The ADXL363 measures both dynamic acceleration, resulting from motion or shock, and static acceleration, such as tilt. Acceleration is reported digitally and the device communicates via the SPI protocol. Built-in digital logic enables autonomous operation and implements functionality that enhances system level power savings.

Mechanical Device Operation

The moving component of the sensor is a polysilicon surface-micromachined structure that is built on top of a silicon wafer. Polysilicon springs suspend the structure over the surface of the wafer and provide a resistance against acceleration forces.

Deflection of the structure is measured using differential capacitors that consist of independent fixed plates and plates attached to the moving mass. Acceleration deflects the structure and unbalances the differential capacitor, resulting in a sensor output whose amplitude is proportional to acceleration. Phase sensitive demodulation determines the magnitude and polarity of the acceleration.

Operating Modes

The ADXL363 has two operating modes: measurement mode for continuous, wide bandwidth sensing; and wake-up mode for limited bandwidth activity detection. In addition, measurement is suspended altogether by placing the device in standby.

Measurement Mode

Measurement mode is the normal operating mode of the ADXL363. In this mode, acceleration data is read continuously and the accelerometer consumes less than 3.5 µA across its entire range of output data rates of up to 400 Hz using a 2.0 V supply (see Figure 29). All features described in this data sheet are available when operating the ADXL363 in this mode.

The ability to continuously output data from the minimum 12.5 Hz to the maximum 400 Hz data rate while still delivering less than 3.5 µA of current consumption is what defines the ADXL363 as an ultralow power accelerometer. Other accelerometers derive low current by using a specific low power mode that power cycles acceleration sensing. The result is a small effective bandwidth in the low power modes and undersampling of input data; therefore, unwanted aliasing can occur. Undersampling and aliasing do not occur with the ADXL363 because it continuously samples the full bandwidth of its sensor at all data rates.

Wake-Up Mode

Wake-up mode is ideal for simple detection of the presence or absence of motion at extremely low power consumption (270 nA at a 2.0 V supply voltage). Wake-up mode is useful particularly for implementation of a motion activated on/off switch, allowing the rest of the system to power down until activity is detected.

Wake-up mode reduces current consumption to a very low level by measuring acceleration only about six times per second to determine whether motion is present. If motion is detected, the accelerometer can respond autonomously in the following ways:

- Switch into full bandwidth measurement mode
- Signal an interrupt to a microcontroller
- Wake up downstream circuitry, depending on the configuration

In wake-up mode, all accelerometer features are available with the exception of the activity timer. All registers can be accessed, and real-time data can be read and/or stored in the FIFO.

Standby

Placing the ADXL363 in standby suspends measurement and reduces the current consumption to 10 nA (typical). Pending interrupts and data are preserved, and no new interrupts are generated.

The ADXL363 powers up in standby with all sensor functions turned off.

Selectable Measurement Ranges

The ADXL363 has selectable measurement ranges of ±2 *g*, ±4 *g*, and ±8 *g*. Acceleration samples are always converted by a 12-bit ADC; therefore, the scale factor scales with *g* range. Ranges and corresponding scale factor values are listed in Table 2.

When acceleration exceeds the measurement extremes, data is clipped at the full-scale value (0x0FFF), and no damage is caused to the accelerometer. Table 5 lists the absolute maximum ratings for acceleration, indicating the acceleration level that can cause permanent damage to the device.

Selectable Output Data Rates

The ADXL363 can report acceleration data at various data rates ranging from 12.5 Hz to 400 Hz. The internal low-pass filter pole is automatically set to ¼ or ½ the selected ODR (based on the HALF_BW setting) to ensure that the Nyquist sampling criterion is met and no aliasing occurs.

Current consumption varies somewhat with output data rate as shown in Figure 29, remaining below approximately 5.0 µA over the entire range of data rates and operating voltages.

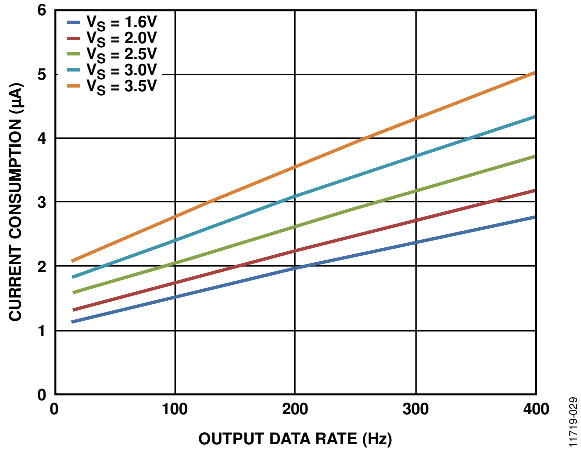

Figure 29. Current Consumption vs. Output Data Rate at Several Supply Voltages, ADC_EN = 0

Antialiasing

The analog-to-digital converter (ADC) of the ADXL363 samples at the user selected output data rate. In the absence of antialiasing filtering, it aliases any input signals whose frequency is more than half the data rate. To mitigate this, a two-pole low-pass filter is provided at the input of the ADC.

The user can set this antialiasing filter to a bandwidth that is at ½ the output data rate or ¼ the output data rate. Setting the antialiasing filter pole to ½ of the output data rate provides less aggressive antialiasing filtering, but maximizes bandwidth and is adequate for most applications. Setting the pole to ¼ of the data rate reduces bandwidth for a given data rate, but provides more aggressive antialiasing.

The antialiasing filter of the ADXL363 defaults to the more conservative setting, where bandwidth is set to ¼ the output data rate.

Power/Noise Tradeoff

The ADXL363 offers a few options for decreasing noise at the expense of only a small increase in current consumption.

The noise performance of the ADXL363 in normal operation, typically 7 LSB rms at 100 Hz bandwidth, is adequate for most applications, depending on bandwidth and the desired resolution. For cases where lower noise is needed, the ADXL363 provides two lower noise operating modes that trade reduced noise for a somewhat higher current consumption.

Table 9 lists the noise densities and current consumption obtained for normal operation and the two lower noise modes at a typical 2.0 V supply.

Table 9. Noise and Current Consumption: Normal Operation, Low Noise Mode, and Ultralow Noise Mode at V_S = 2.0 V, ODR = 100 Hz

Mode	Noise (µg/√Hz) Typical	Current Consumption (µA) Typical
Normal Operation	550	1.8
Low Noise	400	3.3
Ultralow Noise	250	13

Operating the ADXL363 at a higher supply voltage also decreases noise. Table 10 lists the noise densities and current consumption obtained for normal operation and the two lower noise modes at the highest recommended supply, 3.3 V.

Table 10. Noise and Current Consumption: Normal Operation, Low Noise Mode, and Ultralow Noise Mode at V_S = 3.3 V, ODR = 100 Hz

Mode	Noise (µg/√Hz) Typical	Current Consumption (µA) Typical
Normal Operation	380	2.7
Low Noise	280	4.5
Ultralow Noise	175	15

Free Fall Detection

Many digital output accelerometers include a built-in free fall detection feature. In the ADXL363, this function can be implemented using the inactivity interrupt. Refer to the Applications Information section for more details, including suggested threshold and timing values.

ADC

In addition to a built-in accelerometer and temperature sensor, the ADXL363 incorporates a 12-bit analog-to-digital converter (ADC) for digitization of an external analog input. The ADC is best suited for use with a sensor input due to its synchronization with the accelerometer and temperature sensor.

Use of the ADC adds approximately 150 nA to the total current consumption when operating at 100 Hz ODR. The ADXL363 enables the user to power down the ADC to save power when it is not needed.

Analog Inputs

The ADXL363 ADC can convert analog inputs ranging from 10% to 90% of the supply voltage. For example, when V_S = 2 V, the acceptable voltage range of the analog input is 0.2 V to 1.8 V.

Figure 30 shows an equivalent circuit of the input structure of the ADXL363.

The two diodes, D1 and D2, provide ESD protection for the analog input, ADC_IN. Take care to ensure that the analog input signal never exceeds the supply rails by more than 0.3 V because this causes these diodes to begin to forward bias and start conducting current.

During the acquisition phase, the impedance of the analog input (ADC_IN) can be modeled by the series connection of R_{IN} and C_{IN}. R_{IN} is typically 1 kΩ and is a lumped component made up of some serial resistors and the on resistance of the switches. C_{IN} is typically 23 pF and is mainly the ADC sampling capacitor.

The acquisition time required is calculated using the following formula:

$$t_{ACQ} = 8.5 \times ((R_{SOURCE} + R_{IN})\ C_{IN})$$

where R_{SOURCE} is the source impedance.

For 12-bit settling, t_{ACQ} must be less than 75 µs. The acquisition time, t_{ACQ}, sets an upper limit on the source impedance, R_{SOURCE}, of approximately 380 kΩ.

During the conversion phase, the switches are opened and the input impedance is limited to the pin capacitance, typically 1 pF to 2 pF. R_{IN} and C_{IN} make a one-pole, low-pass filter that reduces undesirable aliasing effects and limits the noise.

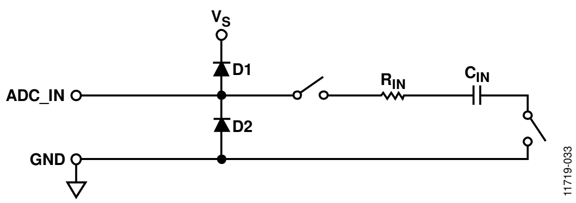

Figure 30. Equivalent Analog Input Circuit

Digital Output

The 12-bit digitized signal is in twos complement format and is stored in output registers, accessible via the SPI interface. ADC samples are always captured and updated concurrently with accelerometer and temperature samples. The maximum throughput of the ADC is 400 samples per second when using the internal timer, although a slightly faster throughput can be achieved when supplying the ADXL363 with an external trigger.

The ADC data is provided in output registers only and is not saved in the FIFO.

TEMPERATURE SENSOR

The ADXL363 includes an integrated 12-bit temperature sensor, which the system designer can use to monitor internal system temperature or to improve the temperature stability of the device via calibration. For example, acceleration outputs vary with temperature at a rate of ±0.5 m*g*/°C (typical), but the relationship of the outputs to temperature is repeatable and the designer can, therefore, use the temperature sensor output to calibrate the acceleration temperature drift.

To use the temperature sensor to monitor absolute temperature, measure and calibrate its initial bias (its output at some known temperature).

To use the temperature sensor for calibration of the acceleration signal, it is sufficient to correlate acceleration to temperature sensor output, rather than to absolute temperature. In this case it is not necessary to convert the temperature reading to an absolute temperature; therefore, calibration of initial bias is not required.

The designer can configure the device to save data from the temperature sensor in the FIFO. Temperature samples, whether read from the output registers or from the FIFO, always update concurrently with acceleration (and ADC) samples.

POWER SAVINGS FEATURES

Designed for the most power conscious applications, the ADXL363 includes several features (as described in this section) for enabling power savings at the system level, as well as at the device level.

ULTRALOW POWER CONSUMPTION IN ALL MODES, OPERATING ALL SENSORS

At the device level, the most obvious power saving feature of the ADXL363 is its ultralow current consumption in all configurations. The ADXL363 consumes between 1.1 µA (typical) and 5 µA (typical) across all data rates up to 400 Hz and all supply voltages up to 3.5 V (see Figure 29). An even lower power, 270 nA (typical) motion triggered wake-up mode is provided for simple motion detection applications that require a power consumption lower than 1 µA.

At these current levels, the ADXL363 consumes less power in full operation than the standby currents of many other system components, and is, therefore, optimal for applications that require continuous acceleration monitoring and very long battery life. Because the accelerometer is always on, it can act as a motion-activated switch. The accelerometer signals to the rest of the system when to turn on, thereby managing power at the system level.

As important as its low operating current, the 10 nA (typical) standby current of the ADXL363 contributes to a much longer battery life in applications that spend most of their time in a sleep state and wake up via an external trigger.

MOTION DETECTION

The ADXL363 features built-in logic that detects activity (presence of acceleration above a threshold) and inactivity (lack of acceleration above a threshold). Activity and inactivity events can be used as triggers to manage the accelerometer mode of operation, trigger an interrupt to a host processor, and/or autonomously drive a motion switch.

Detection of an activity or inactivity event is indicated in the status register and can be configured to generate an interrupt. In addition, the activity status of the device, that is, whether it is moving or stationary, is indicated by the awake bit, described in the Using the Awake Bit section.

Activity and inactivity detection can be used when the accelerometer is in either measurement mode or wake-up mode.

Activity Detection

An activity event is detected when acceleration remains above a specified threshold for a specified time period.

Referenced and Absolute Configurations

Activity detection can be configured as referenced or absolute.

When using absolute activity detection, acceleration samples are compared to a user set threshold to determine whether motion is present. For example, if a threshold of 0.5 *g* is set and the acceleration on the z-axis is 1 *g* for longer than the user defined activity time, the activity status asserts.

In many applications, it is advantageous for activity detection to be based not on an absolute threshold, but on a deviation from a reference point or orientation. This is particularly useful because it removes the effect on activity detection of the static 1 *g* imposed by gravity. When an accelerometer is stationary, its output can reach 1 *g*, even when it is not moving. In absolute activity, when the threshold is set to less than 1 *g*, activity is immediately detected in this case.

In the referenced configuration, activity is detected when acceleration samples are at least a user set amount above an internally defined reference for the user defined amount of time, as described in Equation 1.

$$|Acceleration - Reference| > Threshold \quad (1)$$

Consequently, activity is detected only when the acceleration has deviated sufficiently from the initial orientation. The reference for activity detection is calculated when activity detection is engaged in one of the following scenarios:

- When the activity function is turned on and measurement mode is engaged
- If link mode is enabled: when inactivity is detected and activity detection begins
- If link mode is not enabled: when activity is detected and activity detection repeats

The referenced configuration results in a very sensitive activity detection that detects even the most subtle motion events.

Fewer False Positives

Ideally, the intent of activity detection is to wake up a system only when motion is intentional, ignoring noise or small, unintentional movements. In addition to being sensitive to subtle motion events, the ADXL363 activity detection algorithm is robust in filtering out undesired triggers.

The ADXL363 activity detection functionality includes a timer to filter out unwanted motion and ensure that only sustained motion is recognized as activity. The duration of this timer, as well as the acceleration threshold, are user adjustable from one sample (that is, no timer) to up to 20 seconds of motion.

Note that the activity timer is operational in measurement mode only. In wake-up mode, one-sample activity detection is used.

Inactivity Detection

An inactivity event is detected when acceleration remains below a specified threshold for a specified time. Inactivity detection is also configurable as referenced or absolute.

When using absolute inactivity detection, acceleration samples are compared to a user set threshold for the user set time to determine the absence of motion. Inactivity is detected when a large enough number of consecutive samples are below the threshold. Use the absolute configuration of inactivity for implementing free fall detection.

When using referenced inactivity detection, inactivity is detected when acceleration samples are within a user specified amount of an internally defined reference (as described by Equation 2) for a user defined amount of time.

$$|Acceleration - Reference| < Threshold \quad (2)$$

The reference for inactivity detection is updated every time a sample is detected that violates the inactivity condition; that is,

$(Sample - Reference) \geq Threshold$.

Referenced inactivity, like referenced activity, is particularly useful for eliminating the effects of the static acceleration due to gravity. With absolute inactivity, if the inactivity threshold is set lower than 1 *g*, a device resting motionless may never detect inactivity. With referenced inactivity, the same device under the same configuration detects inactivity.

The inactivity timer can be set to anywhere from 2.5 ms (a single sample at 400 Hz ODR) to almost 90 minutes (65,535 samples at 12.5 Hz ODR) of inactivity. A requirement for inactivity detection is that, for whatever period of time the inactivity timer has been configured, the accelerometer detects inactivity only when it has been stationary for that amount of time.

For example, if the accelerometer is configured for 90 minutes, the accelerometer detects inactivity when it is stationary for 90 minutes. The wide range of timer settings means that in applications where power conservation is critical, the system can be put to sleep after very short periods of inactivity. In applications where continuous operation is critical, the system stays on for as long as any motion is present.

Linking Activity and Inactivity Detection

The activity and inactivity detection functions can be used independently and processed manually by a host processor, or they can be configured to interact in linked mode, loop mode, and autosleep.

Default Mode

The user must enable the activity and inactivity functions because these functions are not automatically enabled by default. After the user enables the activity and inactivity functions, the ADXL363 exhibits the following behavior when it enters default mode:

- Both activity and inactivity detection remain enabled
- All interrupts must be serviced by a host processor; that is, a processor must read each interrupt before it is cleared and can be used again.

Default mode operation is illustrated in the flowchart in Figure 31.

Linked Mode

In linked mode, activity and inactivity detection are linked to each other such that only one of the functions is enabled at any given time. As soon as activity is detected, the device is assumed moving (or awake) and stops looking for activity; rather, inactivity is expected as the next event. Therefore, only inactivity detection operates.

Similarly, when inactivity is detected, the device is assumed stationary (or asleep). Thus, activity is expected as the next event; therefore, only activity detection operates.

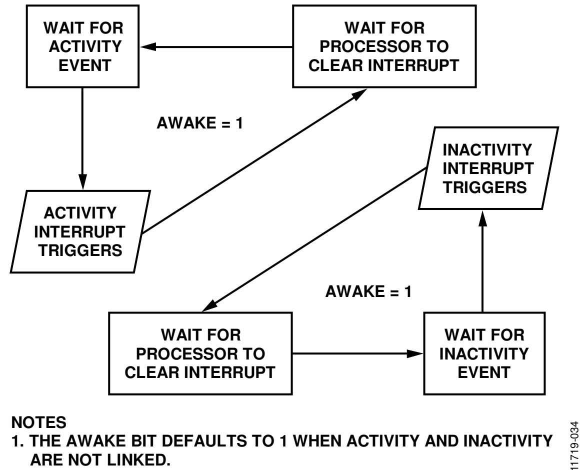

Figure 31. Flowchart Illustrating Activity and Inactivity Operation in Default Mode

In linked mode, each interrupt must be serviced by a host processor before the next interrupt is enabled.

Linked mode operation is illustrated in the flowchart in Figure 32.

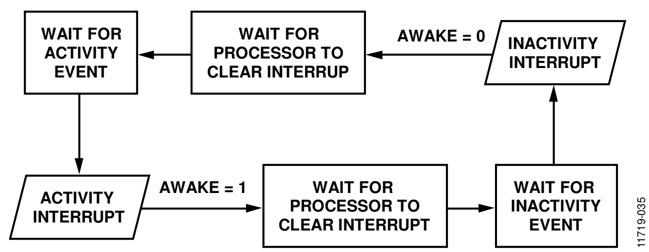

Figure 32. Flowchart Illustrating Activity and Inactivity Operation in Linked Mode

Loop Mode

In loop mode, motion detection operates as described in the Linked Mode section, but interrupts do not need servicing by a host processor. This configuration simplifies the implementation of commonly used motion detection and enhances power savings by reducing the amount of power used in bus communication.

Loop mode operation is illustrated in the flowchart in Figure 33.

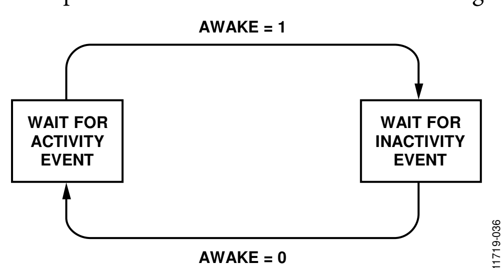

Figure 33. Flowchart Illustrating Activity and Inactivity Operation in Loop Mode

Autosleep

When in linked or loop mode, enabling autosleep causes the device to enter wake-up mode autonomously (see the Wake-Up Mode section) when inactivity is detected, and to reenter measurement mode when activity is detected.

The autosleep configuration is active only if linked or loop modes are enabled. In the default mode, the autosleep setting is ignored.

Using the Awake Bit

The awake bit is a status bit that indicates whether the ADXL363 is awake or asleep. The device is awake upon experiencing an activity condition, and it is asleep when upon experiencing an inactivity condition.

Used in conjunction with loop mode, the awake bit makes an autonomous motion activated switch easy to implement: simply map the bit to the INT1 or INT2 pin, and tie this pin to the gate of a switch (see Figure 43). When the ADXL363 detects activity, the awake bit becomes high, causing the switch to close and current to flow to downstream circuitry. When the ADXL363 detects inactivity, the awake bit deasserts and the switch opens, disconnecting downstream circuitry from power entirely.

If the system can tolerate the turn-on time of downstream circuitry, this motion switch configuration saves significant system level power by eliminating the standby current consumption of the remainder of the application. This standby current often exceeds the full operating current of the ADXL363.

FIFO

The ADXL363 includes a deep 512-sample first in, first out (FIFO) buffer that stores acceleration and, if desired, temperature data. The FIFO provides two primary benefits: system level power savings and data recording/event context.

System Level Power Savings

Appropriate use of the FIFO enables system level power savings by enabling the host processor to sleep for extended periods of time while the accelerometer autonomously collects data. Alternatively, using the FIFO to collect data unburdens the host while it tends to other tasks.

Data Recording/Event Context

The FIFO can be used in trigger mode to record all data leading up to an activity detection event, thereby providing context for the event. In the case of a system that identifies impact events, for example, the accelerometer can keep the entire system off while it stores acceleration data in its FIFO and looks for an activity event. When the impact event occurs, data collected prior to the event is frozen in the FIFO. The accelerometer then wakes the rest of the system and transfers this data to the host processor, thereby providing context for the impact event.

Generally, more context enables more intelligent decisions, making a deep FIFO especially useful. The ADXL363 FIFO stores up to more than 13 seconds of data, providing a clear picture of events prior to an activity trigger.

All FIFO modes of operation, as well as the structure of the FIFO and instructions for retrieving data from it, are described in further detail in the FIFO Modes section.

COMMUNICATIONS

SPI Instructions

The digital interface of the ADXL363 is implemented with system level power savings in mind. The following features enhance power savings:

- Burst reads and writes reduce the number of SPI communication cycles required to configure the device and retrieve data.
- Concurrent operation of activity and inactivity detection enables set it and forget it operation. Loop mode further reduces communications power by enabling the clearing of interrupts without processor intervention.
- The FIFO is implemented such that consecutive samples can be read continuously via a multibyte read of unlimited length; thus, one FIFO read instruction can clear the entire contents of the FIFO. In many other accelerometers, each read instruction retrieves a single sample only. In addition, the ADXL363 FIFO construction allows the use of direct memory access (DMA) to read the FIFO contents.

Bus Keepers

The ADXL363 includes bus keepers on all digital interface pins: MISO, MOSI, SCLK, $\overline{CS}$, INT1, and INT2. Bus keepers prevent tristate bus lines from floating when nothing is driving them, thus preventing through current in any gate inputs that are on the bus.

MSB Registers

Acceleration and temperature measurements are converted to 12-bit values and transmitted via the SPI using two registers per measurement. To read a full sample set of 3-axis acceleration data, six registers must be read.

Many applications do not require the accuracy that 12-bit data provides and prefer, instead, to save system level power. The MSB registers (XDATA, YDATA, and ZDATA) enable this trade-off. These registers contain the eight MSBs of the x-, y-, and z-axis acceleration data; reading them effectively provides 8-bit acceleration values. Only three (consecutive) registers must be read to retrieve a full data set, significantly reducing the time during which the SPI bus is active and drawing current.

12-bit and 8-bit data are available simultaneously so that both data formats can be used in a single application, depending on the needs of the application at a given time. For example, the processor reads 12-bit data when higher resolution is required and switches to 8-bit data (simply by reading a different set of registers) when application requirements change.

ADDITIONAL FEATURES

EXTERNAL CLOCK

The ADXL363 has a built-in 51.2 kHz (typical) clock that, by default, serves as the time base for internal operations.

ODR and bandwidth scale proportionally with the clock. The ADXL363 provides a discrete number of options for ODR, such as 100 Hz, 50 Hz, 25 Hz, and so forth, in factors of 2 (see the Filter Control Register section for a complete listing). To achieve data rates other than those provided, an external clock can be used at the appropriate clock frequency. The output data rate scales with the clock frequency, as shown in Equation 3.

$$ODR_{ACTUAL} = ODR_{SELECTED} \times \frac{f}{51.2\ \text{kHz}} \quad (3)$$

For example, to achieve an 80 Hz ODR, select the 100 Hz ODR setting and provide a clock frequency that is 80% of nominal, or 41.0 kHz.

The ADXL363 can operate with external clock frequencies ranging from the nominal 51.2 kHz down to 25.6 kHz to allow the user to achieve any desired output data rate.

Alternatively, use an external clock where improved clock frequency accuracy is required. The distribution of clock frequencies among a sampling of >1000 parts has a standard deviation of approximately 3%. To achieve tighter tolerances, a more accurate clock can be provided externally.

Accelerometer bandwidth automatically scales to ½ or ¼ of the ODR (based on the HALF_BW setting), and this ratio is preserved, regardless of clock frequency. Power consumption also scales with clock frequency; higher clock rates increase power consumption. Figure 34 shows how power consumption varies with clock rate.

The ODR setting applies to the ADC and temperature sensor data rates but does not affect their bandwidth. Especially in the case of the ADC, the system designer must ensure that the bandwidth of the signal input into the ADC is appropriate for the selected ODR.

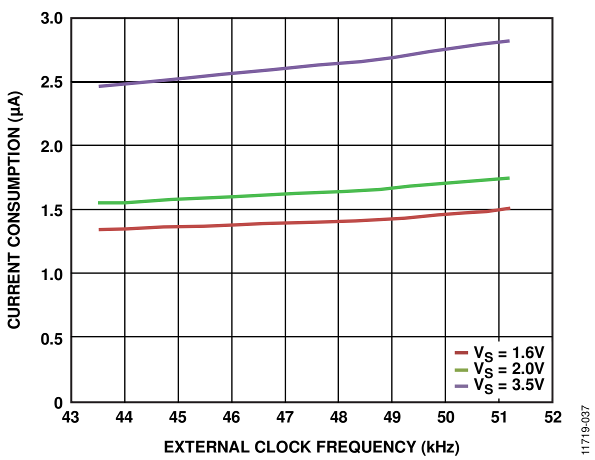

Figure 34. Current Consumption vs. External Clock Frequency

SYNCHRONIZED DATA SAMPLING

For applications that require a precisely timed acceleration measurement, the ADXL363 features an option to synchronize acceleration sampling to an external trigger.

SELF TEST

The ADXL363 incorporates a self test feature that effectively tests its mechanical and electronic systems simultaneously. When the self test function is invoked, an electrostatic force is applied to the mechanical sensor. This electrostatic force moves the mechanical sensing element in the same manner as acceleration, and it is additive to the acceleration experienced by the device. This added electrostatic force results in an output change on all three axes.

USER REGISTER PROTECTION

The ADXL363 includes user register protection for single event upsets (SEUs). An SEU is a change of state caused by ions or electromagnetic radiation striking a sensitive node in a micro-electronic device. The state change is a result of the free charge created by ionization in or near an important node of a logic element (for example, a memory bit). The SEU, itself, is not considered permanently damaging to transistor or circuit functionality, but it can create erroneous register values. The ADXL363 registers that are protected from SEUs are Register 0x20 to Register 0x2E.

SEU protection is implemented via a 99-bit error correcting (Hamming-type) code that detects both single-bit and double-bit errors. The check bits are recomputed any time a write to any of the protected registers occurs. At any time, if the stored version of the check bits is not in agreement with the current check bit calculation, the ERR_USER_REGS status bit is set.

The ERR_USER_REGS bit in the status register is set upon power-up prior to device configuration; it clears upon the first register write to that device.

SERIAL COMMUNICATIONS

The ADXL363 communicates via a 4-wire SPI and operates as a slave. Ignore data that is transmitted from the ADXL363 to the master device during writes to the ADXL363.

As shown in Figure 36 to Figure 40, the MISO pin is in a high impedance state, held by a bus keeper, except when the ADXL363 is sending read data (to conserve bus power).

Wire the ADXL363 for SPI communication as shown in the connection diagram in Figure 35. The recommended SPI clock speeds are 1 MHz to 5 MHz, with 12 pF maximum loading.

The SPI timing scheme follows CPHA = CPOL = 0.

Figure 36 to Figure 40 show the data sequences for SPI transactions. For correct operation of the part, the logic thresholds and timing parameters in Table 11 and Table 12 must be met at all times. Figure 36 to Figure 40 are divided into send (shaded) and receive portions. Refer to Figure 41 and Figure 42 for visual diagrams of the timing parameters for the receive and send portions, respectively.

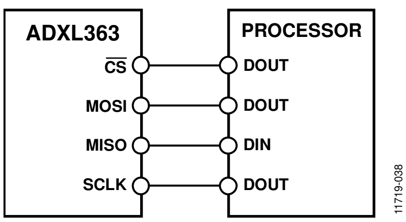

Figure 35. 4-Wire SPI Connection Diagram

SPI COMMANDS

The SPI port uses a multibyte structure wherein the first byte is a command. The ADXL363 command set is

- 0x0A: write register
- 0x0B: read register
- 0x0D: read FIFO

Read and Write Register Commands

The command structure for the read register and write register commands is as follows (see Figure 36 and Figure 37):

```
<CS down>
<command byte (0x0A or 0x0B)>
<address byte>
<data byte>
<additional data bytes for multi-byte>
…
<CS up>
```

The read and write register commands support multibyte (burst) read/write access. The waveform diagrams for multibyte read and write commands are shown in Figure 38 and Figure 39.

Read FIFO Command

Reading from the FIFO buffer is a command structure that does not have an address.

```
<CS down>
<command byte (0x0D)>
<data byte> <data byte>
…
<CS up>
```

It is recommended that an even number of bytes be read (using a multibyte transaction) because each sample consists of two bytes: two bits of axis information and 14 bits of data. If an odd number of bytes is read, it is assumed that the desired data was read; therefore, the second half of the last sample is discarded so that a read from the FIFO always starts on a properly aligned even-byte boundary. Data is presented least significant byte first, followed by the most significant byte.

MULTIBYTE TRANSFERS

Multibyte transfers, also known as burst transfers, are supported for all SPI commands: register read, register write, and FIFO read commands. It is recommended that data be read using multibyte transfers to ensure that a concurrent and complete set of x-, y-, and z-acceleration (and temperature, where applicable) data is read.

The FIFO runs on the serial port clock during FIFO reads and sustains bursting at the SPI clock rate as long as the SPI clock is 1 MHz or faster.

Register Read/Write Auto-Increment

A register read or write command begins with the address specified in the command and auto-increments for each additional byte in the transfer. To avoid address wrapping and side effects of reading registers multiple times, the auto-increment halts at the invalid Register Address 63 (0x3F).

INVALID ADDRESSES AND ADDRESS FOLDING

The ADXL363 has a 6-bit address bus, mapping only 64 registers in the possible 256 register address space. The addresses do not fold to repeat the registers at addresses above 64. Attempted access to register addresses above 64 map to the invalid register at 63 (0x3F) and have no functional effect.

Address 0x00 to Address 0x2E are for customer access, as described in the Register Map section. Address 0x2F to Address 0x3F are reserved for factory use.

LATENCY RESTRICTIONS

Reading any of the data registers (Register 0x08 to Register 0x0A or Register 0x0E to Register 0x15) clears the data ready interrupt. There can be as much as an 80 µs delay from reading a register to the clearing of the data ready interrupt.

Other register reads, register writes, and FIFO reads have no latency restrictions.

INVALID COMMANDS

Commands other than 0x0A, 0x0B, and 0x0D have no effect. The MISO output remains in a high impedance state, and the bus keeper holds the MISO line at its last value.

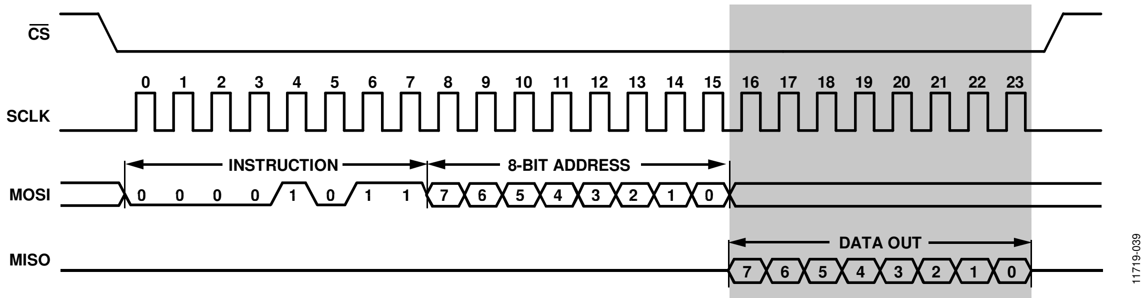

Figure 36. Register Read

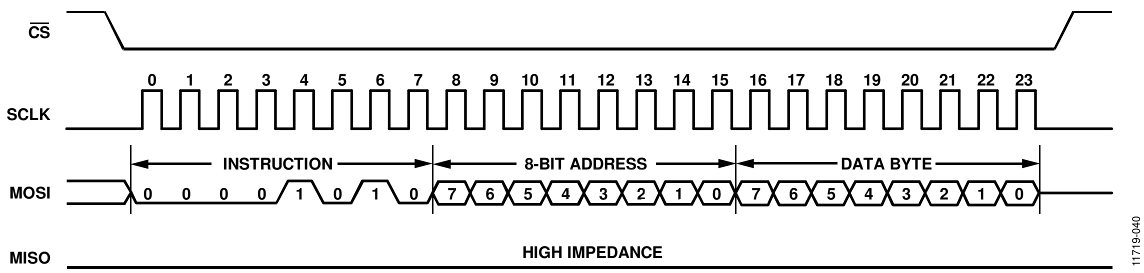

Figure 37. Register Write (Receive Instruction Only)

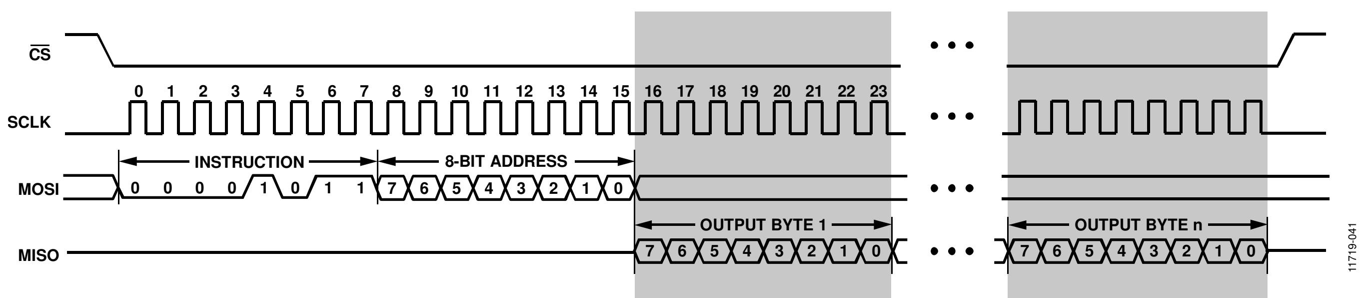

Figure 38. Burst Read

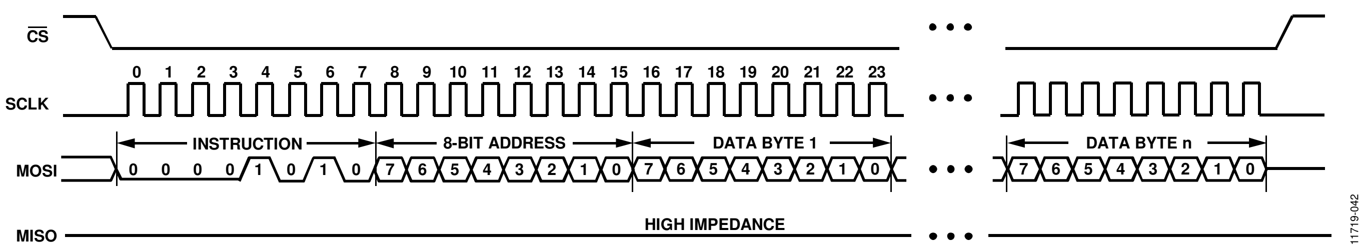

Figure 39. Burst Write (Receive Instruction Only)

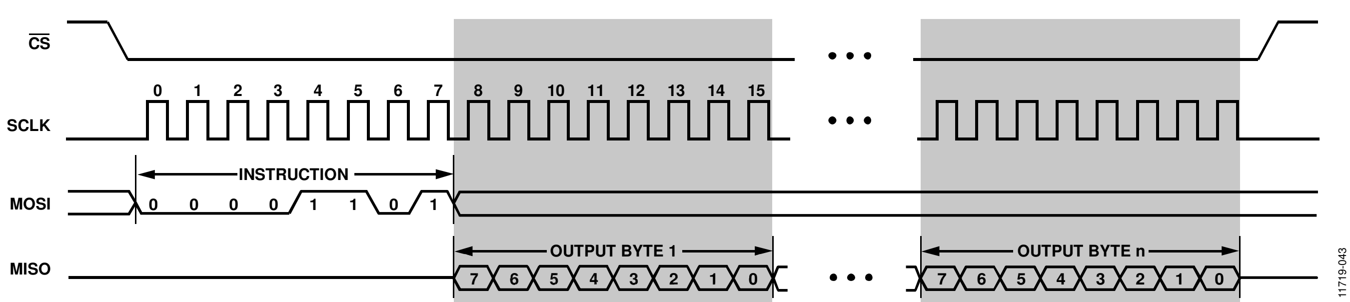

Figure 40. FIFO Read

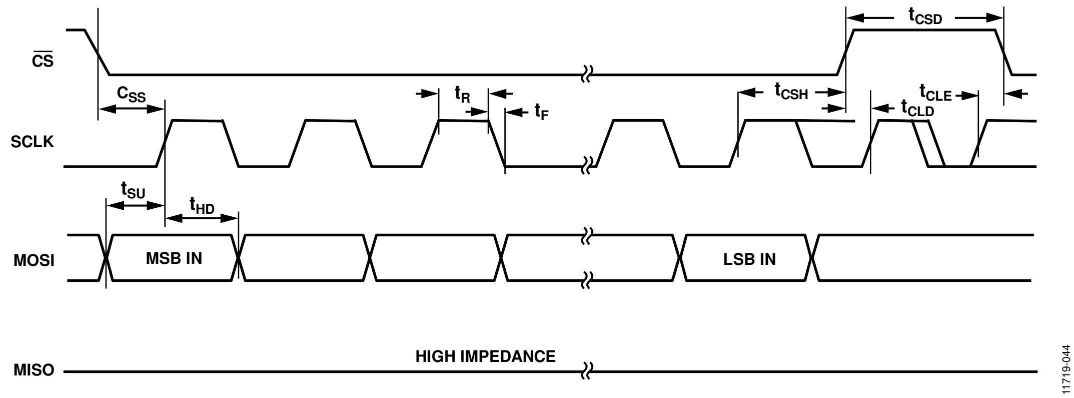

Figure 41. Timing Diagram for SPI Receive Instructions

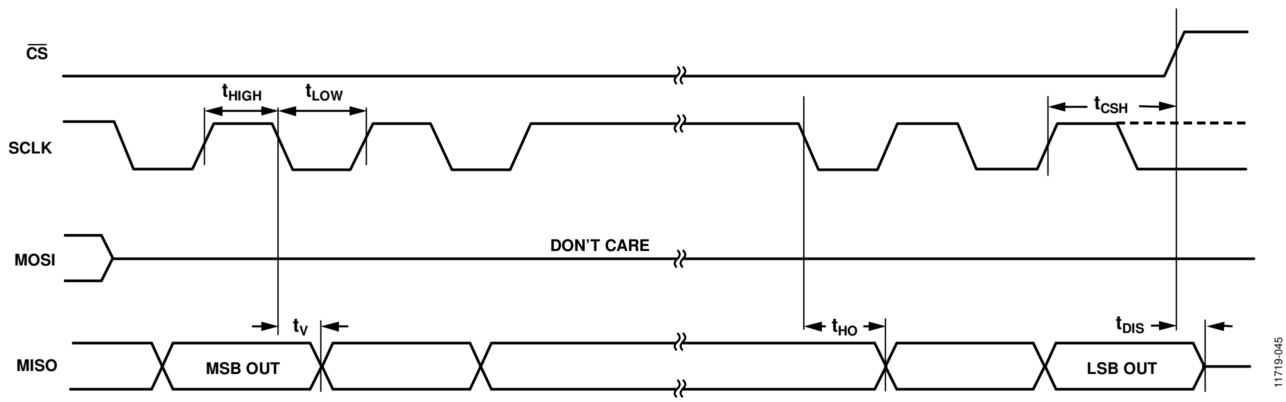

Figure 42. Timing Diagram for SPI Send Instructions (Shaded Portions of Figure 36, Figure 38, and Figure 40)

Table 11. SPI Digital Input/Output

Parameter	Test Conditions/Comments	Limit[1]		Unit
		Min	Max	
Digital Input				
Low Level Input Voltage (V_{IL})			$0.3 \times V_{DD\ I/O}$	V
High Level Input Voltage (V_{IH})		$0.7 \times V_{DD\ I/O}$		V
Low Level Input Current (I_{IL})	$V_{IN} = V_{DD\ I/O}$		0.1	µA
High Level Input Current (I_{IH})	$V_{IN} = 0$ V	−0.1		µA
Digital Output				
Low Level Output Voltage (V_{OL})	$I_{OL} = 10$ mA		$0.2 \times V_{DD\ I/O}$	V
High Level Output Voltage (V_{OH})	$I_{OH} = -4$ mA	$0.8 \times V_{DD\ I/O}$		V
Low Level Output Current (I_{OL})	$V_{OL} = V_{OL,\ max}$	10		mA
High Level Output Current (I_{OH})	$V_{OH} = V_{OH,\ min}$		−4	mA

[1] Limits based on characterization results; not production tested.

Table 12. SPI Timing (T_A = 25°C, V_S = 2.0 V, $V_{DD\ I/O}$ = 2.0 V)

	Limit[1, 2]			
Parameter	Min	Max	Unit	Description
f_{CLK}		1	MHz	SCLK Frequency
C_{SS}	100		ns	$\overline{CS}$ Setup Time
t_{CSH}	100		ns	$\overline{CS}$ Hold Time
t_{CSD}	10		ns	$\overline{CS}$ Disable Time
t_{SU}	50		ns	Data Setup Time
t_{HD}	50		ns	Data Hold Time
t_R	0	100	ns	SCLK Rise Time
t_F	0	100	ns	SCLK Fall Time
t_{HIGH}	100		ns	SCLK High Time
t_{LOW}	100		ns	SCLK Low Time
t_{CLD}	100		ns	SCLK Delay Time
t_{CLE}	100		ns	SCLK Enable Time
t_V	0		ns	Output Valid from SCLK Low
t_{HO}	0	200	ns	Output Hold Time
t_{DIS}	0	200	ns	Output Disable Time

[1] Limits based on design targets; not production tested.
[2] The timing values are measured corresponding to the input thresholds (V_{IL} and V_{IH}) given in Table 11.