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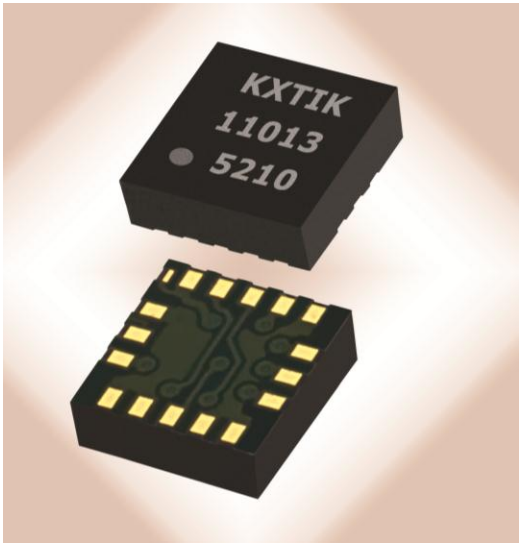
Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTIK-1004** **Rev. 3** **Dec-2012**

Product Description



The KXTIK is a tri-axis +/-2g, +/-4g or +/-8g silicon micromachined accelerometer with integrated orientation, tap/double tap, and activity detecting algorithms. The sense element is fabricated using Kionix's proprietary plasma micromachining process technology. Acceleration sensing is based on the principle of a differential capacitance arising from acceleration-induced motion of the sense element, which further utilizes common mode cancellation to decrease errors from process variation, temperature, and environmental stress. The sense element is hermetically sealed at the wafer level by bonding a second silicon lid wafer to the device using a glass frit. A separate ASIC device packaged with the sense element provides signal conditioning, and intelligent user-programmable application algorithms. The accelerometer is delivered in a 3 x 3 x 0.9 mm LGA plastic package operating from a 1.8 – 3.6V DC supply. Voltage regulators are used to maintain constant internal operating voltages over the range of input supply voltages. This results in stable operating characteristics over the range of input supply voltages and virtually undetectable ratiometric error. I^2C digital protocol is used to communicate with the chip to configure and check for updates to the orientation, Directional Tap™ detection and activity monitoring algorithms.

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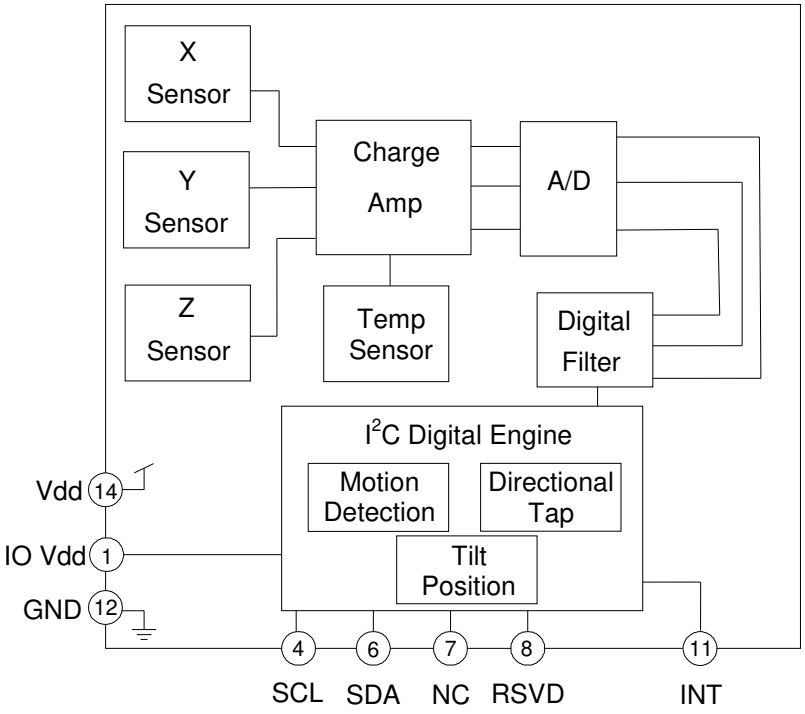
Functional Diagram



Kionix®	**± 2g / 4g / 8g Tri-axis Digital Accelerometer Specifications**	**PART NUMBER:** **KXTIK-1004** **Rev. 3** **Dec-2012**

Product Specifications

Table 1. Mechanical

(specifications are for operation at 2.6V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Operating Temperature Range		ºC	-40	-	85
Zero-g Offset		mg		±25	±125
Zero-g Offset Variation from RT over Temp.		mg/ºC		0.7 (xy) 0.4 (z)	
Sensitivity (12-bit)[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	988	1024	1060
	GSEL1=0, GSEL0=1 (± 4g)		494	512	530
	GSEL1=1, GSEL0=0 (± 8g)		247	256	265
Sensitivity (8-bit)[1]	GSEL1=0, GSEL0=0 (± 2g)	counts/g	61	64	67
	GSEL1=0, GSEL0=1 (± 4g)		30	32	34
	GSEL1=1, GSEL0=0 (± 8g)		15	16	17
Sensitivity Variation from RT over Temp.		%/ºC		0.01 (xy) 0.03 (z)	
Self Test Output change on Activation		g		0.7 (xy) 0.5 (z)	
Mechanical Resonance (-3dB)[2]		Hz		3500 (xy) 1800 (z)	
Non-Linearity		% of FS		0.6	
Cross Axis Sensitivity		%		2	

Notes:

1. Resolution and acceleration ranges are user selectable via I^2C.
2. Resonance as defined by the dampened mechanical sensor.

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Table 2. Electrical

(specifications are for operation at 2.6V and T = 25C unless stated otherwise)

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Operating	V	1.71	2.6	3.6
I/O Pads Supply Voltage (V_{IO})		V	1.7		V_{dd}
Current Consumption	All On (RES = 1)	µA		325	
	Directional Tap™ (RES = 0, ODR = 400Hz)			165	
	Low Power (RES = 0, ODR ≤ 25Hz)			100	
	Standby			10	
Output Low Voltage (V_{io} < 2V)[1]		V	-	-	0.2 * V_{io}
Output Low Voltage (V_{io} > 2V)[1]		V	-	-	0.4
Output High Voltage		V	0.8 * V_{io}	-	-
Input Low Voltage		V	-	-	0.2 * V_{io}
Input High Voltage		V	0.8 * V_{io}	-	-
Input Pull-down Current		µA		0	
Start Up Time[2]	RES = 0	ms		0.050	
	RES = 1, ODR = 12.5Hz			81	
	RES = 1, ODR = 25 Hz			41	
	RES = 1, ODR = 50Hz			21	
	RES = 1, ODR = 100Hz			11	
	RES = 1, ODR = 200Hz			6	
	RES = 1, ODR = 400Hz			4	
	RES = 1, ODR = 800Hz			2.5	
Power Up Time[3]		ms		10	
I^2C Communication Rate		kHz			400
Output Data Rate (ODR)[4]		Hz	12.5	50	800
Bandwidth (-3dB)[5]	RES = 0	kHz		1.59	
	RES = 1	Hz		ODR/2	

Notes:

1. For I^2C communication, this assumes a minimum 1.5kΩ pull-up resistor on SCL and SDA pins.
2. Start up time is from PC1 set to valid outputs.
3. Power up time is from Vdd valid to device boot completion.
4. User selectable through I^2C.
5. User selectable and dependant on ODR and RES.

Table 3. Environmental

Parameters		Units	Min	Typical	Max
Supply Voltage (V_{dd})	Absolute Limits	V	-0.5	-	3.63
Operating Temperature Range		ºC	-40	-	85
Storage Temperature Range		ºC	-55	-	150
Mech. Shock (powered and unpowered)		g	-	-	5000 for 0.5ms 10000 for 0.2ms
ESD	HBM	V	-	-	2000

Caution: ESD Sensitive and Mechanical Shock Sensitive Component, improper handling can cause permanent damage to the device.

This product conforms to Directive 2002/95/EC of the European Parliament and of the Council of the European Union (RoHS). Specifically, this product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB), or polybrominated diphenyl ethers (PBDE) above the maximum concentration values (MCV) by weight in any of its homogenous materials. Homogenous materials are "of uniform composition throughout."

HF

This product is halogen-free per IEC 61249-2-21. Specifically, the materials used in this product contain a maximum total halogen content of 1500 ppm with less than 900-ppm bromine and less than 900-ppm chlorine.

Soldering

Soldering recommendations are available upon request or from www.kionix.com.

Application Schematic

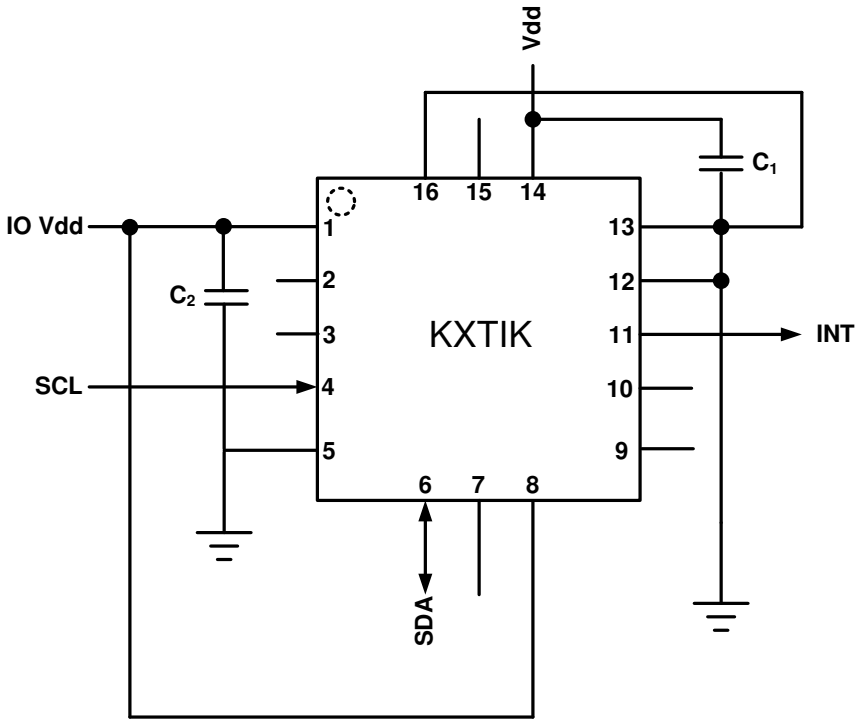


Table 4. KXTIK Pin Descriptions

Pin	Name	Description
1	IO Vdd	The power supply input for the digital communication bus. Optionally decouple this pin to ground with a 0.1uF ceramic capacitor.
2	RSVD	Reserved – Not Connected Internally
3	DNC	Reserved – Do Not Connect
4	SCL	I^2C Serial Clock
5	GND	Ground
6	SDA	I^2C Serial Data
7	NC	Not Internally Connected – Can be connected to Vdd, GND or Float
8	RSVD	Reserved – connect to IO Vdd
9	RSVD	Reserved – Internally connected to GND – Can be connected to GND or Float
10	RSVD	Reserved – Internally connected to GND – Can be connected to GND or Float
11	INT	Physical Interrupt
12	GND	Ground
13	RSVD	Reserved – Internally connected to GND – Can be connected to GND or Float
14	Vdd	The power supply input. Decouple this pin to ground with a 0.1uF ceramic capacitor.
15	NC	Not Internally Connected – Can be connected to Vdd, GND or Float
16	RSVD	Reserved – Internally connected to GND – Can be connected to GND or Float

Test Specifications

***Special Characteristics**:*

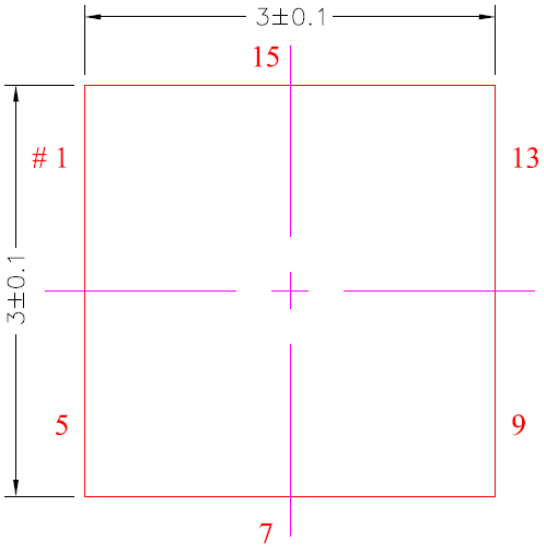
These characteristics have been identified as being critical to the customer. Every part is tested to verify its conformance to specification prior to shipment.

Table 5. Test Specifications

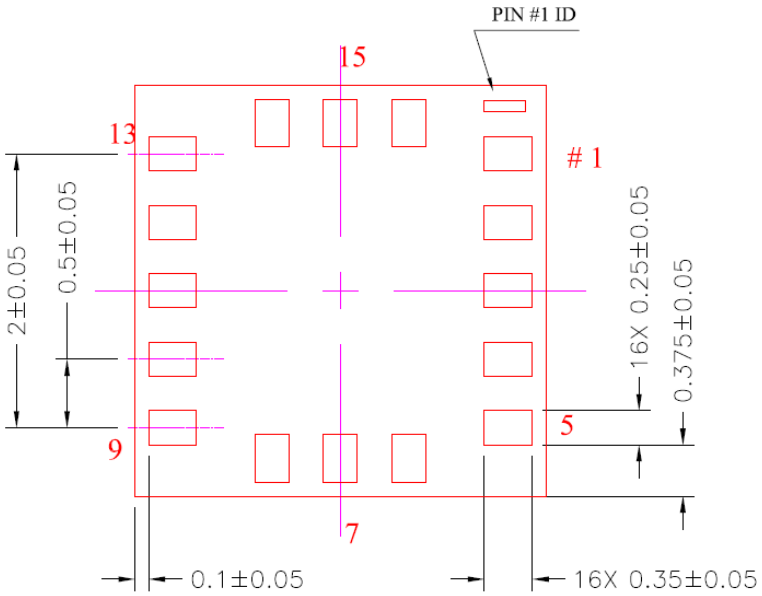
Parameter	Specification	Test Conditions
Zero-g Offset @ RT	0 +/- 128 counts	25C, Vdd = 2.6 V
Sensitivity @ RT	1024 +/- 35.8 counts/g	25C, Vdd = 2.6 V

Package Dimensions and Orientation

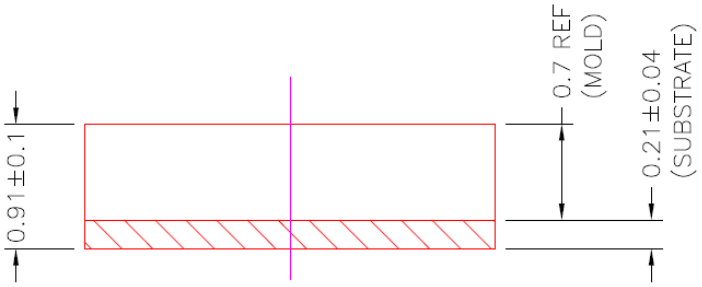
3 x 3 x 0.9 mm LGA



TOP VIEW



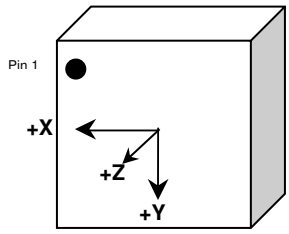
BOTTOM VIEW



SIDE VIEW

All dimensions and tolerances conform to ASME Y14.5M-1994

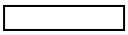
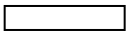
Orientation

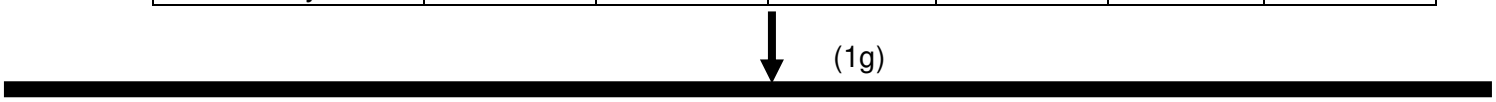


When device is accelerated in +X, +Y or +Z direction, the corresponding output will increase.

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=0 (± 2g)

Position	**1**		**2**		**3**		**4**		**5**		**6**	
Diagram									Top  Bottom		Bottom  Top	
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	-1024	-64	0	0	1024	64	0	0	0	0
Y (counts)	-1024	-64	0	0	1024	64	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	1024	64	-1024	-64
X-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Y-Polarity	**-**		**0**		**+**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



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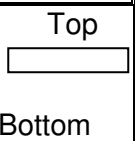
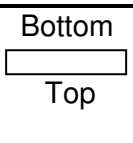
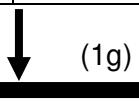
Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=0, GSEL0=1 (± 4g)

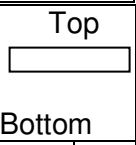
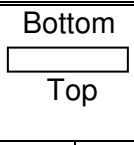
Position	1		2		3		4		5		6	
Diagram												
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	-512	-32	0	0	512	32	0	0	0	0
Y (counts)	-512	-32	0	0	512	32	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	512	32	-512	-32
X-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Y-Polarity	**-**		**0**		**+**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	

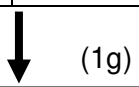


Earth's Surface

Static X/Y/Z Output Response versus Orientation to Earth's surface (1g):

GSEL1=1, GSEL0=0 (± 8g)

Position	1		2		3		4		5		6	
Diagram												
Resolution (bits)	12	8	12	8	12	8	12	8	12	8	12	8
X (counts)	0	0	-256	-16	0	0	256	16	0	0	0	0
Y (counts)	-256	-16	0	0	256	16	0	0	0	0	0	0
Z (counts)	0	0	0	0	0	0	0	0	256	16	-256	-16
X-Polarity	**0**		**-**		**0**		**+**		**0**		**0**	
Y-Polarity	**-**		**0**		**+**		**0**		**0**		**0**	
Z-Polarity	**0**		**0**		**0**		**0**		**+**		**-**	



Earth's Surface

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KXTIK Digital Interface

The Kionix KXTIK digital accelerometer has the ability to communicate on the I²C digital serial interface bus. This flexibility allows for easy system integration by eliminating analog-to-digital converter requirements and by providing direct communication with system micro-controllers. In doing so, all of the digital communication pins have shared responsibilities.

The serial interface terms and descriptions as indicated in Table 6 below will be observed throughout this document.

Term	Description
Transmitter	The device that transmits data to the bus.
Receiver	The device that receives data from the bus.
Master	The device that initiates a transfer, generates clock signals, and terminates a transfer.
Slave	The device addressed by the Master.

Table 6. Serial Interface Terminologies

I²C Serial Interface

As previously mentioned, the KXTIK has the ability to communicate on an I²C bus. I²C is primarily used for synchronous serial communication between a Master device and one or more Slave devices. The Master, typically a micro controller, provides the serial clock signal and addresses Slave devices on the bus. The KXTIK always operates as a Slave device during standard Master-Slave I²C operation.

I²C is a two-wire serial interface that contains a Serial Clock (SCL) line and a Serial Data (SDA) line. SCL is a serial clock that is provided by the Master, but can be held low by any Slave device, putting the Master into a wait condition. SDA is a bi-directional line used to transmit and receive data to and from the interface. Data is transmitted MSB (Most Significant Bit) first in 8-bit per byte format, and the number of bytes transmitted per transfer is unlimited. The I²C bus is considered free when both lines are high.

I²C Operation

Transactions on the I²C bus begin after the Master transmits a start condition (S), which is defined as a high-to-low transition on the data line while the SCL line is held high. The bus is considered busy after this condition. The next byte of data transmitted after the start condition contains the Slave Address (SAD) in the seven MSBs (Most Significant Bits), and the LSB (Least Significant Bit) tells whether the Master will be receiving data '1' from the Slave or transmitting data '0' to the Slave. When a Slave Address is sent, each device on the bus compares the seven MSBs with its internally stored address. If they match, the device considers itself addressed by the Master. The Slave Address associated with the KXTIK is 0001111.

It is mandatory that receiving devices acknowledge (ACK) each transaction. Therefore, the transmitter must release the SDA line during this ACK pulse. The receiver then pulls the data line low so that it remains stable low during the high period of the ACK clock pulse. A receiver that has been addressed, whether it is Master or Slave, is obliged to generate an ACK after each byte of data has been received. To conclude a transaction, the Master must transmit a stop condition (P) by transitioning the SDA line from low to high while SCL is high. The I^2C bus is now free.

Writing to a KXTIK 8-bit Register

Upon power up, the Master must write to the KXTIK's control registers to set its operational mode. Therefore, when writing to a control register on the I^2C bus, as shown Sequence 1 on the following page, the following protocol must be observed: After a start condition, SAD+W transmission, and the KXTIK ACK has been returned, an 8-bit Register Address (RA) command is transmitted by the Master. This command is telling the KXTIK to which 8-bit register the Master will be writing the data. Since this is I^2C mode, the MSB of the RA command should always be zero (0). The KXTIK acknowledges the RA and the Master transmits the data to be stored in the 8-bit register. The KXTIK acknowledges that it has received the data and the Master transmits a stop condition (P) to end the data transfer. The data sent to the KXTIK is now stored in the appropriate register. The KXTIK automatically increments the received RA commands and, therefore, multiple bytes of data can be written to sequential registers after each Slave ACK as shown in Sequence 2 on the following page.

Reading from a KXTIK 8-bit Register

When reading data from a KXTIK 8-bit register on the I^2C bus, as shown in Sequence 3 on the next page, the following protocol must be observed: The Master first transmits a start condition (S) and the appropriate Slave Address (SAD) with the LSB set at '0' to write. The KXTIK acknowledges and the Master transmits the 8-bit RA of the register it wants to read. The KXTIK again acknowledges, and the Master transmits a repeated start condition (Sr). After the repeated start condition, the Master addresses the KXTIK with a '1' in the LSB (SAD+R) to read from the previously selected register. The Slave then acknowledges and transmits the data from the requested register. The Master does not acknowledge (NACK) it received the transmitted data, but transmits a stop condition to end the data transfer. Note that the KXTIK automatically increments through its sequential registers, allowing data to be read from multiple registers following a single SAD+R command as shown below in Sequence 4 on the following page.

If a receiver cannot transmit or receive another complete byte of data until it has performed some other function, it can hold SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases SCL.

Data Transfer Sequences

The following information clearly illustrates the variety of data transfers that can occur on the I^2C bus and how the Master and Slave interact during these transfers. Table 7 defines the I^2C terms used during the data transfers.

Term	Definition
S	Start Condition
Sr	Repeated Start Condition
SAD	Slave Address
W	Write Bit
R	Read Bit
ACK	Acknowledge
NACK	Not Acknowledge
RA	Register Address
Data	Transmitted/Received Data
P	Stop Condition

Table 7. I^2C Terms

Sequence 1. The Master is writing one byte to the Slave.

Master	S	SAD + W		RA		DATA		P
Slave			ACK		ACK		ACK	

Sequence 2. The Master is writing multiple bytes to the Slave.

Master	S	SAD + W		RA		DATA		DATA		P
Slave			ACK		ACK		ACK		ACK	

Sequence 3. The Master is receiving one byte of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			NACK	P
Slave			ACK		ACK			ACK	DATA		

Sequence 4. The Master is receiving multiple bytes of data from the Slave.

Master	S	SAD + W		RA		Sr	SAD + R			ACK		NACK	P
Slave			ACK		ACK			ACK	DATA		DATA		

KXTIK Embedded Registers

The KXTIK has 44 embedded 8-bit registers that are accessible by the user. This section contains the addresses for all embedded registers and also describes bit functions of each register. Table 8 below provides a listing of the accessible 8-bit registers and their addresses.

Register Name	Type Read/Write	I2C Address Hex	I2C Address Binary
XOUT_HPF_L	R	0x00	0000 0000
XOUT_HPF_H	R	0x01	0000 0001
YOUT_HPF_L	R	0x02	0000 0010
YOUT_HPF_H	R	0x03	0000 0011
ZOUT_HPF_L	R	0x04	0000 0100
ZOUT_HPF_H	R	0x05	0000 0101
XOUT_L	R	0x06	0000 0110
XOUT_H	R	0x07	0000 0111
YOUT_L	R	0x08	0000 1000
YOUT_H	R	0x09	0000 1001
ZOUT_L	R	0x0A	0000 1010
ZOUT_H	R	0x0B	0000 1011
DCST_RESP	R	0x0C	0000 1100
Not Used	-	0x0D	0000 1101
Not Used	-	0x0E	0000 1110
WHO_AM_I	R	0x0F	0000 1111
TILT_POS_CUR	R	0x10	0001 0000
TILT_POS_PRE	R	0x11	0001 0001
Kionix Reserved	-	0x12	0001 0010
Kionix Reserved	-	0x13	0001 0011
Kionix Reserved	-	0x14	0001 0100
INT_SRC_REG1	R	0x15	0001 0101
INT_SRC_REG2	R	0x16	0001 0110
Not Used	-	0x17	0001 0111
STATUS_REG	R	0x18	0001 1000
Not Used	-	0x19	0001 1001
INT_REL	R	0x1A	0001 1010
CTRL_REG1*	R/W	0x1B	0001 1011
CTRL_REG2*	R/W	0x1C	0001 1100

CTRL_REG3*	R/W	0x1D	0001 1101
INT_CTRL_REG1*	R/W	0x1E	0001 1110
INT_CTRL_REG2*	R/W	0x1F	0001 1111
INT_CTRL_REG3*	R/W	0x20	0010 0000
DATA_CTRL_REG*	R/W	0x21	0010 0001
Not Used	-	0x22 – 0x27	-
TILT_TIMER*	R/W	0x28	0010 1000
WUF_TIMER*	R/W	0x29	0010 1001
Not Used	-	0x2A	0010 1010
TDT_TIMER*	R/W	0x2B	0010 1011
TDT_H_THRESH*	R/W	0x2C	0010 1100
TDT_L_THRESH*	R/W	0x2D	0010 1101
TDT_TAP_TIMER*	R/W	0x2E	0010 1110
TDT_TOTAL_TIMER*	R/W	0x2F	0010 1111
TDT_LATENCY_TIMER*	R/W	0x30	0011 0000
TDT_WINDOW_TIMER*	R/W	0x31	0011 0001
BUF_CTRL1*	R/W	0x32	0011 0010
BUF_CTRL2*	R/W	0x33	0011 0011
BUF_STATUS_REG1	R	0x34	0011 0100
BUF_STATUS_REG2	R	0x35	0011 0101
BUF_CLEAR	W	0x36	0011 0110
Reserved	-	0x37 – 0x39	-
SELF_TEST	R/W	0x3A	0011 1010
Reserved	-	0x3B – 0x59	-
WUF_THRESH*	R/W	0x5A	0101 1010
Reserved	-	0x5B	0101 1011
TILT_ANGLE*	R/W	0x5C	0101 1100
Reserved	-	0x5D – 0x5E	-
HYST_SET*	R/W	0x5F	0101 1111
BUF_READ	R	0x7F	0111 1111

* Note: When changing the contents of these registers, the PC1 bit in CTRL_REG1 must first be set to “0”.

Table 8. KXTIK Register Map

KXTIK Register Descriptions

Accelerometer Outputs

These registers contain up to 12-bits of valid acceleration data for each axis depending on the setting of the RES bit in CTRL_REG1, where the acceleration outputs are represented in 12-bit valid data when RES = '1' and 8-bit valid data when RES = '0'. The data is updated every user-defined ODR period, is protected from overwrite during each read, and can be converted from digital counts to acceleration (g) per Figure 1 below. The register acceleration output binary data is represented in N-bit 2's complement format. For example, if N = 12 bits, then the Counts range is from -2048 to 2047, and if N = 8 bits, then the Counts range is from -128 to 127.

12-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111 1111	2047	+1.999g	+3.998g	+7.996g
0111 1111 1110	2046	+1.998g	+3.996g	+7.992g
…	…	…	…	…
0000 0000 0001	1	+0.001g	+0.002g	+0.004g
0000 0000 0000	0	0.000g	0.000g	0.000g
1111 1111 1111	-1	-0.001g	-0.002g	-0.004g
…	…	…	…	…
1000 0000 0001	-2047	-1.999g	-3.998g	-7.996g
1000 0000 0000	-2048	-2.000g	-4.000g	-8.000g

8-bit Register Data (2's complement)	Equivalent Counts in decimal	Range = +/-2g	Range = +/-4g	Range = +/-8g
0111 1111	127	+1.984g	+3.968g	+7.936g
0111 1110	126	+1.968g	+3.936g	+7.872g
…	…	…	…	…
0000 0001	1	+0.016g	+0.032g	+0.064g
0000 0000	0	0.000g	0.000g	0.000g
1111 1111	-1	-0.016g	-0.032g	-0.064g
…	…	…	…	…
1000 0001	-127	-1.984g	-3.968g	-7.936g
1000 0000	-128	-2.000g	-4.000g	-8.000g

Figure 1. Acceleration (g) Calculation

Note: *The High Pass Filter outputs are only available if the Wake Up Function is enabled.*

XOUT_HPF_L

X-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x00h		

XOUT_HPF_H

X-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x01h		

YOUT_HPF_L

Y-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x02h		

YOUT_HPF_H

Y-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x03h		

ZOUT_HPF_L

Z-axis high-pass filtered accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x04h		

ZOUT_HPF_H

Z-axis high-pass filtered accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x05h		

XOUT_L

X-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
XOUTD3	XOUTD2	XOUTD1	XOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x06h		

XOUT_H

X-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
XOUTD11	XOUTD10	XOUTD9	XOUTD8	XOUTD7	XOUTD6	XOUTD5	XOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x07h		

YOUT_L

Y-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
YOUTD3	YOUTD2	YOUTD1	YOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x08h		

YOUT_H

Y-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
YOUTD11	YOUTD10	YOUTD9	YOUTD8	YOUTD7	YOUTD6	YOUTD5	YOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x09h		

ZOUT_L

Z-axis accelerometer output least significant byte

R	R	R	R	R	R	R	R
ZOUTD3	ZOUTD2	ZOUTD1	ZOUTD0	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Ah		

ZOUT_H

Z-axis accelerometer output most significant byte

R	R	R	R	R	R	R	R
ZOUTD11	ZOUTD10	ZOUTD9	ZOUTD8	ZOUTD7	ZOUTD6	ZOUTD5	ZOUTD4
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x0Bh		

DCST_RESP

This register can be used to verify proper integrated circuit functionality. It always has a byte value of 0x55h unless the DCST bit in CTRL_REG3 is set. At that point this value is set to 0xAAh. The byte value is returned to 0x55h after reading this register.

R	R	R	R	R	R	R	R	
DCSTR7	DCSTR6	DCSTR5	DCSTR4	DCSTR3	DCSTR2	DCSTR1	DCSTR0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	01010101
					I^2C Address: 0x0Ch			

WHO_AM_I

This register can be used for supplier recognition, as it can be factory written to a known byte value. The default value is 0x05h.

R	R	R	R	R	R	R	R	
WIA7	WIA6	WIA5	WIA4	WIA3	WIA2	WIA1	WIA0	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000101
					I^2C Address: 0x0Fh			

Tilt Position Registers

These two registers report previous and current tilt position data that is updated at the user-defined ODR frequency and is protected during register read. Table 9 describes the reported position for each bit value.

TILT_POS_CUR

Current tilt position register

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
					I^2C Address: 0x10h			

TILT_POS_PRE

Previous tilt position register

R	R	R	R	R	R	R	R	
0	0	LE	RI	DO	UP	FD	FU	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00100000
					I^2C Address: 0x11h			

Bit	Description
LE	Left State (X-)
RI	Right State (X+)
DO	Down State (Y-)
UP	Up State (Y+)
FD	Face-Down State (Z-)
FU	Face-Up State (Z+)

Table 9. KXTIK Tilt Position

Interrupt Source Registers

These two registers report function state changes. This data is updated when a new state change or event occurs and each application's result is latched until the interrupt release register is read. The motion interrupt bit WUFS can be configured to report data in an unlatched manner via the interrupt control registers.

INT_SRC_REG1

This register reports which axis and direction detected a single or double tap event, per Table 10.

R	R	R	R	R	R	R	R
0	0	TLE	TRI	TDO	TUP	TFD	TFU
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x15h		

Bit	Description
TLE	X Negative (X-) Reported
TRI	X Positive (X+) Reported
TDO	Y Negative (Y-) Reported
TUP	Y Positive (Y+) Reported
TFD	Z Negative (Z-) Reported
TFU	Z Positive (Z+) Reported

Table 10. KXTIK Directional Tap™ Reporting

INT_SRC_REG2

This register reports which function caused an interrupt. Reading from the interrupt release register will clear the entire contents of this register.

R	R	R	R	R	R	R	R
0	0	WMI	DRDY	TDTS1	TDTS0	WUFS	TPS
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x16h		

DRDY *indicates that new acceleration data is available. This bit is cleared when acceleration data is read or the interrupt release register is read.*
DRDY = 0 – new acceleration data not available
DRDY = 1 – new acceleration data available

TDTS1, TDTS0 *indicates whether a single or double-tap event was detected per Table 11.*

TDTS1	TDTS0	Event
0	0	No Tap
0	1	Single Tap
1	0	Double Tap
1	1	DNE

Table 11. Directional Tap™ Event Description

WUFS *- Wake up, This bit is cleared when acceleration data is read or the interrupt release register is read.*
0 = No motion
1 = Motion has activated the interrupt

TPS *reflects the status of the tilt position function.*
TPS = 0 – tilt position state has not changed
TPS = 1 – tilt position state has changed

WMI *indicates that the buffer's sample threshold has been reached when in FIFO, FILO, or Stream mode. Not used in Trigger mode.*
WMI = 0 – sample threshold has not been reached
WMI = 1 – sample threshold has been reached

STATUS_REG

This register reports the status of the interrupt.

R	R	R	R	R	R	R	R
0	0	0	INT	0	0	0	0
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x18h		

INT *reports the combined interrupt information of all enabled functions. This bit is released to 0 when the interrupt source latch register (1Ah) is read.*
INT = 0 – no interrupt event
INT = 1 – interrupt event has occurred

INT_REL

Latched interrupt source information (INT_SRC_REG1 and INT_SRC_REG2), the status register, and the physical interrupt pin (11) are cleared when reading this register.

R	R	R	R	R	R	R	R
X	X	X	X	X	X	X	X
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
					I^2C Address: 0x1Ah		

CTRL_REG1

Read/write control register that controls the main feature set.

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PC1	RES	DRDYE	GSEL1	GSEL0	TDTE	WUFE	TPE	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00000000
					I^2C Address: 0x1Bh			

PC1 *controls the operating mode of the KXTIK.*

PC1 = 0 - stand-by mode
PC1 = 1 – operating mode

RES *determines the performance mode of the KXTIK. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

RES = 0 – low current, 8-bit valid
RES = 1- high current, 12-bit valid

DRDYE *enables the reporting of the availability of new acceleration data as an interrupt. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

DRDYE = 0 - new acceleration data not available
DRDYE = 1- new acceleration data available

GSEL1, GSEL0 *selects the acceleration range of the accelerometer outputs per Table 12. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

GSEL1	GSEL0	Range
0	0	+/-2g
0	1	+/-4g
1	0	+/-8g
1	1	NA

Table 12. Selected Acceleration Range

TDTE *enables the Directional Tap™ function that will detect single and double tap events. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

TDTE = 0 – disable
TDTE = 1- enable

WUFE *enables the Wake Up (motion detect) function that will detect a general motion event. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

WUFE = 0 – disable
WUFE = 1- enable

TPE *enables the Tilt Position function that will detect changes in device orientation. Note that to change the value of this bit, the PC1 bit must first be set to "0".*

TPE = 0 – disable
TPE = 1- enable

CTRL_REG2

Read/write control register that primarily controls tilt position state enabling. Per Table 13, if a state's bit is set to one (1), a transition into the corresponding orientation state will generate an interrupt. If it is set to zero (0), a transition into the corresponding orientation state will not generate an interrupt. Note that to properly change the value of this register, the PC1 bit in CTRL_REG1 must first be set to "0".

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
OTDTH	0	LEM	RIM	DOM	UPM	FDM	FUM	Reset Value
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	00111111
					I^2C Address: 0x1Ch			