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Product Specification

Applicant / Manufacturer Hardware	Panasonic Industrial Devices Europe GmbH Zeppelinstrasse 19 21337 Lüneburg Germany
Applicant / Manufacturer Software	Please refer to chapter 30 / 30.1 Information regarding Software Versions
Software Version	Please refer to chapter 30 / 30.1 Information regarding Software Versions

By purchase of any of products described in this document the customer accepts the document's validity and declares their agreement and understanding of its contents and recommendations. Panasonic reserves the right to make changes as required without notification.

TABLE OF CONTENTS

1. SCOPE OF THIS DOCUMENT

This product specification applies to Panasonic's Wi-Fi IEEE 802.11 b/g/n radio module with series number PAN9020 USB, PAN9010 USB, PAN9020 SDIO and PAN9010 SDIO.

2. HISTORY FOR THIS DOCUMENT

Revision	Date	Modification / Remarks
0.1	May 2014	1st preliminary version
0.2	May 2014	- Add Host Interface specification for USB 2.0 and SDIO (19.8 Host Interface Specification)
0.3	July 2014	- Change order of chapters, move 3. Data Sheet Status, 4. Related Documents, 9. Difference PAN9020 USB to PAN9020 SDIO and 10. Difference PAN9020 to PAN9010, restructure chapter numbers - Add contents of 802.11n - Supported data rates (20.1 WLAN Radio Specification) - Change parameter information of EVM and Minimum Receiver Sensitivity (20.2.2 / 20.2.3 / 20.2.4)

3. DATA SHEET STATUS

This data sheet contains the PRELIMINARY specification. Supplementary data will be published at a later date.

Panasonic reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Please consult the most recently issued data sheet before initiating or completing a design.

4. RELATED DOCUMENTS

For an update, please search in the suitable homepage.

[1] PAN9020 and PAN9010 Design-Guide
TBP

[2] Semiconductor Datasheet
88W8782U from Marvell®
88W8782 from Marvell®

[3] Application Note Land Grid Array
http://www.pideu.panasonic.de/pdf/184ext.pdf

[4] REACH and RoHS Certificate
http://www.pideu.panasonic.de/pdf/182ext2.jpg

5. KEY FEATURES

- Surface Mount Type 22.75 x 13.5 x 2.4 mm³
- Wireless Local Area Network (WLAN) Technology
- Operating in the 2.4GHz ISM band
- Supports IEEE 802.11
  - IEEE 802.11b/g payload data rates
  - IEEE 802.11n high throughput data rates
  - IEEE 802.11i security standards AES-CCMP, WEP, TKIP, AES-CMAC and WAPI
  - IEEE 802.11e Quality of Service (QoS)
- Coexistence Interface for external co-located 2.4GHz radios (e.g. Bluetooth)
- Tx power up to +18 dBm (IEEE 802.11b CCK) and 14dBm (IEEE 802.11g ODFM)
- High Rx sensitivity
  - -98dBm (IEEE 802.11b DSSS 1Mbps)
  - -76dBm (IEEE 802.11g OFDM 54Mbps)
  - -74dBm (IEEE 802.11n MCS7 HT20 65Mbps)
  - -71dBm (IEEE 802.11n MCS7 HT40 135Mbps)
- Marvell® 88W8782 WLAN System-on-Chip (SoC) solution inside
- High performance low power CPU core
- Two powerful independent DMA channels
- Power Management Unit with internal or external Sleep Clock (for Power Save Mode)
- Internal crystal oscillator (40MHz)
- USB2.0 or SDIO interface
- Integrated shielding to resist EMI
- Manufactured in conformance with RoHS

6. APPLICATIONS FOR THE MODULE

All Embedded Wireless Applications

- Imaging Platform
- Gaming Platform
- Consumer Electronic
- Portable Application
- Health & Fitness
- Smart Energy
- Printer, Digital Picture Frame
- Game Console
- TV, Media Player
- PC, Tablet, eBook
- Home Gateways, Medical devices
- Thermostat, Control panels

7. WIRELESS LOCAL AREA NETWORK

Wireless Local Area Network (WLAN) is indicating a local radio network meant as a part of the standard IEEE 802.11 family. The IEEE 802.11 is an international standard describing the wireless network. The standard defines the lower layers of the OSI model for wireless communication with the Physical Layer (PHY) and the Data Link Layer (DLL) with its two sub-layers Logical Link Control (LLC) and Media Access Control (MAC). It makes it possible to use any protocol over a IEEE 802.11 wireless network as used at an Ethernet network. Basically WLAN networks using two operating modes for connecting station computers (STA) equipped with a wireless network adapter. The first one is the infrastructure mode where the wireless clients are connected via one or more access points (AP) to a wired network. In this case the network is configured with the same Service Set Identifier (SSID) network name in order to communicate. The second one is the Ad-hoc mode where wireless clients are connected without any access point to the internet.

WLAN devices typically have a higher transmit power to cover a radio range about 100m. Furthermore WLAN is commonly used to transmit high throughput data using upon other the Orthogonal Frequency Division Multiplexing (OFDM) modulation technique. The Carrier Sense Multiple Access with Collosion Avoidance (CSMA/CA) mechanism enables the parallel access of more than one device to the media of a IEEE 802.11 network. By implementation of security mechanisms like Adavanced Encryption Standard (AES) with Counter Mode CBC-MAC Protocol (CCMP) or Cipher-Based Message Authentication Code (CMAC) and Wired Equivalent Privacy (WEP) with Temporal Key Integrity Protocol (TKIP) the network is supporting the security standard IEEE 802.11i. Video, voice and multimedia applications are supported by the IEEE 802.11e Quality of Service amendment.

8. DESCRIPTION FOR THE MODULE

The ENW49801x1JF is a 2.4GHz ISM band wireless radio module for implementing WLAN functionality into various electronic devices. A block diagram can be found in chapter 16.

The ENW49801x1JF is a cost-effective, low-power operation, system-on-chip (SoC) solution for WLAN applications. It enables wireless network adapters and cards to be built with low total bill-of-material costs. The ENW49801x1JF combines an excellent 802.11 wireless radio, baseband processor, medium access controller, encryption unit, CPU, boot ROM with patching capability, internal SRAM, in-system programmable flash memory and many other powerful supporting features and peripherals. The low-power operation supporting deep sleep and standby modes by using the on-board power management unit. The ENW49801x1JF is suitable for wireless network systems based on WLAN IEEE 802.11 b/g/n 2.4GHz where small form factor, highly integration, high throughput data rates and low RF expertise are required.

Panasonic offers the software package supporting various Fedora Core Kernel versions. It includes the WLAN SoC Firmware binary that powers the WLAN SoC for client (STA), micro access point (uAP) and Ad-hoc mode (Wi-Fi direct) applications. In addition it includes the HOST Driver-Firmware Interface (API) which represents the interface between the host driver and SoC firmware.

The Driver-Firmware Interface handles all 802.11 MAC management tasks by converting standard 802.3 frames to the SoC firmware to transmit over the wireless link as 802.11 frames and processes the received 802.11 frames and converts them into 802.3 frames before forwarding them to the host driver. The HOST driver is seperated in three modules. The Standard Ethernet driver, the 802.11 Extensions and the Hardware Interface Driver. The 802.11 Extensions module extends the Standard Ethernet driver in order to view and control the state of the WLAN adapter. The Hardware Interface Driver controls the hardware interface on the HOST side. Furtheron the software package from Marvell® consists of various applications, demonstrations and utilities.

Refer to [1] PAN9020 and PAN9010 Design-Guide and chapter 30 Ordering Information.

Please contact your local sales office for further details on additional options and services:

www.panasonic.com/rfmodules for the US,

http://industrial.panasonic.com/eu/i/29606/wireless_modules/wireless_modules.html for EU

or write an e-mail to wireless@eu.panasonic.com.

9. DIFFERENCE PAN9020 USB TO PAN9020 SDIO

Both the PAN9020 USB and PAN9020 SDIO are refered to the PAN9020 in this document.

The PAN9020 USB is pin-compatible with the PAN9020 SDIO, with the exception that USB is the hardware communication interface on the PAN9020 USB and SDIO is the hardware communication interface on the PAN9020 SDIO. The PAN9020 SDIO does not have the USB interface found on the PAN9020 USB. The RF performance on both PAN9020 USB and PAN9020 SDIO are the same.

Additional details, which have an impact on the module can be found in the datasheets from Marvell®.

88W8782U from Marvell®

88W8782 from Marvell®

10. DIFFERENCE PAN9020 TO PAN9010

The PAN9010 is the non antenna version with bottom pad where the PAN9020 is the version with antenna.

11. DETAILED DESCRIPTION

11.1. PAN9020 / PAN9010 TERMINAL LAYOUT

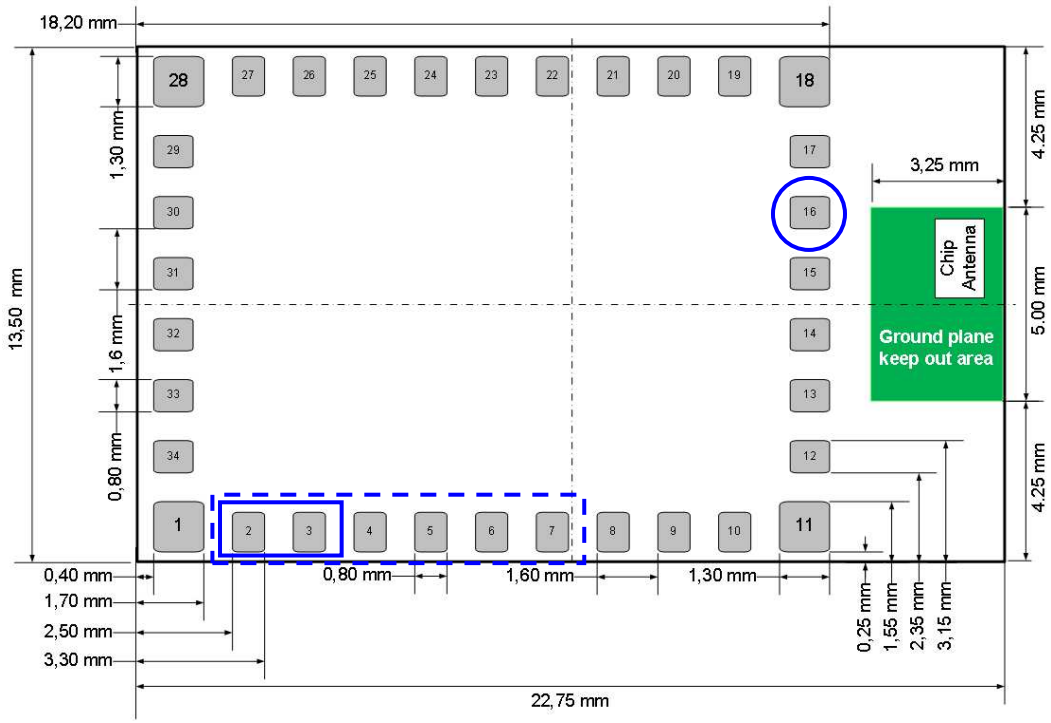
PAN9020 USB pins are marked with a blue rectangular box.

PAN9020 SDIO pins are marked with a blue dashed rectangular box.

PAN9010 USB / SDIO antenna pin is marked with a blue circle.

Top View, Application PCB

Top View



11.2. PAN9020 / PAN9010 COMMON TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description
1	GND	Ground Pin	Connect to Ground
2-7	…	…	… for USB see chapter 0 and for SDIO see chapter 11.4
8	GND	Ground Pin	Connect to Ground
9	PDn	Input Signal	Power down, active-low
10	GPIO[5]	Digital I/O	Port 5 – optional GPIO or W1_CNTL for PMD programming I/F control
11	GND	Ground Pin	Connect to Ground
12	GND	Ground Pin	Connect to Ground
13	GND	Ground Pin	Connect to Ground
14	GND	Ground Pin	Connect to Ground
15	NC	NC	… for PAN9010 see chapter 11.5
16	GND	Ground Pin	Connect to Ground
17	GND	Ground Pin	Connect to Ground
18	GND	Ground Pin	Connect to Ground
19	GND	Ground Pin	Connect to Ground
20	GND	Ground Pin	Connect to Ground
21	RESETn	Input Signal	Reset, active-low
22	GND	Ground Pin	Connect to Ground
23	GPIO[0]	Digital I/O	Port 0 – GPIO
24	GPIO[1]	Digital Output	Port 1 – LED output with 10mA drive capability
25	GPIO[2]	Digital I/O	Port 2 – optional GPIO or SoC-to-Host wake-up
26	GPIO[3]	Digital I/O	Port 3 – optional GPIO or external sleep clock 32.768 KHz input
27	GPIO[4]	Digital I/O	Port 4 – optional GPIO or Host-to-SoC wake-up (for USB used internally)
28	GND	Ground Pin	Connect to Ground
29	BT_FREQ	Input Signal	Information BT using channel which overlaps WLAN channel or not
30	BT_GRANTn	Output Signal	Indicate permission to transmit, low BT can transmit
31	BT_REQ	Input Signal	BT device request access to medium
32	BT_STATE	Input Signal	Information BT_REQ priority (1- or 2-bit) and direction BT RX/TX
33	3.3V	Power	3.0V – 3.6V power supply connection
34	3.3V	Power	3.0V – 3.6V power supply connection

11.3. PAN9020 / PAN9010 USB SPECIFIC TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description
2	USB_DMNS	D-	USB Bus Data Minus
3	USB_DPLS	D+	USB Bus Data Plus
4-7	NC (4x)	NC	Do not connect (4x)

11.4. PAN9020 / PAN9010 SDIO SPECIFIC TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description		
			4-bit mode	1-bit mode	SPI mode
2	SD_CMD	Digital I/O	-	Command Line	Data Input
3	SD_DAT[0]	Digital I/O	Data Line bit [0]	Data Line	Data Output
4	SD_DAT[1]	Digital I/O	Data Line bit [1]	Interrupt	Interrupt
5	SD_DAT[2]	Digital I/O	Data Line bit [2] or … Read Wait (optional)		Reserved
6	SD_DAT[3]	Digital I/O	Data Line bit [3]	Not used	Chip Select, act. low
7	SD_CLK	Digital I/O	Clock	Clock	Clock

11.5. PAN9010 RF-TERMINAL PIN-CONFIGURATION

No	Pin Name	Pin Type	Description
15	RF	RF Port	50Ω bottom pad

12. GENERAL FEATURES

- Embedded WLAN SoC with following features:
  - Integrated CPU with maximum clock speed of 128 MHz
  - Single-chip integration of 802.11 wireless radio, baseband, MAC, CPU, memory and HOST interface
  - SRAM for Tx frame queues and Rx data buffer
  - Boot ROM and ROM patching capability
  - Independent 2-Channel Direct Memory Access (DMA)
  - Low power operation supporting deep sleep and stand-by modes
  - Optional power management with external sleep clock for near zero deep sleep
- Optional embedded EEPROM for storing e.g. serial number

13. HOST INTERFACES

13.1. PAN9020 / PAN9010 USB VARIANT

- USB 2.0 Interface
  - Compliant with the Universal Serial Bus Specification, Revision 2.0
  - Allows HOST controller using USB cable bus and USB 2.0 device interface
  - High/full speed operation with (480/12 Mbps)
  - Suspend / host resume / device resume (remote wake-up)
  - USB 2.0 device interface with integrated level shifter for 3.3V signal level

13.2. PAN9020 / PAN9010 SDIO VARIANT

- SDIO Interface
  - Conforms to the industry SDIO Full-Speed card specification
  - Supports SPI, 1-bit SDIO and 4-bit SDIO transfer modes at the full clock range

14. PERIPHERAL BUS INTERFACE

- Embedded WLAN SoC with following features:
  - Clocked Serial Unit (CSU)
    - 3-Wire, 4-Wire (3W4W) Interface
    - 2-Wire Serial Interface (TWSI)
    - 1-Wire Serial Interface
  - General-Purpose I/O (GPIO) Interface
    - User-defined GPIOs, I/O configured to either input or output
    - GPIOs independently controlled
    - GPIO1 with LED output functionality
      - LED Pulse Stretching to observe short duration of status events
      - Two software controlled blink rates to indicate events

15. WLAN FEATURES

15.1. IEEE 802.11 / STANDARDS

- 802.11 data rates 1 and 2 Mbps (DSSS)
- 802.11b data rates 5.5 and 11 Mbps (CCK)
- 802.11g data rates 6, 9, 12, 18, 24, 36, 48 and 54 Mbps (OFDM)
- 802.11b/g performance enhancements
- 802.11n compliant with maximum data rates up to 72 Mbps (20 MHz channel) and 150 Mbps (40 MHz channel)
- 802.11d international roaming
- 802.11i enhanced security (WEP, WPA, WPA2)
- 802.11k radio resource measurement
- 802.11r fast hand-off for AP roaming
- 802.11w protected management frames
- Fully supports clients (stations) implementing IEEE Power Save mode
- Wi-Fi Direct connectivity

15.2. WLAN MAC

- Ad-Hoc and Infrastructure Modes
- RTS/CTS for operation und DCF
- Hardware filtering of 32 multicast addresses and duplicate frame detection for up to 32 unicast addresses
- WLAN SoC with Tx and Rx FIFO for maximum throughput
- Open System and Shared Key Authentication services
- A-MPDU Rx (de-aggregation) and Tx (aggregation)
- 20/40 MHz channel coexistence
- Reduced Inter-Frame Spacing (RIFS) bursting
- Management Information Base (MIB) counter
- Radio resource measurement counters
- Block acknowledgement with 802.11n extensions
- Transmit beamformee support
- Transmit rate adaptation
- Transmit power control
- Long and short preamble generation on a frame-by-frame basis for 802.11b frames
- Marvell® Mobile Hotspot technology (MMH)

15.3. WLAN BASEBAND

- 802.11n 1x1 SISO (WLAN SoC with SISO RF radio)
- Backward compatibility with legacy 802.11b/g technology
- PHY data rates up to 150 Mbps (802.11n - MCS7)
- 20 MHz bandwidth/channel, 40 MHz bandwidth/channel, upper/lower 20 MHz bandwidth in 40 MHz channel and 20 MHz duplicate legacy bandwidth in 40 MHz channel mode operation
- Modulation and Coding Scheme MCS 0 ~ 7 and MCS 32 (duplicate 6 Mbps)
- Radio resource measurement
- Optional 802.11n SISO features:
  - 20/40 MHz coexistence
  - 1-stream Space-Time-Block-Coding (STBC) reception
  - Short Guard Interval
  - RIFS on receive path
  - Beamformee function and hardware acceleration
  - Greenfield Tx/Rx

15.4. WLAN RADIO

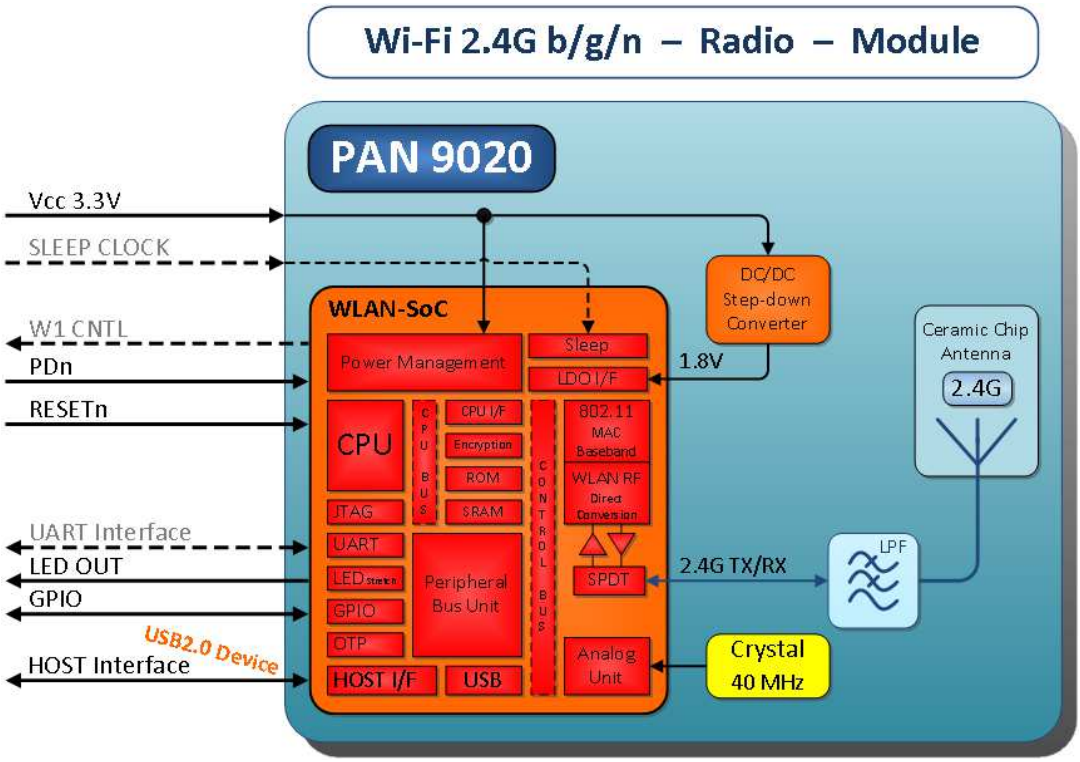
- 20 and 40 MHz channel bandwidth
- Embedded WLAN SoC with following features:
  - Direct conversion radio (no SAW filter)
  - 2.4GHz Tx/Rx switch, Power Amplifier (PA) and Low Noise Amplifier (LNA) path
  - Gain selectable LNAs with optimized noise figure and power consumption
  - Power Amplifiers with power control
  - Closed/Open loop power control (0.5 dB step increments)
  - Optimized Tx gain distribution for linearity and noise performance
  - Fine channel step with AFC (adaptive frequency control)

15.5. WLAN ENCRYPTION

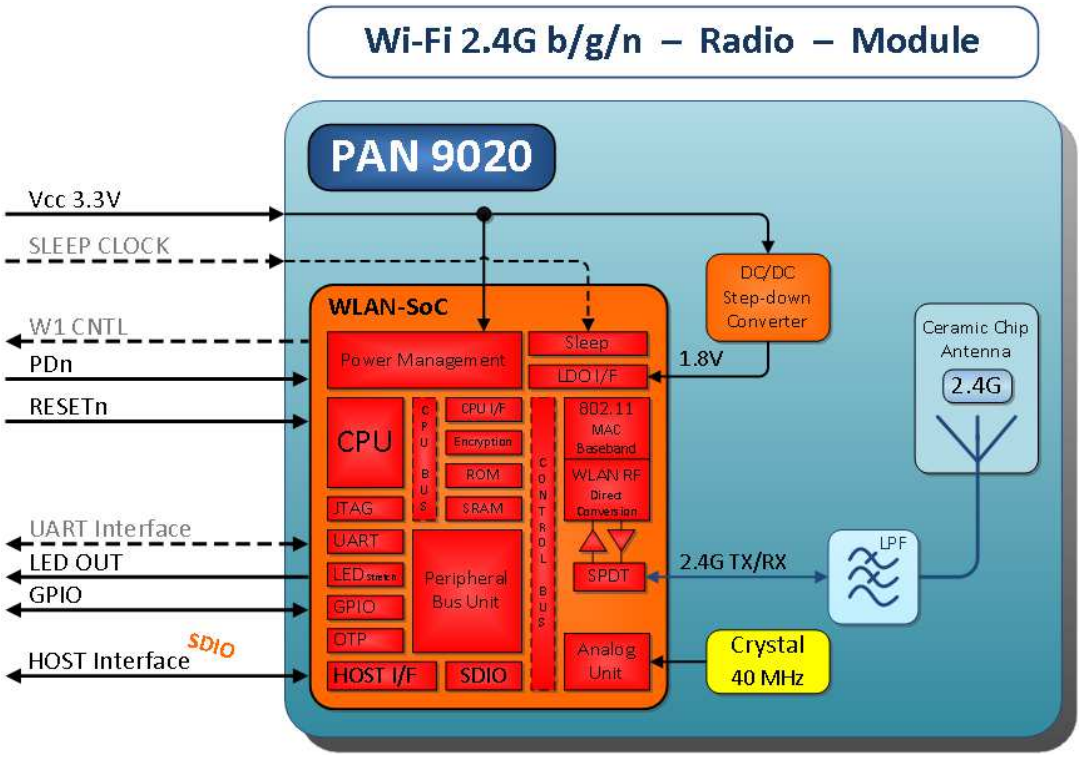
- Embedded WLAN SoC with following features:
  - WEP 64-bit and 128-bit encryption with hardware TKIP processing (WPA)
  - AES-CCMP hardware implementation as part of 802.11i security standard (WPA2)
  - Enhanced AES engine performance
  - AES-Chipher-Based Message Authentication Code (CMAC) as part of the 802.11w security standard
  - WLAN Authentication and Privacy Infrastructure (WAPI)

16. PAN9020 / PAN9010 BLOCK DIAGRAM

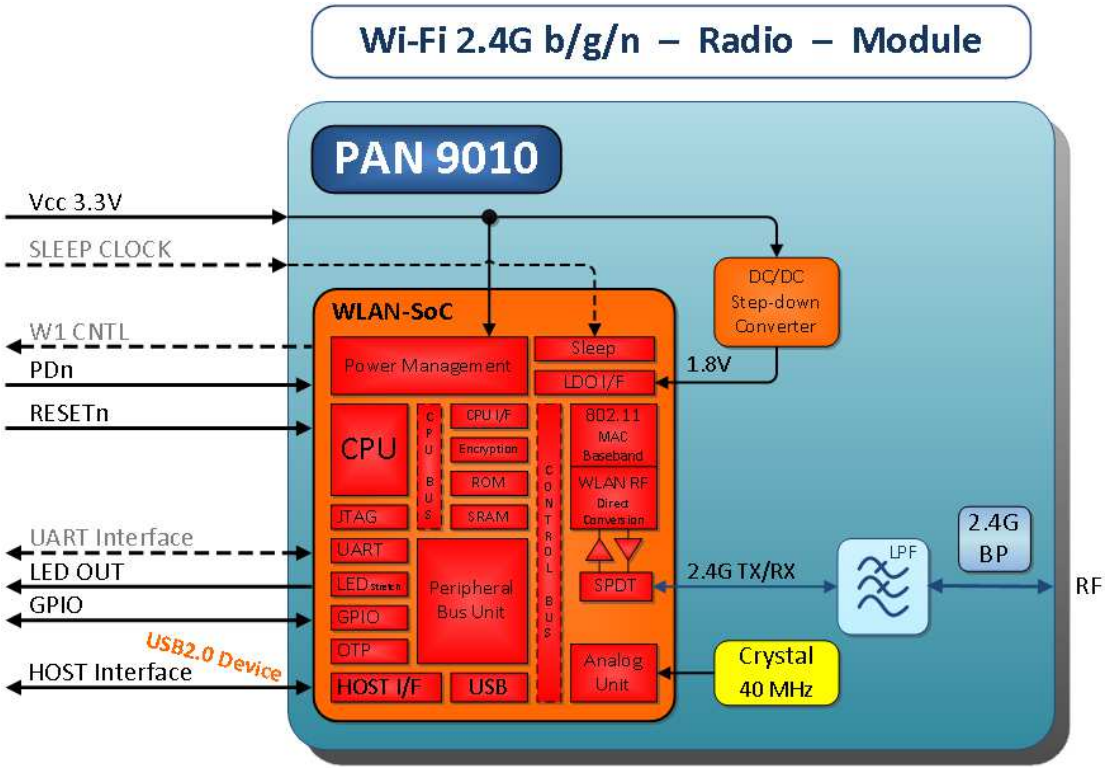
16.1. PAN9020 USB VARIANT



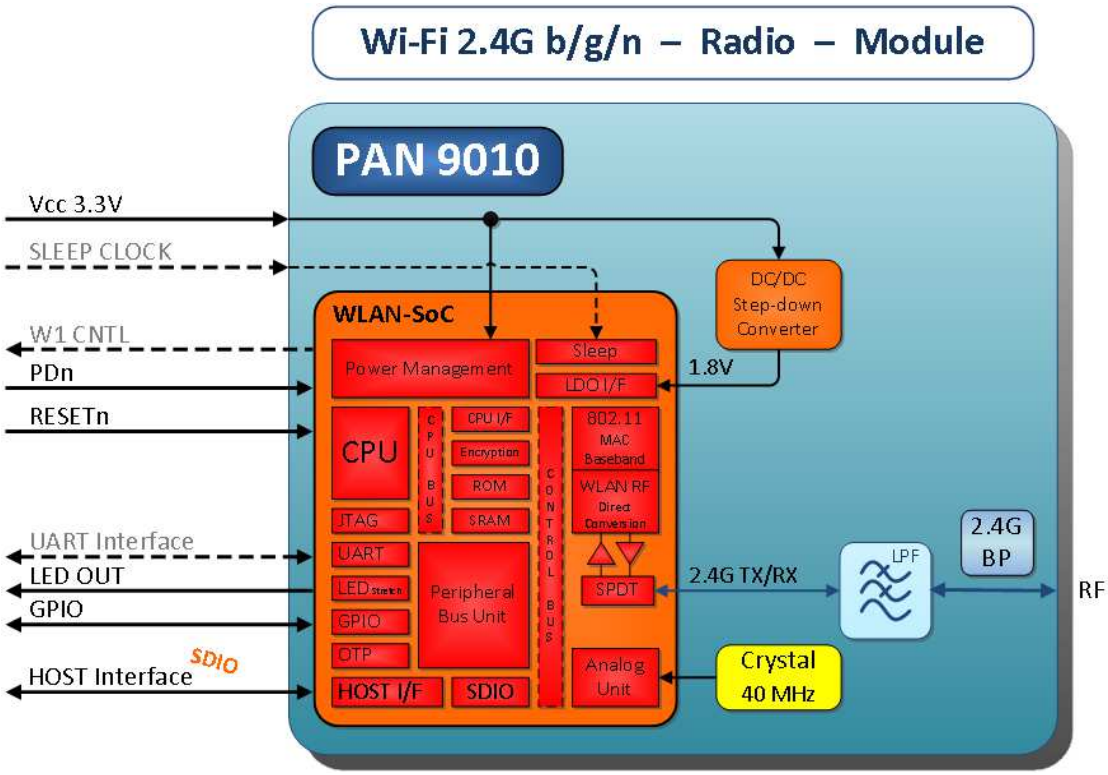
16.2. PAN9020 SDIO VARIANT



16.3. PAN9010 USB VARIANT



16.4. PAN9010 SDIO VARIANT



17. KEY PARTS LIST

Part Name	Material
P.W.Board	Glass cloth epoxide resin with gold plating
Casing	Material: C7521 or ZSNC S1S8 8/8, thickness 0.30mm
IC part name	88W8782 (Marvell®, www.marvell.com)

18. TEST CONDITIONS

Measurements shall be made under operating free-air temperature range unless otherwise specified.

Temperature	25 ± 10°C
Humidity	40 to 85%RH
Supply Voltage	3.3V

19. GENERAL REQUIREMENTS AND OPERATION

All specifications are over temperature and process, unless indicated otherwise.

19.1. ABSOLUTE MAXIMUM RATINGS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_{STOR}	Storage temperature		-40		+125	°C
V_{ESD}	ESD robustness	All pads, according to human-body model, JEDEC STD 22, method A114			1000	V
		According to charged-device model, JEDEC STD 22, method C101			500	V
P_{RF}	RF input level				+20	dBm
V_{DDMAX}	Maximum voltage	Maximum power supply voltage from any pin with respect to V_{SS} (GND)	-0.3		3.9	V
V_{DIG}	Voltage on any digital pins	GPIOs, PDn, RESETn, Coex I/F	-0.3		V_{DDMAX}	V

19.2. RECOMMENDED OPERATING CONDITIONS

The maximum ratings may not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the module will result.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
T_A	Ambient operating temperature range	Commercial grade	0		+70	°C
V_{DD}	3V3 Supply voltage[1]	Voltage on pins 33, 34 (3.3V) I/O supply voltage internally connected to V_{DD}	3.0	3.3	3.6	V

19.3. DIGITAL PIN CHARACTERISTICS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage[2]	3.3V Operation ($V_{IO} = V_{DD}$)	$0.7V_{DD}$		$V_{DD}+0.3$	V
V_{IL}	Low level input voltage[2]	3.3V Operation ($V_{IO} = V_{DD}$)	-0.3		$0.3V_{DD}$	V
V_{HYS}	Input hysteresis voltage[2]	3.3V Operation ($V_{IO} = V_{DD}$)	200			mV
V_{OH}	High level output voltage[2]	3.3V Operation ($V_{IO} = V_{DD}$)	$V_{DD} - 0.4$			V
V_{OL}	Low level output voltage[2]	3.3V Operation ($V_{IO} = V_{DD}$)			0.4	V

[1] The supply current must be limited to max. 1A

[2] The capacitive load should not be larger than 50 pF for all I/O's when using the default driver strength settings. Generally, large capacitance loads increase the overall current consumption.

19.4. ELECTRICAL CHARACERISTICS

The current consumption depends on the user scenario and the setup and timing in the power modes. Assume V_{DD} = 3.3V, T_{amb} = 25°C if nothing else stated

19.4.1. Current consumption PAN9020 / PAN9010 USB Variant

Symbol	Parameter Current Consumption	Condition	Min.	Typ.	Max.	Units
I_{TX}	Active Transmit [3]	P_{TX} = +18 dBm for 802.11b @ 11 Mbps		430		mA
		P_{TX} = +14 dBm for 802.11g @ 54 Mbps		400		mA
		P_{TX} = +13 dBm for 802.11n @ 65 Mbps		390		mA
I_{RX}	Active Receive [4]	802.11b @ 11 Mbps		105		mA
		802.11g @ 54 Mbps		110		mA
		802.11n @ 65 Mbps		115		mA
I_{RXIdle}	Receive Idle [5]	Passive receive state, ready to receive packets, but no active decoding		100		mA
I_{PDn}	Power Down [6]	Grounding of PDn pin		350		µA
$I_{USBSusp}$	USB Suspend [7]	Low-power device automatically enters a suspend state after 3ms of no bus activity		450		µA
$I_{DeepSleep}$	Deep Sleep [8]	Low-power state used in sleep state		200		µA

19.4.2. Current consumption PAN9020 / PAN9010 SDIO Variant

Symbol	Parameter Current consumption	Condition	Min.	Typ.	Max.	Units
I_{TX}	Active Transmit [3]	P_{TX} = +18 dBm for 802.11b @ 11 Mbps		390		mA
		P_{TX} = +14 dBm for 802.11g @ 54 Mbps		330		mA
		P_{TX} = +13 dBm for 802.11n @ 65 Mbps		315		mA
I_{RX}	Active Receive [4]	802.11b @ 11 Mbps		65		mA
		802.11g @ 54 Mbps		70		mA
		802.11n @ 65 Mbps		75		mA
I_{RXIdle}	Receive Idle [5]	Passive receive state, ready to receive packets, but no active decoding		60		mA
I_{PDn}	Power Down [6]	Grounding of PDn pin		100		µA
$I_{IEEE-PS}$	IEEE Power Save [9]	DTIM = 1 with beacon interval 100ms				mA
$I_{DeepSleep}$	Deep Sleep [8]	Low-power state used in sleep state		150		µA

[3] Peak values for specified output power level and data rate with UDP traffic between the AP and Device (STA).

[4] Peak values for specified data rate with UDP traffic between the AP and DUT.

[5] The device is powered on, had the firmware download and is ready to receive packets, but is not actively decoding.

[6] Power Down state can be achieved by grounding the PDn pin. All internal clocks are shut down, the registers and memory are not maintained. Upon exiting power down mode, a rest is automatically performed and a firmware re-download is required.

[7] USB Suspend Mode is valid only for PAN9020 USB and PAN9010 USB. The low-power device automatically enters a suspend state after 3ms of no bus activity.

[8] It is a low-power mode used in the deep sleep state of power save mode. In this case the external reference clock and many WLAN SoC specific blocks are switched-off. Only an internal slow sleep clock is used to maintain register and memory states.

[9] In IEEE Power Save the device automatically wakes up on beacons. This is dependent on the DTIM value of the AP it is connected to. If it is a DTIM value of 1 along with a beacon interval of 100ms, the device wakes up every 100ms.

19.5. INTERNAL OPERATING FREQUENCIES

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
f_{SYSCLK}	CPU/System/Encryption clock speed	Refers to clock speed of WLAN SoC			128	MHz
f_{REFCLK}	Crystal fundamental frequency	Frequency tolerance < ±10 ppm over operating temperature and process		40		MHz

19.6. EXTERNAL SLEEP CLOCK REQUIREMENTS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$f_{SLEEPCLK}$	Sleep Clock frequency [10]	CMOS input clock signal type, ±250 ppm over temperature, aging and process		32.768		kHz
V_{IH}	High level input voltage		0.8		1.98	V
V_{IL}	Low level input voltage		0.0		0.25	V
PN	Phase Noise	Phase Noise requirement @ 100 kHz		-125		dBc/Hz
J_C	Cycle Jitter			1.5		ns (RMS)
SR	Slew rate limit (10-90%)				100	ns
DC	Duty cycle tolerance		20		80	%

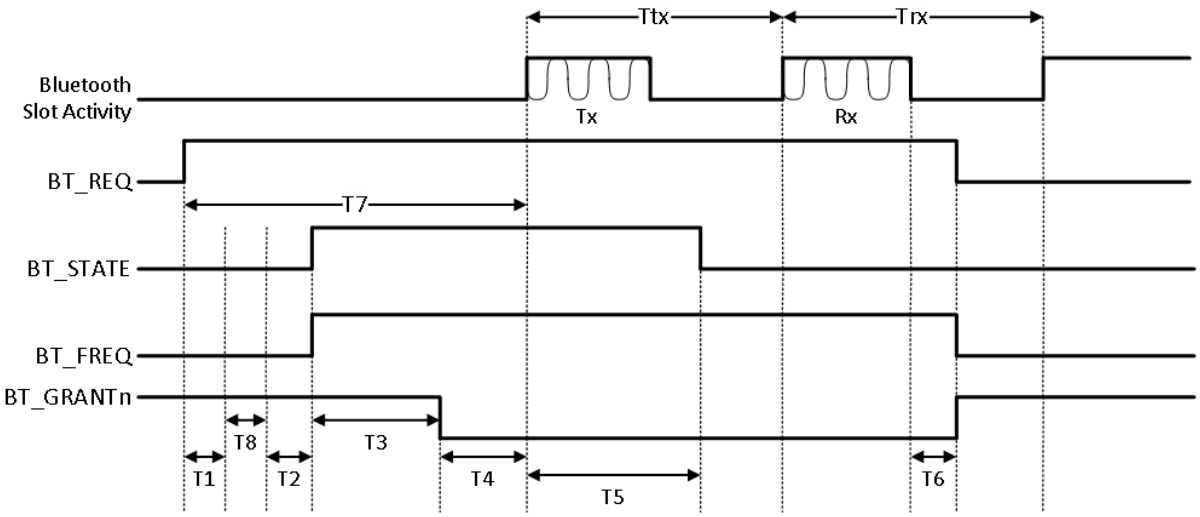
[10] Need to provide external sleep clock when low power operation mode near zero deep sleep is necessary. The external sleep clock is not necessary for normal power modes.

19.7. COEXISTENCE INTERFACE SPECIFICATION

The Coexistence Interface pins are powered from the VIO voltage supply internally connected to V_{DD} = 3.3V. See Chapter 19.3 Digital Pin Characteristics for DC specification.

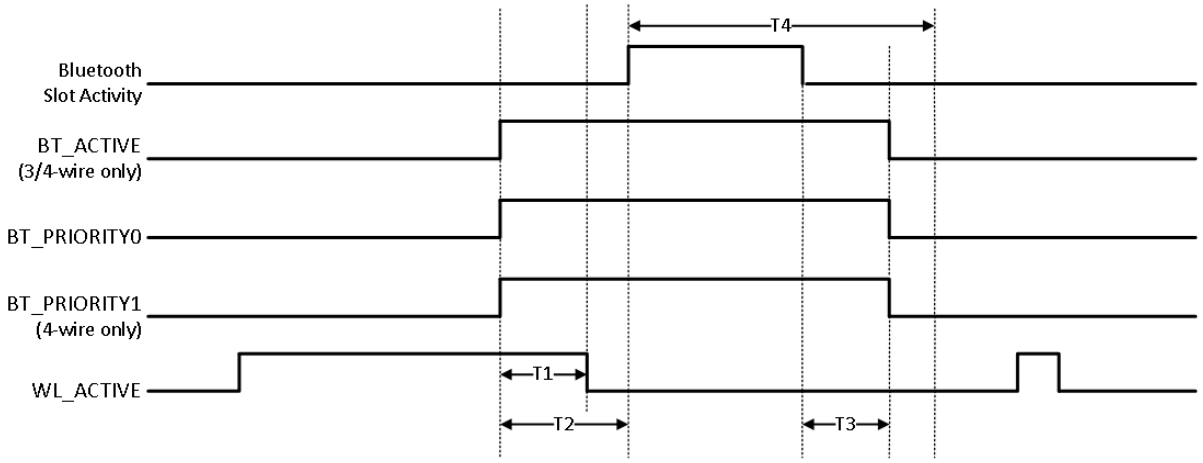
19.7.1. Marvell® 3/4-Wire Timing Data

Symbol	Parameter	Min.	Typ.	Max.	Units
T1	Priority[0] info is valid in BT_STATE on and after T1 from BT_REQ rise.	0	1	100	µs
T2	TxRx Info is valid in BT_STATE on and after T2. The BT_STATE must hold until there is any change of direction in the next slots.	2	19	100	µs
T3	Time from TxRx Info valid to BCA grant decision (T3 = T7 – T4 – T2 – T8 – T1).	2	40	594	µs
T4	BT_GRANTn needs to be valid T4 time before the upcoming slot. BT_GRANTn indicates Tx grant, and may also indicate Rx grant. Once a slot is granted, the subsequent slots are also granted unless there is a change in direction from Rx to Tx. Rx to Tx change always re-arbitrates.	2	80	594	µs
T5	TxRx Info for the next slot is valid on and after T5 to the start of the next slot. If direction remains the same for the next slot, then BT_STATE must not change during the current slot. If the direction changes for the next slot, the BT_STATE must change only after the last bit of Bluetooth data is transferred; otherwise the transfer may be disrupted.	5	40	600	µs
T6	The BT_REQ signal de-asserts T6 time after last bit of Bluetooth data is transferred.	0	15	25	µs
T7	Time from BT_REQ rise to first Bluetooth slot boundary. Bluetooth slot boundary is marked by first bit of Bluetooth data.	8	150	600	µs
T8	Optional Priority[1] information is valid in BT_STAT on and after T8. This time parameter only exists if BCA is configured for 2-bit priority on same BT_STATE pin. Otherwise, the start of T2 would come after T1.	2	10	100	µs
Ttx	Slot time (fixed fpr Bluetooth)		625		µs
Trx	Slot time (fixed fpr Bluetooth)		625		µs



19.7.2. WL_ACTIVE 2/3/4-Wire Timing Data

Symbol	Parameter	Min.	Typ.	Max.	Units
T1	• If WLAN can be stopped, WL_ACTIVE will de-asser prior to Bluetooth slot start (T1 < T2) • If the Bluetooth device samples WL_ACTIVE before starting priority transfer, WL_ACTIVE needs to de-assert earlier than the sampling time.	0		499	µs
T2	Time from BT_PRIORITY rise to start of Bluetooth activity.	20	50	499	µs
T3	Time from end of Bluetooth activity to BT_PRIORITY fall.	0	0	499	µs
T4	Slot time (fixed fpr Bluetooth)		625		µs



19.8. HOST INTERFACE SPECIFICATION

19.8.1. USB 2.0 Interface (PAN9020 / PAN9010 USB)

The USB 2.0 Host Interface pins are powered internally from the V_{DD} = 3.3V. It supports the high / full speed operation (480 / 12 Mbps) depending on the USB bus termination. The default mode is high speed operation.

19.8.1.1. Common Electrical Characteristics

Symbol	*Parameter*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Input Levels for Low / Full Speed						
V_{IH}	Input high voltage (driven)		2.0			V
V_{IHZ}	Input high voltage (floating)		2.7		3.6	V
V_{IL}	Input low voltage				0.8	V
V_{DI}	Differential input sensitivity		0.2			V
V_{CM}	Differential common mode range		0.8		2.5	V
Input Levels for High Speed						
V_{HSSQ}	High-speed squelch detection threshold (differential signal amplitude)		100		150	mV
V_{HSDSC}	High-speed disconnect detection threshold (differential signal amplitude)		525		625	mV
---	High-speed differential input signaling levels	Specified by eye pattern templates; see Section 7.1.7.2 in the USB 2.0 specification				
V_{HSCM}	High-speed data signaling common mode voltage range		-50		500	mV
Output Levels for Low / Full Speed						
V_{OL}	Output low voltage		0.0		0.3	V
V_{OH}	Output high voltage (driven)		2.8		3.6	V
V_{OSE1}	Output SE1 voltage		0.8			V
V_{CRS}	Output signal crossover voltage		1.3		2.0	V
Outpu Levels for High Speed						
V_{HSOI}	High-speed idle level		-10		10	mV
V_{HSOH}	High-speed data signaling high		360		440	mV
V_{HSOL}	High-speed data signaling low		-10		10	mV
V_{CHIRPJ}	Chirp J level (differential voltage)		700		1100	mV
V_{CHIRPK}	Chirp K level (differential voltage)		-900		-500	mV

17.8.1.1 Common Electrical Characteristics (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Decoupling Capacitance						
C_{RPB}	Upstream facing port bypass capacitance		1		10	µF
Input Capacitance for Low / Full Speed						
C_{INUB}	Upstream facing port capacitance (without cable)				100	pF
C_{EDGE}	Transceiver edge rate control capacitance				75	pF
Input Impedance for High Speed						
---	TDR specification for high-speed termination	Differential impedance	80		100	Ω
Terminations						
R_{PUI}	Bus pull-up resistor on upstream port (idles bus)		0.900		1.575	kΩ
R_{PUA}	Bus pull-up resistor on upstream port (receiving)		1.425		3.090	kΩ
Z_{INP}	Input impedance exclusive of pull-up / pull-down (for low / full speed)		300			kΩ
V_{TERM}	Termination voltage for upstream facing port pull-up resistor (R_{PU})		3.0		3.6	V
Terminations in High Speed						
V_{HSTERM}	Termination voltage in high speed		-10		10	mV

19.8.1.2. High Speed Source Electrical Characteristics

Symbol	*Parameter*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Driver Characteristics						
T_{HSR}	Rise Time (10% - 90%)		500			ps
T_{HSF}	Fall Time (10% - 90%)		500			ps
---	Driver waveform requirements	Specified by eye pattern templates; see Section 7.1.2 in the USB 2.0 specification				
Z_{HSDRV}	Driver output resistance (which also serves as high speed termination)		40.5		49.5	Ω
Clock Timings						
T_{HSDRAT}	High speed data rate		479.76		480.24	Mbps
T_{HSFRAM}	Microframe interval		124.9375		125.0625	µs
T_{HSRFI}	Consecutive microframe interval difference				4 high-speed bit times	
High Speed Data Timings						
---	Data source jitter	Specified by eye pattern templates; see Section 7.1.2.2 in the USB 2.0 specification				
---	Receiver jitter tolerance	Specified by eye pattern templates; see Section 7.1.2.2 in the USB 2.0 specification				

19.8.1.3. Full Speed Source Electrical Characteristics

Symbol	*Parameter*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
Driver Characteristics						
T_{FR}	Rise Time		4		20	ns
T_{FF}	Fall Time		4		20	ns
T_{FRFM}	Differential rise and fall time matching	T_{FR} / T_{FF}	90		111.11	%
Clock Timings						
$T_{FDRATHS}$	Full speed data rate	Average bit rate	11.994		12.006	Mbps
T_{FDRATE}	Frame interval		0.9995		1.0005	µs
T_{HSRFI}	Consecutive frame interval difference	No clock adjustment			42	ms
Full Speed Data Timings						
T_{DJ1}	Source Jitter total to next transition (including frequency tolerance)		-3.5		3.5	ns
T_{DJ2}	Source Jitter total to paired transitions (including frequency tolerance)		-4		4	ns
T_{FDEOP}	Source Jitter for differential transition to SE0 transition		-2		5	ns
T_{JR1}	Receiver Jitter to next transition		-18.5		18.5	ns
T_{JR2}	Receiver Jitter to paired transition		-9		9	ns
T_{FEOPT}	Source SE0 interval of EOP		160		175	ns
T_{FEOPR}	Receiver SE0 interval of EOP		82			ns
T_{FST}	Width of SE0 interval during differential transition				14	ns

19.8.1.4. Device Event Timings

Symbol	*Parameter*	*Condition*	*Min.*	*Typ.*	*Max.*	*Units*
T_{SIGATT}	Time from internal power good device pulling D+/D- beyond V_{IHZ} (min) (signaling attach)				100	ms
T_{ATTDB}	Debounce interval provided by USB system software after attach				100	ms
T_{2SUSP}	Maximum time a device can draw power > suspend power when bus is continuously in idle state				10	ms
$T_{SUSAVGI}$	Maximum duration of suspend averaging interval				1	s
T_{WTRSM}	Period of idle bus before device can initiate resum	Device must be remote-wake-up enabled	5			ms
T_{DRSMUP}	Duration of driving resume upstream		1		15	ms
T_{RSMCY}	Resume recovery time	Provided by USB system software	10			ms
$T_{RSTRCYI}$	Reset recovery time				10	ms
T_{IPD}	Inter-packet delay (for low/full speed)		2			bit times
$T_{RSPIPD1}$	Inter-packet delay for device response with detachable cable for low/full speed				6.5	bit times
$T_{RSPIPD2}$	Inter-packet delay for device response with captive cable for low/full speed				7.5	bit times
$T_{DSETADDR}$	SetAddress() completion time				50	ms

17.8.1.4 Device Event Timings (continued)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$T_{DRQCMPLTND}$	Time to complete standard request with no data				50	ms
$T_{DRETDATA1}$	Time to deliver first and subsequent (except last) data for standard request				500	ms
$T_{DRETDATAN}$	Time to deliver last data for standard request				50	ms
$T_{HSRSPIPD2}$	Inter-packet delay for device response with captive cable (high speed)				192 bit times + 52ns	ms
Reset Handshake Protocol						
$F_{FILTSE0}$	Time for which a suspended high speed capable device must see a continuous SE0 before beginning the high speed detection handshake		2.5			µs
$T_{WTRSTFS}$	Time for which high speed capable device operating in non-suspended full speed must wait after start of SE0 before beginning the high speed detection handshake		2.5		3000	µs
T_{WTREV}	Time for which high speed capable device operating in high speed must wait after start of SE0 before reverting to full speed		3.0		3.125	ms
$T_{WTRSTHS}$	Time for which a device must wait after reverting to full speed before sampling the bus state for SE0 and beginning the high speed detection handshake		100		875	µs
T_{UCH}	Minimum duration of a Chirp K from a high speed capable device within the reset protocol		1.0			ms
T_{UCHEND}	Time after start of SE0 by which a high speed capable device is required to have completed its Chirp K within the reset protocol				7.01	ms
T_{WTHS}	Time after end of upstream chirp at which device enters the high speed default state if downstream chirp is detected				500	µs
T_{WTFS}	Time after end of upstream chirp at which device reverts to full speed default state if no downstream chirp is detected		1.0		2.5	ms