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Digital Input, Mono 2 W, Class-D Audio Power Amplifier

Data Sheet

SSM2529

FEATURES

Filterless mono, digital input Class-D amplifier
I²C control interface
Serial digital audio interface supports common formats (I²S, PCM, LJ, RJ, TDM1-16, PDM)
Supports wide range of sample rates: 8.0 kHz to 96.0 kHz
MCLK and BCLK can be provided by built-in phase-locked loop (PLL)
Supports single power supply mode; DVDD can be provided by built-in low dropout (LDO) regulator
2.5 V to 5.5 V SPKVDD operating supply voltage
1.08 V to 1.98 V DVDD operating supply voltage
Support off-chip volume control without I²C
2.4 W into 4 Ω and 1.4 W into 8 Ω at 5 V supply with <1% THD + N
Available in a 16-ball, 1.92 mm × 1.94 mm, 0.4 mm pitch WLCSP
Efficiency 95% at full scale into 8 Ω
Signal-to-noise ratio (SNR): 103 dB, A-weighted
Power supply rejection ratio (PSRR): >80 dB at 217 Hz
Digital volume control: −70 dB to +24 dB in 0.375 dB steps
Ultralow idle current
Autosample rate detection
Pop-and-click suppression
Short-circuit and thermal protection with programmable autorecovery
Supports smart power-down when no input signal is detected
Power-on reset and UVLO voltage monitoring
Selectable ultralow EMI emission mode
Supports SPKVDD voltage monitor
Digital audio processing
- **7-band programmable equalizer**
- **Programmable dynamic range compression (DRC) with noise gate, expander, compressor, and limiter**

APPLICATIONS

Mobile phones
Portable media players
Laptop PCs
Wireless speakers
Portable gaming
Navigation systems

GENERAL DESCRIPTION

The SSM2529 is a digital input, Class-D power amplifier that combines a digital-to-analog converter (DAC), a low power audio specific digital signal processor, and a sigma-delta (Σ-Δ) Class-D modulator. This unique architecture enables extremely low real-world power consumption from digital audio sources with excellent audio performance. The SSM2529 is ideal for power sensitive applications, such as mobile phones and portable media players, where system noise can the corrupt small analog signals that are sent to an analog input audio amplifier.

Using the SSM2529, audio data can be transmitted to the amplifier over a standard digital audio serial interface, thereby significantly reducing the effect of noise sources such as GSM interference or other digital signals on the transmitted audio. The closed-loop digital input design retains the benefits of an all-digital amplifier, yet enables very good PSRR and audio performance. The three-level, Σ-Δ Class-D modulator is designed to provide the least amount of EMI, the lowest quiescent power dissipation, and the highest audio efficiency without sacrificing audio quality.

The audio input is provided via a serial audio interface that can be programmed to accept all common audio formats, including I²S, TDM, and PDM. Control of the IC is provided via an I²C control interface. An alternative to I²C control is standalone operation mode, which allows several settings that are adjusted by off-chip external resistors. The SSM2529 can accept a variety of input MCLK frequencies and can use BCLK as the clock source in some configurations. An integrated PLL can also provide the device master clock.

The integrated DSP includes soft digital volume control circuits; a de-emphasis, high-pass filter; a seven-band programmable equalizer; and a programmable digital dynamic range compressor. In addition, the part includes a feedforward speaker temperature prediction module to protect the loudspeaker.

The SSM2529 supports single-supply mode, where DVDD is provided by the on-chip LDO regulator, eliminating the need for an external digital core supply.

The digital interface is very flexible and convenient. It can offer a better system solution for other products whose sole audio source is digital, such as wireless speakers, laptop PCs, portable digital televisions, and navigation systems.

The SSM2529 is specified over the industrial temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a 16-ball, 1.92 mm × 1.94 mm wafer level chip scale package (WLCSP).

Rev. 0

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Last Content Update: 02/23/2017

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DOCUMENTATION

Data Sheet

- SSM2529: Digital Input, Mono 2 W, Class-D Audio Power Amplifier Data Sheet

DESIGN RESOURCES

- SSM2529 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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REVISION HISTORY

7/12—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

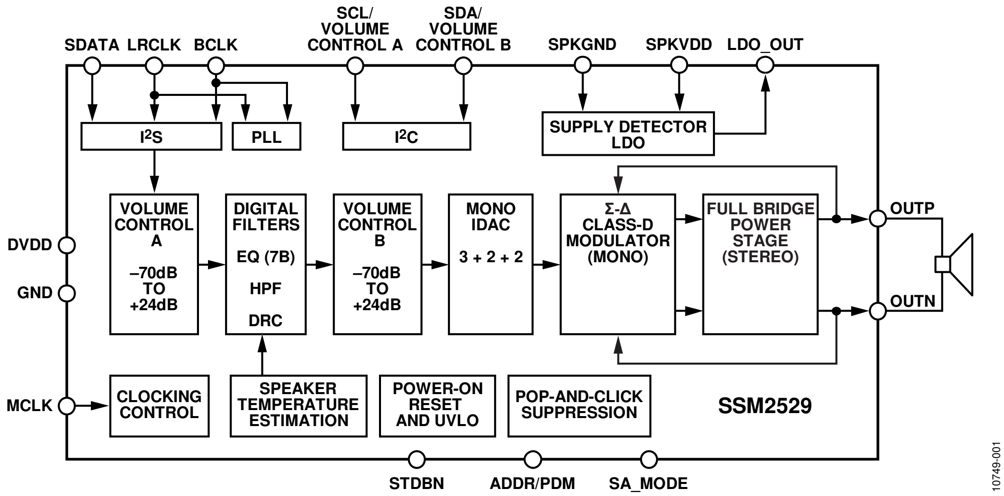

Figure 1.

SPECIFICATIONS

Standard test condition: SPKVDD = 4.2 V; DVDD = 1.8 V; f_S = 48 kHz; MCLK = 128 × f_S; T_A = 25°C; R_L = 8 Ω + 33 μH; LP_MODE = 0; 0 dB volume control setting, unless otherwise noted.

PERFORMANCE SPECIFICATIONS

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_{OUT}	f = 1 kHz, BW = 20 kHz				
		R_L = 4 Ω, THD = 1%, SPKVDD = 5.0 V		2.4		W
		R_L = 4 Ω, THD = 10%, SPKVDD = 5.0 V		3.1		W
		R_L = 8 Ω, THD = 1%, SPKVDD = 5.0 V		1.4		W
		R_L = 8 Ω, THD = 10%, SPKVDD = 5.0 V		1.8		W
		R_L = 4 Ω, THD = 1%, SPKVDD = 4.2 V		1.7		W
		R_L = 4 Ω, THD = 10%, SPKVDD = 4.2 V		2.2		W
		R_L = 8 Ω, THD = 1%, SPKVDD = 4.2 V		0.95		W
		R_L = 8 Ω, THD = 10%, SPKVDD = 4.2 V		1.2		W
		R_L = 4 Ω, THD = 1%, SPKVDD = 3.6 V		1.2		W
		R_L = 4 Ω, THD = 10%, SPKVDD = 3.6 V		1.6		W
		R_L = 8 Ω, THD = 1%, SPKVDD = 3.6 V		0.7		W
		R_L = 8 Ω, THD = 10%, SPKVDD = 3.6 V		0.9		W
		R_L = 4 Ω, THD = 1%, SPKVDD = 2.5 V		0.55		W
		R_L = 4 Ω, THD = 10%, SPKVDD = 2.5 V		0.72		W
		R_L = 8 Ω, THD = 1%, SPKVDD = 2.5 V		0.32		W
		R_L = 8 Ω, THD = 10%, SPKVDD = 2.5 V		0.42		W
Efficiency	η	P_{OUT} = 2 W into 4 Ω, SPKVDD = 5.0 V		91		%
		P_{OUT} = 1.4 W into 8 Ω, SPKVDD = 5.0 V, normal operation		95		%
		P_{OUT} = 1.4 W into 8 Ω, SPKVDD = 5.0 V, ultralow EMI operation		86		%
Total Harmonic Distortion Plus Noise	THD + N	P_{OUT} = 1 W into 8 Ω, f = 1 kHz, SPKVDD = 5.0 V		0.03		%
		P_{OUT} = 0.7 W into 8 Ω, f = 1 kHz, SPKVDD = 4.2 V		0.03		%
		P_{OUT} = 0.5 W into 8 Ω, f = 1 kHz, SPKVDD = 3.6 V		0.03		%
Average Switching Frequency	f_{SW}			280		kHz
Differential Output Offset Voltage	V_{OOS}			2.0		mV
Power Supply Rejection Ratio	PSRR (DC)	SPKVDD = 2.5 V to 5.0 V	70	80		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV rms at 217 Hz, dither input		80		dB
Supply Current	I_{SPKVDD}	Dither input, SPKVDD = 5.0 V		3.0		mA
		Dither input, SPKVDD = 4.2 V		2.8		mA
		Dither input, SPKVDD = 3.6 V		2.7		mA
		Dither input, SPKVDD = 2.5 V		2.4		mA
		Power-down		100		nA
Supply Current	I_{DVDD}	Dither input, DVDD = 1.8 V		0.6		mA
		Dither input, DVDD = 1.08 V		0.3		mA
		Power-down		2		μA
Output Voltage Noise	e_n	f = 20 Hz to 20 kHz, dither input		22		μV
Signal-to-Noise Ratio	SNR	A-weighted reference to 0 dBFS, SPKVDD = 4.2 V		103		dB
Mute Attenuation		Soft mute on	100			dB

POWER SUPPLY REQUIREMENTS

Table 2.

Parameter	Min	Typ	Max	Unit
SPKVDD	2.5	4.2	5.5	V
DVDD	1.08	1.8	1.98	V

DIGITAL INPUT/OUTPUT

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Input Voltage, High	V_{IH}		0.7 × DVDD		3.6	V
Input Voltage, Low	V_{IL}		−0.3		+0.3 × DVDD	V
Input Leakage Current, High	I_{IH}	Excluding MCLK			1	µA
Input Leakage Current, Low	I_{IL}	Excluding MCLK and bidirectional pins			1	µA
MCLK Input Leakage, High	I_{IH}				3	µA
MCLK Input Leakage, Low	I_{IL}				3	µA
Input Capacitance					5	pF

DIGITAL INTERPOLATION FILTER

Table 4.

Parameter	Mode	Factor	Min	Typ	Max	Unit
Pass Band (−3 dB)	48 kHz mode, typical at 48 kHz	0.423 f_S		20		kHz
Pass-Band Ripple	48 kHz mode, typical at 48 kHz	0.5 f_S			±0.03	dB
Transition Band	48 kHz mode, typical at 48 kHz			24		kHz
Stop Band	48 kHz mode, typical at 48 kHz	0.582 f_S		28		kHz
Stop Band Attenuation	48 kHz mode, typical at 48 kHz		60			dB
Group Delay	48 kHz mode, typical at 48 kHz	$14/f_S$		292		µs

DIGITAL TIMING

All timing specifications are given for the default setting (I^2S mode) of the serial input port.

Table 5.

	Limit			
Parameter	T_{MIN}	T_{MAX}	Unit	Description
MASTER CLOCK (See Figure 2)				
t_{BP}	74	136	ns	MCLK period, 256 f_S mode
t_{BP}	148	271	ns	MCLK period, 128 f_S mode
SERIAL PORT (See Figure 2)				
t_{BIL}	40		ns	BCLK low pulse width
t_{BIH}	40		ns	BCLK high pulse width
t_{LIS}	10		ns	LRCLK setup; time to BCLK rising
t_{LIH}	10		ns	LRCLK hold; time from BCLK rising
t_{SIS}	10		ns	SDATA setup; time to BCLK rising
t_{SIH}	10		ns	SDATA hold; time from BCLK rising

Parameter	Limit T_{MIN}	T_{MAX}	Unit	Description
I²C PORT (See Figure 3)				
f_{SCL}		400	kHz	SCL frequency (not shown in Figure 3)
t_{SCLH}	0.6		µs	SCL high
t_{SCLL}	1.3		µs	SCL low
t_{SCS}	0.6		µs	Setup time, relevant for repeated start condition
t_{SCH}	0.6		µs	Hold time; after this period, the first clock is generated
t_{DS}	100		ns	Data setup time
t_{SCR}		300	ns	SCL rise time
t_{SCF}		300	ns	SCL fall time
t_{SDR}		300	ns	SDA rise time (not shown in Figure 3)
t_{SDF}		300	ns	SDA fall time (not shown in Figure 3)
t_{BFT}	0.6		µs	Bus-free time; time between stop and start

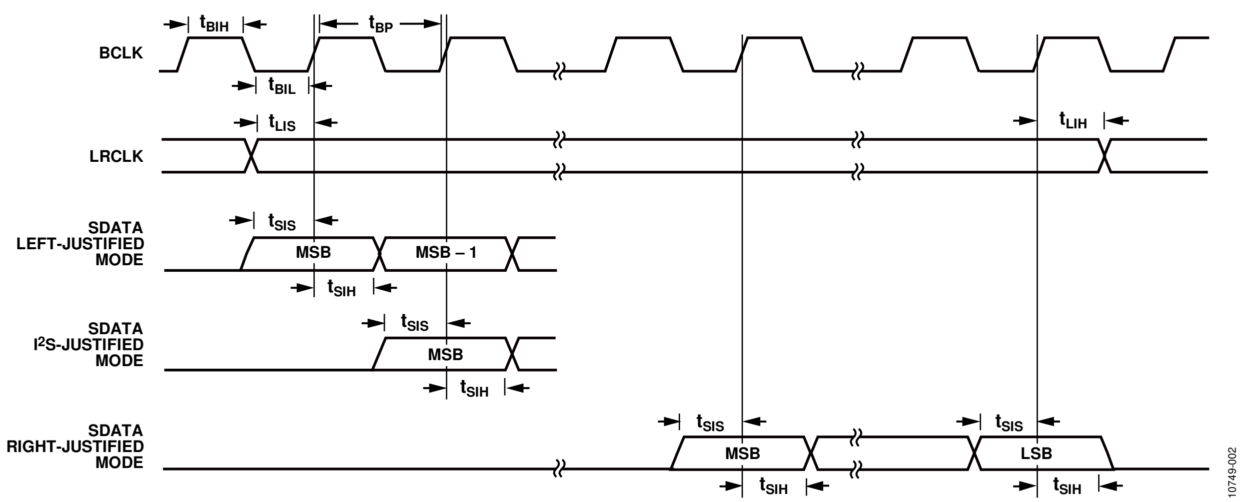

Figure 2. Serial Input Port Timing

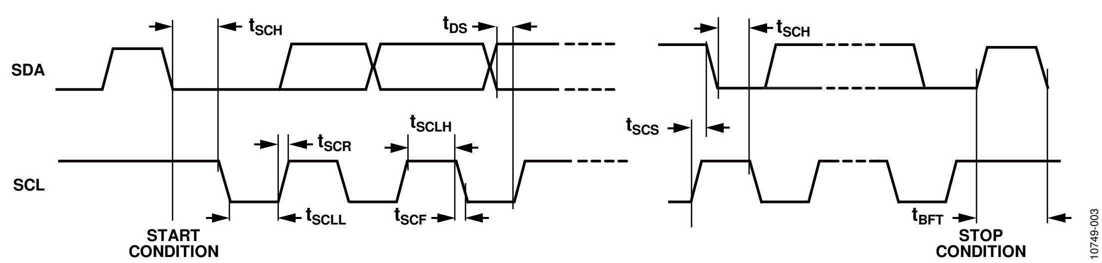

Figure 3. I²C Port Timing

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
SPKVDD Supply Voltage	−0.3 V to +5.5 V
DVDD Supply Voltage	−0.3 V to +1.98 V
Input Voltage (Signal Source)	−0.3 V to +3.6 V
ESD Susceptibility	4 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
16-Ball, 1.92 mm × 1.94 mm WLCSP	56.1	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

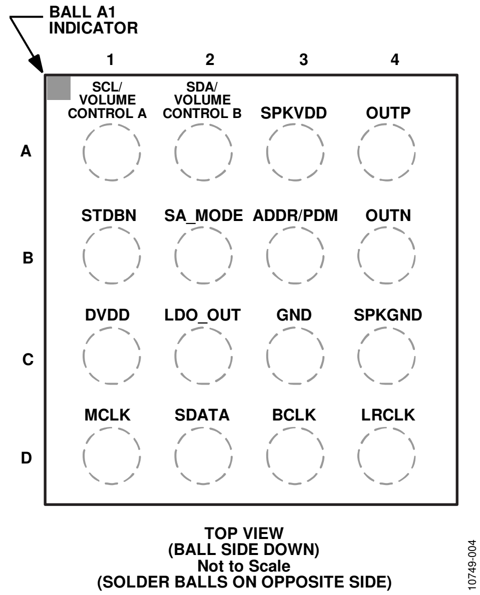

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin Number	Mnemonic	Function	Description
A1	SCL/VOLUME CONTROL A	Input	I^2C Clock in I^2C Mode/Volume Controller A in Standalone Mode
A2	SDA/VOLUME CONTROL B	Input/Output	I^2C Data in I^2C Mode/Volume Controller B in Standalone Mode
A3	SPKVDD	Power	2.5 V to 5.5 V Amplifier Power
A4	OUTP	Output	Positive Output
B1	STDBN	Input	Power-Down Control; Active Low
B2	SA_MODE	Input	Standalone and Hardware Selection; 1 = Standalone Mode
B3	ADDR/PDM	Input	I^2C Chip Address Select/Input Interface Select in Standalone Mode
B4	OUTN	Output	Negative Output
C1	DVDD	Power	Digital Power
C2	LDO_OUT	Power	LDO Output
C3	GND	Power	Digital and Analog Ground
C4	SPKGND	Power	Amplifier Ground
D1	MCLK	Input	Serial Audio Interface Master Clock and I^2S/TDM/PDM Channel Select
D2	SDATA	Input	I^2S Serial Data/PDM Data
D3	BCLK	Input	I^2S Bit Clock/PDM Clock
D4	LRCLK	Input	I^2S Left-Right Frame Clock

TYPICAL PERFORMANCE CHARACTERISTICS

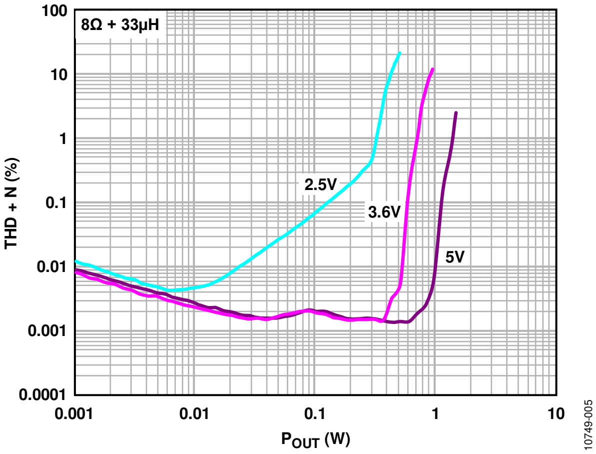

Figure 5. THD + N vs. Output Power into 8 Ω, 5.0 V Gain Setting

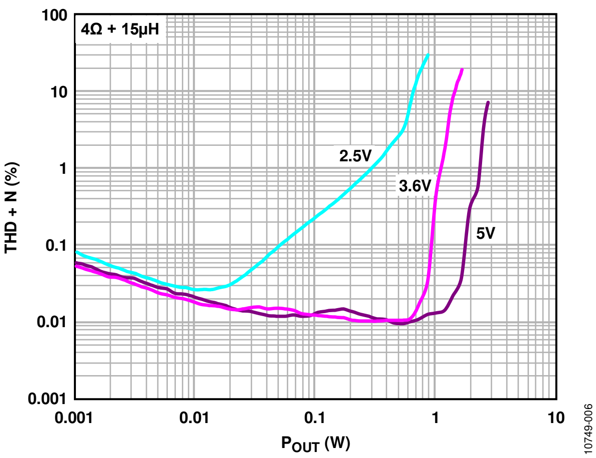

Figure 6. THD + N vs. Output Power into 4 Ω, 5.0 V Gain Setting

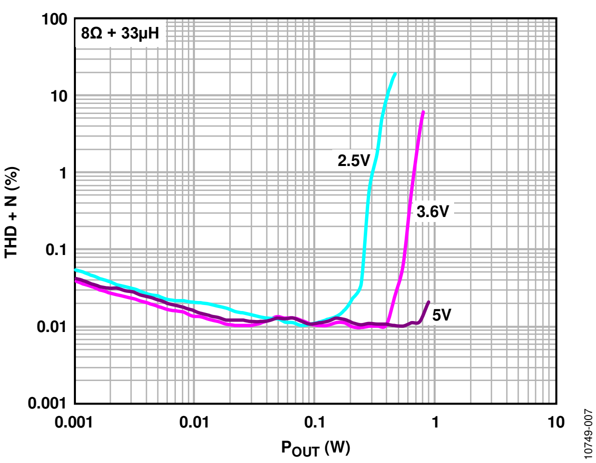

Figure 7. THD + N vs. Output Power into 8 Ω, 3.6 V Gain Setting

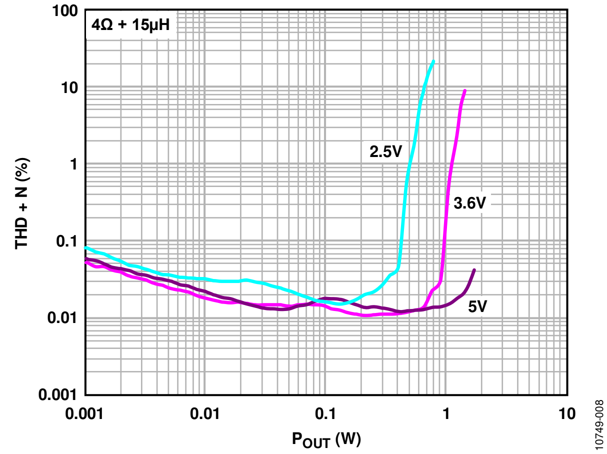

Figure 8. THD + N vs. Output Power into 4 Ω, 3.6 V Gain Setting

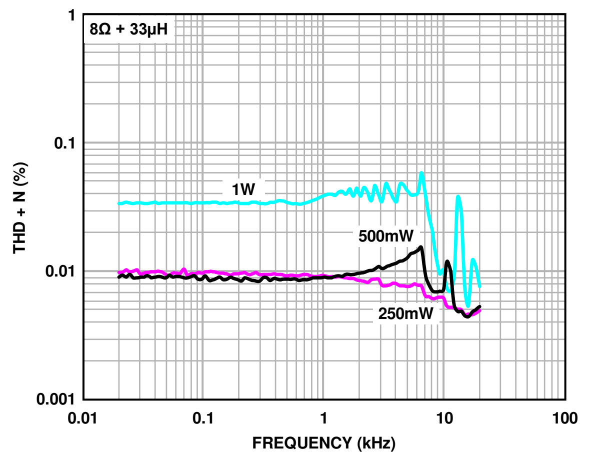

Figure 9. THD + N vs. Frequency into 8 Ω, SPKVDD = 5.0 V

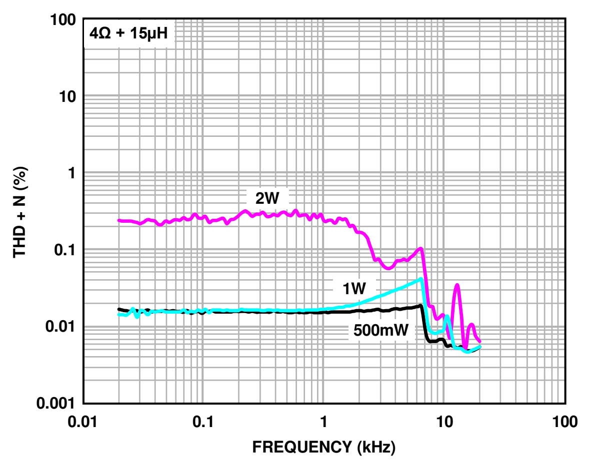

Figure 10. THD + N vs. Frequency into 4 Ω, SPVKDD = 5.0 V

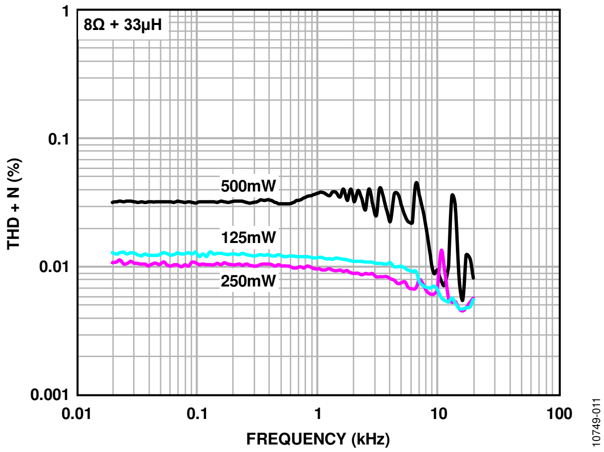

Figure 11. THD + N vs. Frequency into 8 Ω, SPVKDD = 3.6 V

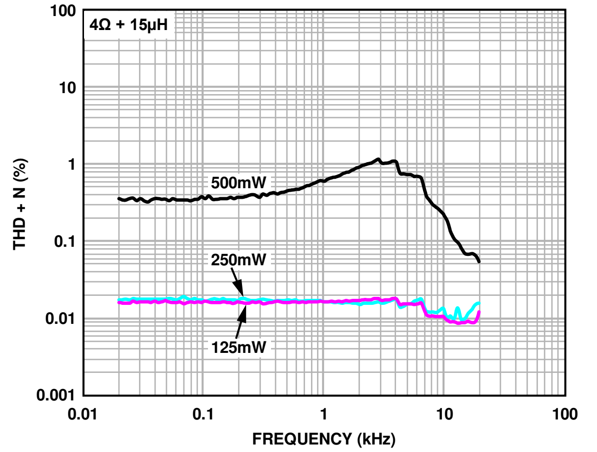

Figure 14. THD + N vs. Frequency into 4 Ω, SPVKDD = 2.5 V

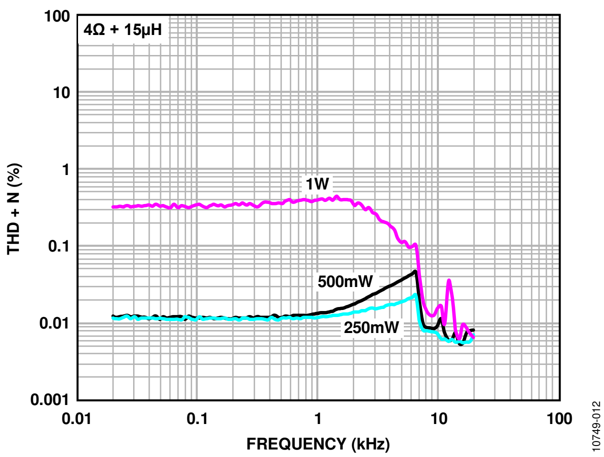

Figure 12. THD + N vs. Frequency into 4 Ω, SPVKDD = 3.6 V

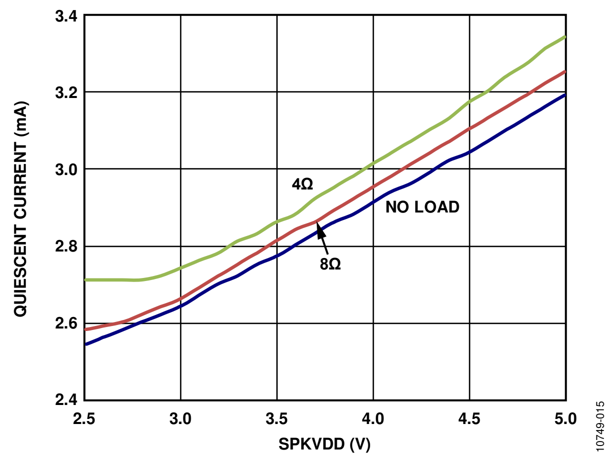

Figure 15. Quiescent Current (Power Stage) vs. Supply Voltage

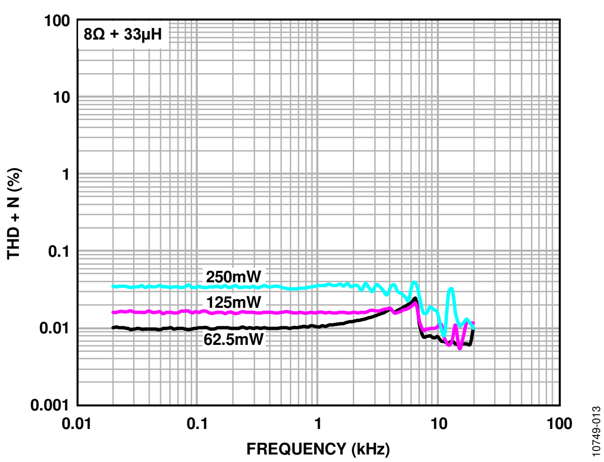

Figure 13. THD + N vs. Frequency into 8 Ω, SPKVDD = 2.5 V

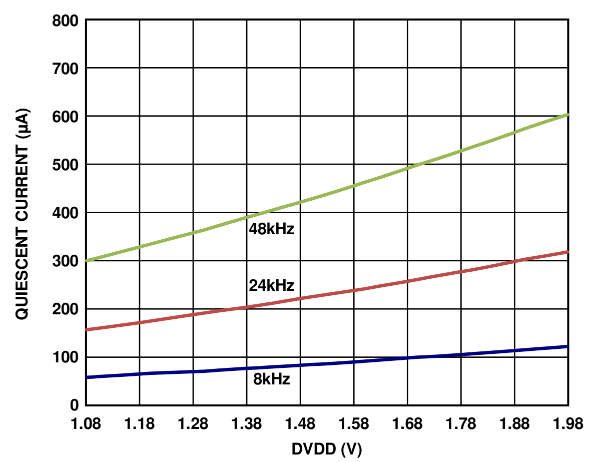

Figure 16. Quiescent Current (Digital Core) vs. Supply Voltage

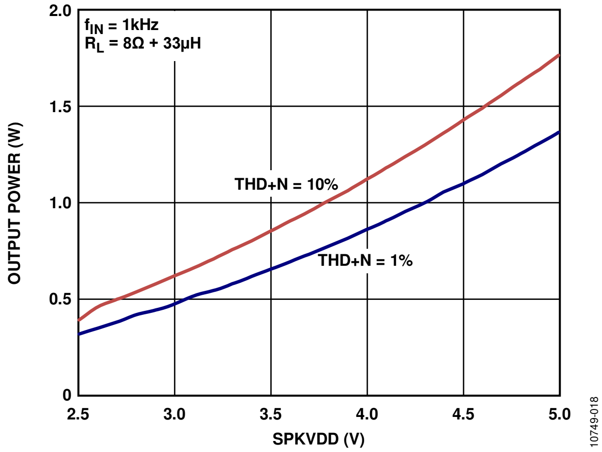

Figure 17. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω

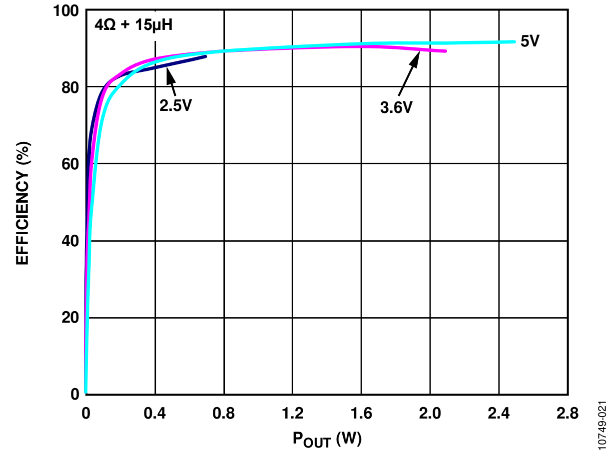

Figure 20. Efficiency vs. Output Power into 4 Ω

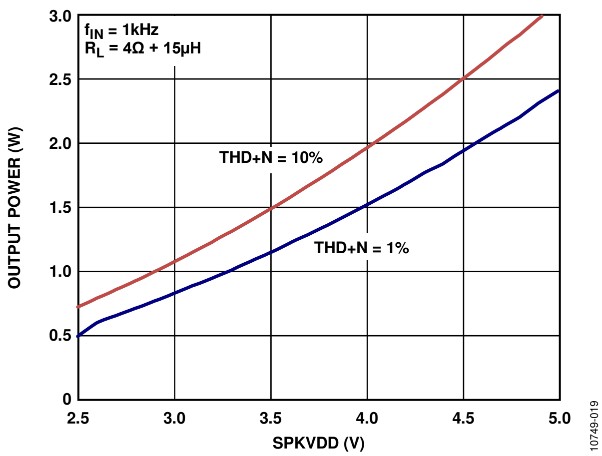

Figure 18. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω

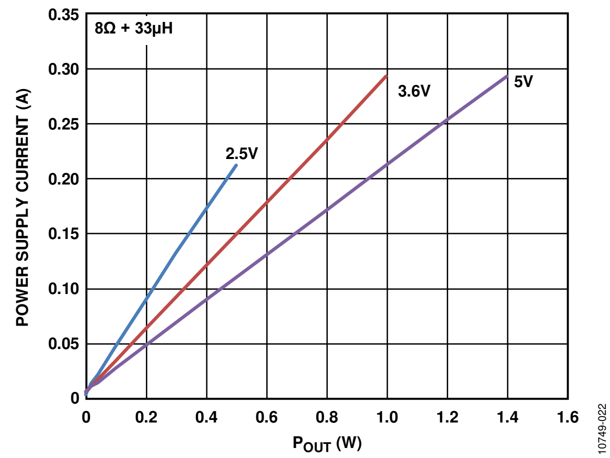

Figure 21. Power Supply Current vs. Output Power, R_L = 8 Ω

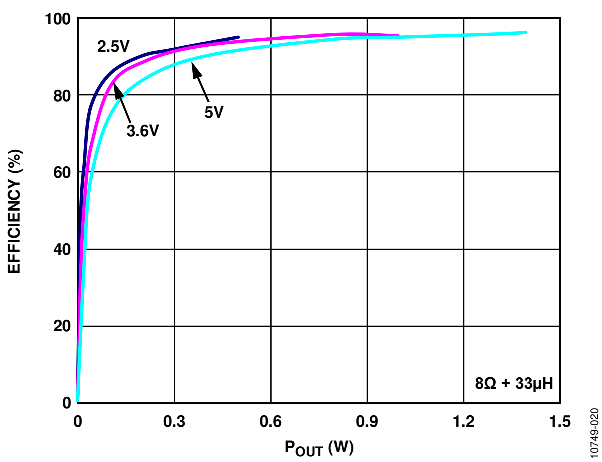

Figure 19. Efficiency vs. Output Power into 8 Ω

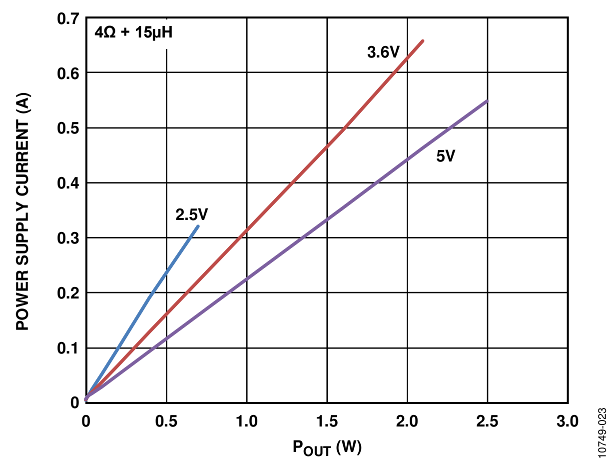

Figure 22. Power Supply Current vs. Output Power, R_L = 4 Ω

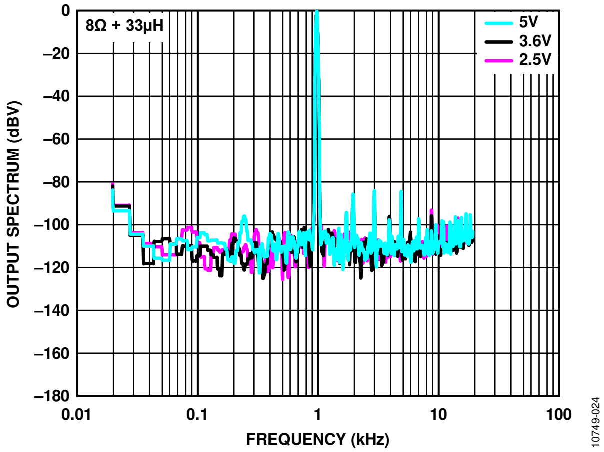

Figure 23. Output Spectrum vs. Frequency (FFT with 100 mW Output Power into 8 Ω Load)

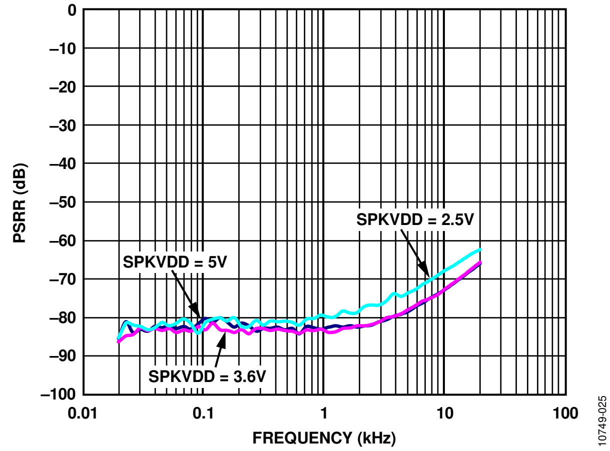

Figure 24. PSRR vs. Frequency

THEORY OF OPERATION

OVERVIEW

The SSM2529 is a fully integrated, mono, digital switching audio amplifier. The SSM2529 receives digital audio inputs and produces the PDM differential switching outputs using the internal power stage. The part has built-in protections for overtemperature and overcurrent conditions. The SSM2529 also has built-in soft turn-on and soft turn-off for pop-and-click suppression. The part has programmable register control via the I^2C port.

MASTER CLOCK

In master mode, the built-in PLL can provide the master clock. In slave mode, the SSM2529 receives an external clock at the MCLK or BCLK input pin. The external clock must be fully synchronous with the incoming digital audio on the serial interface. The internal clock for the SSM2529 always runs at 5.6448 MHz to 8.192 MHz, depending on the input sample rate. The three options for providing the master clock to the part are as follows:

- Using the clock generated by the built-in PLL
- Using the BCLK pin
- Using the MCLK pin

The MCLK option can use the built-in PLL or the BCLK pin to generate the internal clock as long as the clock is provided at the same rate that is required by the MCLK pin. By setting the PLLEN bit in Register 0x0E, this is enabled. In this case, there is no need to provide the master clock to the MCLK pin, which in turn saves a pin connection from the audio source. If using the MCLK pin, various multiples of the sample frequency can be used for MCLK. See Table 48 for all available options and settings. When the SSM2529 enters its power-down state, it is possible to gate this clock to further conserve system power. However, an MCLK must be present for the audio amplifier to operate. The input MCLK rate is determined by setting the MCS bits in Register 0x00. For more information, see Table 48.

INTERNAL CLOCK GENERATOR

The digital core clock can be derived directly from the external clock, or it can be generated using the PLL. Clocks for the DSPs, the serial ports, and the converters are derived from the core clock. The core clock rate is always an integer multiple of the sample rate used for the part.

The clock generation block is composed of a digital PLL and an analog PLL. The analog PLL can accept input frequencies in the 8 MHz to 27 MHz range. To support lower frequencies (8 kHz to 8 MHz), the chip provides a digital PLL. It can boost the input clock frequency by 2^N, where N = 1 to 10.

Figure 25 shows the clock generation block diagram.

For the digital PLL, the source clock is selected by the DPLL_REF_SEL bits (Register 0x08), and the frequency relationship between the DPLL input and the output clock is defined by the DPLL_NDIV bit.

The frequency relationship between the APLL input and output is

$$f_{PLL} = f_{IN} \times (R + (N/M))/X$$

where R, N, M, and X are defined by the corresponding PLL registers (Register 0x09 to Register 0x0D).

DIGITAL INPUT SERIAL AUDIO INTERFACE

The SSM2529 includes a standard serial audio interface that is slave only. The interface is capable of receiving I^2S, left justified, right justified, PCM/TDM, or PDM input formats. The number of data bits must be set when in right-justified mode only.

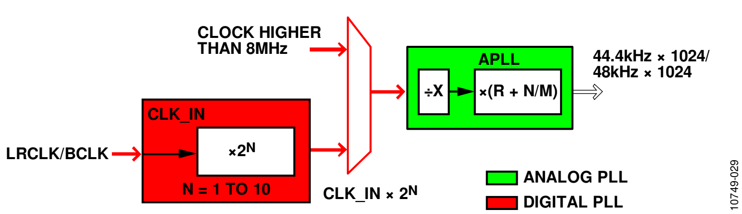

Figure 25. Clock Generation Block Diagram

PDM MODE SETUP AND CONTROL

If the ADDR pin is tied to DVDD while in standalone mode, or the PDM_MODE bit (Register 0x01, Bit 7) is set to 1 while in I²C mode, the SSM2529 operates in PDM mode. In PDM mode, the SDATA pin receives the 1-bit PDM input to the DAC, and the BCLK pin provides the system clock for registering the input data. The PDM data input is registered directly on each clock edge.

The left or right data can be registered on either the rising or falling BCLK edge in both standalone mode or in I²C mode by setting the BCLK_EDGE bit (Register 0x03, Bit 0).

When the part is in standalone mode and the PDM interface is selected, pull the MCLK pin to logic level low to register the left channel data (L data) on the rising BCLK edge, and the right channel data (R data) on the falling BCLK edge. When the MCLK pin is connected to logic high, the R data is registered on the rising BCLK edge, and the L data is registered on the falling BCLK edge.

When this part is in I²C PDM mode, if BCLK_EDGE = 0, the L data is registered on the rising BCLK edge and the R data is registered on the falling BCLK edge. If BCLK_EDGE = 1, the L data is registered on the falling BCLK edge, and the R data is registered on the rising BCLK edge.

Table 9. PDM Timing Parameters

Parameter	Limit T_{MIN}	T_{MAX}	Unit	Description
t_{FALL}		10	ns	Clock fall time
t_{RISE}		10	ns	Clock rise time
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	7		ns	Data hold time

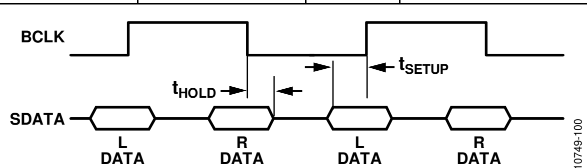

Figure 26. PDM Input Format

HIGH-PASS FILTER

The audio processing block contains a configurable first-order, high-pass filter. When the high-pass filter is enabled, the dc values are continuously calculated and subtracted from the input signal. By setting HPFOR (Register 0x15, Bit 1), the last calculated dc value is stored. When the high-pass filter is disabled, the stored value is still subtracted from the input signal until the HPFOR is cleared to 0.

The high-pass filter can work in audio mode or application mode, as configured by the HPF_CTRL register. In audio mode, the high-pass filter's 3 dB cutoff frequency is 3.7 Hz when the sampling rate is 48 kHz. In application mode, the 3 dB cutoff frequency varies from 50 Hz to 750 Hz, which is selected by using the HPFCUT bits (Register 0x15, Bits[5:2]).

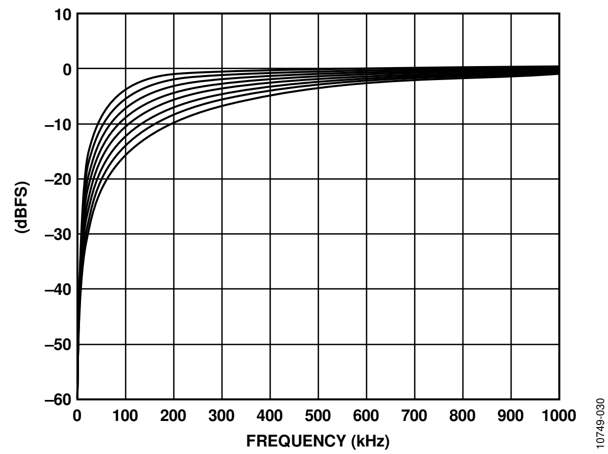

Figure 27. High-Pass Filter Response from HPFCUT Adjustment

Table 10. HPF_CTRL Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved		HPFCUT				HPFOR	HPFEN

Table 11. Bit Description of HPF_CTRL Register

Bit Name	Description	Settings
HPFCUT[3:0]	HPF cut-off frequency selection	See the Table 66
HPFOR	HPF mode selection	0: audio mode (cutoff frequency is 3.7 Hz) 1: application mode (cut-off frequency selectable)
HPFEN	HPF enable	0: disable 1: enable

FULLY PROGRAMMABLE SEVEN-BAND EQUALIZER

The programmable seven-band equalizer comprises five biquad filters (Band 1 to Band 5) and two first-order IIR filters (Band 6 and Band 7). Figure 28 shows the system block diagram.

All filter coefficients are programmable via the corresponding registers. When not all five midfrequency bands are needed, the filter bank can be configured as other filters, such as de-emphasis and notch filters.

To operate as a seven-band equalizer, the two first-order IIR filters are usually configured as one low-pass shelving filter and one high-pass shelving filter, and the biquad filters are configured as peak filters. By using the coefficient registers, the cutoff frequencies and peak gains of the shelving filters and the center frequencies and bandwidths of the peak filters are programmable. For frequency bands lower than 200 Hz, the low-pass shelving filter is suggested.

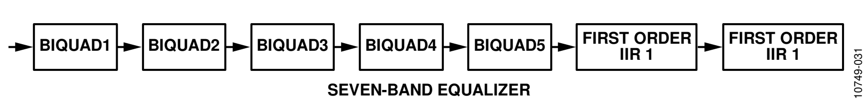

Figure 28. System Block Diagram

The common biquad filter transfer function is

$$H(z)=\frac{P0+P1\times Z^{-1}+P2\times Z^{-2}}{1-D1\times Z^{-1}-D2\times Z^{-2}}$$

The first-order IIR filter transfer function is

$$H(z)=\frac{P0+P1\times Z^{-1}}{1-D1\times Z^{-1}}$$

In normal mode, the supported coefficients range from −4 to approximately +4. For equalizer mode, this range means that the cutoff and center frequencies can vary from 40 Hz to 12 kHz when the input sampling rate is 48 kHz, and the peak gain varies from −18 dB to +18 dB.

The EQ_FORMAT bit in Register 0x54 defines the coefficient format. The default value is 0, and the corresponding format is Q3.13. Setting this bit to 1 achieves a larger coefficient range (from −8 to approximately +8), which enables a larger gain boost or decreases the range.

Online coefficient update is supported. If the filter bank coefficients are updated when the EQ is operating, set the EQ_UPD bit after the coefficient is written. The coefficient update procedure requires approximately 0.05 ms to complete. The read only bit, EQ_UPDING, in the EQ_CTRL1 register represents the coefficient update status. If the system clock is removed during this period, the update procedure cannot be finished, and the EQ_UPD_CLR bit must be set to cancel this update.

The filter bank can be disabled, and all seven bands can be bypassed separately to save power. The corresponding bits are EQEN and EQBP1 to EQBP7 in Register 0x55.

Table 12. EQ Coefficients Registers

Register Address	Register Name	Description
0x16	EQ1_COEF0_HI[15:8]	EQ Band 1, Coefficient 0 MSB
0x17	EQ1_COEF0_LO[7:0]	EQ Band 1, Coefficient 0 LSB
0x18	EQ1_COEF1_HI[15:8]	EQ Band 1, Coefficient 1 MSB
0x19	EQ1_COEF1_LO[7:0]	EQ Band 1, Coefficient 1 LSB
0x1A	EQ1_COEF2_HI[15:8]	EQ Band 1, Coefficient 2 MSB
0x1B	EQ1_COEF2_LO[7:0]	EQ Band 1, Coefficient 2 LSB
...	...	...
0x52	EQ7_COEF2_HI[15:8]	EQ Band 7, Coefficient 2 MSB
0x53	EQ7_COEF2_LO[7:0]	EQ Band 7, Coefficient 2 LSB

Table 13. EQ_CTRL1 Register

D7	D6	D5	D4	D3	D2	D1	D0
EQ_RESERVED				EQ_ UPDING	EQ_UPD_ CLR	EQ_ FORMAT	EQ_ UPD

Table 14. Bit Description of EQ_CTRL1 Register

Bit Name	Description	Settings
EQ_RESERVED	Reserved	
EQ_UPDING	EQ coefficient updating flag	0: EQ coefficients updating 1: None
EQ_UPD_CLR	EQ coefficient update clear	0: normal operation 1: interrupt coefficient update
EQ_FORMAT	EQ coefficient format selection	0: normal 1: large gain
EQ_UPD	EQ coefficient registers update flag	1: update 0: none

Table 15. EQ_CTRL2 Register

D7	D6	D5	D4	D3	D2	D1	D0
EQEN	EQBP7	EQBP6	EQBP5	EQBP4	EQBP3	EQBP2	EQBP1

Table 16. Bit Description of EQ_CTRL2 Register

Bit Name	Description	Settings
EQEN	EQ enabled	0: EQ disabled 1: EQ enabled
EQBP7	EQ Band 7 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 7
EQBP6	EQ Band 6 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 6
EQBP5	EQ Band 5 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 5
EQBP4	EQ Band 4 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 4
EQBP3	EQ Band 3 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 3
EQBP2	EQ Band 2 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 2
EQBP1	EQ Band 1 bypass when EQ enabled	0: no bypass 1: bypass EQ Band 1

The typical characteristic of each EQ band is shown in Figure 29 to Figure 36.

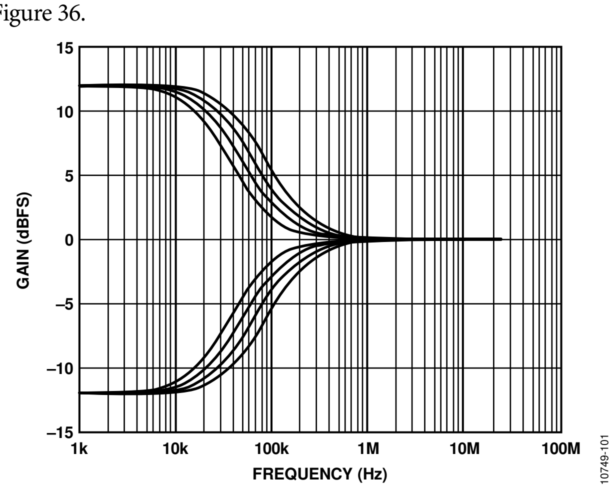

Figure 29. Low-Pass Shelving Filter Frequency Response Across Bandwidth Settings

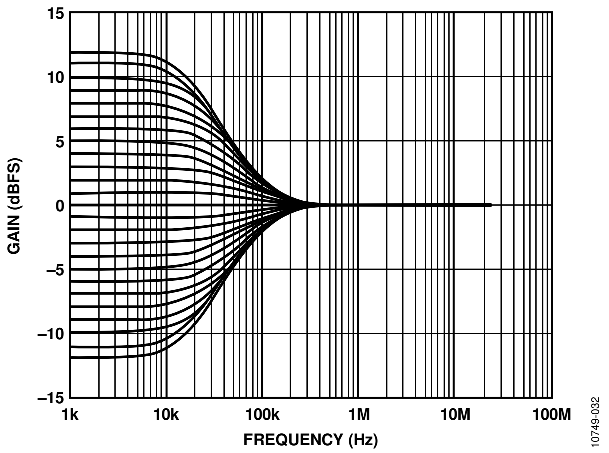

Figure 30. Low-Pass Shelving Filter Frequency Response Across Gain Settings

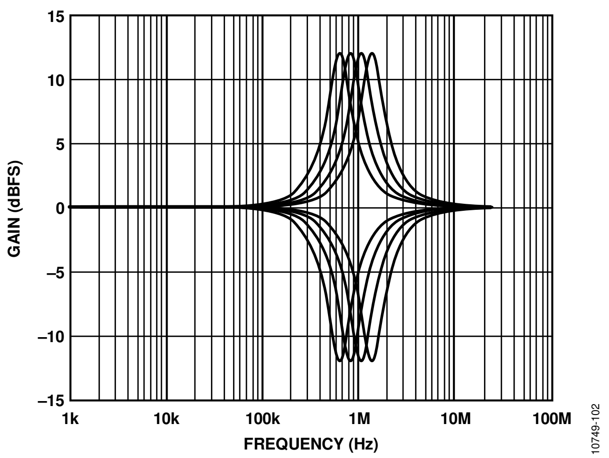

Figure 31. Peak Filter Frequency Response with Different Center Frequencies

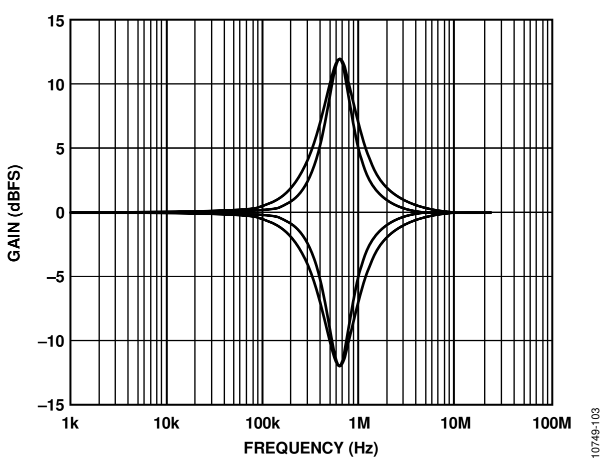

Figure 32. Peak Filter Frequency Response Across Bandwidth Settings

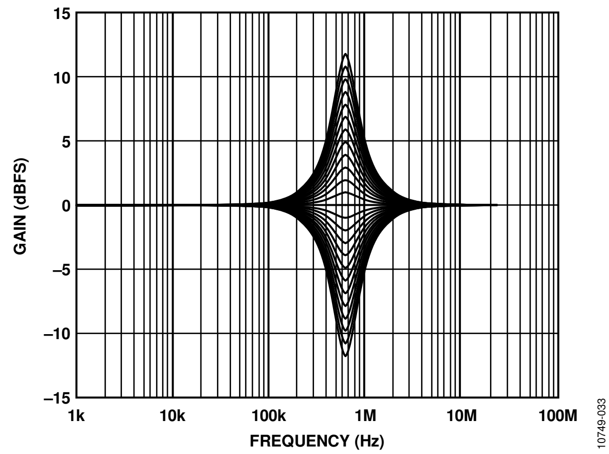

Figure 33. Peak Filter Frequency Response Across Gain Settings

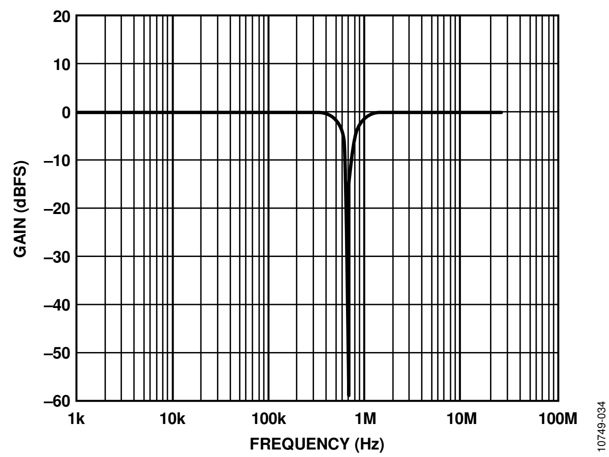

Figure 34. Notch Filter Response (A0 = +1982 to +2048, A1 = −2041 to +2048, Bandwidth = 251 Hz, Center Frequency = 631 Hz)

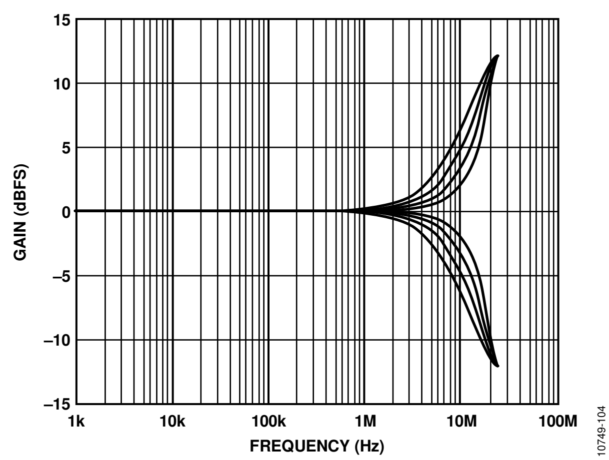

Figure 35. Treble Band Frequency Response Across Bandwidth Settings

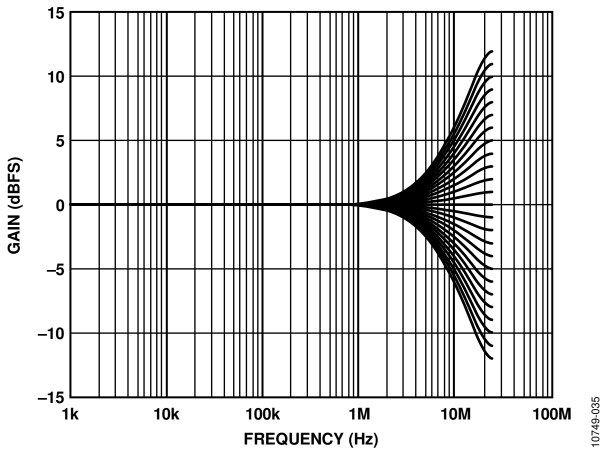

Figure 36. Treble Band Frequency Response Across Gain Settings

DYNAMIC RANGE CONTROL

The dynamic range control function is used to alter (usually reduce) the dynamic range of the audio signal so that a loud signal can be heard without disturbing the hearing perception, and a weak signal can still be heard. In addition, very large signals and very weak signals are usually treated with different methods to ensure the overall sound quality. The DRC functions include the following:

- Limiter
- Compressor
- Expander
- Noise Gate

The dynamic range is not altered when the signal level is in the middle. These functions can be enabled or disabled individually.

Limiter

If the input audio samples are large, the output is clipped at a predefined level so that the speakers are not overdriven.

If the ADC power tracking function is enabled, the maximum output level is set automatically to correspond to the speaker SPKVDD power.

Compressor

The compressor is used to reduce the signal dynamic range when the input level is large and within predefined boundaries. This helps reduce the loudness when the signal level is high.

Expander

The expander is used to increase the signal dynamic range when the input signal level is small and within predefined upper and lower boundaries. This helps increase the loudness when the signal is weak.

Noise Gate

When the signal level is lower than a predefined threshold level, it is treated as noise. Under this condition, the output is set to zero.

The overall DRC characteristics are illustrated in Figure 37. A number of threshold levels (referred to the input) are used, which are defined as the limiter threshold (LT), compressor threshold (CT), expander threshold (ET), noise gate threshold (NT), maximum output signal amplitude (SMAX), and minimum output signal amplitude (SMIN). The corresponding bits are DRC_LT, DRC_CT, DRC_ET, DRC_NT, DRC_SMAX, and DRC_SMIN and can be found in Register 0x59 to Register 0x5D.

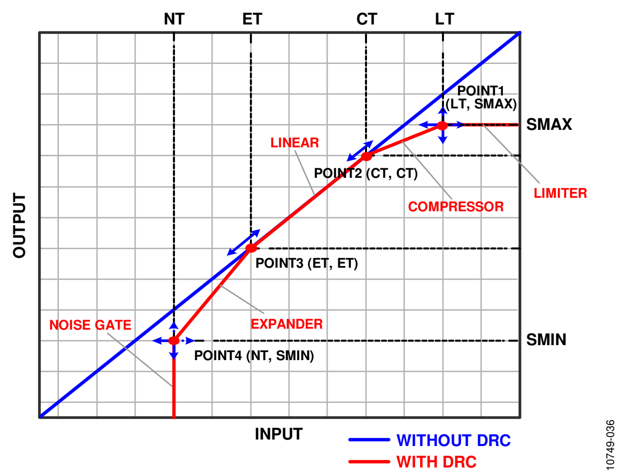

Figure 37. DRC Input/Output Relationship

DRC MODE CONTROL

The DRC_EN bits in Register 0x60 control the DRC. The noise gating function can be disabled by setting the NG_EN bit in Register 0x60.

Table 17. DRC Mode Control Register

D7	D6	D5	D4	D3	D2	D1	D0
VBAT_EN	LIM_SRC	LIM_EN	COMP_EN	EXP_EN	NG_EN	DRC_EN	

Table 18. Bit Description of DRC Mode Control Register

Bit Name	Description	Settings
VBAT_EN	VBAT tracking enabled	0: disable 1: enable
LIM_SRC	Limiter source selection	0: peak 1: RMS
LIM_EN	Limiter enabled	0: disable 1: enable
COMP_EN	Compressor disabled	0: disable 1: enable
EXP_EN	Expander enabled	0: disable 1: enable
NG_EN	Noise gating enabled	0: disable 1: enable
DRC_EN	DRC enabled	0: disable 1: enable

Figure 38 shows a high level system block diagram of the DRC function.

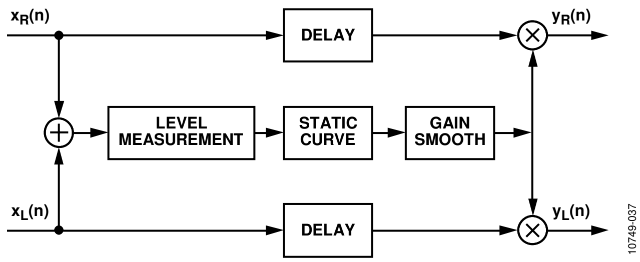

Figure 38. DRC Block Diagram

Level Measurement

The DRC level measurement includes the peak and rms value measurements. The parameters that affect the peak measurement are attack time and release time (AT and RT). The parameter that affects the rms measurement is average time (T_{AV}). The attack time can vary from 0 ms to 1.536 sec; the release time and average time can vary from 0 ms to 24.576 sec. The corresponding bits are PEAK_ATT, PEAK_REL, and DRCLELTAV and can be found in Register 0x56 and Register 0x57.

Table 19. DRC_CTRL1 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				DRCLELTAV[3:0]			

Table 20. Bit Description of DRC_CTRL1 Register

Bit Name	Description	Settings
DRCLELTAV[3:0]	DRC rms detector average time	0000: 0 ms 0001: 0.075 ms 0011: 0.30 ms (default) 1111: 24.576 sec

Table 21. DRC_CTRL2 Register

D7	D6	D5	D4	D3	D2	D1	D0
PEAK_ATT[3:0]				PEAK_REL[3:0]			

Table 22. Bit Description of DRC_CTRL2 Register

Bit Name	Description	Settings
PEAK_ATT[3:0]	DRC peak detector attack time	0000: 0 ms 0001: 0.09 ms 0010: 0.19 ms 0011: 0.37 ms 0100: 0.75 ms 0101: 1.5 ms 0110: 3.0 ms 0111: 6.0 ms … 1111: 1.536 sec
PEAK_REL[3:0]	DRC peak detector decay time	0000: 0 ms 0001: 1.5 ms 0010: 3 ms 0011: 6 ms 0100: 12 ms … 1111: 24.576 sec

Static Curve

The static curve is the DRC core function used to define the targeted input and output relationship. The role for the DRC block is to find the appropriate gain values with the various signal levels. To change the dynamic range of the original audio signal, the gain values vary with the input signal level.

An example of such a static curve is given in Figure 39, which shows the input and output signal levels. The blue line shows a linear relationship where the output dynamic range is identical to the input dynamic range. The red line shows a different output dynamic range from the input. Furthermore, this curve indicates that the signal dynamic range is larger when the input signal is low.

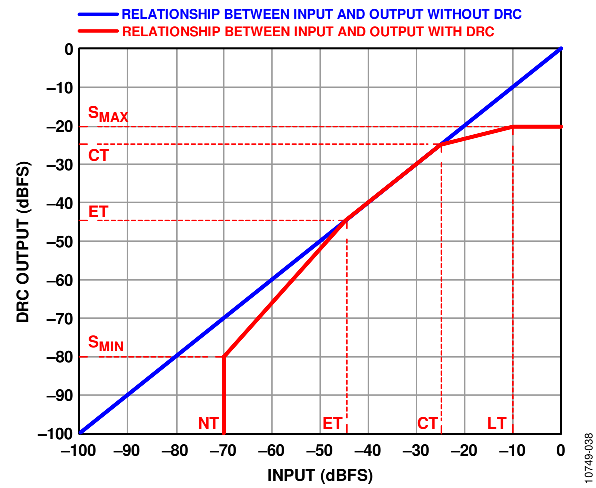

Figure 39. DRC Output vs. Input

Figure 40 shows the gain values at various input signal levels.

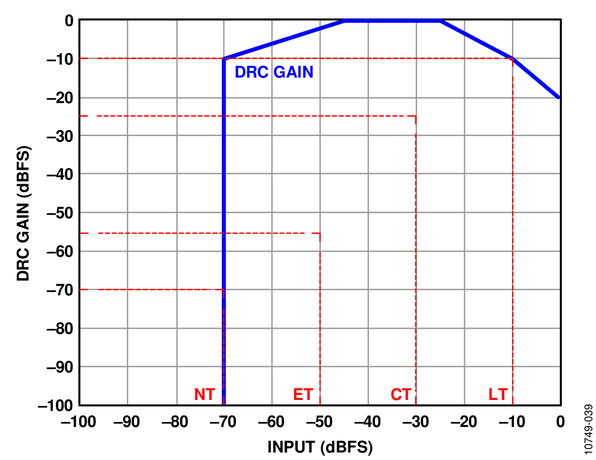

Figure 40. DRC Gain vs. Input

DRC Static Curve Function

A number of threshold levels (referred to the input) are used in Figure 39 and Figure 40; these levels are defined as the limiter threshold (LT), compressor threshold (CT), expander threshold (ET), noise gate threshold (NT), maximum output signal amplitude (SMAX), and minimum output signal amplitude (SMIN). The corresponding bits, DRC_LT, DRC_CT, DRC_ET, DRC_NT, DRC_SMAX, DRC_SMIN, can be found in Register 0x59 to Register 0x5D.

Table 23. DRC_CURVE1 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	DRC_LT[6:0]						

Table 24. Bit Description of DRC_CURVE1 Register

Bit Name	Description	Settings
DRC_LT[6:0]	DRC limiter threshold	0000000: +6 dB 0000001: +5.5 dB −0.5 dB step to 1010000: −35 dB

Table 25. DRC_CURVE2 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	DRC_CT[6:0]						

Table 26. Bit Description of DRC_CURVE2 Register

Bit Name	Description	Settings
DRC_CT[6:0]	DRC compressor threshold	0000000: +6 dB 0000001: +5.5 dB −0.5 dB step to 1010000: −35 dB

Table 27. DRC_CURVE3 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved	DRC_SMAX[6:0]						

Table 28. Bit Description of DRC_CURVE3 Register

Bit Name	Description	Settings
DRC_SMAX[6:0]	DRC maximum output signal amplitude	0000000: +6 dB 0000001: +5.5 dB −0.5 dB step to 1010000: −35 dB

Table 29. DRC_CURVE4 Register

D7	D6	D5	D4	D3	D2	D1	D0
DRC_NT[3:0]				DRC_ET[3:0]			

Table 30. Bit Description of DRC_CURVE4 Register

Bit Name	Description	Settings
DRC_NT[3:0]	DRC noise gating threshold	0000: −51 dB 0001: −54 dB −3 dB step to 1111: −96 dB
DRC_ET[3:0]	DRC expander threshold	0000: −36 dB 0001: −39 dB −3 dB step to 1111: −81 dB

Table 31. DRC_CURVE5 Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved				DRC_SMIN[3:0]			

Table 32. Bit Description of DRC_CURVE5 Register

Bit Name	Description	Settings
DRC_SMIN[3:0]	DRC minimum output signal level	0000: −51 dB 0001: −54 dB −3 dB step to 1111: −96 dB

DRC Gain Smooth

Before the gain calculated by the static curve function multiplies with the input signal, smooth it to ensure that it does not change rapidly for this can lead to noise.

The gain smooth is affected by its attack and decay time parameters. The attack time can vary from 0 ms to 1.536 sec, while the decay time can vary from 0 ms to 24.576 sec. The corresponding bits are DRC_ATT and DRC_DEC and can be found in Register 0x58.

Table 33. DRC_CTRL3 Register

D7	D6	D5	D4	D3	D2	D1	D0
DRC_ATT[3:0]				DRC_DEC[3:0]			

Table 34. Bit Description of DRC_CTRL3 Register

Bit Name	Description	Settings
DRC_ATT[3:0]	DRC attack time	0000: 0 ms 0001: 0.1 ms 0010: 0.19 ms 0011: 0.37 ms 0100: 0.75 ms 0101: 1.5 ms 0110: 3 ms 0111: 6 ms … 1111: 1.536 sec
DRC_DEC[3:0]	DRC decay time	0000: 0 ms 0001: 1.5 ms 0010: 3 ms 0011: 6 ms 0100: 12 ms … 1111: 24.576 sec

DRC Hold Time

Two types of hold time are used in the DRC. One is used in normal mode to prevent the calculated gain from increasing too quickly, and the other is used during DRC transiting from expander mode to noise gating mode to prevent the DRC from entering noise gating too quickly. The DRCHTNOR and DRCHTNG bits in Register 0x5E set which type is used.

Table 35. DRC_HOLD_TIME Register

D7	D6	D5	D4	D3	D2	D1	D0
DRCHTNG[3:0]				DRCHTNOR[3:0]			

Table 36. Bit Description of DRC_HOLD_TIME Register

Bit Name	Description	Settings
DRCHTNG[3:0]	DRC hold time for noise gating	0000: 0 ms 0001: 0.67 ms xxxx: double time 0111: 42.67 ms (default) 1111: 43.7 sec
DRCHTNOR[3:0]	DRC hold time for normal operation	0000: 0 ms 0001: 0.67 ms 0010: 1.33 ms 0011: 2.67 ms 0100: 5.33 ms …. 1111: 43.7 sec

GAIN RIPPLE REMOVE

Due to the swing of the peak/rms value detected by the level measurement, the gain to apply to the input signal has a little ripple, which leads to the modulation of the output signal. The ripple remove function suppresses this effect. The ripple threshold is defined by the DRCRRH bit in Register 0x5F.

Table 37. DRC_RIPPLE_CTRL Register

D7	D6	D5	D4	D3	D2	D1	D0
Reserved						DRCRRH[1:0]	

Table 38. Bit Description of DRC_RIPPLE_CTRL Register

Bit Name	Description	Settings
DRCRRH[1:0]	DRC ripple remove threshold	00: 0 dB 01: 0.28 dB 10: 0.47 dB 11: 0.75 dB (default)

SPEAKER PROTECTION

The IC includes a speaker temperature prediction module to protect the loudspeaker. Loudspeakers can be damaged when the voice coil overheats due to operation higher than the rated power. Typically, the thermal time constants of the loudspeakers are long, approximately 1 sec for voice coil and 60 sec for core. They can handle momentary power spikes without overheating; however, they cannot handle sustained high power. The speaker protection method used in the IC can reduce the volume when the temperature of the loudspeaker exceeds the temperature threshold set by the user while preserving the maximum power of the loudspeaker. The temperature prediction method is based on the general thermal model of the loudspeaker.

In this thermal model, R1, R2, C1, and C2 are temperature coefficients derived by measuring loudspeaker characteristics. They are set by the I²C control registers, Register 0x84 to Register 0x8B (SP_CF1_H, SP_CF1_L, SP_CF2_H, SP_CF2_L, SP_CF3_H, SP_CF3_L, SP_CF4_H and SP_CF4_L).

Other critical parameters needed include ambient temperature, dc resistance of the loudspeaker, and temperature coefficient of the voice coil material. These parameters are set by Register 0x81 to Register 0x83 (TEMP_AMBIENT, SPKR_DCR, and SPKR_TC).

After running the thermal model by setting the speaker protection enable bit (SP_EN, Register 0x80), the speaker voice coil temperature status and speaker magnet temperature status can be obtained by an I²C reading of the SPKR_TEMP register (Register 0x8C) and the SPKR_TEMP_MAG register (Register 0x8D). The user sets the voice coil temperature threshold (maximum speaker voice coil temperature before gain reduction occurs) by using the MAX_SPKR_TEMP register (Register 0x8E). If this threshold is crossed, the output volume is reduced according to the speed set by the SP_AR bits (speaker protection gain reduction attack rate, Register 0x8F, Bits[7:4]) and the SP_RR bits (speaker protection gain reduction release rate, Register 0x8F, Bits[3:0]).

POWER SUPPLIES

The SSM2529 has two internal power supplies that must be provided: SPKVDD and DVDD. The SPKVDD supply powers to the full bridge power stage of the MOSFET and its associated drive, control, and protection circuitry. SPKVDD can operate from 2.5 V to 5.5 V and must be present to obtain audio output. Lowering the SPKVDD supply results in lower output power and correspondingly lower power consumption, and it does not affect audio performance.

DVDD provides power to the digital logic and analog components. DVDD can operate from 1.08 V to 1.98 V, and it must be provided to write to the I²C or to obtain audio output. Lowering the supply voltage results in lower power consumption; however, it also results in lower audio performance.

POWER CONTROL

The SSM2529 includes various programmable power-down modes that are contained in the first I²C register (Register 0x00), power/reset control. By default, the IC is set in software power-down, which is the I²C programmable master power-down. Only I²C functionality operates when in software power-down mode.

The SSM2529 also contains a smart power-down feature that, when enabled, looks at the incoming digital audio. In addition, if the audio is zero for 1024 consecutive samples, regardless of sample rate, it puts the IC in a smart power-down state. In this state, all circuitry, except the I²S and I²C ports, are placed in a low power state. After a single nonzero input is received, the SSM2529 leaves this state and resumes normal operation.

POWER-ON RESET/VOLTAGE SUPERVISOR

The SSM2529 includes an internal power-on reset and voltage supervisor circuit. This circuit provides an internal reset to all circuitry during initial power-up. It also monitors the power supplies to the IC, and it mutes the outputs and issues a reset when the voltages are lower than the minimum operating range. This ensures that no damage due to low voltage operation occurs and that no pops can occur under nearly any power removal conditions.

STANDALONE MODE

When the SA_MODE pin is pulled high, the SSM2529 can operate without any I²C control. In this mode, the automatic sample rate detection and smart power-down are always enabled. Volume Control A and Volume Control B can be controlled via the SCL and SDA pins.

In standalone mode, the DRC function is disabled. The EQ and HPF are also disabled. When ADDR = 1, the input interface is PDM. Otherwise, I²S and TDM serial interface formats can be selected via MCLK. In standalone mode, the working clock is generated by the internal PLL.

Table 39. Standalone Mode Pin Configuration

Conventional Operation Pin	SA_MODE = 1
SCL	Volume Control A
SDA	Volume Control B
STDBN	0: shutdown/mute 1: normal operation
ADDR	1: PDM 0: I²S/TDM
BCLK	0: 16 BCLK cycles provided by PLL 1: 32 BCLK cycles provided by PLL Clock: 32 BCLK cycles provided off chip
MCLK	0: I²S (ADDR = 0) or PDM L channel (ADDR = 1) 1: TDM (ADDR = 0) or PDM R channel (ADDR = 1)

I²C PORT

The SSM2529 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the SSM2529 and the system I²C master controller. The SSM2529 is always a slave on the bus, meaning that it cannot initiate a data transfer. Each slave device is recognized by a unique address. The address byte format is shown in Table 40. The address resides in the first seven bits of the I²C write. The LSB of this byte either sets a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation The full byte addresses are shown in Figure 41, where the subaddresses are automatically incremented at word boundaries, and can be used for writing large amounts of data to contiguous memory locations. This increment happens automatically after a single-word write unless a stop condition is encountered. A data transfer is always terminated by a stop condition.

Both SDA and SCL must have a 2.2 kΩ pull-up resistor on the lines connected to them. The voltage on these signal lines must not be more than 3.6 V.

Table 40. I²C Address Byte Format

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0	1	1	0	1	0	0	$R/\overline{W}$

Addressing

Initially, each device on the I²C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high-to-low transition on SDA, while SCL remains high. This indicates that an address/data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the $R/\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. The device address for the SSM2529 is 0x34. The ninth bit is known as the acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition.

The $R/\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means that the master writes information to the peripheral, whereas a Logic 1 means that the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer takes place until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I²C port is shown in Figure 3.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM2529 immediately jumps to the idle condition. During an SCL high period, issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued, the SSM2529 does not issue an acknowledge and returns to the idle condition. If the highest subaddress is exceeded while in auto-increment mode, one of two actions is taken. In read mode, the SSM2529 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of the read. When the SDA line is not pulled low on the ninth clock pulse of SCL, a no acknowledge occurs. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM2529, and the part returns to the idle condition.

I²C Read and Write Operations

Table 42 shows the timing of a single-word write operation. Every ninth clock, the SSM2529 issues an acknowledge by pulling SDA low.

Table 43 shows the timing of a burst mode write sequence as an example where the target destination registers are two bytes. The SSM2529 knows to increment its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single-word read operation is shown in Table 44. Note that the first R/$\overline{W}$ bit is 0, indicating a write operation. This is because the subaddress still needs to be written to set up the internal address. After the SSM2529 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ bit set to 1 (read). This causes the SSM2529 SDA to reverse and begin driving data back to the master. The master then responds every ninth pulse with an acknowledge pulse to the SSM2529.

Table 42 to Table 45 use the abbreviations shown in Table 41.

Table 41. Symbols for Table 42 to Table 45

Symbol	Meaning
S	Start bit
P	Stop bit
A_M	Acknowledge by master
A_S	Acknowledge by slave

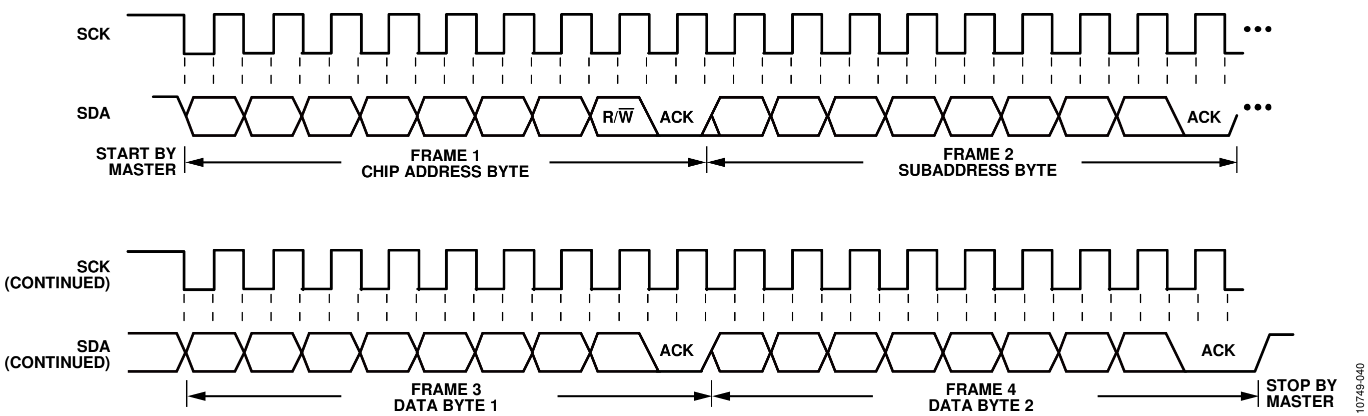

Figure 41. I²C Read and Write Timing

Table 42. Single-Word I²C Write Format

S	IC Address (7 Bits)	R/$\overline{W}$ = 0	A_S	Subaddress (8 bits)	A_S	Data Byte 1 (8 Bits)	P

Table 43. Burst Mode I²C Write Format

S	Chip address, R/$\overline{W}$ = 0	A_S	Subaddress	A_S	Data-Word 1	A_S	Data-Word 2	A_S	…	P

Table 44. Single-Word I²C Read Format

S	Chip address, R/$\overline{W}$ = 0	A_S	Subaddress	A_S	S	Chip address, R/$\overline{W}$ = 1	A_S	Data Byte 1	A_M	Data Byte N	P

Table 45. Burst Mode I²C Read Format

S	Chip address, R/$\overline{W}$ = 0	A_S	Subaddress	A_S	S	Chip address, R/$\overline{W}$ = 1	A_S	Data-Word 1	A_M	…	P

REGISTER SUMMARY

The SSM2529 contains eighteen 8-bit registers that can be accessed via the I^{2}C port. See Table 46 for the control register mapping. The register settings are described in detail in Table 47 through Table 159.

Table 46.

Hex	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
00	PWR_CTRL	[7:0]	SYS_RST	APWDN_ANA	APWDN_EN	LP_MODE	MCS			SPWDN	0x23	RW
01	SYS_CTRL	[7:0]	PDM_MODE	PDM_FS	PDB_ADC	BCLK_RATE	BCLK_GEN	EDGE		ASR	0x20	RW
02	SAI_FMT1	[7:0]	SDATA_FMT		SAI			SR			0x02	RW
03	SAI_FMT2	[7:0]	LPST	LR_SEL		LRCLK_MODE	LRCLK_POL	SAI_MSB	BCLK_TDMC	BCLK_EDGE	0x00	RW
04	Channel mapping control	[7:0]	CH_SEL_R				CH_SEL_L				0x10	RW
05	VOL_BF_FDSP	[7:0]	DIG_VOL								0x40	RW
06	VOL_AF_FDSP	[7:0]	PDP_VOL								0x40	RW
07	Volume and mute control	[7:0]	CLK_LOSS_DET	SR_AUTO			Reserved	PDP_VOL_ FORCE	DIG_VOL_ FORCE	ANA_GAIN	0x20	RW
08	DPLL_CTRL	[7:0]	Reserved	DPLL_REF_SEL			DPLL_NDIV				0x00	RW
09	APLL_CTRL1	[7:0]	M_HI								0x00	RW
0A	APLL_CTRL2	[7:0]	M_LO								0x00	RW
0B	APLL_CTRL3	[7:0]	N_HI								0x00	RW
0C	APLL_CTRL4	[7:0]	N_LO								0x00	RW
0D	APLL_CTRL5	[7:0]	Reserved	R				X		Type	0x00	RW
0E	APLL_CTRL6	[7:0]	FSYS_DPLL		DPLL_BYPASS	APLL_BYPASS	DPLL_LOCK	APLL_LOCK	PLLEN	COREN	0x30	RW
0F	FAULT_CTRL1	[7:0]	Reserved			PDB_LINE	PDB_ZC	CLK_LOSS	OC	OT	0x000	RW
10	FAULT_CTRL2	[7:0]	Reserved	AR_TIME		MRCV	MAX_AR		ARCV		0x4C	RW
14	DEEMP_CTRL	[7:0]	Reserved					DEEMP_FS		DEEMP_EN	0x00	RW
15	HPF_CTRL	[7:0]	Reserved		HPFCUT				HPFOR	HPFEN	0x00	RW
16	EQ1_COEF0_HI	[7:0]	EQ1_COEF0_HI								0x00	RW
17	EQ1_COEF0_LO	[7:0]	EQ1_COEF0_LO								0x00	RW
18	EQ1_COEF1_HI	[7:0]	EQ1_COEF1_HI								0x00	RW
19	EQ1_COEF1_LO	[7:0]	EQ1_COEF1_LO								0x00	RW
1A	EQ1_COEF2_HI	[7:0]	EQ1_COEF2_HI								0x00	RW
1B	EQ1_COEF2_LO	[7:0]	EQ1_COEF2_LO								0x00	RW
1C	EQ1_COEF3_HI	[7:0]	EQ1_COEF3_HI								0x00	RW
1D	EQ1_COEF3_LO	[7:0]	EQ1_COEF3_LO								0x00	RW
1E	EQ1_COEF4_HI	[7:0]	EQ1_COEF4_HI								0x00	RW
1F	EQ1_COEF4_LO	[7:0]	EQ1_COEF4_LO								0x00	RW
20	EQ2_COEF0_HI	[7:0]	EQ2_COEF0_HI								0x00	RW
21	EQ2_COEF0_LO	[7:0]	EQ2_COEF0_LO								0x00	RW
22	EQ2_COEF1_HI	[7:0]	EQ2_COEF1_HI								0x00	RW
23	EQ2_COEF1_LO	[7:0]	EQ2_COEF1_LO								0x00	RW
24	EQ2_COEF2_HI	[7:0]	EQ2_COEF2_HI								0x00	RW
25	EQ2_COEF2_LO	[7:0]	EQ2_COEF2_LO								0x00	RW
26	EQ2_COEF3_HI	[7:0]	EQ2_COEF3_HI								0x00	RW
27	EQ2_COEF3_LO	[7:0]	EQ2_COEF3_LO								0x00	RW
28	EQ2_COEF4_HI	[7:0]	EQ2_COEF4_HI								0x00	RW
29	EQ2_COEF4_LO	[7:0]	EQ2_COEF4_LO								0x00	RW
2A	EQ3_COEF0_HI	[7:0]	EQ3_COEF0_HI								0x00	RW
2B	EQ3_COEF0_LO	[7:0]	EQ3_COEF0_LO								0x00	RW
2C	EQ3_COEF1_HI	[7:0]	EQ3_COEF1_HI								0x00	RW
2D	EQ3_COEF1_LO	[7:0]	EQ3_COEF1_LO								0x00	RW
2E	EQ3_COEF2_HI	[7:0]	EQ3_COEF2_HI								0x00	RW
2F	EQ3_COEF2_LO	[7:0]	EQ3_COEF2_LO								0x00	RW
30	EQ3_COEF3_HI	[7:0]	EQ3_COEF3_HI								0x00	RW
31	EQ3_COEF3_LO	[7:0]	EQ3_COEF3_LO								0x00	RW
32	EQ3_COEF4_HI	[7:0]	EQ3_COEF4_HI								0x00	RW
33	EQ3_COEF4_LO	[7:0]	EQ3_COEF4_LO								0x00	RW
34	EQ4_COEF0_HI	[7:0]	EQ4_COEF0_HI								0x00	RW
35	EQ4_COEF0_LO	[7:0]	EQ4_COEF0_LO								0x00	RW
36	EQ4_COEF1_HI	[7:0]	EQ4_COEF1_HI								0x00	RW