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HMCAD1510

v03.0711

HIGH SPEED MULTI-MODE 8-BIT 30 TO 500 MSPS A/D CONVERTER

Features

- 8-bit High Speed Single/ Dual/ Quad ADC
  Single Channel Mode: FSmax = 500 MSPS
  Dual Channel Mode: FSmax = 250 MSPS
  Quad Channel Mode: FSmax = 125 MSPS
- Integrated Cross Point Switches (Mux Array)
- 1X to 50X Digital Gain.
  No Missing Codes up to 32X
- 1X Gain: 49.8 dB SNR. 10X Gain: 48 dB SNR
- Internal Low Jitter Programmable Clock Divider
- Ultra Low Power Dissipation
  295 mW Including I/O at 500 MSPS
  and Reduced Bias
- 0.5 µs Start-up Time From Sleep,
  15 µs From Power Down
- Internal Reference Circuitry with no
  External Components Required
- Coarse and Fine Gain Control
- Digital Fine Gain Adjustment for each ADC
- Internal Offset Correction
- 1.8V Supply Voltage
- 1.7 - 3.6V CMOS Logic on Control Interface Pins
- Serial LVDS/RSDS Output
- 7 x 7 mm QFN 48 (LP7D) Package

Typical Applications

- USB Powered Oscilloscopes
- Digital Oscilloscopes
- Satellite Receivers

Pin compatible parts

- HMCAD1510 is pin compatible with HMCAD1511 and HMCAD1520

Functional Diagram

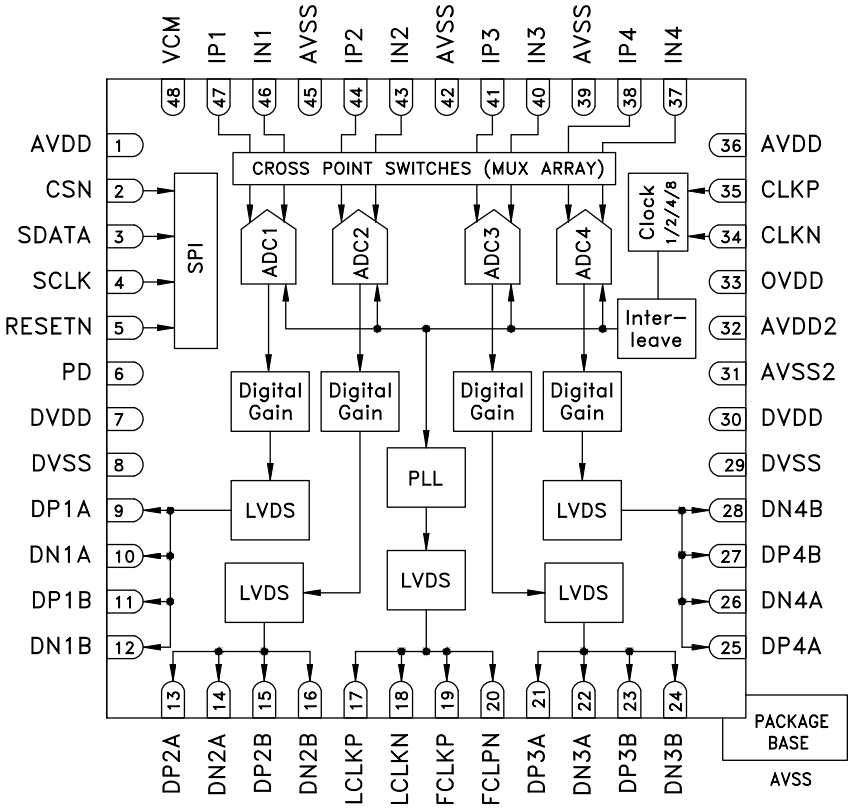

Figure 1. Functional Block Diagram

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- HMCAD1510 Evaluation Board

DOCUMENTATION

Data Sheet

- HMCAD1510 Data Sheet

REFERENCE MATERIALS

Quality Documentation

- HMC Legacy PDN: PCN140115-A
- Semiconductor Qualification Test Report: CMOS-C (QTR: 2013-00139)

DESIGN RESOURCES

- HMCAD1510 Material Declaration
- PCN-PDN Information
- Quality And Reliability
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HIGH SPEED MULTI-MODE 8-BIT 30 TO 500 MSPS A/D CONVERTER

General Description

The HMCAD1510 is a versatile high performance low power analog-to-digital converter (ADC), utilizing time-interleaving to increase sampling rate. Integrated Cross Point Switches activate the input selected by the user.

In single channel mode, one of the four inputs can be selected as a valid input to the single ADC channel. In dual channel mode, any two of the four inputs can be selected to each ADC channel. In quad channel mode, any input can be assigned to any ADC channel.

An internal, low jitter and programmable clock divider makes it possible to use a single clock source for all operational modes.

The HMCAD1510 is based on a proprietary structure, and employs internal reference circuitry, a serial control interface and serial LVDS/RSDS output data. Data and frame synchronization clocks are supplied for data capture at the receiver. Internal 1 to 50X digital coarse gain with ENOB > 7.5 up to 16X gain, allows digital implementation of oscilloscope gain settings. Internal digital fine gain can be set separately for each ADC to calibrate for gain errors.

Various modes and configuration settings can be applied to the ADC through the serial control interface (SPI). Each channel can be powered down independently and data format can be selected through this interface. A full chip idle mode can be set by a single external pin. Register settings determine the exact function of this pin.

HMCAD1510 is designed to easily interface with Field Programmable Gate Arrays (FPGAs) from several vendors.

Electrical Specifications

DC Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, FS = 125 MSPS, Quad Channel Mode, 50% clock duty cycle, -1 dBFS 70 MHz input signal, 1x/0 dB digital gain (fine and coarse), unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
DC accuracy					
No missing codes		Guaranteed			
Offset	Offset error after internal digital offset correction		0.05		LSB
G_{abs}	Gain error			±6	%FS
G_{rel}	Gain matching between channels. ±3 sigma value at worst case conditions		±0.5		%FS
DNL	Differential non linearity		±0.2		LSB
INL	Integral non linearity		±0.5		LSB
$V_{CM,out}$	Common mode voltage output		$V_{AVDD}/2$		
Analog Input					
$V_{CM,in}$	Analog input common mode voltage	V_{CM} -0.1		V_{CM} +0.2	V
FSR	Differential input voltage full scale range		2		Vpp
$C_{in,Q}$	Differential input capacitance, Quad channel mode		5		pF
$C_{in,D}$	Differential input capacitance, Dual channel mode		7		pF
$C_{in,S}$	Differential input capacitance, Single channel mode		11		pF
Power Supply					
V_{AVDD}	Analog Supply Voltage	1.7	1.8	2	V
V_{DVDD}	Digital and output driver supply voltage	1.7	1.8	2	V
V_{OVDD}	Digital CMOS Input Supply Voltage	1.7	1.8	3.6	V
Temperature					
T_A	Operating free-air temperature	-40		85	°C

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AC Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50% clock duty cycle, -1dBFS 70 MHz input signal, Gain = 1X, ADC current scaling -40%, RSDS output data levels unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Performance					
SNR	Signal to Noise Ratio, excluding interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS	48.5	49.9		dBFS
	Single Ch Mode , F_S = 500 MSPS, Gain = 10X		48		dBFS
	Dual Ch Mode , F_S = 250 MSPS	48.5	49.8		dBFS
	Quad Ch Mode , F_S = 125 MSPS	48.5	49.7		dBFS
$SINAD_{incl}$	Signal to Noise and Distortion Ratio, including interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS		47		dBFS
	Dual Ch Mode , F_S = 250 MSPS		49.5		dBFS
	Quad Ch Mode , F_S = 125 MSPS		49.6		dBFS
$SINAD_{excl}$	Signal to Noise and Distortion Ratio, excluding interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS	48	49.4		dBFS
	Single Ch Mode , F_S = 500 MSPS, Gain = 10X		47.7		dBFS
	Dual Ch Mode , F_S = 250 MSPS	48	49.5		dBFS
	Quad Ch Mode , F_S = 125 MSPS	48	49.6		dBFS
$SFDR_{incl}$	Spurious Free Dynamic Range, including interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS		49		dBc
	Dual Ch Mode , F_S = 250 MSPS		59		dBc
	Quad Ch Mode , F_S = 125 MSPS		60		dBc
$SFDR_{excl}$	Spurious Free Dynamic Range, excluding interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS	56	65		dBc
	Single Ch Mode , F_S = 500 MSPS, Gain = 10X		65		dBc
	Dual Ch Mode , F_S = 250 MSPS	60	69		dBc
	Quad Ch Mode , F_S = 125 MSPS	60	69		dBc
HD2/3	Worst of HD2/HD3				
	Single Ch Mode , F_S = 500 MSPS	60	67		dBc
	Single Ch Mode , F_S = 500 MSPS, Gain = 10X		65		dBc
	Dual Ch Mode , F_S = 250 MSPS	60	70		dBc
	Quad Ch Mode , F_S = 125 MSPS	60	70		dBc
$ENOB_{excl}$	Effective number of Bits, excluding interleaving spurs				
	Single Ch Mode , F_S = 500 MSPS		7.9		bits
	Single Ch Mode , F_S = 500 MSPS, Gain = 10X		7.6		bits
	Dual Ch Mode , F_S = 250 MSPS		7.9		bits
	Quad Ch Mode , F_S = 125 MSPS		7.9		bits
$X_{tlk,2}$	CrossTalk Dual Ch Mode. Signal applied to 1 channel (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		65		dBc
$X_{tlk,4}$	CrossTalk Quad Ch Mode. Signal applied to 1 channel (F_{IN0}). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		70		dBc
$X_{tlk,4}$	CrossTalk Quad Ch Mode. Signal applied to 1 channel (FIN0). Measurement taken on one channel with full scale at F_{IN1}. F_{IN1} = 71 MHz, F_{IN0} = 70 MHz		70		dBc
Power Supply	Single Ch: F_S = 500 MSPS, Dual Ch: F_S = 250 MSPS, Quad Ch: F_S = 125 MSPS.				
I_{AVDD}	Analog Supply Current		99		mA
I_{DVDD}	Digital and output driver Supply Current		65		mA
P_{AVDD}	Analog Power		178		mW
P_{DVDD}	Digital Power		117		mW
P_{TOT}	Total Power Dissipation		295		mW

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HIGH SPEED MULTI-MODE 8-BIT 30 TO 500 MSPS A/D CONVERTER

AC Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, 50% clock duty cycle, -1dBFS 70 MHz input signal, Gain = 1X, ADC current scaling -40%, RSDS output data levels unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
P_{PD}	Power Down Mode dissipation		15		µW
P_{SLP}	Deep sleep Mode power dissipation		49		mW
P_{SLPCH}	Power dissipation with all channels in sleep channel mode (Light sleep)		67		mW
P_{SLPCH_SAV}	Power dissipation savings per channel off (Quad Channel mode)		57		mW
Analog Input					
F_{PBW}	Full Power Bandwidth		500		MHz
Clock Inputs					
F_{smax}	Max. Conversion Rate in Modes: Single Ch Dual Ch / Quad Ch	500 / 250 / 125			MSPS
F_{smin}	Min. Conversion Rate in Modes: Single Ch Dual Ch / Quad Ch			120 / 60 / 30	MSPS

Digital and Switching Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
Clock Inputs					
DC	Duty Cycle	45		55	% high
Compliance	LVDS supported up to 700 MHz	LVPECL, Sine wave, CMOS, LVDS			
$V_{CK,sine}$	Differential input voltage swing, sine wave clock input	1500			mVpp
$V_{CK,CMOS}$	Voltage input range CMOS (CLKN connected to ground)		V_{OVDD}		
$V_{CM,CK}$	Input common mode voltage. Keep voltages within ground and voltage of OVDD	0.3		V_{OVDD} -0.3	V
C_{CK}	Differential Input capacitance		3		pF
Logic inputs (CMOS)					
V_{HI}	High Level Input Voltage. $V_{OVDD} \geq 3.0V$	2			V
V_{HI}	High Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0.8 ·V_{OVDD}			V
V_{LI}	Low Level Input Voltage. $V_{OVDD} \geq 3.0V$	0		0.8	V
V_{LI}	Low Level Input Voltage. V_{OVDD} = 1.7V – 3.0V	0		0.2 ·V_{OVDD}	V
I_{HI}	High Level Input leakage Current			+/-10	µA
I_{LI}	Low Level Input leakage Current			+/-10	µA
C_I	Input Capacitance		3		pF
Data Outputs					
Compliance		LVDS / RSDS			
V_{OUT}	Differential output voltage, LVDS		350		mV
V_{OUT}	Differential output voltage, RSDS		150		mV
V_{CM}	Output common mode voltage		1.2		V
Output coding	Default/optional	Offset Binary/ 2's complement			
Timing Characteristics					
t_A	Aperture delay		1.5		ns
t_j	Aperture jitter, One bit set to '1' in jitter_ctrl<7:0>		160		fsrms
T_{skew}	Timing skew between ADC channels		2.5		psrms

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Digital and Switching Specifications

AVDD = 1.8V, DVDD = 1.8V, OVDD = 1.8V, RSDS output data levels, unless otherwise noted

Parameter	Description	Min	Typ	Max	Unit
T_{SU}	Start up time from Power Down Mode and Deep Sleep Mode to Active Mode in µs. See section "Clock Frequency" for details.		15		µs
T_{SLPCH}	Start up time from Sleep Channel Mode to Active Mode				µs
T_{OVR}	Out of range recovery time		1		clock cycles
$T_{LATHSMQ}$	Pipeline delay, Quad Channel Mode		32		clock cycles
$T_{LATHSMD}$	Pipeline delay, Dual Channel Mode		64		clock cycles
$T_{LATHSMS}$	Pipeline delay, Single Channel Mode		128		clock cycles
LVDS Output Timing Characteristics					
t_{data}	LCLK to data delay time (excluding programmable phase shift)		50		ps
T_{PROP}	Clock propagation delay.	$6*T_{LVDS}$ +2.2	$7*T_{LVDS}$ +3.5	$7*T_{LVDS}$ +5.0	ns
	LVDS bit-clock duty-cycle	45		55	% LCLK cycle
	Frame clock cycle-to-cycle jitter			2.5	% LCLK cycle
T_{EDGE}	Data rise- and fall time 20% to 80%		0.7		ns
$T_{CLKEDGE}$	Clock rise- and fall time 20% to 80%		0.7		ns

Table 1: Maximum Voltage Ratings

Pin	Reference pin	Rating
AVDD	AVSS	-0.3V to +2.3V
DVDD	DVSS	-0.3V to +2.3V
OVDD	AVSS	-0.3V to +3.9V
AVSS / DVSS	DVSS / AVSS	-0.3V to +0.3V
Analog inputs and outputs	AVSS	-0.3V to +2.3V
CLKx	AVSS	-0.3V to +3.9V
LVDS outputs	DVSS	-0.3V to +2.3V
Digital inputs	DVSS	-0.3V to +3.9V

Applying voltages to the pins beyond those specified in Table 1 could cause permanent damage to the circuit.

Table 2: Maximum Temperature Ratings

Operating Temperature	-40 to +85 °C
Storage Temperature	-60 to +150 °C
Maximum Junction Temperature	110 °C
Thermal Resistance (Rth)	29 °C/W
Soldering Profile Qualification	J-STD-020
ESD Sensivity HBM	Class 1C
ESD Sensivity CDM	Class III

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Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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HIGH SPEED MULTI-MODE 8-BIT 30 TO 500 MSPS A/D CONVERTER

Pin Configuration and Description

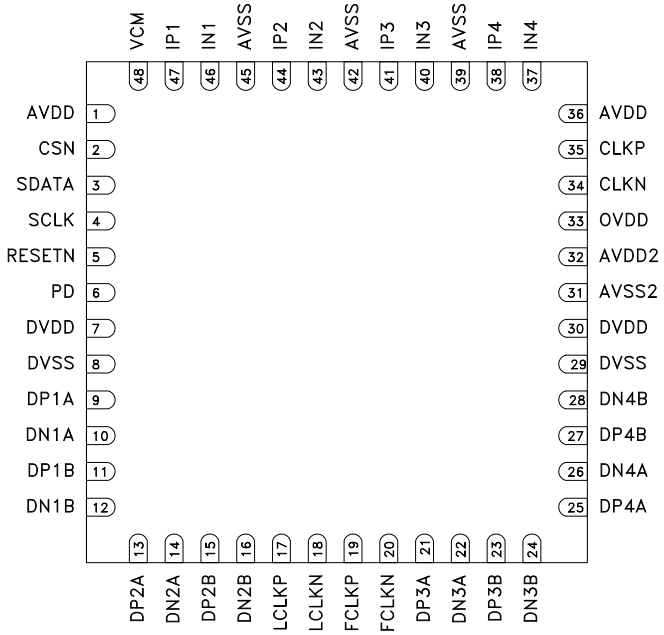

Figure 2: Package diagram

Table 3: Pin descriptions

Pin Name	Description	Pin Number	# Of Pins
AVDD	Analog power supply, 1.8V	1, 36	2
CSN	Chip select enable. Active low	2	1
SDATA	Serial data input	3	1
SCLK	Serial clock input	4	1
RESETN	Reset SPI interface. Active low	5	1
PD	Power-down input. Activate after applying power in order to initialize the ADC correctly. Alternatively use the SPI power down feature	6	1
DVDD	Digital and I/O power supply, 1.8V	7, 30	2
DVSS	Digital ground	8, 29	2
DP1A	LVDS channel 1A, positive output	9	1
DN1A	LVDS channel 1A, negative output	10	1
DP1B	LVDS channel 1B, positive output	11	1
DN1B	LVDS channel 1B, negative output	12	1
DP2A	LVDS channel 2A, positive output	13	1
DN2A	LVDS channel 2A, negative output	14	1
DP2B	LVDS channel 2B, positive output	15	1
DN2B	LVDS channel 2B, negative output	16	1
LCLKP	LVDS bit clock, positive output	17	1
LCLKN	LVDS bit clock, negative output	18	1
FCLKP	LVDS frame clock (1X), positive output	19	1
FCLKN	LVDS frame clock (1X), negative output	20	1
DP3A	LVDS channel 3A, positive output	21	1
DN3A	LVDS channel 3A, negative output	22	1
DP3B	LVDS channel 3B, positive output	23	1

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Table 3: Pin descriptions

Pin Name	Description	Pin Number	# Of Pins
DN3B	LVDS channel 3B, negative output	24	1
DP4A	LVDS channel 4A, positive output	25	1
DN4A	LVDS channel 4A, negative output	26	1
DP4B	LVDS channel 4B, positive output	27	1
DN4B	LVDS channel 4B, negative output	28	1
AVSS2	Analog ground domain 2	31	1
AVDD2	Analog power supply domain 2, 1.8V	32	1
OVDD	Digital CMOS Inputs supply voltage	33	1
CLKN	Negative differential input clock.	34	1
CLKP	Positive differential input clock	35	1
IN4	Negative differential input signal, channel 4	37	1
IP4	Positive differential input signal, channel 4	38	1
AVSS	Analog ground	39, 42, 45	3
IN3	Negative differential input signal, channel 3	40	1
IP3	Positive differential input signal, channel 3	41	1
IN2	Negative differential input signal, channel 2	43	1
IP2	Positive differential input signal, channel 2	44	1
IN1	Negative differential input signal, channel 1	46	1
IP1	Positive differential input signal, channel 1	47	1
VCM	Common mode output pin, 0.5*AVDD	48	1

Start up Initialization

As part of the HMCAD1510 power-on sequence both a reset and a power down cycle have to be applied to ensure correct start-up initialization. Make sure that the supply voltages are properly settled before the start up initialization is being performed. Reset can be done in one of two ways:

1. By applying a low-going pulse (minimum 20 ns) on the RESETN pin (asynchronous).
2. By using the serial interface to set the ‘rst’ bit high. Internal registers are reset to default values when this bit is set. The ‘rst’ bit is self-reset to zero. When using this method, do not apply any low-going pulse on the RESETN pin.

Power down cycling can be done in one of two ways:

1. By applying a high-going pulse (minimum 20 ns) on the PD pin (asynchronous).
2. By cycling the ‘pd’ bit in register 0Fhex to high (reg value ‘0200’hex) and then low (reg value ‘0000’hex).

Serial Interface

The HMCAD1510 configuration registers can be accessed through a serial interface formed by the pins SDATA (serial interface data), SCLK (serial interface clock) and CSN (chip select, active low). The following occurs when CSN is set low:

- Serial data are shifted into the chip
- At every rising edge of SCLK, the value present at SDATA is latched
- SDATA is loaded into the register every 24th rising edge of SCLK

Multiples of 24-bit words data can be loaded within a single active CSN pulse. If more than 24 bits are loaded into SDATA during one active CSN pulse, only the first 24 bits are kept. The excess bits are ignored. Every 24-bit word is

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divided into two parts:

- The first eight bits form the register address
- The remaining 16 bits form the register data

Acceptable SCLK frequencies are from 20MHz down to a few hertz. Duty-cycle does not have to be tightly controlled.

Timing Diagram

Figure 3 shows the timing of the serial port interface. Table 4 explains the timing variables used in figure 3.

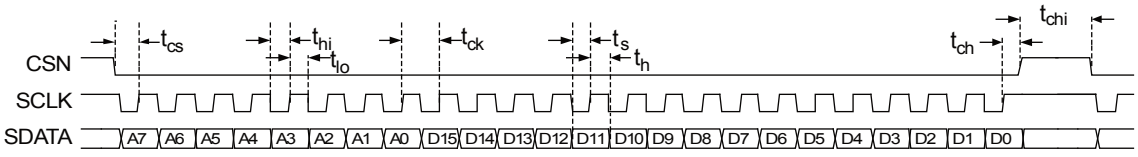

Figure 3: Serial Port Interface timing

Table 4: Serial Port Interface Timing Definitions

Parameter	Description	Minimum value	Unit
t_{cs}	Setup time between CSN and SCLK	8	ns
t_{ch}	Hold time between CSN and SCLK	8	ns
t_{hi}	SCLK high time	20	ns
t_{lo}	SCLK low time	20	ns
t_{ck}	SCLK period	50	ns
t_{s}	Data setup time	5	ns
t_{h}	Data hold time	5	ns

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Timing Diagrams

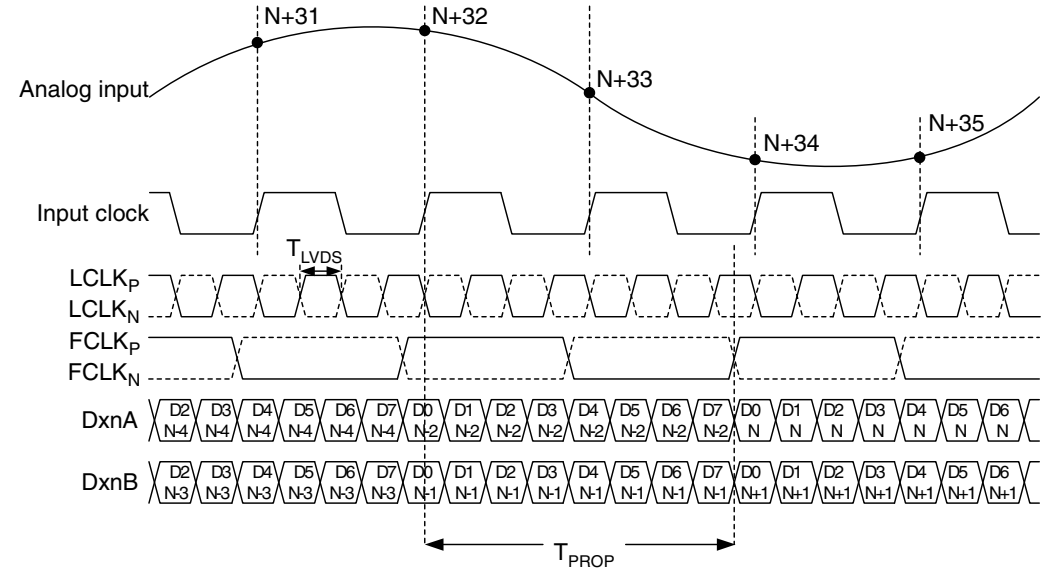

Figure 4: Quad channel - LVDS timing 8-bit output

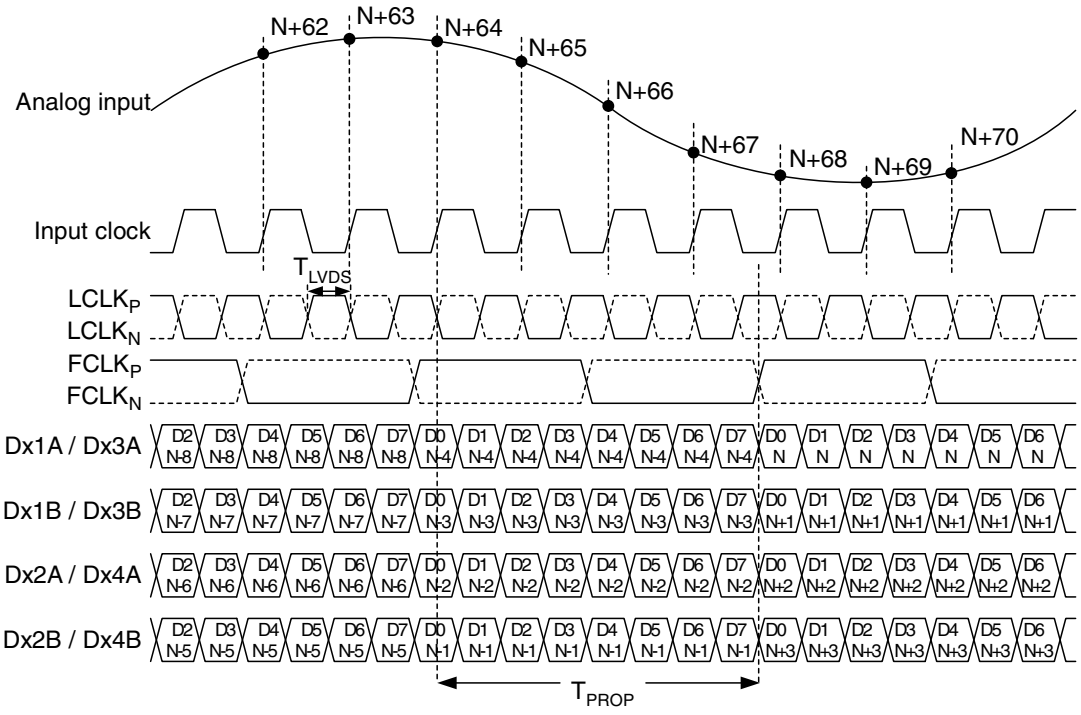

Figure 5: Dual channel - LVDS timing 8-bit output

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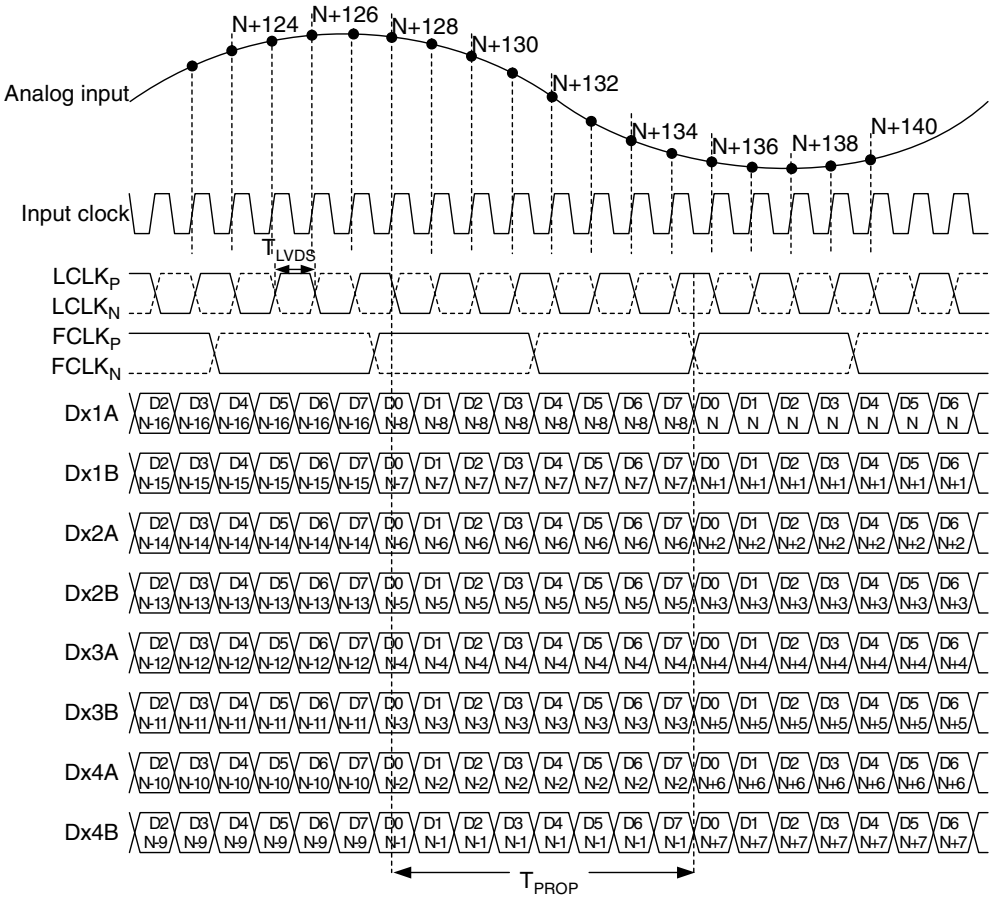

Figure 6: Single channel - LVDS timing 8-bit output

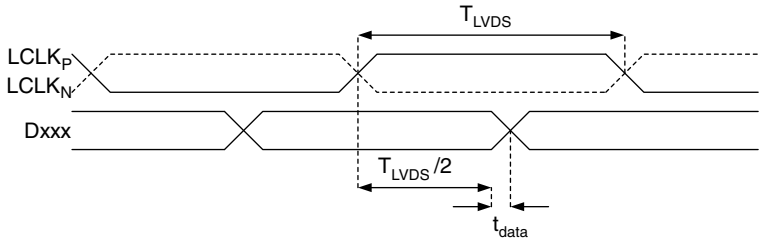

Figure 7: LVDS data timing

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Register Map Summary

Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst *	Self-clearing software reset.	Inactive																X	0x00
sleep4_ch <4:1>	Channel-specific sleep mode for a Quad Channel setup.	Inactive													X	X	X	X	0x0F
sleep2_ch <2:1>	Channel-specific sleep mode for a Dual Channel setup.	Inactive											X	X					
sleep1_ch1	Channel-specific sleep mode for a Single Channel setup.	Inactive										X							
sleep	Go to sleep-mode.	Inactive								X									
pd	Go to power-down.	Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin function.	PD pin configured for power-down mode					X	X											
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	3.5 mA drive														X	X	X	0x11
ilvds_frame <2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	3.5 mA drive										X	X	X					
ilvds_dat <2:0>	LVDS current drive programmability for output data pins.	3.5 mA drive						X	X	X									
en_lvds_ term	Enables internal termination for LVDS buffers.	Termination disabled		X															0x12
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers.	Termination disabled		1												X	X	X	
term_frame <2:0>	Programmable termination for FCLKN and FCLKP buffers.	Termination disabled		1								X	X	X					
term_dat <2:0>	Programmable termination for output data buffers.	Termination disabled		1				X	X	X									
invert4_ch <4:1>	Channel specific swapping of the analog input signal for a Quad Channel setup.	IPx is positive input													X	X	X	X	0x24
invert2_ch <2:1>	Channel specific swapping of the analog input signal for a Dual Channel setup.	IPx is positive input											X	X					
invert1_ch1	Channel specific swapping of the analog input signal for a Single Channel setup.	IPx is positive input										X							
en_ramp	Enables a repeating full-scale ramp pattern on the outputs.	Inactive										X	0	0					0x25
dual_ custom_pat	Enable the mode wherein the output toggles between two defined codes.	Inactive										0	X	0					
single_ custom_pat	Enables the mode wherein the output is a constant specified code.	Inactive										0	0	X					
bits_custom1 <7:0>	Bits for the single custom pattern and for the first code of the dual custom pattern.	0x00	X	X	X	X	X	X	X	X									0x26
bits_custom2 <7:0>	Bits for the second code of the dual custom pattern.	0x00	X	X	X	X	X	X	X	X									0x27
cgain4_ch1 <3:0>	Programmable coarse gain channel 1 in a Quad Channel setup.	1x gain													X	X	X	X	0x2A
cgain4_ch2 <3:0>	Programmable coarse gain channel 2 in a Quad Channel setup.	1x gain									X	X	X	X					
cgain4_ch3 <3:0>	Programmable coarse gain channel 3 in a Quad Channel setup.	1x gain					X	X	X	X									
cgain4_ch4 <3:0>	Programmable coarse gain channel 4 in a Quad Channel setup.	1x gain	X	X	X	X													

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Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
cgain2_ch1 <3:0>	Programmable coarse gain channel 1 in a Dual Channel setup.	1x gain													X	X	X	X	0x2B
cgain2_ch2 <3:0>	Programmable coarse gain channel 2 in a Dual Channel setup.	1x gain									X	X	X	X					
cgain1_ch1 <3:0>	Programmable coarse gain channel 1 in a Single Channel setup.	1x gain					X	X	X	X									
jitter_ctrl <7:0>	Clock jitter adjustment.	160 fsrms									X	X	X	X	X	X	X	X	0x30
channel_ num <2:0> *	Set number of channels: 1, 2 or 4 channels.	4 channels														X	X	X	0x31
clk_divide <1:0>*	Define clock divider factor: 1, 2, 4 or 8	Divide by 1							X	X									
coarse_ gain_cfg	Configures the coarse gain setting	x-gain enabled																X	0x33
fine_gain_en	Enable use of fine gain.	Disabled															X		
fgain_ branch1 <6:0>	Programmable fine gain for branch1.	0dB gain										X	X	X	X	X	X	X	0x34
fgain_ branch2 <6:0>	Programmable fine gain for branch 2.	0dB gain		X	X	X	X	X	X	X									
fgain_ branch3 <6:0>	Programmable fine gain for branch 3.	0dB gain										X	X	X	X	X	X	X	0x35
fgain_ branch4 <6:0>	Programmable fine gain for branch 4.	0dB gain		X	X	X	X	X	X	X									
fgain_ branch5 <6:0>	Programmable fine gain for branch 5.	0dB gain										X	X	X	X	X	X	X	0x36
fgain_ branch6 <6:0>	Programmable fine gain for branch 6.	0dB gain		X	X	X	X	X	X	X									
fgain_ branch7 <6:0>	Programmable fine gain for branch 7.	0dB gain										X	X	X	X	X	X	X	0x37
fgain_ branch8 <6:0>	Programmable fine gain for branch 8.	0dB gain		X	X	X	X	X	X	X									
inp_sel_adc1 <4:0>	Input select for adc 1.	Signal input: IP1/IN1												X	X	X	X	0	0x3A
inp_sel_adc2 <4:0>	Input select for adc 2.	Signal input: IP2/ IN2				X	X	X	X	0									
inp_sel_adc3 <4:0>	Input select for adc 3.	Signal input: IP3/ IN3												X	X	X	X	0	0x3B
inp_sel_ adc4<4:0>	Input select for adc 4.	Signal input: IP4/ IN4				X	X	X	X	0									
phase_ddr <1:0>	Controls the phase of the LCLK output relative to data.	90 degrees										X	X						0x42
pat_deskew	Enable deskew pattern mode.	Inactive															0	X	0x45
pat_sync	Enable sync pattern mode.	Inactive															X	0	
btc_mode	Binary two's complement format for ADC output data.	Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first.	LSB first													X				
adc_curr <2:0>	ADC current scaling.	Nominal														X	X	X	0x50
ext_vcm_bc <1:0>	VCM buffer driving strength control.	Nominal											X	X					
lvds_pd_ mode	Controls LVDS power down mode	High z-mode																X	0x52

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Table 5: Register Map

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
low_clk_ freq *	Low clock frequency used.	Inactive													X	0	0	0	0x53
lvds_ advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X		0	0	0	
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0		0	0	0	
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	0x55
startup_ctrl <2:0> *	Controls start-up time.	'000'														X	X	X	0x56

Undefined register addresses must not be written to; incorrect behavior may be the result.

Unused register bits (blank table cells) must be set to '0' when programming the registers.

All registers can be written to while the chip is in power down mode.

* These registers requires a power down cycle when written to (See Start up Initialization).

Register Description

Software Reset

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
rst	Self-clearing software reset.	Inactive																X	0x00

Setting the rst register bit to '1', restores the default value of all the internal registers including the rst register bit itself.

Modes of Operation and Clock Divide Factor

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
channel_ num <2:0>	Set number of channels: 1, 2 or 4 channels.	4 channels														X	X	X	0x31
clk_divide <1:0>	Define clock divider factor: 1, 2, 4 or 8	Divide by 1							X	X									

The HMCAD1510 has three main operating modes controlled by the register bits channel_num<2:0> as defined in table 6. Power down mode, as described in section 'Startup Initialization', must be activated after or during a change of operating mode to ensure correct operation. All active operating modes utilize interleaving to achieve high sampling speed. Quad channel mode interleaves 2 ADC branches, dual channel mode interleaves 4 ADC branches, while single channel mode interleave all 8 ADC branches.

Table 6: Modes of operation

channel_num <2:0>			Mode of operation	Description
0	0	1	Single channel	Single channel by interleaving ADC1 to ADC4
0	1	0	Dual channel	Dual channel where channel 1 is made by interleaving ADC1 and ADC2, channel 2 by interleaving ADC3 and ADC4
1	0	0	Quad channel	Quad channel where channel 1 corresponds to ADC1, channel2 to ADC2, channel3 to ADC3 and channel 4 to ADC4

Only one of the 3bits should be activated at the same time.

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clk_divide<1:0> allows the user to apply an input clock frequency higher than the sampling rate. The clock divider will divide the input clock frequency by a factor of 1, 2, 4, or 8, defined by the clk_divide<1:0> register. By setting the clk_divide<1:0> value relative to the channel_num<2:0> value, the same input clock frequency can be used for all settings on number of channels. e.g: When increasing the number of channels from 1 to 4, the maximum sampling rate is reduced by a factor of 4. By letting clk_divide<1:0> follow the channel_num<2:0> value, and change it from 1 to 4, the internal clock divider will provide the reduction of the sampling rate without changing the input clock frequency.

Table 7: Clock Divider Factor

clk_divide<1:0>	Clock Divider Factor	Sampling rate (FS)
00 (default)	1	Input clock frequency / 1
01	2	Input clock frequency / 2
10	4	Input clock frequency / 4
11	8	Input clock frequency / 8

Input Select

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
inp_sel_adc1 <4:0>	Input select for adc 1.	Signal input: IP1/IN1												X	X	X	X	0	0x3A
inp_sel_adc2 <4:0>	Input select for adc 2.	Signal input: IP2/IN2				X	X	X	X	0									
inp_sel_adc3 <4:0>	Input select for adc 3.	Signal input: IP3/IN3												X	X	X	X	0	0x3B
inp_sel_adc4 <4:0>	Input select for adc 4.	Signal input: IP4/IN4				X	X	X	X	0									

Each ADC is connected to the four input signals via a full flexible cross point switch, set up by inp_sel_adcx. In single channel mode, any one of the four inputs can be selected as valid input to the single ADC channel. In dual channel mode, any two of the four inputs can be selected to each ADC channel. In quad channel mode any input can be assigned to any ADC channel. The switching of inputs can be done during normal operation, and no additional actions are needed. The switching will occur instantaneously at the end of each SPI command.

Table 8: ADC Input Select

inp_sel_adcx<4:0>	Selected Input
0001 0	IP1/IN1
0010 0	IP2/IN2
0100 0	IP3/IN3
1000 0	IP4/IN4
other	Do not use

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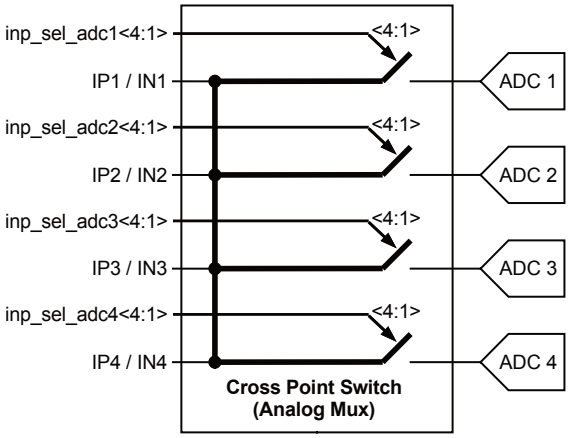

Figure 8: ADC input signals through Cross Point Switch

Full-Scale Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
fs_cntrl <5:0>	Fine adjust ADC full scale range	0% change											X	X	X	X	X	X	0x55

The full-scale voltage range of HMCAD1510 can be adjusted using an internal 6-bit DAC controlled by the fs_cntrl register. Changing the value in the register by one step, adjusts the full-scale range by approximately 0.3%. This leads to a maximum range of ±10% adjustment. Table 9 shows how the register settings correspond to the full-scale range. Note that the values for full-scale range adjustment are approximate. The DAC is, however, guaranteed to be monotonous.

The full-scale control and the programmable gain features differ in two major ways:

1. The full-scale control feature controls the full-scale voltage range in an analog fashion, whereas the programmable gain is a digital feature.
2. The programmable gain feature has much coarser gain steps and larger range than the full-scale control.

Table 9: Register Values with Corresponding Change in Full-Scale Range

fs_cntrl<5:0>	Full-Scale Range Adjustment
111111	9.70%
111110	9.40%
100001	0.30%
100000	0%
011111	-0.3%
000001	-9.7%
000000	-10%

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Current Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
adc_curr<2:0>	ADC current scaling.	Nominal														X	X	X	0x50
ext_vcm_bc<1:0>	VCM buffer driving strength control.	Nominal											X	X					

There are two registers that impact performance and power dissipation.

The adc_curr register scales the current consumption in the ADC core. The performance is guaranteed at the nominal setting. Lower power consumption can be achieved by reducing the adc_curr value, see table 10. The impact on performance is low for settings down to minimum, but will depend on the ADC sampling rate.

Table 10: ADC Current Control Settings

adc_curr<2:0>	ADC Core Current
100	-40% (lower performance)
101	-30%
110	-20%
111	-10%
000 (default)	Nominal
001	Do not use
010	Do not use
011	Do not use

The ext_vcm_bc register controls the driving strength in the buffer supplying the voltage on the VCM pin. If this pin is not in use, the buffer can be switched off. If current is drawn from the VCM pin, the driving strength can be increased to keep the voltage on this pin at the correct level.

Table 11: External Common Mode Voltage Buffer Driving Strength

ext_vcm_bc<1:0>	**VCM buffer driving strength (µA)** Max current sinked/sourced from VCM pin with < 20 mV voltage change.
00	Off (VCM floating)
01 (default)	±20
10	±400
11	±700

Start-up and Clock Jitter Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
startup_ctrl<2:0>	Controls start-up time.	'000'														X	X	X	0x56
jitter_ctrl<7:0>	Clock jitter adjustment.	160 fsrms									X	X	X	X	X	X	X	X	0x30

To optimize start up time, a register is provided where the start-up time in number of clock cycles can be set. Some internal circuitry have start up times that are clock frequency independent. Default counter values are set to accommodate these start up times at the maximum clock frequency (sampling rate). This will lead to increased start up times at low clock frequencies. Setting the value of this register to the nearest higher clock frequency will reduce the count values of the internal counters, to better fit the actual start up time, such that the start up time will be reduced. The start up times from power down and sleep modes are changed by this register setting. If the clock divider is used (set to other than 1), the input clock frequency must be divided by the divider factor to find the correct clock frequency range (see table 7).

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Table 12: Start-Up Time Control Settings

Quad Channel			
startup_ctrl <2:0>	Clock Frequency Range (MSPS)	Startup Delay (clock cycles)	Startup Delay (µs)
100	160 - 250	3072	12.3 - 19.2
000	100 - 160	1984	12.4 - 19.8
001	65 - 100	1280	12.8 - 19.7
101	40 - 65	840	12.9 - 21
011	30 - 40	520	13 - 17.3
other	Do not use	-	-

Dual Channel			
startup_ctrl <2:0>	Clock Frequency Range (MSPS)	Startup Delay (clock cycles)	Startup Delay (µs)
100	320 - 500	6144	12.3 - 19.2
000	200 - 320	3968	12.4 - 19.8
001	130 – 200	2560	12.8 - 19.7
101	80 - 130	1680	12.9 - 21
011	60 – 80	1040	13 - 17.3
other	Do not use	-	-

Single Channel			
startup_ctrl <2:0>	Clock frequency range (MSPS)	Startup Delay (clock cycles)	Startup delay (µs)
100	640 - 1000	12288	12.3 - 19.2
000	400 - 640	7936	12.4 - 19.8
001	260 - 400	5120	12.8 - 19.7
101	160 - 260	3360	12.9 - 21
011	120 - 160	2080	13 - 17.3
other	Do not use	-	-

jitter_ctrl<7:0> allows the user to set a trade-off between power consumption and clock jitter. If all bits in the register is set low, the clock signal is stopped. The clock jitter depends on the number of bits set to '1' in the jitter_ctrl<7:0> register. Which bits are set high does not affect the result.

Table 13: Clock Jitter Performance

Number of bits to '1' in jitter_ctrl<7:0>	Clock Jitter Performance (fsrms)	Module Current Consumption (mA)
1	160	1
2	150	2
3	136	3
4	130	4
5	126	5
6	124	6
7	122	7
8	120	8
0	Clock stopped	

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LVDS Output Configuration and Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
low_clk_freq	Low clock frequency used.	Inactive													X	0	0	0	0x53
lvds_advance	Advance LVDS data bits and frame clock by one clock cycle	Inactive											0	X		0	0	0	
lvds_delay	Delay LVDS data bits and frame clock by one clock cycle	Inactive											X	0		0	0	0	
phase_ddr<1:0>	Controls the phase of the LCLK output relative to data.	90 degrees										X	X						0x42
btc_mode	Binary two's complement format for ADC output data.	Straight offset binary														X			0x46
msb_first	Serialized ADC output data comes out with MSB first.	LSB first													X				

The HMCAD1510 uses an 8-bit serial LVDS output interface as shown in the Timing Diagrams section. The different selection of number of channels uses the LVDS outputs as defined by table 14.

Table 14: Use of LVDS Outputs

Channel Set-Up	LVDS Outputs Used
Single channel	D1A, D1B, D2A, D2B, D3A, D3B, D4A, D4B
Dual channel, channel 1	D1A, D1B, D2A, D2B
Dual channel, channel 2	D3A, D3B, D4A, D4B
Quad channel, channel 1	D1A, D1B
Quad channel, channel 2	D2A, D2B
Quad channel, channel 3	D3A, D3B
Quad channel, channel 4	D4A, D4B

Maximum data output bit-rate for HMCAD1510 is 500Mb/s. The maximum sampling rate for the different configurations is given by table 15. The sampling rate is set by the frequency of the input clock (FS). The frame-rate, i.e. the frequency of the FCLK signal on the LVDS outputs, depends on the selected mode and the sampling frequency (FS) as defined in table 16.

Table 15: Maximum Sampling Rate

Product	Single Channel (MSPS)	Dual Channel (MSPS)	Quad Channel (MSPS)
HMCAD1511	1000	500	250
HMCAD1510	500	250	125

Table 16: Output Data Frame Rate

Mode of Operation	Frame-Rate (FCLK Frequency)
Single channel	$F_S / 8$
Dual channel	$F_S / 4$
Quad channel	$F_S / 2$

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To ease timing in the receiver when using multiple HMCAD1510s, the device has the option to adjust the timing of the output data and the frame clock. The propagation delay with respect to the ADC input clock can be moved one LVDS clock cycle forward or backward, by using lvds_delay and lvds_advance, respectively. See figure 9 for details. Note that LCLK is not affected by lvds_delay or lvds_advance settings.

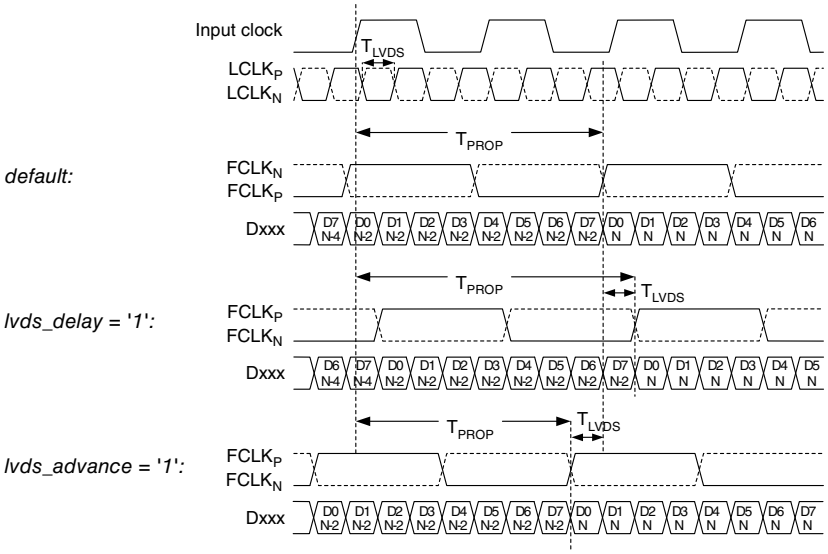

Figure 9: LVDS output timing adjustment

The LVDS output interface of HMCAD1510 is a DDR interface. The default setting is with the LCLK rising and falling edge transitions in the middle of alternate data windows. The phase for LCLK can be programmed relative to the output frame clock and data bits using phase_ddr<1:0>. The LCLK phase modes are shown in figure 10. The default timing is identical to setting phase_ddr<1:0>='10'.

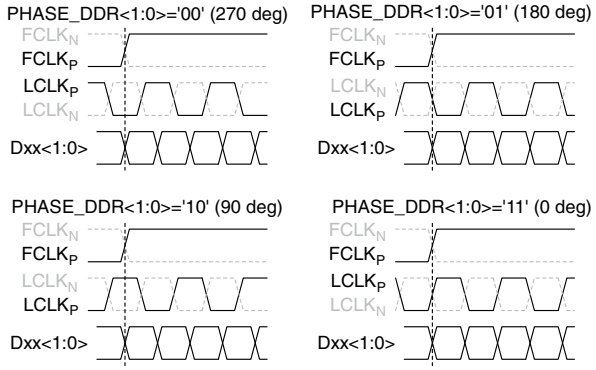

Figure 10: Phase programmability modes for LCLK

The default data output format is offset binary. Two's complement mode can be selected by setting the btc_mode bit to '1' which inverts the MSB.

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The first bit of the frame (following the rising edge of FCLKP) is the LSB of the ADC output for default settings. Programming the msb_first mode results in reverse bit order, and the MSB is output as the first bit following the FCLKP rising edge.

LVDS Drive Strength Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
ilvds_lclk <2:0>	LVDS current drive programmability for LCLKP and LCLKN pins.	3.5 mA drive														X	X	X	
ilvds_frame <2:0>	LVDS current drive programmability for FCLKP and FCLKN pins.	3.5 mA drive										X	X	X					0x11
ilvds_dat <2:0>	LVDS current drive programmability for output data pins.	3.5 mA drive						X	X	X									

The current delivered by the LVDS output drivers can be configured as shown in table 17. The default current is 3.5mA, which is what the LVDS standard specifies.

To reduce power consumption in the HMCAD1510, Reduced Swing Data Signaling (RSDS), is recommended. The output current drive setting should then be 1.5 mA.

Setting the ilvds_lclk<2:0> register controls the current drive strength of the LVDS clock output on the LCLKP and LCLKN pins.

Setting the ilvds_frame<2:0> register controls the current drive strength of the frame clock output on the FCLKP and FCLKN pins.

Setting the ilvds_dat<2:0> register controls the current drive strength of the data outputs on the D[8:1]P and D[8:1]N pins.

Table 17: LVDS Output Drive Strength for LCLK, FCLK & Data

ilvds_*<2:0>	LVDS Drive Strength
000	3.5 mA (default)
001	2.5 mA
101	1.5 mA (RSDS)
011	0.5 mA
100	7.5 mA
101	6.5 mA
110	5.5 mA
111	4.5 mA

LVDS Internal Termination Programmability

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
en_lvds_term	Enables internal termination for LVDS buffers.	Termination disabled		X															
term_lclk <2:0>	Programmable termination for LCLKN and LCLKP buffers.	Termination disabled		1												X	X	X	
term_frame <2:0>	Programmable termination for FCLKN and FCLKP buffers.	Termination disabled		1								X	X	X					0x12
term_dat <2:0>	Programmable termination for output data buffers.	Termination disabled		1				X	X	X									

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The off-chip load on the LVDS buffers may represent a characteristic impedance that is not perfectly matched with the PCB traces. This may result in reflections back to the LVDS outputs and loss of signal integrity. This effect can be mitigated by enabling an internal termination between the positive and negative outputs of each LVDS buffer. Internal termination mode can be selected by setting the en_lvds_term bit to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 18 shows how the internal termination of the LVDS buffers are programmed. The values are typical values and can vary by up to ±20% from device to device and across temperature.

Table 18: LVDS Output Internal Termination for LCLK, FCLK and Data

term_*<2:0>	LVDS Internal Termination
000	Termination disabled
001	260Ω
101	150Ω
011	94Ω
100	125Ω
101	80Ω
110	66Ω
111	55Ω

Power Mode Control

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
sleep4_ch <4:1>	Channel-specific sleep mode for a Quad Channel setup.	Inactive													X	X	X	X	0x0F
sleep2_ch <2:1>	Channel-specific sleep mode for a Dual Channel setup.	Inactive											X	X					
sleep1_ch1	Channel-specific sleep mode for a Single Channel setup.	Inactive										X							
sleep	Go to sleep-mode.	Inactive								X									
pd	Go to power-down.	Inactive							X										
pd_pin_cfg <1:0>	Configures the PD pin function.	PD pin configured for power-down mode					X	X											
lvds_pd_mode	Controls LVDS power down mode	High z-mode																X	0x52

The HMCAD1510 device has several modes for power management, from sleep modes with short start up time to full power down with extremely low power dissipation. There are two sleep modes, both with the LVDS clocks (FCLK, LCLK) running, such that the synchronization with the receiver is maintained. The first is a light sleep mode (sleep*_ch) with short start up time, and the second a deep sleep mode (sleep) with the same start up time as full power down.

Setting sleep4_ch<n> = '1' sets channel <n> in a Quad Channel setup in sleep mode. Setting sleep2_ch<n> = '1' sets channel <n> in a Dual Channel setup in sleep mode. Setting sleep1_ch1 = '1' sets the ADC channel in a Single Channel setup in sleep mode. This is a light sleep mode with short start up time.

Setting sleep = '1', puts all channels to sleep, but keeps FCLK and LCLK running to maintain LVDS synchronization. The start up time is the same as for complete power down. Power consumption is significantly lower than for setting all channels to sleep by using the sleep*_ch register.

Setting pd = '1' completely powers down the chip, including the band-gap reference circuit. Start-up time from this mode is significantly longer than from the sleep*_ch mode. The synchronization with the LVDS receiver is lost since LCLK and FCLK outputs are put in high-Z mode.

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Setting pdn_pin_cfg<1:0> = 'x1' configures the circuit to enter sleep channel mode (all channels off) when the PD pin is set high. This is equal to setting all channels to sleep by using sleep*_ch. The channels can not be powered down separately using the PD pin. Setting pdn_pin_cfg<1:0> = '10' configures the circuit to enter (deep) sleep mode when the PD pin is set high (equal to setting sleep='1'). When pdn_pin_cfg <1:0>= '00', which is the default, the circuit enters the power down mode when the PD pin is set high.

The lvds_pd_mode register configures whether the LVDS data output drivers are powered down or kept alive in sleep and sleep channel modes. LCLK and FCLK drivers are not affected by this register, and are always on in sleep and sleep channel modes. If lvds_pd_mode is set low (default), the LVDS output is put in high Z mode, and the driver is completely powered down. If lvds_pd_mode is set high, the LVDS output is set to constant 0, and the driver is still on during sleep and sleep channel modes.

Programmable Gain

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
cgain_cfg	Configures the coarse gain setting	x-gain enabled																X	0x33
fine_gain_en	Enable use of fine gain.	Disabled															X		
cgain4_ch1 <3:0>	Programmable coarse gain channel 1 in a Quad Channel setup.	1x gain													X	X	X	X	0x2A
cgain4_ch2 <3:0>	Programmable coarse gain channel 2 in a Quad Channel setup.	1x gain									X	X	X	X					
cgain4_ch3 <3:0>	Programmable coarse gain channel 3 in a Quad Channel setup.	1x gain					X	X	X	X									
cgain4_ch4 <3:0>	Programmable coarse gain channel 4 in a Quad Channel setup.	1x gain	X	X	X	X													
cgain2_ch1 <3:0>	Programmable coarse gain channel 1 in a Dual Channel setup.	1x gain													X	X	X	X	0x2B
cgain2_ch2 <3:0>	Programmable coarse gain channel 2 in a Dual Channel setup.	1x gain									X	X	X	X					
cgain1_ch1 <3:0>	Programmable coarse gain channel 1 in a 1 channel setup.	1x gain					X	X	X	X									
fgain_branch1<6:0>	Programmable fine gain for branch1.	0dB gain										X	X	X	X	X	X	X	0x34
fgain_branch2<6:0>	Programmable fine gain for branch 2.	0dB gain		X	X	X	X	X	X	X									
fgain_branch3<6:0>	Programmable fine gain for branch 3.	0dB gain										X	X	X	X	X	X	X	0x35
fgain_branch4<6:0>	Programmable fine gain for branch 4.	0dB gain		X	X	X	X	X	X	X									
fgain_branch5<6:0>	Programmable fine gain for branch 5.	0dB gain										X	X	X	X	X	X	X	0x36
fgain_branch6<6:0>	Programmable fine gain for branch 6.	0dB gain		X	X	X	X	X	X	X									
fgain_branch7<6:0>	Programmable fine gain for branch 7.	0dB gain										X	X	X	X	X	X	X	0x37
fgain_branch8<6:0>	Programmable fine gain for branch 8.	0dB gain		X	X	X	X	X	X	X									

The device includes a digital programmable gain in addition to the Full-scale control. The programmable gain of each channel can be individually set using a four bit code, indicated as cgain*<3:0>. The gain is configured by the register cgain_cfg, when cgain_cfg equals '0' a gain in dB steps is enabled as defined in table 19 otherwise if cgain_cfg equals '1' the gain is defined by table 20. There will be no missing codes for gain settings lower than 32x (30dB), due to higher than 8 bit resolution internally.

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Table 19: Gain setting – dB Step

cgain_cfg	cgain*<3:0>	Implemented Gain (dB)
0	0000	0
0	0001	1
0	0010	2
0	0011	3
0	0100	4
0	0101	5
0	0110	6
0	0111	7
0	1000	8
0	1001	9
0	1010	10
0	1011	11
0	1100	12
0	1101	Not used
0	1110	Not used
0	1111	Not used

Table 20: Gain Setting – x Step

cgain_cfg	cgain*<3:0>	Implemented Gain Factor (x)
1	0000	1
1	0001	1.25
1	0010	2
1	0011	2.5
1	0100	4
1	0101	5
1	0110	8
1	0111	10
1	1000	12.5
1	1001	16
1	1010	20
1	1011	25
1	1100	32
1	1101	50
1	1110	Not used
1	1111	Not used

There is a digital fine gain implemented for each ADC to adjust the fine gain errors between the ADCs. The gain is controlled by fgain_branch* as defined in table 21. There will be no missing codes when using digital fine gain, due to higher resolution internally.

To enable the fine gain function the register bit fine_gain_en has to be activated, set to '1'.

Table 21: Fine Gain Setting

fgain_branchx<6:0>							Arithmetic Function	Implemented Gain (x)	Gain (dB)
0	1	1	1	1	1	1	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12} + 2^{-13}) * IN	1.0077	0.0665
0	1	1	1	1	1	0	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-12}) * IN	1.0076	0.0655
0	1	1	1	1	0	1	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11} + 2^{-13}) * IN	1.0074	0.0644
0	1	1	1	1	0	0	OUT = (1 + 2^{-8} + 2^{-9} + 2^{-10} + 2^{-11}) * IN	1.0073	0.0634
0	0	0	0	0	1	1	OUT = (1 + 2^{-12} + 2^{-13}) * IN	1.0004	0.0031
0	0	0	0	0	1	0	OUT = (1 + 2^{-12}) * IN	1.0002	0.0021
0	0	0	0	0	0	1	OUT = (1 + 2^{-13}) * IN	1.0001	0.001
0	0	0	0	0	0	0	OUT = IN	1.0000	0.0000
1	1	1	1	1	1	1	OUT = IN	1.0000	0.0000
1	1	1	1	1	1	0	OUT = (1 - 2^{-13}) * IN	0.9999	-0.0011
1	1	1	1	1	0	1	OUT = (1 - 2^{-12}) * IN	0.9998	-0.0021
1	1	1	1	1	0	0	OUT = (1 - 2^{-12} - 2^{-13}) * IN	0.9996	-0.0032
1	0	0	0	0	1	1	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11}) * IN	0.9927	-0.0639
1	0	0	0	0	1	0	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-13}) * IN	0.9926	-0.0649
1	0	0	0	0	0	1	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-12}) * IN	0.9924	-0.0660
1	0	0	0	0	0	0	OUT = (1 - 2^{-8} - 2^{-9} - 2^{-10} - 2^{-11} - 2^{-12} - 2^{-13}) * IN	0.9923	-0.0670

Analog Input Invert

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
invert4_ch <4:1>	Channel specific swapping of the analog input signal for a Quad Channel setup.	IPx is positive input													X	X	X	X	0x24
invert2_ch <2:1>	Channel specific swapping of the analog input signal for a Dual Channel setup.	IPx is positive input											X	X					
invert1_ch1	Channel specific swapping of the analog input signal for a 1 channel setup.	IPx is positive input										X							

The IPx pin represents the positive analog input pin, and INx represents the negative (complementary) input. Setting the bits marked invertx_ch<n:1> (individual control for each channel) causes the inputs to be swapped. INx would then represent the positive input, and IPx the negative input.

LVDS Test Patterns

Name	Description	Default	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Hex Address
en_ramp	Enables a repeating full-scale ramp pattern on the outputs.	Inactive										X	0	0					0x25
dual_custom_pat	Enable the mode wherein the output toggles between two defined codes.	Inactive										0	X	0					
single_custom_ pat	Enables the mode wherein the output is a constant specified code.	Inactive										0	0	X					
bits_custom1 <7:0>	Bits for the single custom pattern and for the first code of the dual custom pattern. <0> is the LSB.	0x00	X	X	X	X	X	X	X	X									0x26
bits_custom2 <7:0>	Bits for the second code of the dual custom pattern.	0x00	X	X	X	X	X	X	X	X									0x27
pat_deskew	Enable deskew pattern mode.	Inactive															0	X	0x45
pat_sync	Enable sync pattern mode.	Inactive															X	0	

To ease the LVDS synchronization setup of HMCAD1510, several test patterns can be set up on the outputs. Normal ADC data are replaced by the test pattern in these modes. Setting en_ramp to '1' sets up a repeating full-scale ramp pattern on all data outputs. The ramp starts at code zero and is increased 1LSB every clock cycle. It returns to zero code and starts the ramp again after reaching the full-scale code.

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