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Application Note

AN- EVALQRS-ICE2QS03G

36W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS03G

Power Management & Supply

N e v e r s t o p t h i n k i n g .

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Title

Revision History:	**12 November 2011**	**V1.2**
Previous Version:	**V1.1**	

Page	Subjects (major changes since last revision)
12, 13	Revise typo in auxiliary winding turns

36W Evaluation Board with Quasi-Resonant PWM Controller ICE2QS03G
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Table of Contents

1 Content

The demo-board described here is a 36W power supply using quasi-resonant flyback converter topology. The PWM controller **ICE2QS03G** is a second generation quasi-resonant controller IC developed by Infineon Technologies. The typical applications are for TV-sets, DVD-players, Set-top boxes, netbook adapters, home audio and printer applications. In normal operation, the digital frequency reduction with decreasing load enables a quasi-resonant operation till very low load. As a result, the system efficiency over the entire load range is significantly improved compared to conventional free running quasi resonant converter implemented with only maximum switching frequency limitation. In addition, numerous protection functions have been implemented in **ICE2QS03G** to protect the system and customize the IC for the chosen application. In case of failure modes, like open control-loop/over load, output overvoltage, and transformer short winding, the device switches into **Auto Restart Mode** or **Latch-off Mode**. By means of the cycle-by-cycle peak current limitation plus foldback point correction, the dimension of the transformer and the secondary diode can be lower which leads to more cost effective design.

2 Evaluation Board

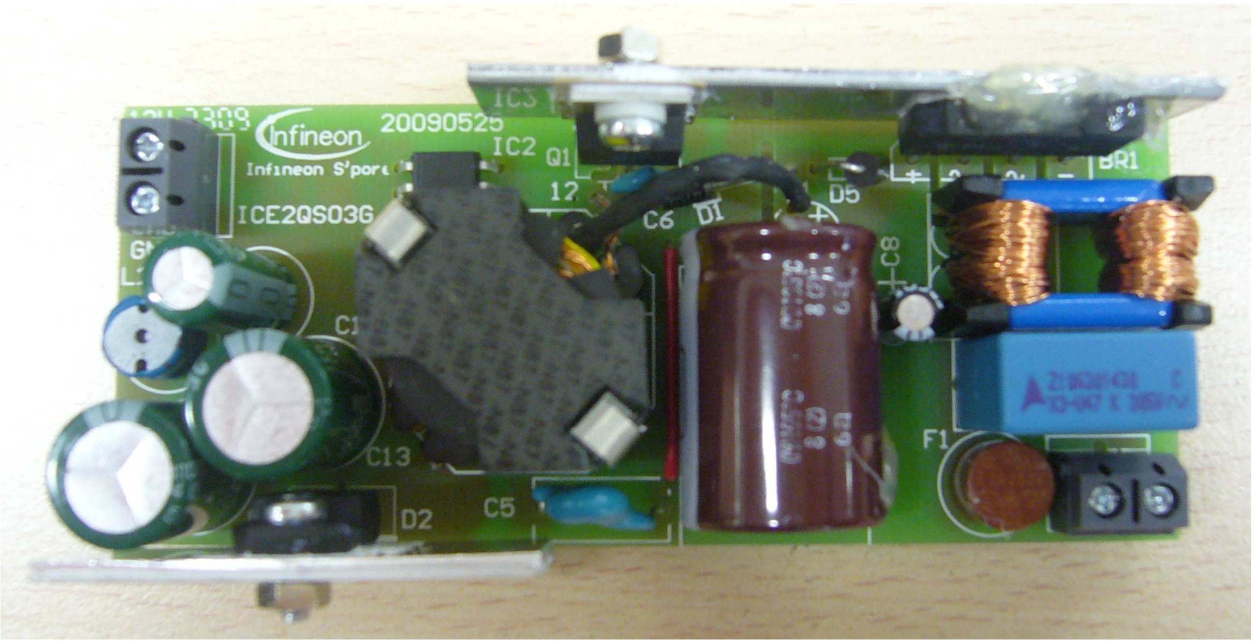


Figure 1-EVALQRS-36W-ICE2QS03G

3 List of Features

Quasi-resonant operation
Digital frequency reduction with decreasing load
Cycle-by-cycle peak current limitation with **foldback point correction**
Built-in **digital soft-start**
Direct current sensing with internal **Leading Edge Blanking Time**
VCC undervoltage protection: **IC stop operation, recover with softstart**
VCC overvoltage protection: **IC stop operation, recover with softstart**
Openloop/Overload protection: **Auto Restart** after fixed blanking time
Output overvoltage protection: **Latch-off with adjustable threshold**
Short-winding protection: **Latch-off**

4 Technical Specifications

Input voltage	**85VAC~265VAC**
Input frequency	**50Hz, 60Hz**
Output voltage and current	**12V 3A**
Output power	**36W**
Efficiency	**>88% at full load**
Minimum switching frequency at full load, minimum input voltage	**38kHz**

5 Circuit Description

5.1 Mains Input and Rectification

The AC line input side comprises the input fuse F1 as overcurrent protection. The X2 Capacitors C1,and Choke L1 forms a main filter to minimize the feedback of RFI into the main supply. After the bridge rectifier BR1, together with a smoothing capacitor C3, provide a voltage of 80VDC to 380 VDC depending on mains input voltage.

5.2 PWM Control

The PWM pulse is generated by the 8-pin Quasi Resonant PWM curremt-mode Controller **ICE2QS03G**. It comprises the complete control for quasi-resonant flyback switch mode power supply especially in netbook adapter, home audio and printer applications. The PWM switch-on is determined by the zero-crossing input signal and the value of the up/down counter. The PWM switch-off is determined by the feedback signal V_{FB} and the current sensing signal V_{CS}. **ICE2QS03G** also performs all necessary protection functions in flyback converters. Details about the information mentioned above are illustrated in the product datasheet.

5.3 Snubber Network

A snubber network D1 and D5 dissipate the energy of the leakage inductance and to suppress ringing on the SMPS transformer. The Transient voltage suppression diode D5 absorbs the voltage spike larger than 207V.

5.4 Output Stage

On the secondary side, 12V output, the power is coupled out via a dual schottky diode D2. The capacitors C12 and C13 provide energy buffering followed by the L-C filters to reduce the output ripple and prevent interference between SMPS switching frequency and line frequency considerably. Storage capacitors C12, C13 are designed to have an internal resistance as small as possible (ESR). This is to minimize the output voltage ripple caused by the triangular current.

5.5 Feedback Loop

For feedback, the output is sensed by the voltage divider of R16, R17 and R18 and compared to TL431 internal reference voltage. C15, C16 and R19 comprise the compensation network. The output voltage of TL431 is converted to the current signal via Optocoupler and two resistors R20 and R21 are for regulation control.

6 Circuit Operation

6.1 Startup Operation

When VCC reaches the turn on voltage threshold 18V, the IC begins with a soft start which is realized internally with a built-in digital block. The maximum soft start time is 12ms. During this period, feedback voltage will be generated internally, which is 1.76V at the first step and increases step by step with preset voltage at a time interval of 4ms. In such a way, the primary peak current and the gate drive pulse width are both gradually increased during the soft start.

6.2 Normal Mode Operation

The secondary output voltage is built up after startup. The secondary regulation control is adopted with TL431 and optocoupler. The compensation network C15, C16 and R19 constitutes the external circuitry of the error amplifier of TL431. This circuitry allows the ouput voltage to be precisely controlled to dynamically varying load conditions, therefore providing stable control.

6.3 Digital Frequency Reduction

During normal operation, the switching frequency for **ICE2QS03G** is digitally reduced with decreasing load. At light load, the MOSFET will be turned on not at the first minimum drain-source voltage time, but on the n_{th}. The counter is in range of 1 to 7, which depends on feedback voltage in a time-base. The feedback voltage decreases when the output power requirement decreases, and vice versa. Therefore, the counter is set by monitoring voltage V_{FB}. The counter will be increased with low V_{FB} and decreased with high V_{FB}. The thresholds are preset inside the IC.

7 Protection Features

7.1 Vcc under voltage protection

During normal operation, the VCC voltage is continuously monitored. When the Vcc voltage falls below the under voltage lock out level (VCCoff), the IC is off and gate signal is disabled.

7.2 Foldback point protection

For a quasi-resonant flyback converter, the maximum possible output power will increas when a constant current limit value is used for all the mains input voltage range. This is usually not desired as it will increase additional cost on transformer and output diode incase of output over power conditions.
The internal fold back protection is implemented to adjust the V_{CS} voltage limit according to the bus voltage. Here, the input line voltage is sensed using the current flowing out of **ZC** pin, during the MOSFET on-time. As the result, the maximum current limit will be lower at high input voltage and the maximum output power can be well limited versus the input voltage. Resistor R2 determines the foldback point by setting the current flowing out the ZC pin.

7.3 Open loop/over load protection

In case of open control loop, feedback voltage is pulled up with internally block. After a fixed blanking time, the IC enters **Auto restart mode**. In case of secondary short-circuit or overload, regulation voltage V_{FB} will also be pulled up, same protection will be applied and IC will enters **Auto restart mode.**

7.4 Adjustable output overvoltage protection

During off-time of the power switch, the voltage at the zero-crossing pin ZC is monitored for output overvoltage detection. If the voltage is higher than the preset threshold 3.7V for a preset period, the IC is latched off. R4 and R2 constitute the voltage divide network.R2 is determined by the foldback point correction voltage. After R2 is determined, R4 can be determined by the over voltage protection point according to the threshold of Vzc OVP voltage.

7.5 Short winding protection

The source current of the MOSFET is sensed via shunt resistors R10. If the voltage at the current sensing pin is higher than the preset threshold V_{CSSW} of 1.68V during the on-time of the power switch, the IC is latched off. This implements a short winding protection. To avoid an accidental latch off, a spike blanking time of 190ns is integrated in the output of internal comparator.

8 Circuit diagram

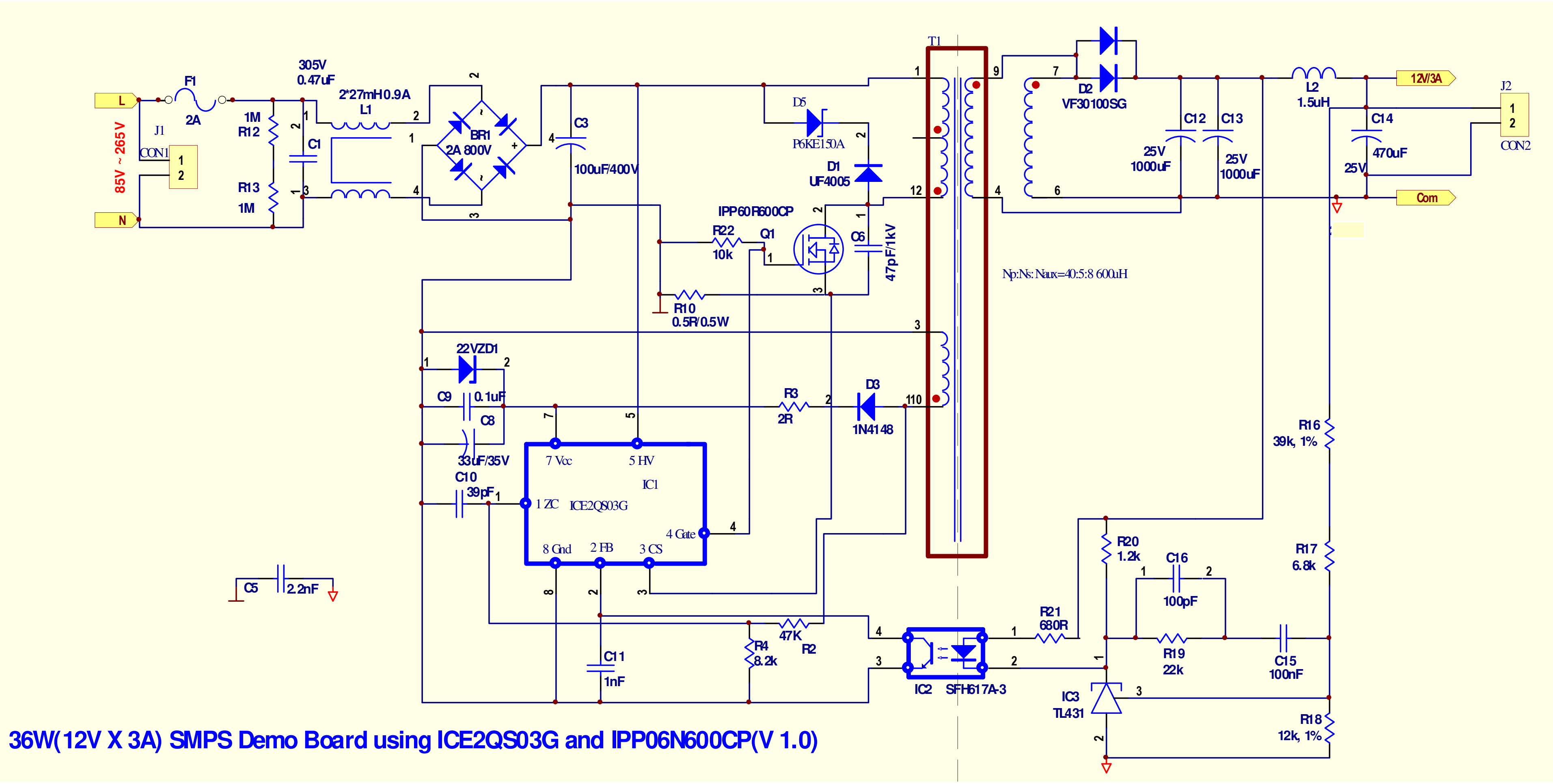


Figure 2 – Schematics

8.1 PCB Topover layer

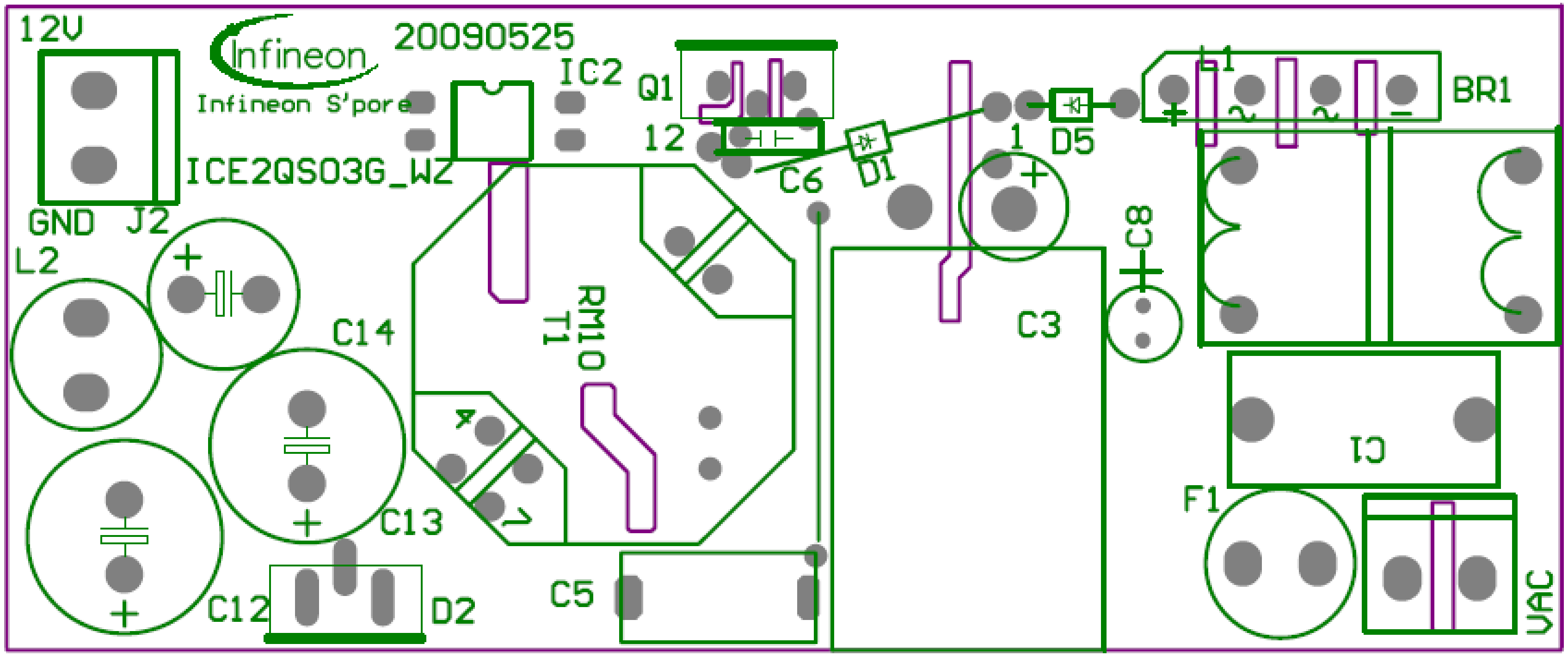


Figure 3 – Component side Component Legend – View from Topside

8.2 PCB Bottom Layer

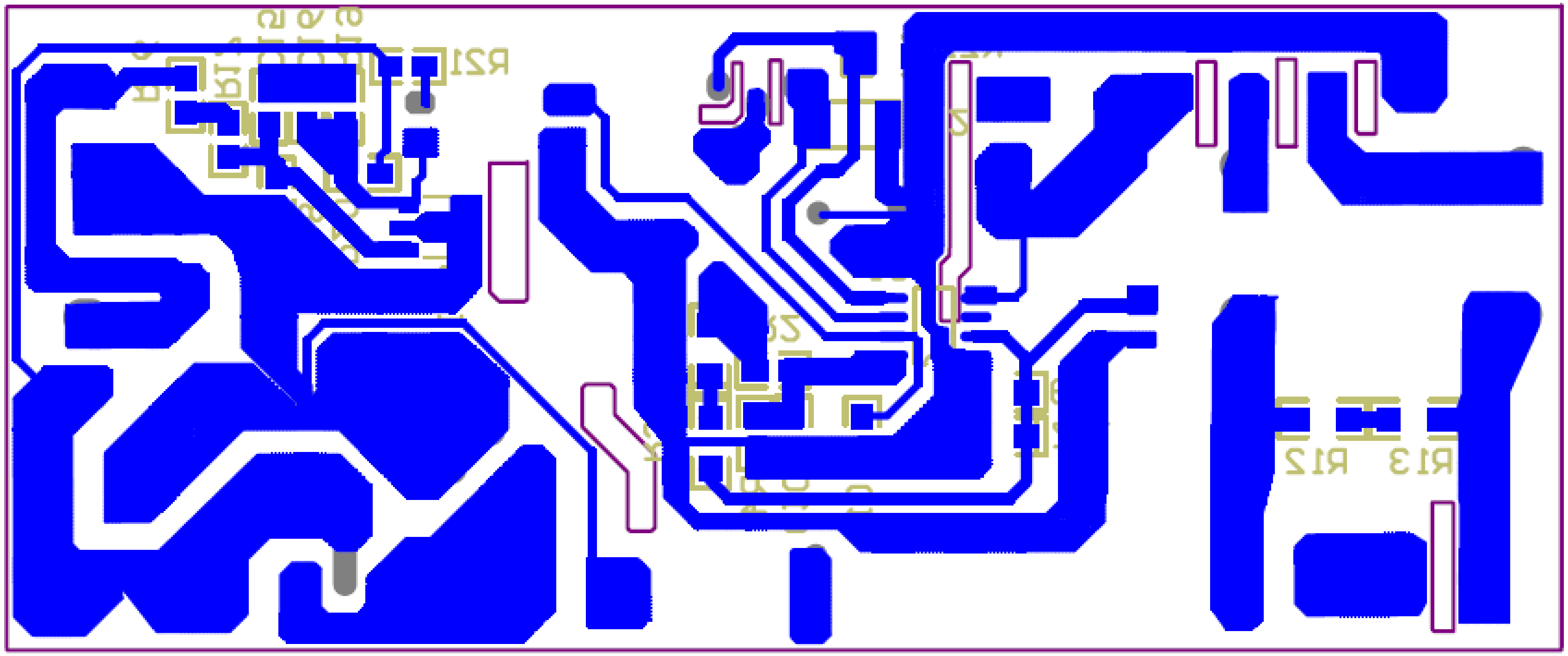


Figure 4 Solder side copper – View from Topside

9 Component List

Items	Circuit code	Description	Part No.	Manufacturer
1	BR1	Bridge rectifier, 2A 800V	2KBB80R	
2	C1	X-cap, 0.47uF 305V	B32922C3474K	Epcos
3	C10	39pF, 50V NPO SMD 0805	39pF, 50V, NPO, SMD 0805	
4	C11	1nF, 50V NPO SMD 0805	1nF, 50V NPO SMD 0805	
5	C12	1000uF/25V KZE 12.5x20	1000uF/25V KZE 12.5x20	
6	C13	1000uF/25V KZE 12.5x20	1000uF/25V KZE 12.5x20	
7	C14	470uF/25V KZE 8x20	470uF/25V KZE 8x20	
8	C15	100nF 50V X7R 0805	100nF 50V X7R 0805	
9	C16	100pF 50V NPO 0805	100pF 50V NPO 0805	
10	C3	100uF/400V18x26	100uF/400V18x26	
11	C5	Y2 cap. 2.2nF/250V	Y2 cap. 2.2nF/250V	
12	C6	47pF/1kV SL	DEA1X3A470JC1B	Murata
13	C8	33uF/35V 5x11	B41851A7336M000	Epcos
14	C9	0.1uF 50V X7R, 1206	0.1uF 50V X7R, 1206	
15	D1	Ultra-fast diode UF4005	UF4005	Vishay
16	D2	Schottky diode 30A 100V	VF30100SG	Vishay
17	D3	Mini MELF diode LL4148	LL4148	
18	D5	TVS 150V 600W	P6KE150A	Vishay
19	F1	Fuse 2A 250V TR5/372	372-2A	
20	IC1	Quasi-Resonant controller ICE2QS03G (SO-8)	ICE2QS03G	Infineon
21	IC2	Opto-coupler SFH617A-3	SFH617A-3	Vishay
22	IC3	Error Amp regulator TL431 SOT89	TL431 SOT89	
23	L1	Input CMC 2*27mH 0.9A	B82732F2901B001	Epcos
24	L2	O/P filter 1.5µH 6.3A	13R152C	Epcos
25	Q1	CoolMOS 60A 600V IPP60R600CP	IPP60R600CP	Infineon
26	R10	0.5Ω / 0.5W (SMD 2010)	WSL2010R5000FEA	Vishay
27	R12	1MΩ SMD 1206	1MΩ SMD 1206	
28	R13	1MΩ SMD 1206	1MΩ SMD 1206	
29	R16	39kΩ, 1% SMD 0805	39kΩ, 1% SMD 0805	
30	R17	6.8kΩ 1% SMD 0805	6.8kΩ 1% SMD 0805	
31	R18	12kΩ, 1% SMD 0805	12kΩ, 1% SMD 0805	
32	R19	22kΩ SMD 0805	22kΩ SMD 0805	
33	R2	47KΩ SMD 0805	47KΩ SMD 0805	
34	R20	1.2kΩ SMD 0805	1.2kΩ SMD 0805	
35	R21	680Ω SMD 0805	680Ω SMD 0805	
36	R22	10kΩ SMD 0805	10kΩ SMD 0805	
37	R3	0Ω SMD 0805	0Ω SMD 0805	
38	R4	8.2kΩ SMD 0805	8.2kΩ SMD 0805	

39	T1	Lp=0.6mH (N87 RM10)	core : B65814N1012D1	EPCOS
40	ZD1	22V zener diode mini MELF	BZV55-B22/TZM525113/ZLL5225	

Table 1– Component List

10 Transformer Construction

Core and material: RM10, N87
Bobbin: 8 pin Version (vertical bobbin)
Primary Inductance, Lp=600µH, measured between pin 1 and pin 12 (Gapped to Inductance)

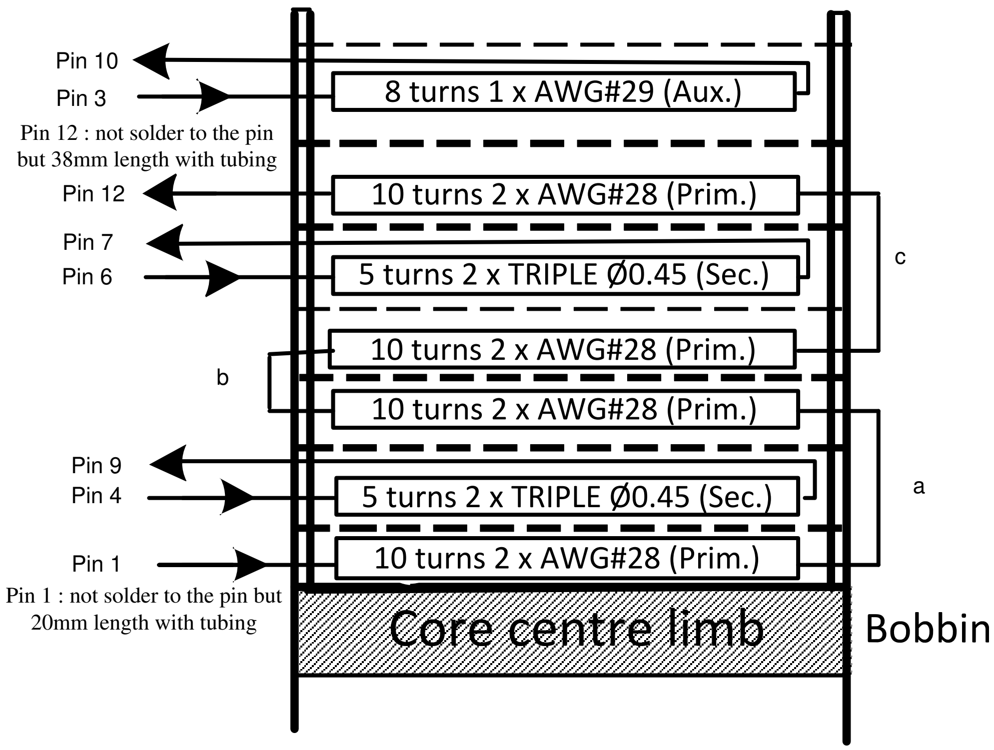
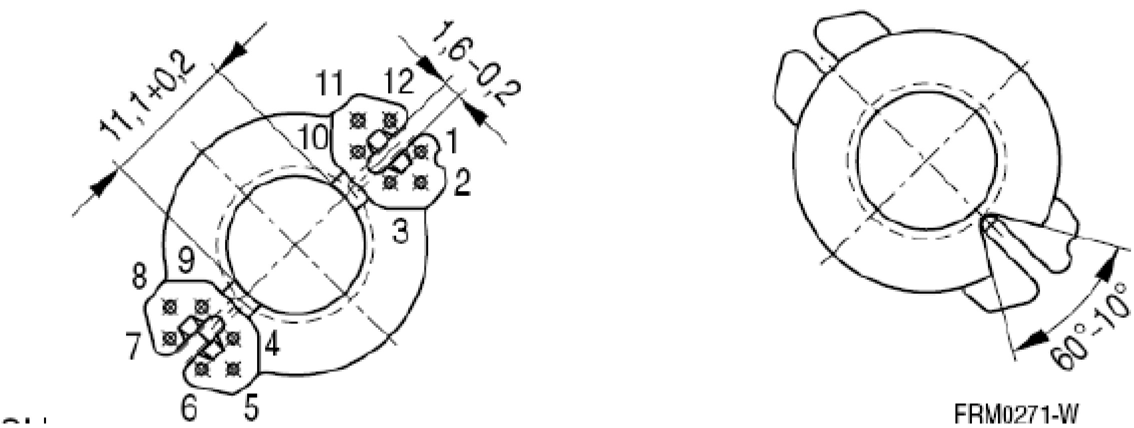


Figure 5 – Transformer structure



Botom view **Top view**

Figure 6 – Transformer complete – bottom and top view

Start	Stop	No. of turns	Wire size	Layer
3	10	8	1XAWG#29	Auxiliary
c	12	10	2XAWG#28	1/4 Primary
6	7	5	2Xtriple wireΦ 0.65	Secondary
b	c (not broken)	10	2XAWG#28	1/4 Primary
a	b (not broken)	10	2XAWG#28	1/4 Primary
4	9	5	2Xtriple wireΦ 0.65	Secondary
1	a (not broken)	10	2XAWG#28	1/4 Primary

Table 2 Wire size requirement

11 Test Results

11.1 Efficiency

Table 3 – Efficiency vs. Load

Vin(AC)	Load	Pin(W)	Vout(V)	Iout(A)	Pout(W)	Efficiency
115	100% load	40.9896	12.003	3.0015	36.027	87.9%
	75% load	30.468	12.005	2.2493	27.00285	88.6%
	50% load	20.2398	12.007	1.499	17.99849	88.9%
	25% load	10.0968	12.009	0.7506	9.013955	89.3%
230	100% load	40.1994	12.003	3.0012	36.0234	89.6%
	75% load	30.1722	12.005	2.249	26.99925	89.5%
	50% load	20.1534	12.007	1.499	17.99849	89.3%
	25% load	10.284	12.009	0.7509	9.017558	87.7%

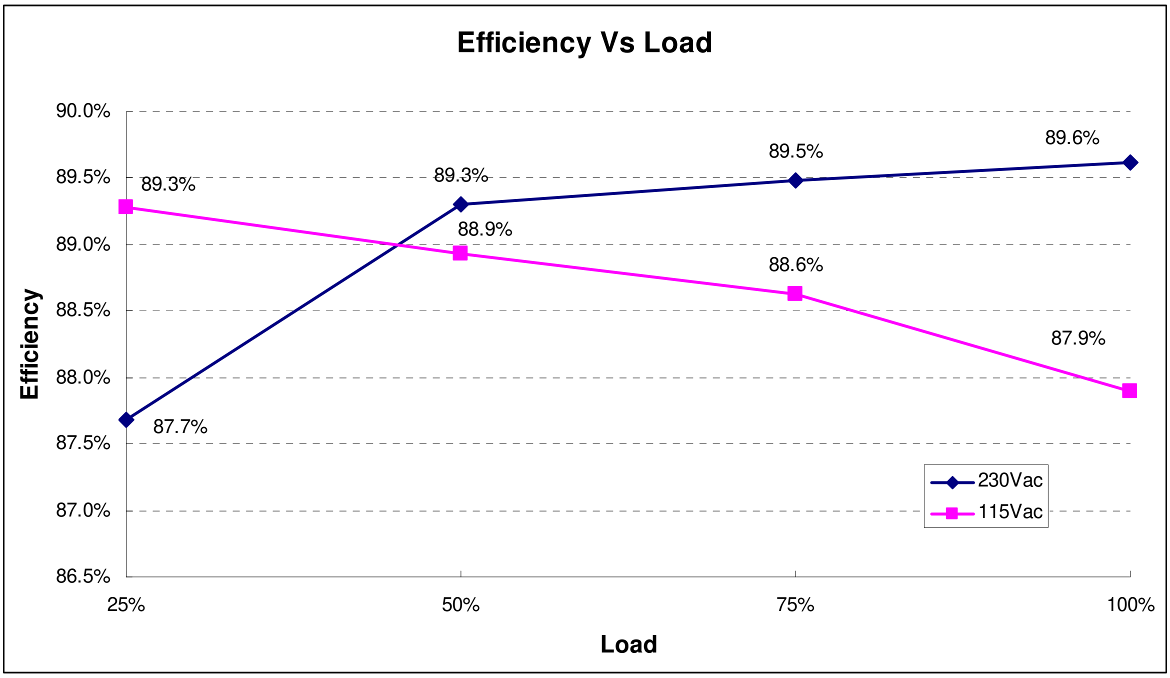


Figure 7 – Active Load Efficiency[1)]

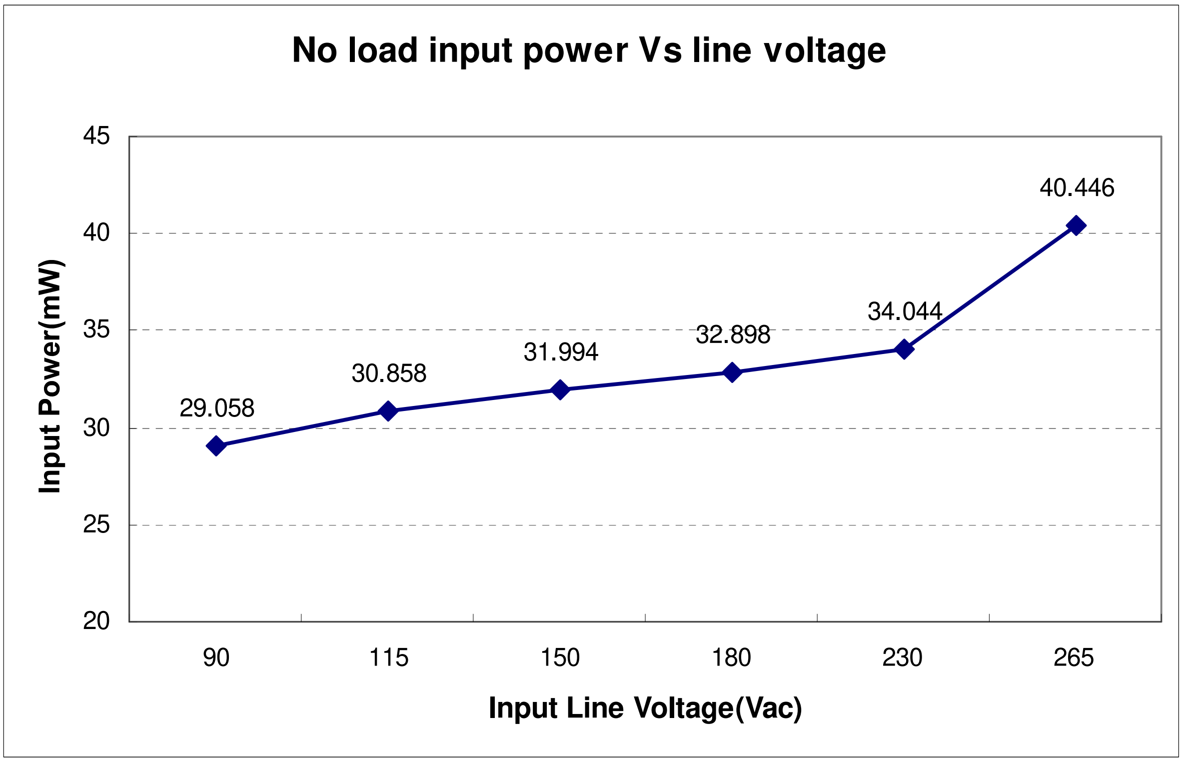


Figure 8 No Load Input Power Vs Line Voltage

1) input discharge resistor R12 and R13 not included

12 References

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