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Enpirion® Power Datasheet EC7401QI 4-Phase PWM Controller with 8-Bit DAC Code

The Altera® Enpirion® EC7401QI controls microprocessor core voltage regulation by driving up to 4 synchronous-rectified buck channels in parallel. The EC7401QI can precision R_{DS}(ON) or DCR Differential Current Sensing. Multiphase buck converter architecture uses interleaved timing to multiply channel ripple frequency and reduce input and output ripple currents. Lower ripple results in fewer components, lower component cost, reduced power dissipation, and smaller implementation area.

Microprocessor loads can generate load transients with extremely fast edge rates. The EC7401QI features a high bandwidth control loop and ripple frequencies up to >4MHz to provide optimal response to the transients.

Today's microprocessors require a tightly regulated output voltage position versus load current (droop). The EC7401QI senses current by utilizing patented techniques to measure the voltage across the on resistance, R_{DS}(ON), of the lower MOSFETs or DCR of the output inductor during the lower MOSFET conduction intervals. Current sensing provides the needed signals for precision droop, channel-current balancing, and overcurrent protection. A programmable internal temperature compensation function is implemented to effectively compensate for the temperature coefficient of the current sense element.

A unity gain, differential amplifier is provided for remote voltage sensing. Any potential difference between remote and local grounds can be completely eliminated using the remote-sense amplifier. Eliminating ground differences improves regulation and protection accuracy. The threshold-sensitive enable input is available to accurately coordinate the start up of the EC7401QI with any other voltage rail. VID Voltage Scaling technology allows seamless on-the-fly VID changes. The offset pin allows accurate voltage offset settings that are independent of VID setting.

Features

- Precision Multiphase Core Voltage Regulation
  - Differential Remote Voltage Sensing
  - ±0.5% System Accuracy Over Life, Load, Line and Temperature
  - Adjustable Precision Reference-Voltage Offset
- Precision R_{DS}(ON) or DCR Current Sensing
  - Accurate Load-Line Programming
  - Accurate Channel-Current Balancing
  - Differential Current Sense
- Microprocessor Voltage Identification Input
  - VID Voltage Scaling Technology
  - 8-Bit VID Input with Selectable VR11 Code and Extended VR10 Code at 6.25mV per Bit
  - 0.5V to 1.6V Operation Range
- Thermal Sensing
- Integrated Programmable Temperature Compensation
- Threshold-Sensitive Enable Function for Power Sequencing and VTT Enable
- Overcurrent Protection
- Overvoltage Protection
- 2-, 3- or 4-Phase Operation
- Adjustable Switching Frequency Up to 1MHz Per Phase
- Package Option
  - QFN Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - QFN Near Chip Scale Package Footprint; Improves PCB Efficiency, Thinner in Profile
- Pb-Free (RoHS Compliant)

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San Jose, CA 95134
www.altera.com

ISO 9001:2008 Registered

Ordering Information

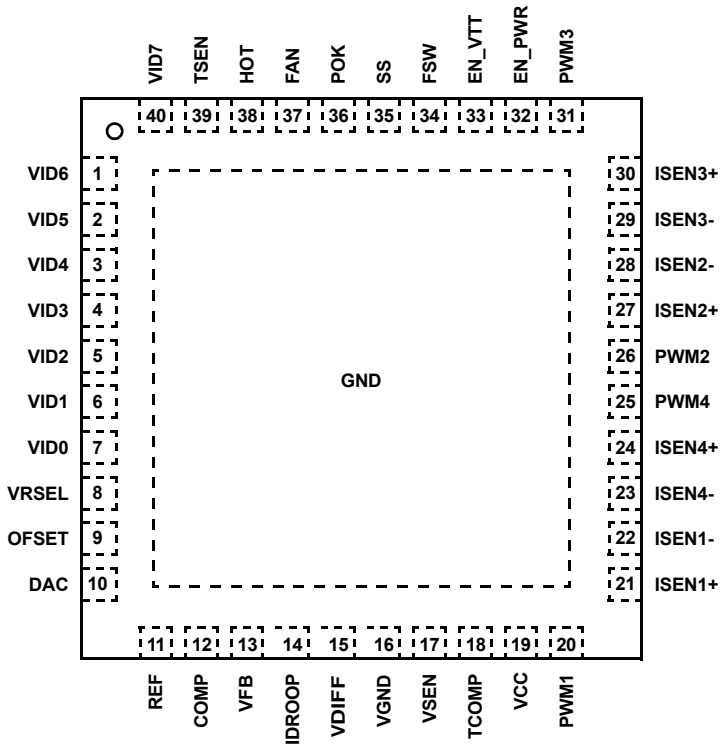
PART NUMBER (Note)	PART MARKING	TEMP. (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
EC7401QI	EC7401	-40 to +85	40 Ld 6x6 QFN	L40.6x6

*Add “-T” suffix for tape and reel.

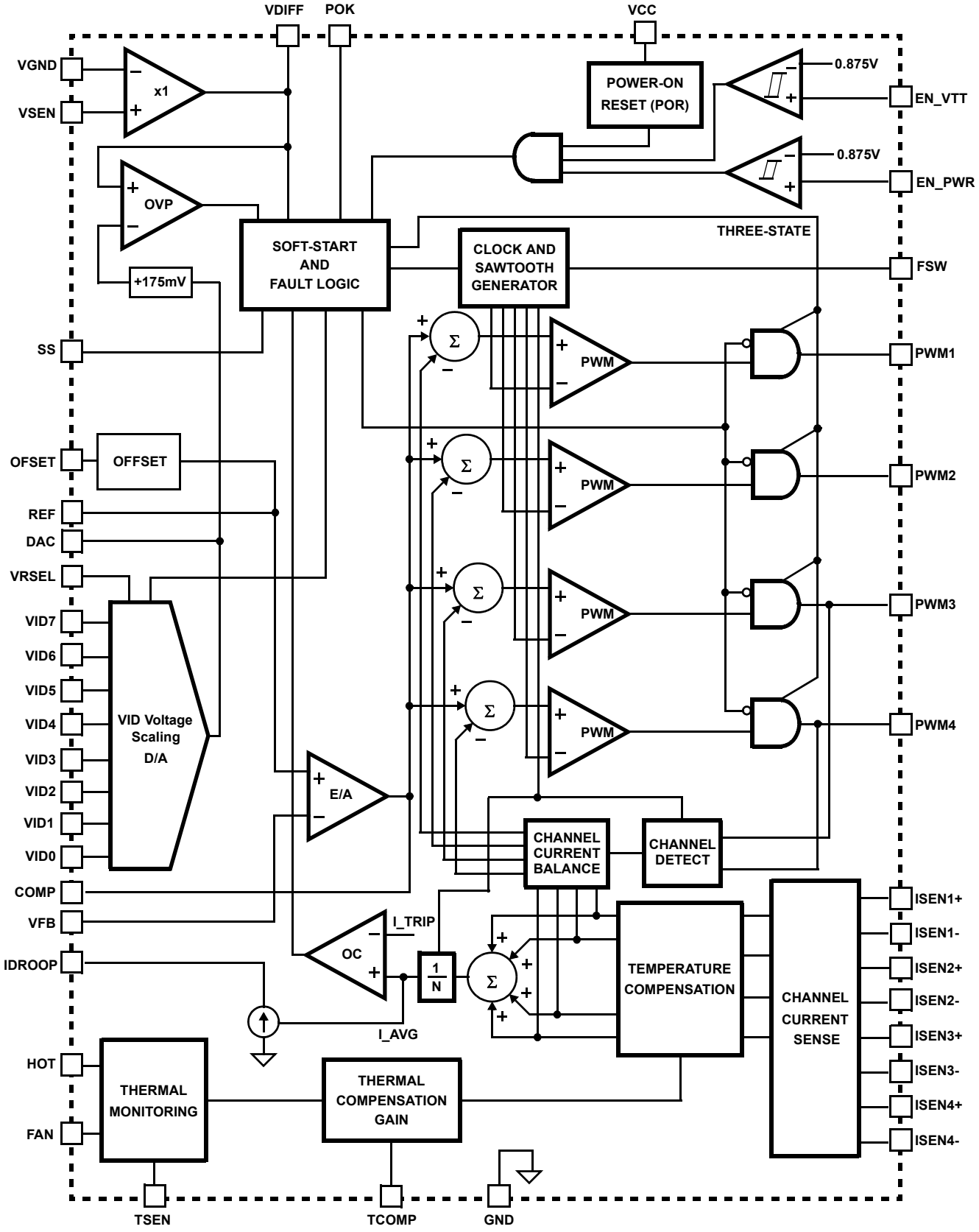
NOTE: These Altera Enpirion Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Altera Enpirion Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Configuration

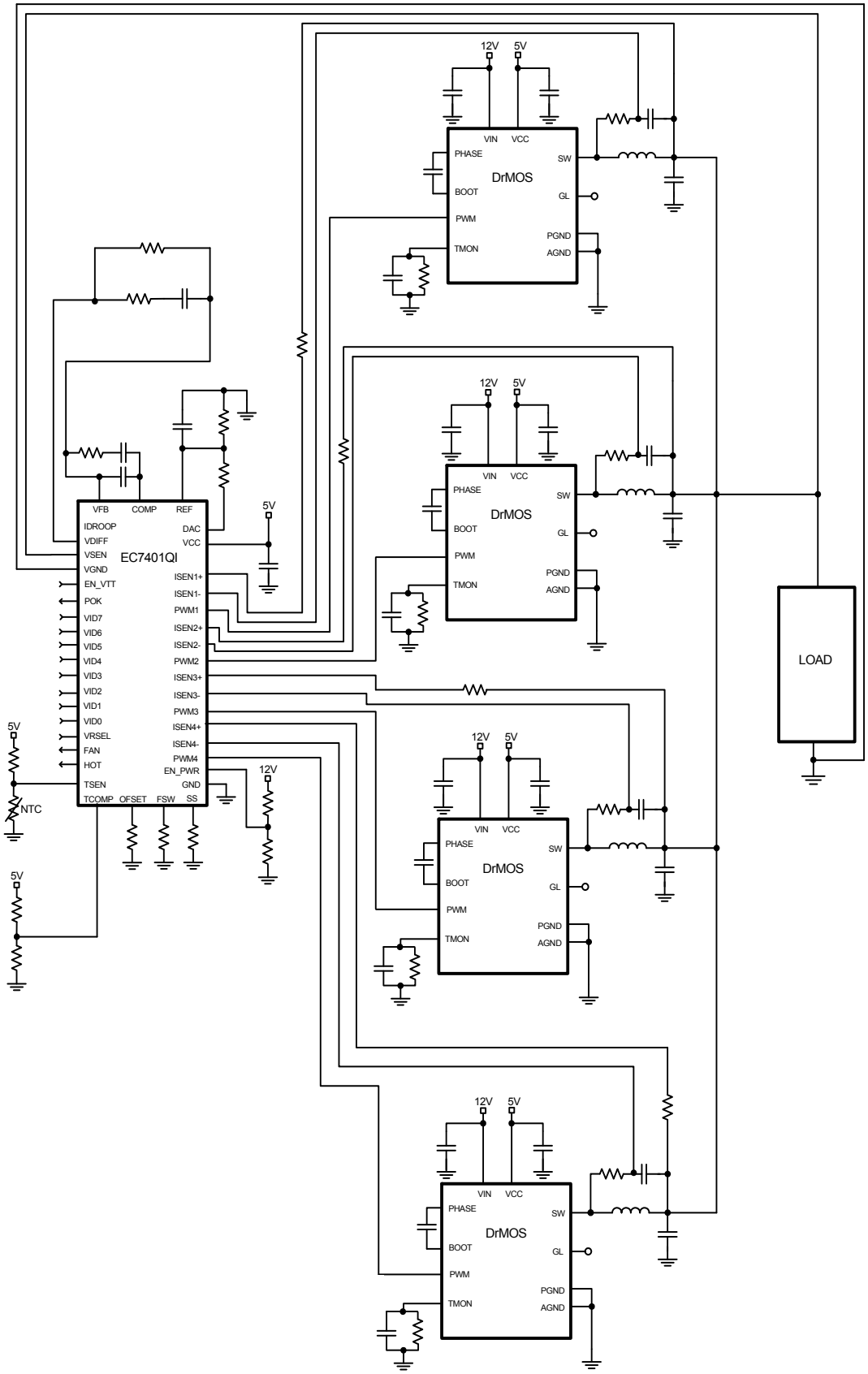
EC7401QI
(40 LD QFN)
TOP VIEW



EC7401QI Block Diagram



Typical Application - 4-Phase Buck Converter with DCR Sensing and External TCOMP



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . +6V
All Pins . . . . . GND -0.3V to VCC + 0.3V
ESD Ratings
Human body model . . . . . >2kV
Machine model . . . . . >200V
Charged device model . . . . . >1.5kV

Thermal Information

Thermal Resistance (Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package	34	6.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . —

Operating Conditions

Supply Voltage (VCC) . . . . . +5V ±5%
Ambient Temperature
EC7401QI . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Operating Conditions: VCC = 5V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT					
	VCC = 5VDC; EN_PWR = 5VDC; R_T = 100kΩ, ISEN1 = ISEN2 = ISEN3 = ISEN4 = -70µA	-	15	20	mA
	VCC = 5VDC; EN_PWR = 0VDC; R_T = 100kΩ	-	10	12	mA
POR Threshold	VCC Rising	4.3	4.5	4.7	V
	VCC Falling	3.7	3.9	4.2	V
EN_PWR Threshold	Nominal Supply	0.850	0.875	0.910	V
	Shutdown Supply	-	130	-	mV
	POWER-ON RESET AND ENABLE				
EN_VTT Threshold	Rising	0.850	0.875	0.910	V
	Hysteresis	-	130	-	mV
	Falling	0.720	0.745	0.775	V
REFERENCE VOLTAGE AND DAC					
System Accuracy of EC7401QI (VID = 1V to 1.6V, **T_J = -40°C to +85°C**)	**(Note 3)**	-0.6	-	0.6	%VID
System Accuracy of EC7401QI (VID = 0.5V to 1V, **T_J = -40°C to +85°C**)	**(Note 3)**	-1	-	1	%VID
VID Pull-up		-60	-40	-20	µA
VID Input Low Level		-	-	0.4	V
VID Input High Level		0.8	-	-	V
VRSEL Input Low Level		-	-	0.4	V
VRSEL Input High Level		0.8	-	-	V
DAC Source Current		-	4	7	mA
DAC Sink Current		-	-	300	µA

Electrical Specifications Operating Conditions: VCC = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
REF Source Current		45	50	55	µA
REF Sink Current		45	50	55	µA
PIN-ADJUSTABLE OFFSET					
Voltage at OFSET Pin of EC7401QI	Offset resistor connected to ground	388	400	412	mV
	Voltage below VCC, offset resistor connected to VCC	1.552	1.600	1.648	V
OSCILLATORS					
Accuracy of Switching Frequency Setting	R_T = 100kΩ	225	250	275	kHz
Adjustment Range of Switching Frequency	**(Note 4)**	0.08	-	1.0	MHz
Soft-Start Ramp Rate	R_S = 100kΩ (Notes 5, 6)	-	1.563	-	mV/µs
Adjustment Range of Soft-start Ramp Rate	**(Note 4)**	0.625	-	6.25	mV/µs
PWM GENERATOR					
Sawtooth Amplitude		-	1.5	-	V
Max Duty Cycle		-	66.7	-	%
ERROR AMPLIFIER					
Open-Loop Gain	R_L = 10kΩ to ground **(Note 4)**	-	96	-	dB
Open-Loop Bandwidth	C_L = 100pF, R_L = 10kΩ to ground **(Note 4)**	-	20	-	MHz
Slew Rate	C_L = 100pF	-	9	-	V/µs
Maximum Output Voltage		3.8	4.3	4.9	V
Output High Voltage @ 2mA		3.6	-	-	V
Output Low Voltage @ 2mA		-	-	1.2	V
REMOTE-SENSE AMPLIFIER					
Bandwidth	**(Note 4)**	-	20	-	MHz
Output High Current	VSEN - VGND = 2.5V	-500	-	500	µA
Output High Current	VSEN - VGND = 0.6	-500	-	500	µA
PWM OUTPUT					
PWM Output Voltage LOW Threshold	I_{LOAD} = ±500µA	-	-	0.5	V
PWM Output Voltage HIGH Threshold	I_{LOAD} = ±500µA	4.3	-	-	V
SENSE CURRENT OUTPUT (IDROOP and IOUT)					
Sensed Current Tolerance	ISEN1 = ISEN2 = ISEN3 = ISEN4 = 80µA	76	80	84	µA
Overcurrent Trip Level		90	100	110	µA
Maximum Voltage at IDROOP Pin		-	2	-	V
THERMAL MONITORING AND FAN CONTROL					
TSEN Input Voltage for FAN Trip		1.6	1.65	1.69	V
TSEN Input Voltage for FAN Reset		1.89	1.93	1.98	V
TSEN Input Voltage for HOT Trip		1.35	1.4	1.44	V
TSEN Input Voltage for HOT Reset		1.6	1.65	1.69	V
Leakage Current of FAN	With externally pull-up resistor connected to VCC	-	-	30	µA

Electrical Specifications Operating Conditions: VCC = 5V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
FAN Low Voltage	With 1.25k resistor pull-up to VCC, I_{FAN} = 4mA	-	-	0.3	V
Leakage Current of HOT	With externally pull-up resistor connected to VCC	-	-	30	µA
HOT Low Voltage	With 1.25k resistor pull-up to VCC, I_{HOT} = 4mA	-	-	0.3	V
VR READY AND PROTECTION MONITORS					
Leakage Current of POK	With externally pull-up resistor connected to VCC	-	-	30	µA
POK Low Voltage	I_{POK} = 4mA	-	-	0.3	V
Undervoltage Threshold	VDIFF Falling	48	50	52	%VID
POK Reset Voltage	VDIFF Rising	58	60	62	%VID
Overvoltage Protection Threshold	Before valid VID	1.250	1.275	1.300	V
	After valid VID, the voltage above VID	150	175	200	mV
Overvoltage Protection Reset Threshold		0.38	0.40	0.42	V

NOTES:

3. These parts are designed and adjusted for accuracy with all errors in the voltage loop included.
4. Limits established by characterization and are not production tested.
5. During soft-start, VDAC rises from 0 to 1.1V first and then ramp to VID voltage after receiving valid VID.
6. Soft-start ramp rate is determined by the adjustable soft-start oscillator frequency at the speed of 6.25mV per cycle.

Functional Pin Description

VCC

Supplies the power necessary to operate the chip. The controller starts to operate when the voltage on this pin exceeds the rising POR threshold and shuts down when the voltage on this pin drops below the falling POR threshold. Connect this pin directly to a +5V supply.

GND

Bias and reference ground for the IC. The bottom metal base of EC7401QI is the GND.

EN_PWR

This pin is a threshold-sensitive enable input for the controller. Connecting the 12V supply to EN_PWR through an appropriate resistor divider provides a means to synchronize power-up of the controller and the MOSFET driver ICs. When EN_PWR is driven above 0.875V, the EC7401QI is active depending on status of EN_VTT, the internal POR, and pending fault states. Driving EN_PWR below 0.745V will clear all fault states and prime the EC7401QI to soft-start when re-enabled.

EN_VTT

This pin is another threshold-sensitive enable input for the controller. It's typically connected to VTT output of VTT voltage regulator in the computer mother board. When EN_VTT is driven above 0.875V, the EC7401QI is active depending on status of ENLL, the internal POR, and pending fault states. Driving EN_VTT below 0.745V will clear all fault states and prime the EC7401QI to soft-start when re-enabled.

FSW

Use this pin to set up the desired switching frequency. A resistor, placed from FSW to ground will set the switching frequency. The relationship between the value of the resistor and the switching frequency will be described by an approximate equation.

SS

Use this pin to set up the desired start-up oscillator frequency. A resistor, placed from SS to ground will set up the soft-start ramp rate. The relationship between the value of the resistor and the soft-start ramp-up time will be described by an approximate equation.

VID7, VID6, VID5, VID4, VID3, VID2, VID1 and VID0

These are the inputs to the internal DAC that generates the reference voltage for output regulation. Connect these pins either to open-drain outputs with or without external pull-up resistors or to active pull-up outputs. All VID pins have 40µA internal pull-up current sources that diminish to zero as the voltage rises above the logic-high level. These inputs can be pulled up externally as high as VCC plus 0.3V.

When an OFF VID code causes shut-down, the controller needs to be reset before it starts again.

VRSEL

Use this pin to select Internal VID code. When it is connected to GND, the extended VR10 code is selected. When it's floated or pulled to high, VR11 code is selected. This input can be pulled up as high as VCC plus 0.3V.

VDIFF, VSEN, and VGND

VSEN and VGND form the precision differential remote-sense amplifier. This amplifier converts the differential voltage of the remote output to a single-ended voltage referenced to local ground. VDIFF is the amplifier's output and the input to the regulation and protection circuitry. Connect VSEN and VGND to the sense pins of the remote load.

VFB and COMP

Inverting input and output of the error amplifier respectively. VFB can be connected to VDIFF through a resistor. A properly chosen resistor between VDIFF and VFB can set the load line (droop), when IDROOP pin is tied to VFB pin. The droop scale factor is set by the ratio of the ISEN resistors and the inductor DCR or the lower MOSFET R_{DS}(ON). COMP is tied back to VFB through an external RC network to compensate the regulator.

DAC and REF

The DAC pin is the output of the precision internal DAC reference. The REF pin is the positive input of the Error Amplifier. In typical applications, a 1kΩ, 1% resistor is used between DAC and REF to generate a precision offset voltage. This voltage is proportional to

the offset current determined by the offset resistor from OFSET to ground or VCC. A capacitor is used between REF and ground to smooth the voltage transition during VID Voltage Scaling operations.

PWM1, PWM2, PWM3, PWM4

Pulse width modulation outputs. Connect these pins to the PWM input pins of the Altera Enpirion driver IC. The number of active channels is determined by the state of PWM3 and PWM4. Tie PWM3 to VCC to configure for 2-phase operation. Tie PWM4 to VCC to configure for 3-phase operation.

ISEN1+, ISEN1-; ISEN2+, ISEN2-; ISEN3+, ISEN3-; ISEN4+ and ISEN4

The ISEN+ and ISEN- pins are current sense inputs to individual differential amplifiers. The sensed current is used for channel current balancing, overcurrent protection, and droop regulation. Inactive channels should have their respective current sense inputs left open (for example, open ISEN4+ and ISEN4- for 3-phase operation).

For DCR sensing, connect each ISEN- pin to the node between the RC sense elements. Tie the ISEN+ pin to the other end of the sense capacitor through a resistor, R_{ISEN}. The voltage across the sense capacitor is proportional to the inductor current. Therefore, the sense current is proportional to the inductor current and scaled by the DCR of the inductor and R_{ISEN}.

When configured for $R_{DS}(ON)$ current sensing, the ISEN1-, ISEN2-, ISEN3-, and ISEN4- pins are grounded at the lower MOSFET sources. The ISEN1+, ISEN2+, ISEN3+, and ISEN4+ pins are then held at a virtual ground. Therefore, a resistor, connected between these current sense pins and the drain terminals of the associated lower MOSFET, will carry the current proportional to the current flowing through that channel. The sensed current is determined by the negative voltage across the lower MOSFET when it is ON, which is the channel current scaled by $R_{DS}(ON)$ and R_{ISEN}.

POK

POK indicates that the soft-start is completed and the output voltage is within the regulated range around VID setting. It is an open-drain logic output. When OCP or OVP occurs, POK will be pulled to low. It will also be pulled low if the output voltage is below the undervoltage threshold.

OFSET

The OFSET pin provides a means to program a DC offset current for generating a DC offset voltage at the REF input. The offset current is generated via an external resistor and precision internal voltage references. The polarity of the offset is selected by connecting the resistor to GND or VCC. For no offset, the OFSET pin should be left unterminated.

TCOMP

Temperature compensation scaling input. The voltage sensed on the TSEN pin is utilized as the temperature input to adjust ldroop and the overcurrent protection limit to effectively compensate for the temperature coefficient of the current sense element. To implement the integrated temperature compensation, a resistor divider circuit is needed with one resistor being connected from TCOMP to VCC of the controller and another resistor being connected from TCOMP to GND. Changing the ratio of the resistor values will set the gain of the integrated thermal compensation. When integrated temperature compensation function is not used, connect TCOMP to GND.

IDROOP

IDROOP is the output pin of sensed average channel current which is proportional to load current. In the application which does not require loadline, leave this pin open. In the application which requires load line, connect this pin to VFB so that the sensed average current will flow through the resistor between VFB and VDIFF to create a voltage drop which is proportional to load current.

TSEN

TSEN is an input pin for VR temperature measurement. Connect this pin through NTC thermistor to GND and a resistor to VCC of the controller. The voltage at this pin is reverse proportional to VR temperature. EC7401QI monitors the VR temperature based on the voltage at TSEN pin and outputs HOT and FAN signals.

HOT

HOT is used as an indication of high VR temperature. It is an open-drain logic output. It will be open when the measured VR temperature reaches a certain level.

FAN

FAN is an output pin with open-drain logic output. It will be open when the measured VR temperature reaches a certain level.

Operation

Multiphase Power Conversion

Microprocessor load current profiles have changed to the point that the advantages of multiphase power conversion are impossible to ignore. The technical challenges associated with producing a single-phase converter which is both cost-effective and thermally viable have forced a change to the cost-saving approach of multiphase. The EC7401QI controller helps reduce the complexity of implementation by integrating vital functions and requiring minimal output components. The block diagram on page 4 provides top level views of multiphase power conversion using the EC7401QI controller.

Interleaving

The switching of each channel in a multiphase converter is timed to be symmetrically out of phase with each of the other channels. In a 3-phase converter, each channel switches 1/3 cycle after the previous channel and 1/3 cycle before the following channel. As a result, the 3-phase converter has a combined ripple frequency three times greater than the ripple frequency of any one phase. In addition, the peak-to-peak amplitude of the combined inductor currents is reduced in proportion to the number of phases (Equations 1 and 2). Increased ripple frequency and lower ripple amplitude mean that the designer can use less per-channel inductance and lower total output capacitance for any performance specification.

Figure 1 illustrates the multiplicative effect on output ripple frequency. The three channel currents (IL1, IL2, and IL3) combine to form the AC ripple current and the DC load current. The ripple component has three times the ripple frequency of each individual channel current. Each PWM pulse is terminated 1/3 of a cycle after the PWM pulse of the previous phase. The peak-to-peak current for each phase is about 7A, and the DC components of the inductor currents combine to feed the load.

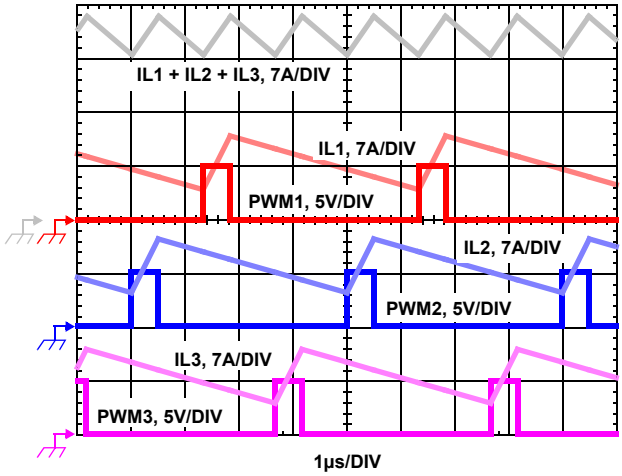


FIGURE 1. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 3-PHASE CONVERTER

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 1 which represents an individual channel's peak-to-peak inductor current.

$$I_{P\text{-}P} = \frac{(V_{IN} - V_{OUT})V_{OUT}}{L f_{SW} V_{IN}} \qquad \textbf{(EQ. 1)}$$

In Equation 1, V_{IN} and V_{OUT} are the input and output voltages respectively, L is the single-channel inductor value, and f_{SW} is the switching frequency.

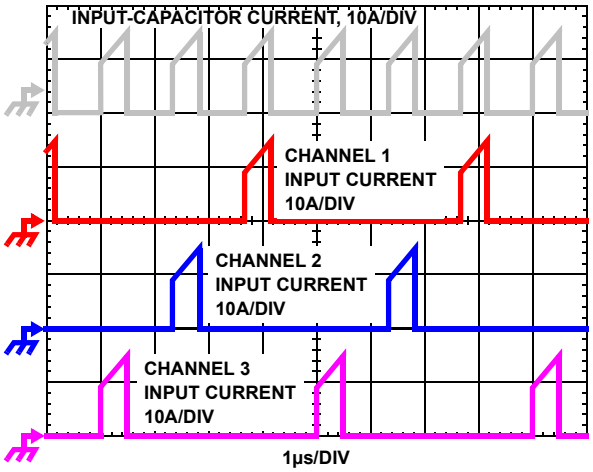


FIGURE 2. CHANNEL INPUT CURRENTS AND INPUT-CAPACITOR RMS CURRENT FOR THREE-PHASE CONVERTER

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels. Compare Equation 1 to the expression for the peak-to-peak current after the summation of N symmetrically phase-shifted inductor currents in Equation 2. Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors.

$$I_{C,P\text{-}P} = \frac{(V_{IN} - N\,V_{OUT})\,V_{OUT}}{L\,f_{SW}\,V_{IN}} \qquad \textbf{(EQ. 2)}$$

Another benefit of interleaving is to reduce input ripple current. Input capacitance is determined in part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 2 illustrates input currents from a 3-phase converter combining to reduce the total input ripple current.

The converter depicted in Figure 2 delivers 36A to a 1.5V load from a 12V input. The RMS input capacitor current is 5.9A. Compare this to a single-phase converter also stepping down 12V to 1.5V at 36A. The single-phase converter has 11.9A RMS input capacitor current. The single-phase converter must use an input capacitor bank with twice the RMS current capacity as the equivalent 3-phase converter.

Figures 21, 22 and 23 in the section entitled “Input Capacitor Selection” on page 41, can be used to determine the input-capacitor RMS current based on load current, duty cycle, and the number of channels. They are provided as aids in determining the optimal input capacitor solution. Figure 23 shows the single-phase input-capacitor RMS current for comparison.

PWM Operation

The timing of each channel is set by the number of active channels. The default channel setting for the EC7401QI is four. The switching cycle is defined as the time between PWM pulse termination signals of each channel. The pulse termination signal is an internally generated clock signal which triggers the falling edge of PWM signal. The cycle time of the pulse termination signal is the inverse of the switching frequency set by the resistor between the FSW pin and ground. Each cycle begins when the clock signal commands the channel PWM signal to go low. The PWM signals command the MOSFET driver to turn on/off the channel MOSFETs.

For 4-channel operation, the channel firing order is 4-3-2-1: PWM3 pulse terminates 1/4 of a cycle after PWM4, PWM2 output follows another 1/4 of a cycle after PWM3, and PWM1 terminates another 1/4 of a cycle after PWM2. For 3-channel operation, the channel firing order is 3-2-1.

Connecting PWM4 to VCC selects three channel operation and the pulse-termination times are spaced in 1/3 cycle increments. If PWM3 is connected to VCC, two channel operation is selected and the PWM2 pulse terminates 1/2 of a cycle later.

Once a PWM signal transitions low, it is held low for a minimum of 1/3 cycle. This forced off time is required to ensure an accurate current sample. Current sensing is described in the next section. After the forced off time expires, the PWM output is enabled. The PWM output state is driven by the position of the error amplifier output signal, V_{COMP}, minus the current correction

signal relative to the sawtooth ramp as illustrated in Figure 7. When the modified V_{COMP} voltage crosses the sawtooth ramp, the PWM output transitions high. The MOSFET driver detects the change in state of the PWM signal and turns off the synchronous MOSFET and turns on the upper MOSFET. The PWM signal will remain high until the pulse termination signal marks the beginning of the next cycle by triggering the PWM signal low.

Current Sampling

During the forced off-time following a PWM transition low, the associated channel current sense amplifier uses the I_{SEN} inputs to reproduce a signal proportional to the inductor current (I_L). This current gets sampled starting 1/6 period after each PWM goes low and continuously gets sampled for 1/3 period, or until the PWM goes high, whichever comes first. No matter the current sense method, the sense current (I_{SEN}) is simply a scaled version of the inductor current. Coincident with the falling edge of the PWM signal, the sample and hold circuitry samples the sensed current signal (I_{SEN}) as illustrated in Figure 3.

Therefore, the sample current (I_n) is proportional to the output current and held for one switching cycle. The sample current is used for current balance, load-line regulation, and overcurrent protection.

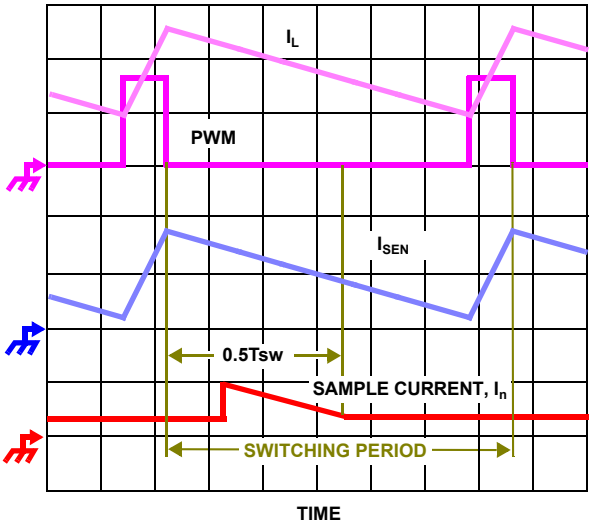


FIGURE 3. SAMPLE AND HOLD TIMING

Current Sensing

The EC7401QI supports inductor DCR sensing, MOSFET $R_{DS}(ON)$ sensing, or resistive sensing techniques. The internal circuitry, shown in Figures 4, 5, and 6, represents one channel of an N-channel converter. This circuitry is repeated for each channel in the converter, but may not be active depending on the status of the PWM3 and PWM4 pins, as described in “PWM Operation” on page 12.

INDUCTOR DCR SENSING

An inductor's winding is characteristic of a distributed resistance as measured by the DCR (Direct Current Resistance) parameter. Consider the inductor DCR as a separate lumped quantity, as shown in Figure 4. The channel current (I_L) flowing through the inductor, will also pass through the DCR. Equation 3 shows the s-domain equivalent voltage across the inductor V_L.

$$V_L = I_L \cdot (s \cdot L + DCR) \quad \textbf{(EQ. 3)}$$

A simple RC network across the inductor extracts the DCR voltage, as shown in Figure 4.

The voltage on the capacitor (V_C) can be shown to be proportional to the channel current (I_L) see Equation 4.

$$V_C = \frac{\left(s \cdot \frac{L}{DCR} + 1\right) \cdot (DCR \cdot I_L)}{(s \cdot RC + 1)} \quad \textbf{(EQ. 4)}$$

If the RC network components are selected such that the RC time constant (= R*C) matches the inductor time constant (= L/DCR), the voltage across the capacitor (V_C) is equal to the voltage drop across the DCR (i.e., proportional to the channel current).

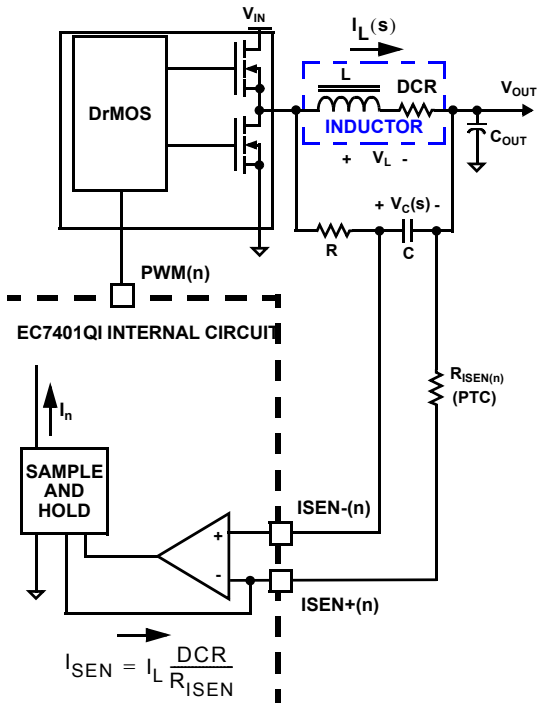


FIGURE 4. DCR SENSING CONFIGURATION

With the internal low-offset current amplifier, the capacitor voltage (V_C) is replicated across the sense resistor (R_{ISEN}). Therefore the current out of ISEN+ pin (I_{SEN}) is proportional to the inductor current.

Equation 5 shows that the ratio of the channel current to the sensed current (I_{SEN}) is driven by the value of the sense resistor and the DCR of the inductor.

$$I_{SEN} = I_L \cdot \frac{DCR}{R_{ISEN}} \quad \textbf{(EQ. 5)}$$

RESISTIVE SENSING

For accurate current sense, a dedicated current-sense resistor (R_{SENSE}) in series with each output inductor can serve as the current sense element (see Figure 5). This technique is more accurate, but reduces overall converter efficiency due to the additional power loss on the current sense element (R_{SENSE}).

Equation 6 shows the ratio of the channel current to the sensed current (I_{SEN}).

$$I_{SEN} = I_L \cdot \frac{R_{SENSE}}{R_{ISEN}} \quad \text{(EQ. 6)}$$

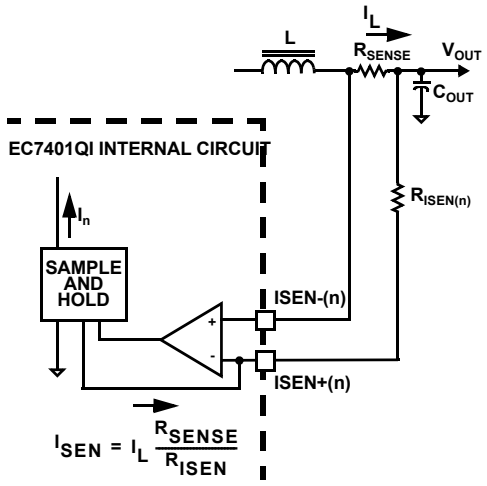


FIGURE 5. SENSE RESISTOR IN SERIES WITH INDUCTORS

MOSFET R_{DS}(ON) SENSING

The controller can also sense the channel load current by sampling the voltage across the lower MOSFET R_{DS}(ON) (see Figure 6). The amplifier is ground-reference by connecting the ISEN- pin to the source of the lower MOSFET. ISEN+ pin is connected to the PHASE node through the current sense resistor (R_{ISEN}). The voltage across R_{ISEN} is equivalent to the voltage drop across the R_{DS}(ON) of the lower MOSFET while it is conducting. The resulting current out of the ISEN+ pin is proportional to the channel current I_L.

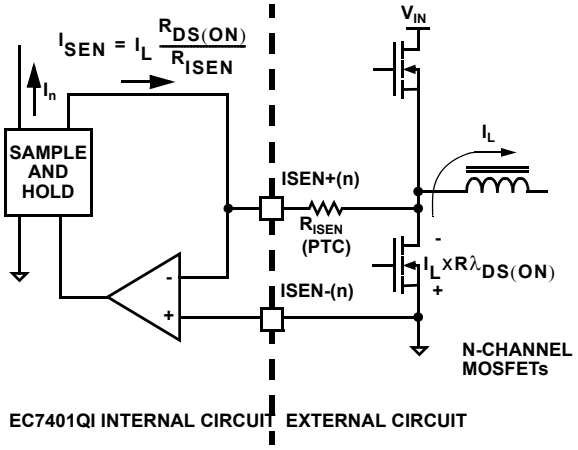


FIGURE 6. MOSFET R_{DS}(ON) CURRENT-SENSING CIRCUIT

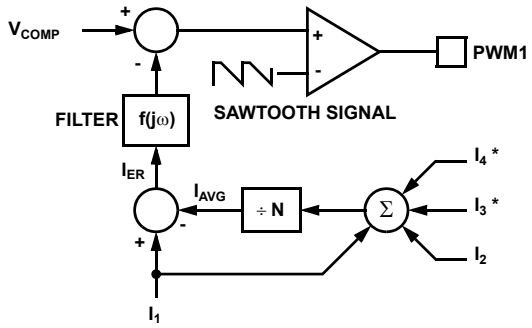
Equation 7 shows the ratio of the channel current to the sensed current I_{SEN}.

$$I_{SEN} = I_L \frac{R_{DS(ON)}}{R_{ISEN}} \quad \text{(EQ. 7)}$$

Both inductor DCR and MOSFET R_{DS}(ON) value will increase as the temperature increases. Therefore the sensed current will increase as the temperature of the current sense element increases. In order to compensate the temperature effect on the sensed current signal, a Positive Temperature Coefficient (PTC) resistor can be selected for the sense resistor (R_{ISEN}), or the integrated temperature compensation function of EC7401QI should be utilized. The integrated temperature compensation function is described in “Temperature Compensation” on page 33.

Channel-Current Balance

The sensed current (I_N) from each active channel are summed together and divided by the number of active channels. The resulting average current (I_{AVG}) provides a measure of the total load current. Channel current balance is achieved by comparing the sampled current of each channel to the average current to make an appropriate adjustment to the WPM duty cycle of each channel. The current-balance method is illustrated in Figure 7. In the figure, the average current combines with the Channel 1 current (I_1) to create an error signal (I_{ER}). The filtered error signal modifies the pulse width commanded by V_{COMP} to correct any unbalance and force I_{ER} toward zero. The same method for error signal correction is applied to each active channel.



NOTE: *Channels 3 and 4 are optional for 2 or 3 phase designs.

FIGURE 7. CHANNEL 1 PWM FUNCTION AND CURRENT-BALANCE ADJUSTMENT

Channel current balance is essential in achieving the thermal advantage of multiphase operation. With good current balance, the power loss is equally dissipated over multiple devices and a greater area.

Voltage Regulation

The compensation network shown in Figure 8 assures that the steady-state error in the output voltage is limited only to the error in the reference voltage (output of the DAC) and offset errors in the OFSET current source, remote-sense and error amplifiers. Altera specifies the guaranteed tolerance of the EC7401QI to include the combined tolerances of each of these elements.

The output of the error amplifier (V_{COMP}) is compared to the sawtooth waveform to generate the PWM signals. The PWM signals control the timing of the MOSFET drivers and regulate the converter output to the specified reference voltage. The internal and external circuitry, which control voltage regulation, are illustrated in Figure 8.

The EC7401QI incorporates an internal differential remote-sense amplifier in the feedback path. The amplifier removes the voltage error encountered when measuring the output voltage relative to the local controller ground reference point resulting in a more accurate means of sensing output voltage. Connect the microprocessor sense pins to the non-inverting input, V_{SEN}, and inverting input, VGND, of the remote-sense amplifier. The remote-sense output (V_{DIF}), is connected to the inverting input of the error amplifier through an external resistor.

A digital-to-analog converter (DAC) generates a reference voltage based on the state of logic signals at pins VID7 through VID0. The DAC decodes the 8 6-bit logic signal (VID) into one of the discrete voltages shown in Table 1. Each VID input offers a 45µA pull-up to an internal 2.5V source for use with open-drain outputs. The pull-up current diminishes to zero above the logic threshold to protect voltage-sensitive output devices. External pull-up resistors can augment the pull-up current sources if case leakage into the driving device is greater than 45µA.

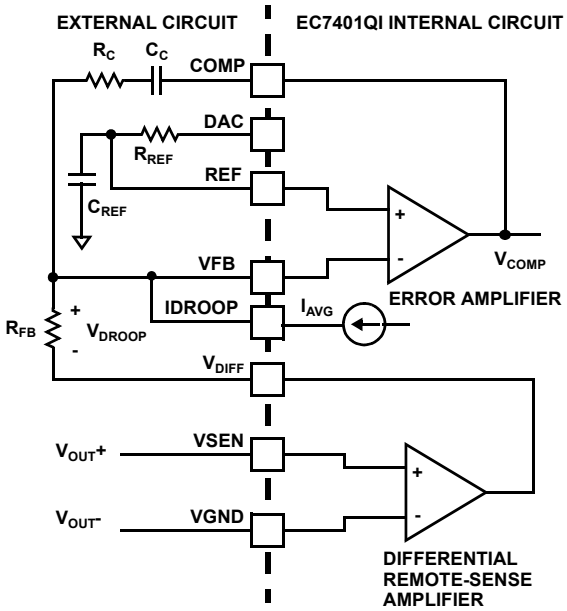


FIGURE 8. OUTPUT VOLTAGE AND LOAD-LINE REGULATION WITH OFFSET ADJUSTMENT

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
0	1	0	1	0	1	1	1.60000
0	1	0	1	0	1	0	1.59375
0	1	0	1	1	0	1	1.58750
0	1	0	1	1	0	0	1.58125
0	1	0	1	1	1	1	1.57500
0	1	0	1	1	1	0	1.56875
0	1	1	0	0	0	1	1.56250
0	1	1	0	0	0	0	1.55625
0	1	1	0	0	1	1	1.55000
0	1	1	0	0	1	0	1.54375
0	1	1	0	1	0	1	1.53750
0	1	1	0	1	0	0	1.53125
0	1	1	0	1	1	1	1.52500
0	1	1	0	1	1	0	1.51875
0	1	1	1	0	0	1	1.51250
0	1	1	1	0	0	0	1.50625
0	1	1	1	0	1	1	1.50000
0	1	1	1	0	1	0	1.49375
0	1	1	1	1	0	1	1.48750
0	1	1	1	1	0	0	1.48125
0	1	1	1	1	1	1	1.47500
0	1	1	1	1	1	0	1.46875
1	0	0	0	0	0	1	1.46250
1	0	0	0	0	0	0	1.45625
1	0	0	0	0	1	1	1.45000
1	0	0	0	0	1	0	1.44375
1	0	0	0	1	0	1	1.43750
1	0	0	0	1	0	0	1.43125
1	0	0	0	1	1	1	1.42500
1	0	0	0	1	1	0	1.41875
1	0	0	1	0	0	1	1.41250
1	0	0	1	0	0	0	1.40625
1	0	0	1	0	1	1	1.40000
1	0	0	1	0	1	0	1.39375
1	0	0	1	1	0	1	1.38750
1	0	0	1	1	0	0	1.38125
1	0	0	1	1	1	1	1.37500
1	0	0	1	1	1	0	1.36875

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
1	0	1	0	0	0	1	1.36250
1	0	1	0	0	0	0	1.35625
1	0	1	0	0	1	1	1.35000
1	0	1	0	0	1	0	1.34375
1	0	1	0	1	0	1	1.33750
1	0	1	0	1	0	0	1.33125
1	0	1	0	1	1	1	1.32500
1	0	1	0	1	1	0	1.31875
1	0	1	1	0	0	1	1.31250
1	0	1	1	0	0	0	1.30625
1	0	1	1	0	1	1	1.30000
1	0	1	1	0	1	0	1.29375
1	0	1	1	1	0	1	1.28750
1	0	1	1	1	0	0	1.28125
1	0	1	1	1	1	1	1.27500
1	0	1	1	1	1	0	1.26875
1	1	0	0	0	0	1	1.26250
1	1	0	0	0	0	0	1.25625
1	1	0	0	0	1	1	1.25000
1	1	0	0	0	1	0	1.24375
1	1	0	0	1	0	1	1.23750
1	1	0	0	1	0	0	1.23125
1	1	0	0	1	1	1	1.22500
1	1	0	0	1	1	0	1.21875
1	1	0	1	0	0	1	1.21250
1	1	0	1	0	0	0	1.20625
1	1	0	1	0	1	1	1.20000
1	1	0	1	0	1	0	1.19375
1	1	0	1	1	0	1	1.18750
1	1	0	1	1	0	0	1.18125
1	1	0	1	1	1	1	1.17500
1	1	0	1	1	1	0	1.16875
1	1	1	0	0	0	1	1.16250
1	1	1	0	0	0	0	1.15625
1	1	1	0	0	1	1	1.15000
1	1	1	0	0	1	0	1.14375
1	1	1	0	1	0	1	1.13750
1	1	1	0	1	0	0	1.13125

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
1	1	1	0	1	1	1	1.12500
1	1	1	0	1	1	0	1.11875
1	1	1	1	0	0	1	1.11250
1	1	1	1	0	0	0	1.10625
1	1	1	1	0	1	1	1.10000
1	1	1	1	0	1	0	1.09375
1	1	1	1	1	0	1	OFF
1	1	1	1	1	0	0	OFF
1	1	1	1	1	1	1	OFF
1	1	1	1	1	1	0	OFF
0	0	0	0	0	0	1	1.08750
0	0	0	0	0	0	0	1.08125
0	0	0	0	0	1	1	1.07500
0	0	0	0	0	1	0	1.06875
0	0	0	0	1	0	1	1.06250
0	0	0	0	1	0	0	1.05625
0	0	0	0	1	1	1	1.05000
0	0	0	0	1	1	0	1.04375
0	0	0	1	0	0	1	1.03750
0	0	0	1	0	0	0	1.03125
0	0	0	1	0	1	1	1.02500
0	0	0	1	0	1	0	1.01875
0	0	0	1	1	0	1	1.01250
0	0	0	1	1	0	0	1.00625
0	0	0	1	1	1	1	1.00000
0	0	0	1	1	1	0	0.99375
0	0	1	0	0	0	1	0.98750
0	0	1	0	0	0	0	0.98125
0	0	1	0	0	1	1	0.97500
0	0	1	0	0	1	0	0.96875
0	0	1	0	1	0	1	0.96250
0	0	1	0	1	0	0	0.95625
0	0	1	0	1	1	1	0.95000
0	0	1	0	1	1	0	0.94375
0	0	1	1	0	0	1	0.93750
0	0	1	1	0	0	0	0.93125
0	0	1	1	0	1	1	0.92500
0	0	1	1	0	1	0	0.91875

TABLE 1. VR10 VID TABLE (WITH 6.25mV EXTENSION) (Continued)

VID4 400mV	VID3 200mV	VID2 100mV	VID1 50mV	VID0 25mV	VID5 12.5mV	VID6 6.25mV	VOLTAGE (V)
0	0	1	1	1	0	1	0.91250
0	0	1	1	1	0	0	0.90625
0	0	1	1	1	1	1	0.90000
0	0	1	1	1	1	0	0.89375
0	1	0	0	0	0	1	0.88750
0	1	0	0	0	0	0	0.88125
0	1	0	0	0	1	1	0.87500
0	1	0	0	0	1	0	0.86875
0	1	0	0	1	0	1	0.86250
0	1	0	0	1	0	0	0.85625
0	1	0	0	1	1	1	0.85000
0	1	0	0	1	1	0	0.84375
0	1	0	1	0	0	1	0.83750
0	1	0	1	0	0	0	0.83125

TABLE 2. VR11 VID 8 BIT

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	0	0	0	0	0	OFF
0	0	0	0	0	0	0	1	OFF
0	0	0	0	0	0	1	0	1.60000
0	0	0	0	0	0	1	1	1.59375
0	0	0	0	0	1	0	0	1.58750
0	0	0	0	0	1	0	1	1.58125
0	0	0	0	0	1	1	0	1.57500
0	0	0	0	0	1	1	1	1.56875
0	0	0	0	1	0	0	0	1.56250
0	0	0	0	1	0	0	1	1.55625
0	0	0	0	1	0	1	0	1.55000
0	0	0	0	1	0	1	1	1.54375
0	0	0	0	1	1	0	0	1.53750
0	0	0	0	1	1	0	1	1.53125
0	0	0	0	1	1	1	0	1.52500
0	0	0	0	1	1	1	1	1.51875
0	0	0	1	0	0	0	0	1.51250
0	0	0	1	0	0	0	1	1.50625
0	0	0	1	0	0	1	0	1.50000
0	0	0	1	0	0	1	1	1.49375
0	0	0	1	0	1	0	0	1.48750
0	0	0	1	0	1	0	1	1.48125

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	0	1	0	1	1	0	1.47500
0	0	0	1	0	1	1	1	1.46875
0	0	0	1	1	0	0	0	1.46250
0	0	0	1	1	0	0	1	1.45625
0	0	0	1	1	0	1	0	1.45000
0	0	0	1	1	0	1	1	1.44375
0	0	0	1	1	1	0	0	1.43750
0	0	0	1	1	1	0	1	1.43125
0	0	0	1	1	1	1	0	1.42500
0	0	0	1	1	1	1	1	1.41875
0	0	1	0	0	0	0	0	1.41250
0	0	1	0	0	0	0	1	1.40625
0	0	1	0	0	0	1	0	1.40000
0	0	1	0	0	0	1	1	1.39375
0	0	1	0	0	1	0	0	1.38750
0	0	1	0	0	1	0	1	1.38125
0	0	1	0	0	1	1	0	1.37500
0	0	1	0	0	1	1	1	1.36875
0	0	1	0	1	0	0	0	1.36250
0	0	1	0	1	0	0	1	1.35625
0	0	1	0	1	0	1	0	1.35000
0	0	1	0	1	0	1	1	1.34375
0	0	1	0	1	1	0	0	1.33750
0	0	1	0	1	1	0	1	1.33125
0	0	1	0	1	1	1	0	1.32500
0	0	1	0	1	1	1	1	1.31875
0	0	1	1	0	0	0	0	1.31250
0	0	1	1	0	0	0	1	1.30625
0	0	1	1	0	0	1	0	1.30000
0	0	1	1	0	0	1	1	1.29375
0	0	1	1	0	1	0	0	1.28750
0	0	1	1	0	1	0	1	1.28125
0	0	1	1	0	1	1	0	1.27500
0	0	1	1	0	1	1	1	1.26875
0	0	1	1	1	0	0	0	1.26250
0	0	1	1	1	0	0	1	1.25625
0	0	1	1	1	0	1	0	1.25000
0	0	1	1	1	0	1	1	1.24375
0	0	1	1	1	1	0	0	1.23750

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	0	1	1	1	1	0	1	1.23125
0	0	1	1	1	1	1	0	1.22500
0	0	1	1	1	1	1	1	1.21875
0	1	0	0	0	0	0	0	1.21250
0	1	0	0	0	0	0	1	1.20625
0	1	0	0	0	0	1	0	1.20000
0	1	0	0	0	0	1	1	1.19375
0	1	0	0	0	1	0	0	1.18750
0	1	0	0	0	1	0	1	1.18125
0	1	0	0	0	1	1	0	1.17500
0	1	0	0	0	1	1	1	1.16875
0	1	0	0	1	0	0	0	1.16250
0	1	0	0	1	0	0	1	1.15625
0	1	0	0	1	0	1	0	1.15000
0	1	0	0	1	0	1	1	1.14375
0	1	0	0	1	1	0	0	1.13750
0	1	0	0	1	1	0	1	1.13125
0	1	0	0	1	1	1	0	1.12500
0	1	0	0	1	1	1	1	1.11875
0	1	0	1	0	0	0	0	1.11250
0	1	0	1	0	0	0	1	1.10625
0	1	0	1	0	0	1	0	1.10000
0	1	0	1	0	0	1	1	1.09375
0	1	0	1	0	1	0	0	1.08750
0	1	0	1	0	1	0	1	1.08125
0	1	0	1	0	1	1	0	1.07500
0	1	0	1	0	1	1	1	1.06875
0	1	0	1	1	0	0	0	1.06250
0	1	0	1	1	0	0	1	1.05625
0	1	0	1	1	0	1	0	1.05000
0	1	0	1	1	0	1	1	1.04375
0	1	0	1	1	1	0	0	1.03750
0	1	0	1	1	1	0	1	1.03125
0	1	0	1	1	1	1	0	1.02500
0	1	0	1	1	1	1	1	1.01875
0	1	1	0	0	0	0	0	1.01250
0	1	1	0	0	0	0	1	1.00625
0	1	1	0	0	0	1	0	1.00000
0	1	1	0	0	0	1	1	0.99375

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
0	1	1	0	0	1	0	0	0.98750
0	1	1	0	0	1	0	1	0.98125
0	1	1	0	0	1	1	0	0.97500
0	1	1	0	0	1	1	1	0.96875
0	1	1	0	1	0	0	0	0.96250
0	1	1	0	1	0	0	1	0.95625
0	1	1	0	1	0	1	0	0.95000
0	1	1	0	1	0	1	1	0.94375
0	1	1	0	1	1	0	0	0.93750
0	1	1	0	1	1	0	1	0.93125
0	1	1	0	1	1	1	0	0.92500
0	1	1	0	1	1	1	1	0.91875
0	1	1	1	0	0	0	0	0.91250
0	1	1	1	0	0	0	1	0.90625
0	1	1	1	0	0	1	0	0.90000
0	1	1	1	0	0	1	1	0.89375
0	1	1	1	0	1	0	0	0.88750
0	1	1	1	0	1	0	1	0.88125
0	1	1	1	0	1	1	0	0.87500
0	1	1	1	0	1	1	1	0.86875
0	1	1	1	1	0	0	0	0.86250
0	1	1	1	1	0	0	1	0.85625
0	1	1	1	1	0	1	0	0.85000
0	1	1	1	1	0	1	1	0.84375
0	1	1	1	1	1	0	0	0.83750
0	1	1	1	1	1	0	1	0.83125
0	1	1	1	1	1	1	0	0.82500
0	1	1	1	1	1	1	1	0.81875
1	0	0	0	0	0	0	0	0.81250
1	0	0	0	0	0	0	1	0.80625
1	0	0	0	0	0	1	0	0.80000
1	0	0	0	0	0	1	1	0.79375
1	0	0	0	0	1	0	0	0.78750
1	0	0	0	0	1	0	1	0.78125
1	0	0	0	0	1	1	0	0.77500
1	0	0	0	0	1	1	1	0.76875
1	0	0	0	1	0	0	0	0.76250
1	0	0	0	1	0	0	1	0.75625
1	0	0	0	1	0	1	0	0.75000

TABLE 2. VR11 VID 8 BIT **(Continued)**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	VOLTAGE
1	0	0	0	1	0	1	1	0.74375
1	0	0	0	1	1	0	0	0.73750
1	0	0	0	1	1	0	1	0.73125
1	0	0	0	1	1	1	0	0.72500
1	0	0	0	1	1	1	1	0.71875
1	0	0	1	0	0	0	0	0.71250
1	0	0	1	0	0	0	1	0.70625
1	0	0	1	0	0	1	0	0.70000
1	0	0	1	0	0	1	1	0.69375
1	0	0	1	0	1	0	0	0.68750
1	0	0	1	0	1	0	1	0.68125
1	0	0	1	0	1	1	0	0.67500
1	0	0	1	0	1	1	1	0.66875
1	0	0	1	1	0	0	0	0.66250
1	0	0	1	1	0	0	1	0.65625
1	0	0	1	1	0	1	0	0.65000
1	0	0	1	1	0	1	1	0.64375
1	0	0	1	1	1	0	0	0.63750
1	0	0	1	1	1	0	1	0.63125
1	0	0	1	1	1	1	0	0.62500
1	0	0	1	1	1	1	1	0.61875
1	0	1	0	0	0	0	0	0.61250
1	0	1	0	0	0	0	1	0.60625
1	0	1	0	0	0	1	0	0.60000
1	0	1	0	0	0	1	1	0.59375
1	0	1	0	0	1	0	0	0.58750
1	0	1	0	0	1	0	1	0.58125
1	0	1	0	0	1	1	0	0.57500
1	0	1	0	0	1	1	1	0.56875
1	0	1	0	1	0	0	0	0.56250
1	0	1	0	1	0	0	1	0.55625
1	0	1	0	1	0	1	0	0.55000
1	0	1	0	1	0	1	1	0.54375
1	0	1	0	1	1	0	0	0.53750
1	0	1	0	1	1	0	1	0.53125
1	0	1	0	1	1	1	0	0.52500
1	0	1	0	1	1	1	1	0.51875
1	0	1	1	0	0	0	0	0.51250
1	0	1	1	0	0	0	1	0.50625