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EN29A0QI 10A Power Module

Step-Down DC-DC Switching Converter with Integrated Inductor

DESCRIPTION

The EN29A0QI is a member of the EN2900 family of PowerSoCs optimized for powering noise sensitive loads which require tight DC and AC tolerance such as transceiver, high speed IO, and RF. PowerSoC devices integrate the controller, MOSFETS, inductor, and high frequency bypass capacitors to provide a low noise, low ripple, easy to use power conversion solution.

The EN29A0QI offers very tight DC accuracy combined with remote ground sense to meet the challenging tolerance requirements for high speed transceivers. The inductor is sized to provide very low output switching ripple while the package is designed for low EMI. The loop topology is based on low impedance voltage mode control combined with a high-performance error amplifier for excellent transient performance. The wide bandwidth loop, combined with the low impedance voltage mode control can enable a significant reduction of expensive bulk decoupling capacitors.

The EN29A0QI features a bidirectional SYNC pin which enables synchronization from an external clock, or can provide a master clock output. Other features include precision enable threshold, glitch free startup into a pre-biased load, and programmable soft-start and soft-shutdown.

FEATURES

- Very low noise and ripple for transceiver power
- High accuracy VREF: 1% over Line, Load, Temp
- Remote ground sense for tight POL regulation
- Optimized for powering VCCR, VCCT, and VCCH
- High efficiency; V_{IN}=12V, V_{OUT}=1.0V; 86.5% @10A
- 10A continuous output current with no derating
- Wide input voltage range (9V to 16V)
- Bidirectional frequency synchronization
- High performance error amplifier
- Precision enable and POK for sequencing
- Programmable soft-start and soft-shutdown
- Full suite of protections: OCP, SCP, OTP, Input OVLO, UVLO, Output OVP with programmable threshold
- Monotonic startup into pre-biased loads
- RoHS compliant, MSL level 3, 260°C reflow

APPLICATIONS

- Noise sensitive FPGA rails such as transceiver and high-speed IO
- Sensitive RF applications such as RRU
- Wireless and Wireline communications systems
- Data Center and Cloud server and storage equipment

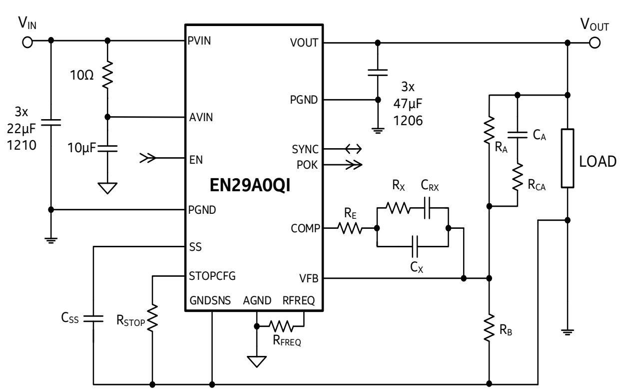


Figure 1: Simplified Applications Circuit

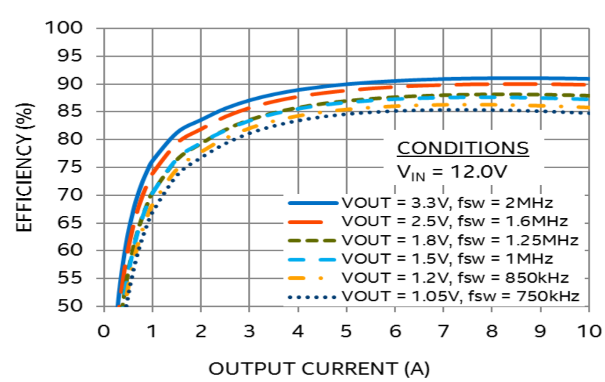


Figure 2: Efficiency at VIN = 12 V

ORDERING INFORMATION

Table 1

Part Number	Package Markings	T_J Rating (°C)	Package Description
EN29A0QI	EN29A0QI	-40 to +125	84-pin (12mm x 14mm x 4mm) QFN
EVB-EN29A0QI	EN29A0QI	QFN Evaluation Board	

Packing and Marking Information: https://www.altera.com/support/quality-and-reliability/packing.html

PIN ASSIGNMENTS

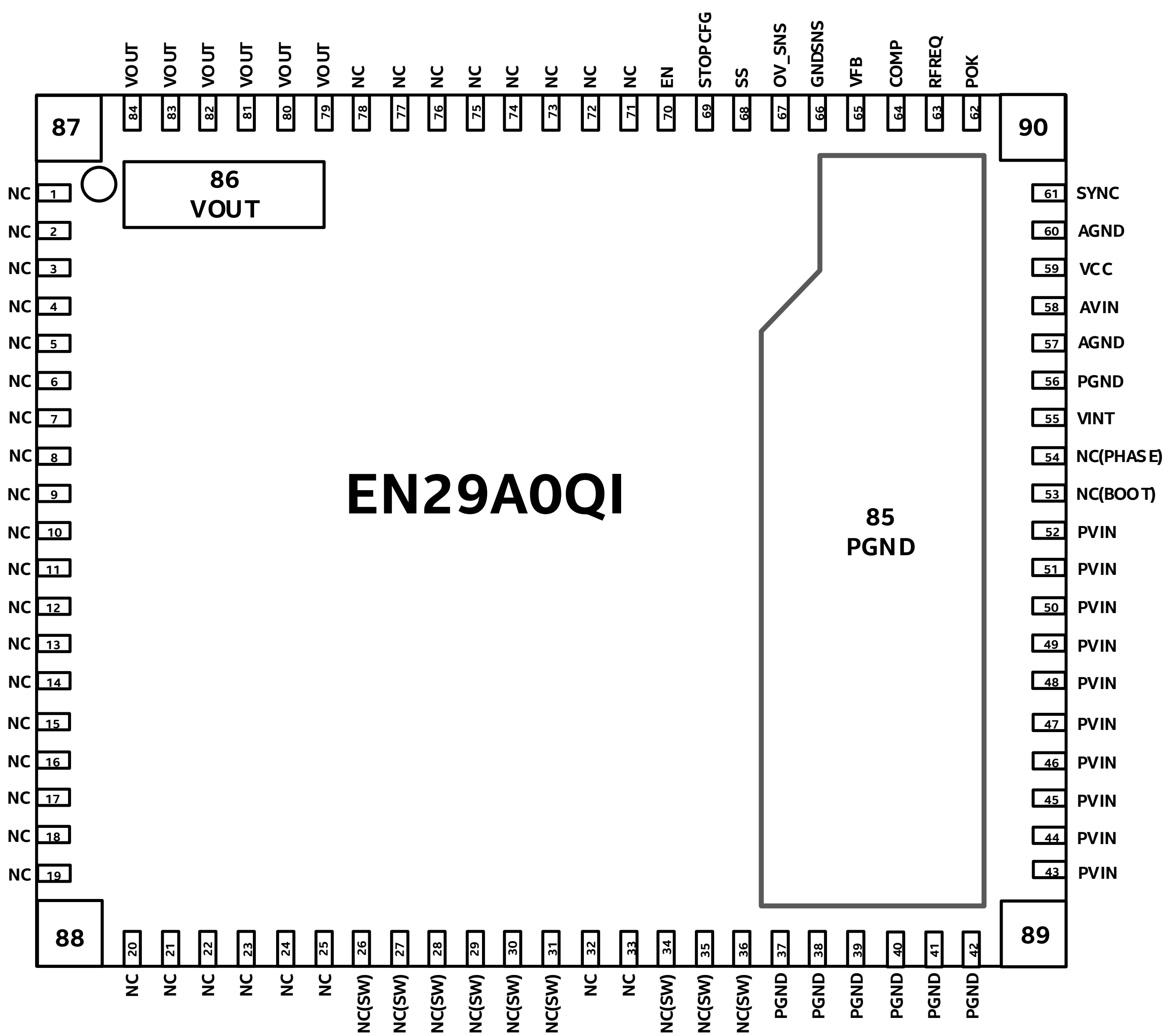


Figure 3: Pin Out Diagram (Top View)

NOTE A: White 'dot' on top left is pin 1 indicator on top of the device package.

PIN DESCRIPTION

Table 2

PIN	NAME	I/O	FUNCTION
1-19	NC	-	These pins must be soldered to PCB. These pins are not tied to any internal signal, voltage, or ground, and may be connected to the VOUT plane. Refer to Layout Recommendation section.
20-25, 32, 33, 71-78	NC	-	No Connect. These pins must be soldered to PCB but not electrically connected to each other or to any external signal, voltage, or ground. These pins may be connected internally. Failure to follow this guideline may result in device damage.
26-31, 34-36	NC(SW)	-	No Connect. These pins are internally connected to the common switching node of the internal MOSFETs. They must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage.
37-42, 56	PGND	Ground	Input/output power ground. Connect to the ground electrode of the input and output filter capacitors. See VOUT and PVIN pin descriptions for more details.
43-52	PVIN	Power	Input power supply. Connect to input power supply. Decouple with input capacitor to PGND pin.
53	NC(BOOT)	-	No Connect. This pin is internally connected to the bootstrap capacitor. It must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage. It is recommended, but not mandatory, to have a test point on this pin for debug purposes.
54	NC(PHASE)	-	No Connect. This pin is internally connected to the switching node and is the return pin of the bootstrap capacitor. It must be soldered to PCB but not be electrically connected to any external signal, ground, or voltage. Failure to follow this guideline may result in device damage. It is recommended, but not mandatory, to have a test point on this pin for debug purposes.
55	VINT	Analog	Internal regulated voltage rail used for internal circuitry. Decouple with 2.2µF ceramic capacitor to PGND. This rail may not be used to power external circuitry.
57, 60	AGND	Power	The quiet ground for the control circuits. Connect to the ground plane with a via right next to the pin.
58	AVIN	Power	Input power supply for the controller. Connect to input voltage at a quiet point through a RC filter.
59	VCC	Analog	Internal regulated voltage rail used for internal circuitry. Decouple with 100nF ceramic capacitor to AGND. This rail may not be used to power external circuitry.

PIN	NAME	I/O	FUNCTION
61	SYNC	Digital	Bidirectional frequency synchronization pin. Depending on whether the part is a SYNC Master or Slave, this pin can provide a synchronization clock to other devices or accept an external clock input. This pin may be left floating when not used. Refer to section on Frequency Synchronization and Master/Slave Operation for details on SYNC configuration.
62	POK	Digital	Power OK is an open drain transistor used for power system state indication. POK is logic high when VOUT is within +10% to -8% of VOUT nominal (refer to Electrical Characteristics Table for range of VOUT within which POK is high).
63	RFREQ	Analog	Frequency adjust pin. This pin must have a resistor to AGND which sets the free running frequency of the internal oscillator.
64	COMP	Analog	Error amplifier output. Allows for customization of control loop.
65	VFB	Analog	This is the external feedback input pin. A resistor divider connects from the output to GNDSNS. The mid-point of the resistor divider is connected to VFB. A feed-forward capacitor (C_A) and resistor (R_{CA}) are required parallel to the upper feedback resistor (R_A). VOUT regulation is based on the VFB node voltage equal to 0.6V.
66	GNDSNS	Analog	Ground sense pin. Connect to load ground. The soft-start capacitor, soft-shutdown resistor and the feedback resistor are referenced to GNDSNS.
67	OV_SNS	Analog	Output over-voltage sense pin. Connect to VFB pin unless external OVP circuit is desired. Connect to AGND when not used. Refer to section on Programming Output Voltage trip-point for details on OV_SNS configuration.
68	SS	Analog	A soft-start capacitor is connected between this pin and GNDSNS. The value of the capacitor controls the soft-start interval. Refer to soft-start in the Functional Description for more details.
69	STOPCFG	Analog	Soft-shutdown configuration. A resistor connected between this pin and GNDSNS sets the output soft-shutdown time. If STOPCFG is open, the output will tri-state when disabled. Refer to Soft-shutdown in the Functional Description for more details.
70	EN	Analog	Input Enable. Applying logic high enables the output and initiates a soft-start. Applying logic low disables the output according to the STOPCFG configuration.
79-84	VOUT	Power	Regulated converter output. Connect to the load and place output filter capacitor(s) between these pins and PGND pins.
85	PGND	Ground	Not a perimeter pin. Device thermal pad to be connected to the system GND plane for heat-sinking purposes. Refer to Layout Recommendation section.

PIN	NAME	I/O	FUNCTION
86	VOUT	Power	Not a perimeter pin. Device thermal pad to be connected to the system VOUT plane for heat-sinking purposes. Refer to Layout Recommendation section.
87-90	NC	-	Corner pads (mechanical purpose). These pins must be soldered to PCB. These pins are not tied to any internal signal, voltage, or ground, and may be connected to the PVIN, VOUT or PGND planes. Refer to Layout Recommendation section.

ABSOLUTE MAXIMUM RATINGS

CAUTION: Absolute Maximum ratings are stress ratings only. Functional operation beyond the recommended operating conditions is not implied. Stress beyond the absolute maximum ratings may impair device life. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Absolute Maximum Pin Ratings

Table 3

PARAMETER	SYMBOL	MIN	MAX	UNITS
PVIN, AVIN, VOUT		-0.3	18.7	V
VFB, SS, COMP, RFREQ, STOPCFG, OVSNS		-0.3	2.5	V
POK, SYNC			6.0	V
EN (internal clamp inactive)			3.6	V
Enable pin input current (EN pulled up to AVIN through resistor)	I_{EN}		200	µA
NC(SW) Voltage DC	V_{SW}	-0.3	PVIN+0.3	V
NC(SW) Voltage Peak < 10ns		-3	25	V

Absolute Maximum Thermal Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
Maximum Operating Junction Temperature			+150	°C
Storage Temperature Range		-65	+150	°C
Reflow Peak Body Temperature	(10 Sec) MSL3 JEDEC J-STD-020A		+260	°C

Absolute Maximum ESD Ratings

PARAMETER	CONDITION	MIN	MAX	UNITS
HBM (Human Body Model)		±2000		V
CDM (Charged Device Model)		±500		V

RECOMMENDED OPERATING CONDITIONS

Table 4

PARAMETER	SYMBOL	MIN	MAX	UNITS
Input Voltage Range	V_{IN}	9	16	V
Output Voltage Range	V_{OUT}	0.75	3.3	V
Output Current Range	I_{OUT}		10	A
Operating Junction Temperature	T_J	-40	+125	°C

THERMAL CHARACTERISTICS

Table 5

PARAMETER	SYMBOL	TYPICAL	UNITS
Thermal Shutdown	T_{SD}	150	°C
Thermal Shutdown Hysteresis	T_{SDH}	30	°C
Thermal Resistance: Junction to Ambient (0 LFM) (1)	θ_{JA}	10	°C/W
Thermal Resistance: Junction to Case (0 LFM)	θ_{JC}	0.5	°C/W

(1) Based on 2oz. external copper layers and proper thermal design in line with EIJ/JEDEC JESD51-7 standard for high thermal conductivity boards.

ELECTRICAL CHARACTERISTICS

NOTE: The minimum and maximum values are over the operating junction temperature range (-40°C to 125°C) unless otherwise noted. Typical values are tested at V_{IN} = 12V and T_A = 25°C.

Table 6

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Input Voltage	V_{IN}	PVIN tied to AVIN with a 10 ohm resistor	9		16	V
Input Under Voltage Lock-Out – AVIN Rising	V_{UVLOR}	Voltage above which UVLO is not asserted	7.75	8.19	8.75	V
Input Under Voltage Lock-Out – AVIN Falling	V_{UVLOF}	Voltage below which UVLO is asserted	7.25	7.83	8.25	V
Input Under Voltage Lock-Out Hysteresis				300		mV
Input Over Voltage Lock-Out – AVIN Rising	V_{OVLOR}	Voltage above which OVLO is asserted	16.5	17.5	18.5	V
Input Over Voltage Lock-Out – AVIN Falling	V_{OVLOF}	Voltage below which OVLO is not asserted	16	17.0	18	V
PVIN Slew rate (2)			1		120	V/ms
Shut-Down Supply Current	I_S	EN = 0; (AVIN + PVIN current)	9	13	25	mA
AVIN Quiescent Current	I_{AVINQ}	EN= 1; AVIN current only	1	10	12	mA
No Load Quiescent Current	I_{VINQ}	PVIN + AVIN current V_{OUT} = 1.2V	35	49	65	mA
Feedback Pin Voltage (3) (Line, Load, Temperature)	V_{FB}	$9V \le V_{IN} \le 16V$ $0A \le I_{LOAD} \le 10A$ $-40°C \le T_A \le 85°C$	0.594	0.6	0.606	V
Feedback pin Input Leakage Current	I_{FB}	VFB pin input leakage current	-10		10	nA
Switching frequency	f_{SW}	Free-running (set with R_{FREQ})	450		2000	kHz
Switching frequency accuracy		Not including R_{FREQ} tolerance (R_{FREQ} = 30.1kΩ, f_{sw} = 1 MHz)	-5		+5	%
Minimum On-time	T_{ON_MIN}	Measured at SW node	20	39	56	ns
External Sync Amplitude – High			1.4		3.6	V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
External Sync Amplitude – Low					0.6	V
Sync pin Rise time[(2)]		When SYNC is an output and driving C_L<30pF			80	ns
External Sync Minimum Pulse Width		3.3V/1.8V logic, edge triggered	50			ns
External Sync Duty Max		3.3V/1.8V logic			90	%
External Sync–Programmed Freq difference	Δf_{SYNC}	Maximum frequency difference to ensure synchronization			15	%
EN pin threshold (precision Enable)	V_{EN}		1.085	1.126	1.165	V
EN Hysteresis	V_{EN_HYST}		75	122	165	mV
EN Pin Current	I_{EN}	V_{EN} = 3.6V			1	µA
EN high Response Delay		Time from when EN is high till soft-start begins to ramp			90	µs
EN low Response Delay		Time from EN low till output mode response			1.8	µs
ENABLE Lockout	t_{ENLO}	Once EN has been pulled low, internal lockout time before device will respond to an EN high event	10	12.2	15.5	ms
ENABLE Spurious Pulse Rejection		Leading edge blanking	200	330	600	ns
SS Pin voltage range [(2)]		Soft-start	0		0.6	V
SS Ramp Time [(2)]	t_{RISE}	3.3nF ≤ C_{SS} ≤ 680nF	0.1		20	ms
SS Pin charging current	I_{SS}		18	20	22	µA
Soft-start Discharge Resistance		Internal resistance	400	590	750	ohms
Soft-shutdown Resistance [(2)(4)]		STOPCFG pin resistor range	1		100	kΩ
Soft-shutdown internal switch Resistance [(2)]		Switch resistance from SS to STOPCFG pins		100		Ω

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POK Threshold VOUT Rising		Range of Output Voltage as a Fraction of Programmed Value above which POK is Asserted.	92	93.8	95.5	%
POK Hysteresis		As a percentage of reference voltage	1	2.1	3.3	%
POK Logic Low		With 5mA current sink into POK pin	0.01	0.19	0.3	V
POK Low to High Delay Time		No Fault present			10	us
POK High to Low Delay Time		Fault or VOUT low			600	ns
OCP trip magnitude (5)	I_{OCP}	V_{OUT} = 1.5V, f_{sw} = 1MHz	11	12.4	15	A
OCP_Timer		Time device may remain in OCP (current-limiting) mode before a fault	15	20	25	ms
OCP Timer Reset		Length of time of non-OCP cycles before OCP Timer is reset	5	10	20	ms
OVP Threshold		When using the same divider ratio as the VFB feedback divider circuit; measured as a percentage of nominal output voltage (V_{GNDSNS} = V_{AGND})	107	110	113	%
OVP Fault Delay		Delay time from OVP fault to fault response			550	ns
Inductor Value			280	350	420	nH
DCR of the Inductor				2		mΩ

(2) Parameter not production tested but is guaranteed by design.

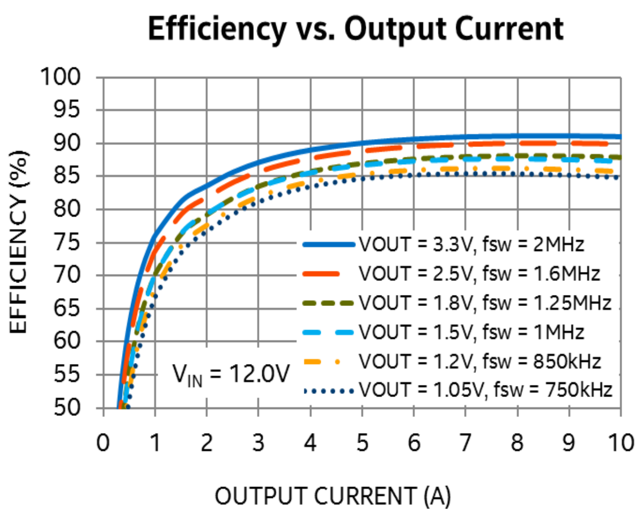
(3) The VFB pin controls the output voltage. Touching or injecting an external signal on the pin during operation may cause the output to change.

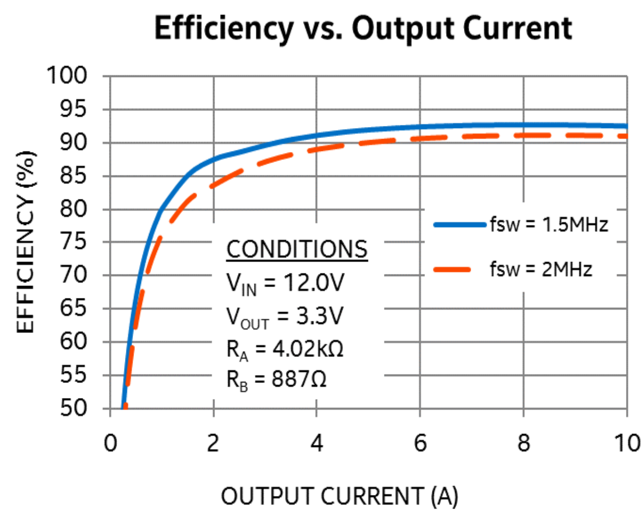
(4) Refer to section on soft-shutdown operation for R_{STOP} recommendations

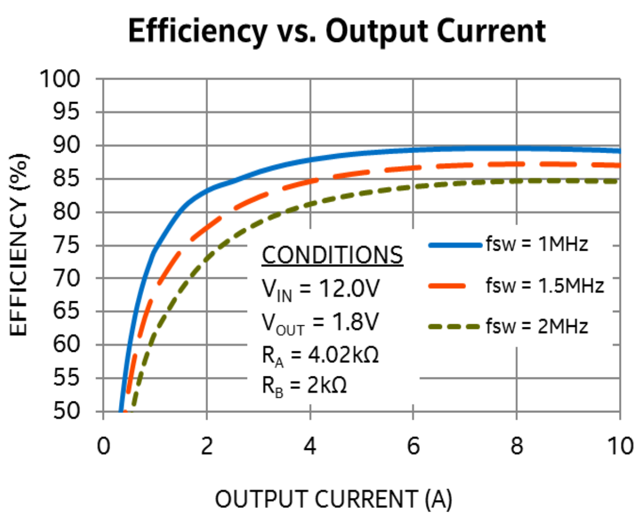
(5) OCP trip magnitude will vary with Switching frequency. Refer to section on programming Switching Frequency

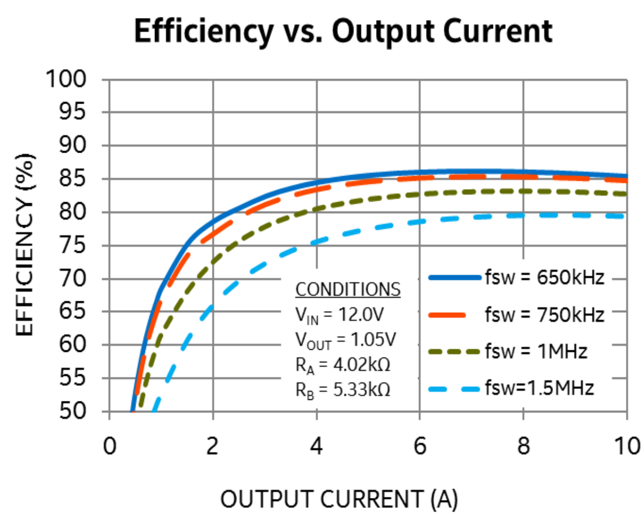
TYPICAL PERFORMANCE CURVES

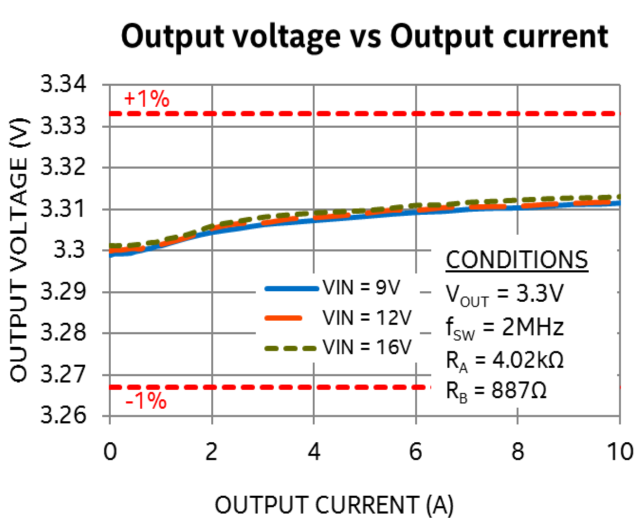
NOTE: Typical performance curves are T_A = 25°C unless otherwise noted.

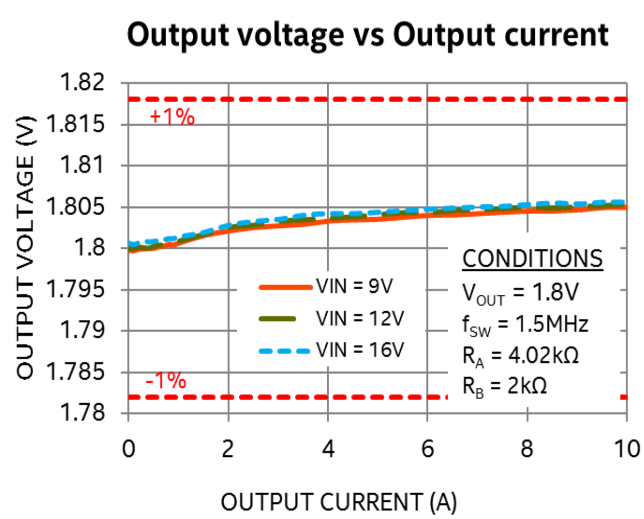




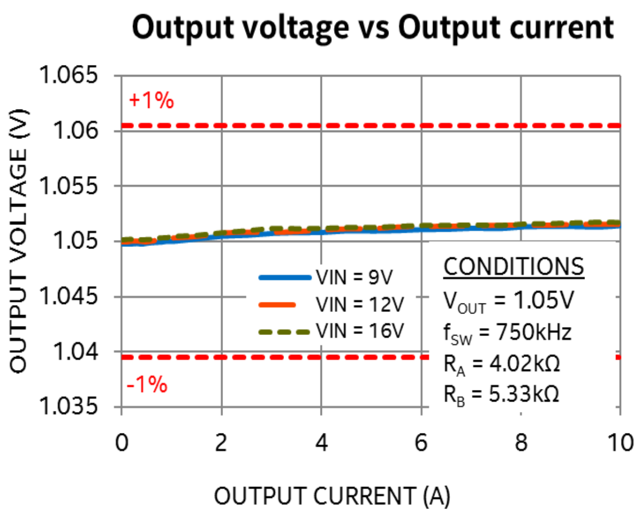


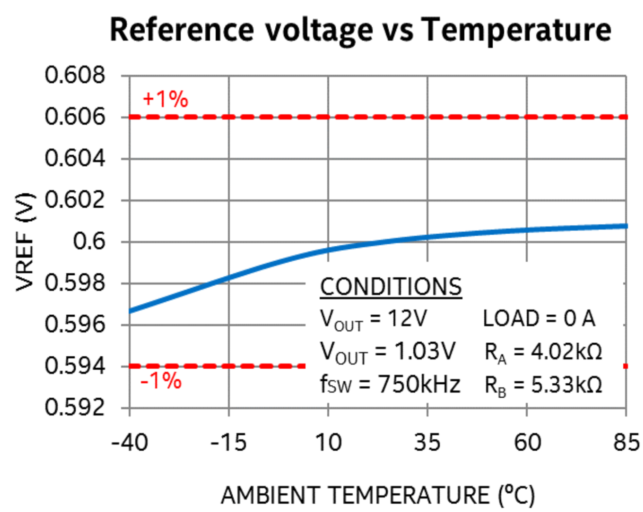


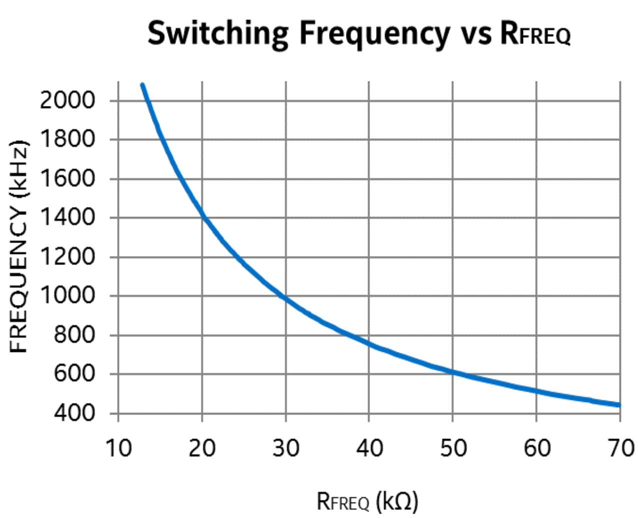


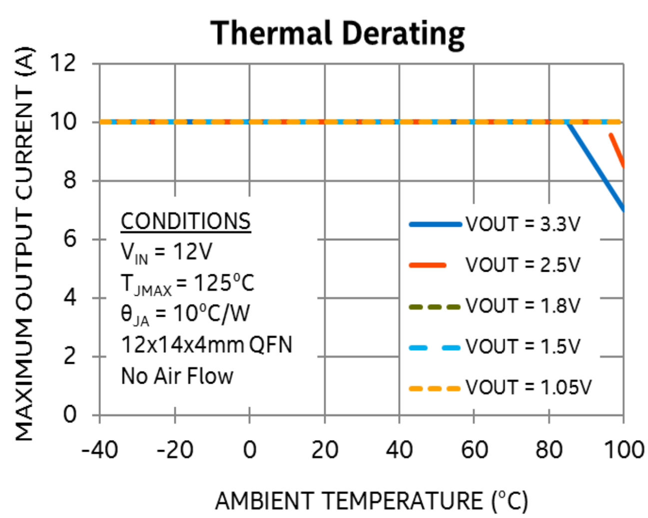


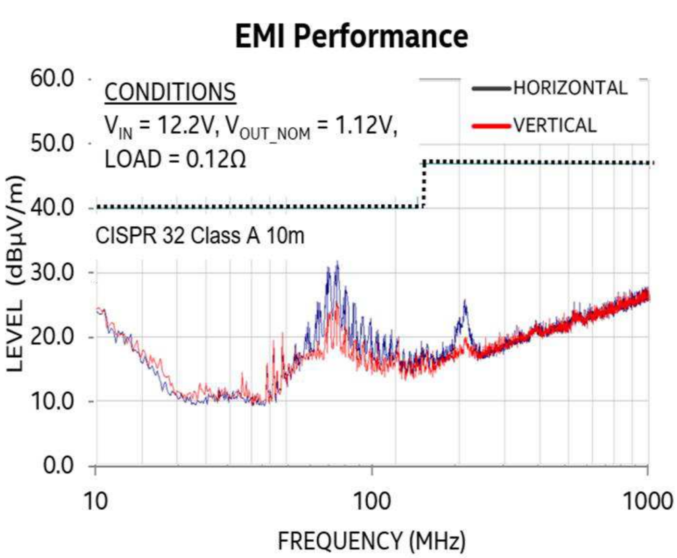
TYPICAL PERFORMANCE CURVES (CONTINUED)

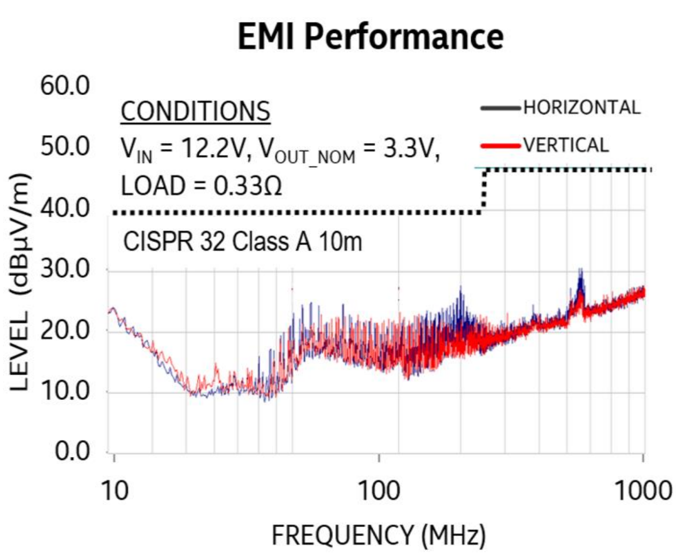








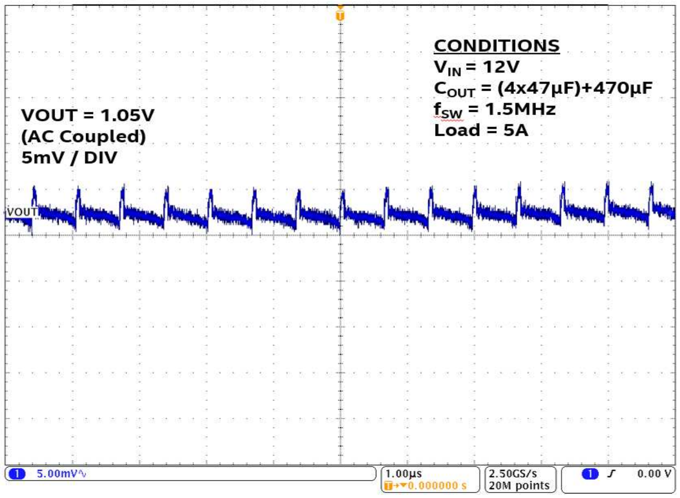




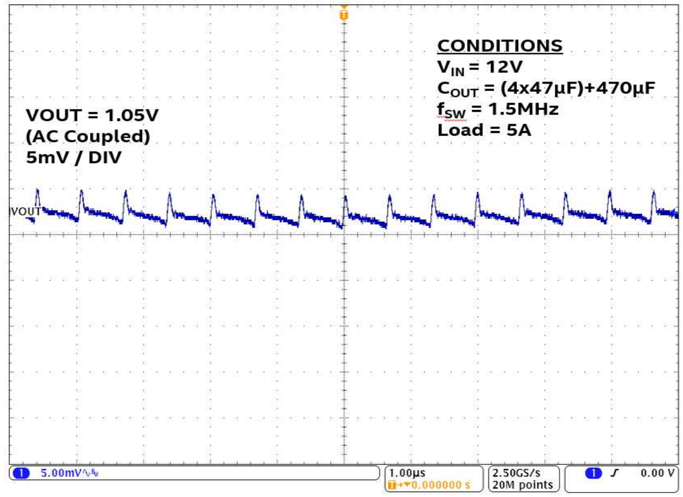
TYPICAL PERFORMANCE CHARACTERISTICS

NOTE: Typical performance characteristics are T_A = 25°C unless otherwise noted.

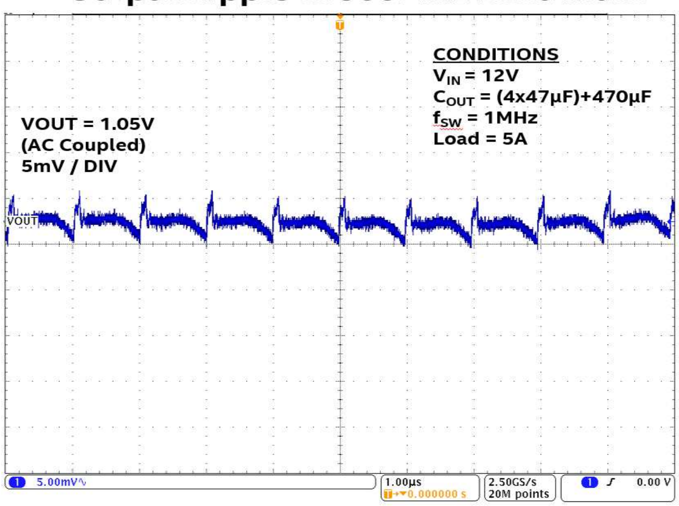
Output Ripple at 500MHz Bandwidth



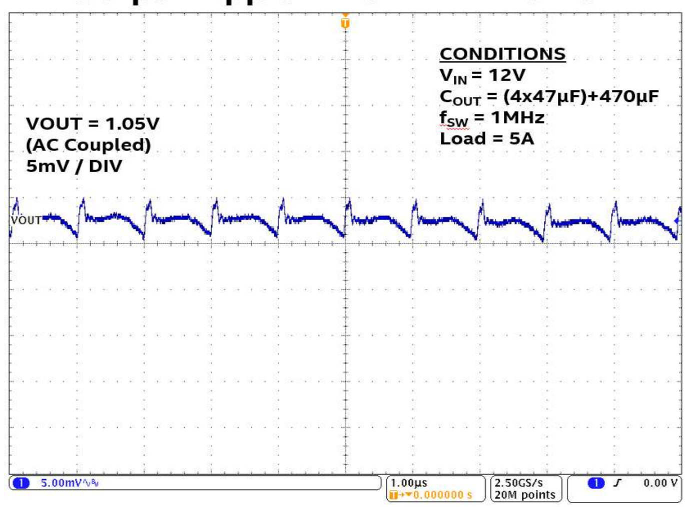
Output Ripple at 20MHz Bandwidth



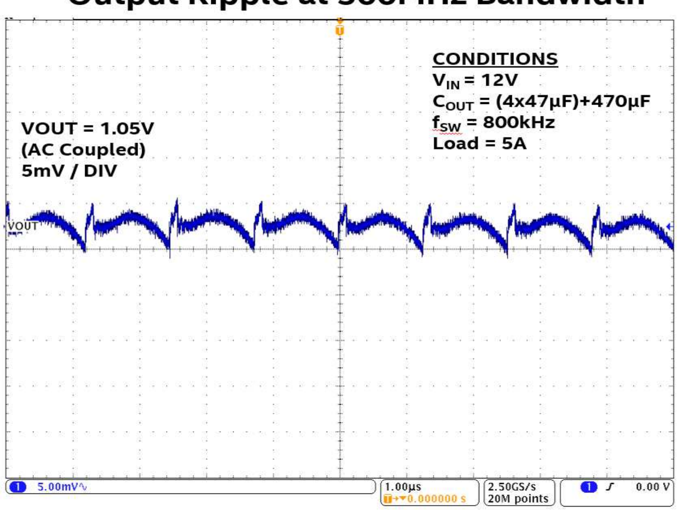
Output Ripple at 500MHz Bandwidth



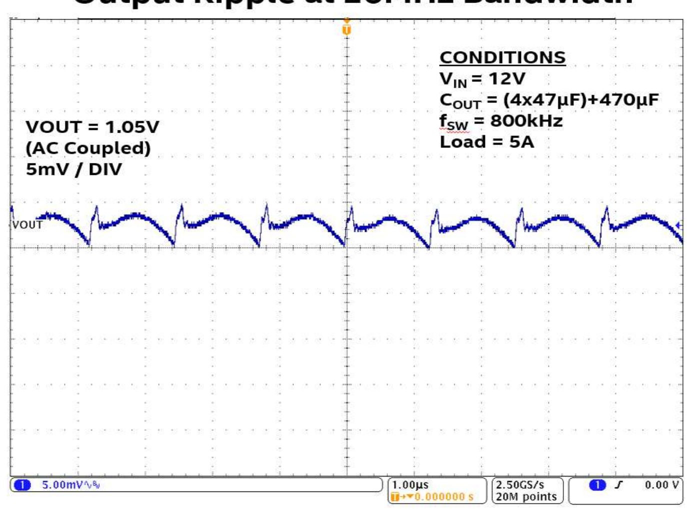
Output Ripple at 20MHz Bandwidth



Output Ripple at 500MHz Bandwidth

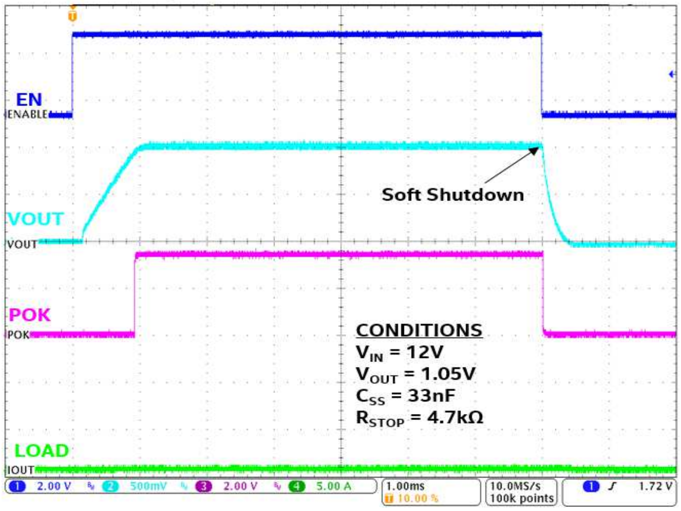


Output Ripple at 20MHz Bandwidth

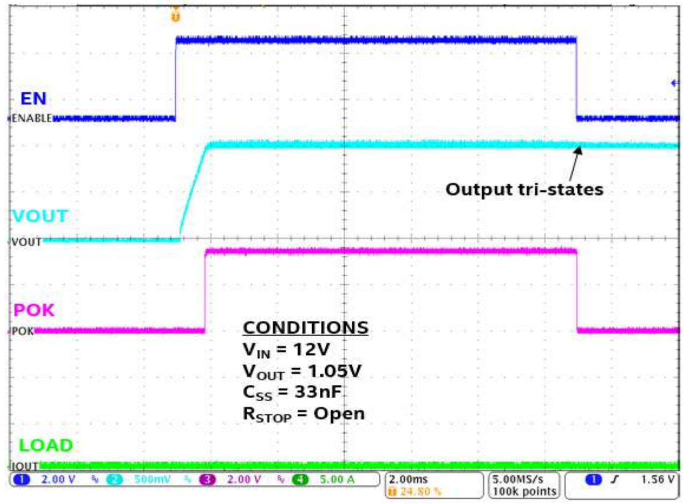


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

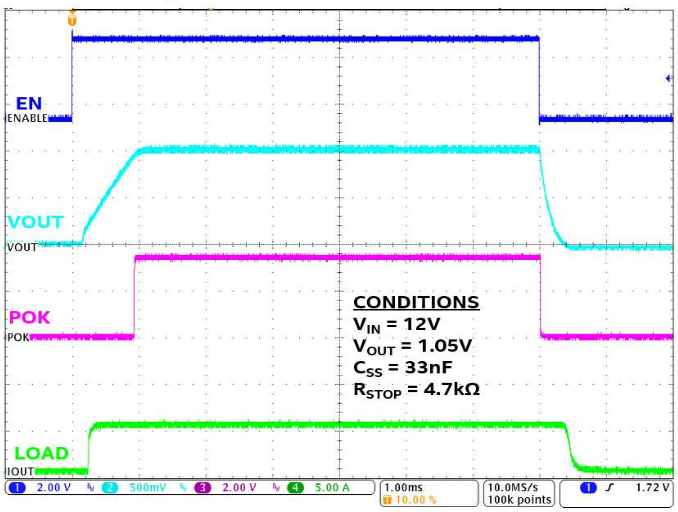
Startup and Shutdown at No Load



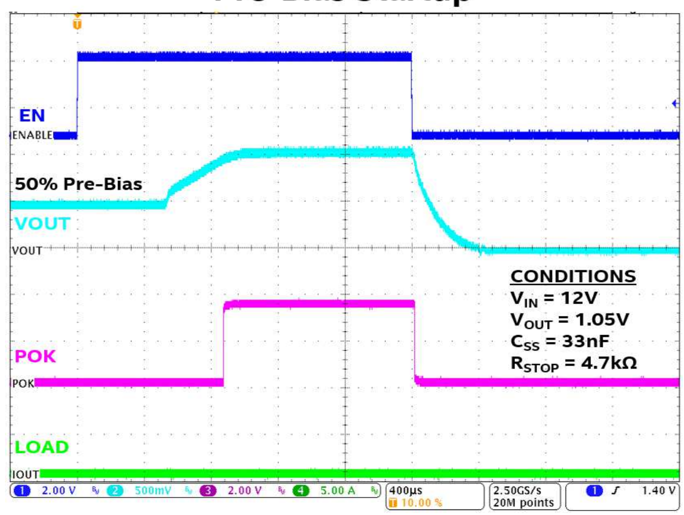
Startup and Shutdown at No Load



Startup and Shutdown at 5A Load



Pre-Bias Startup



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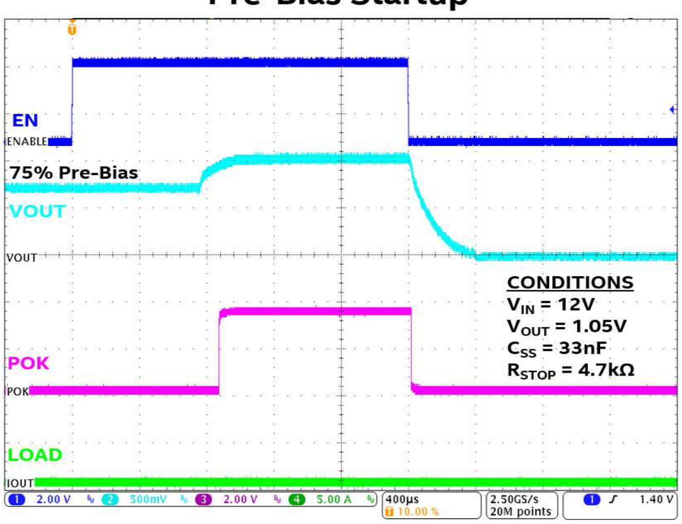
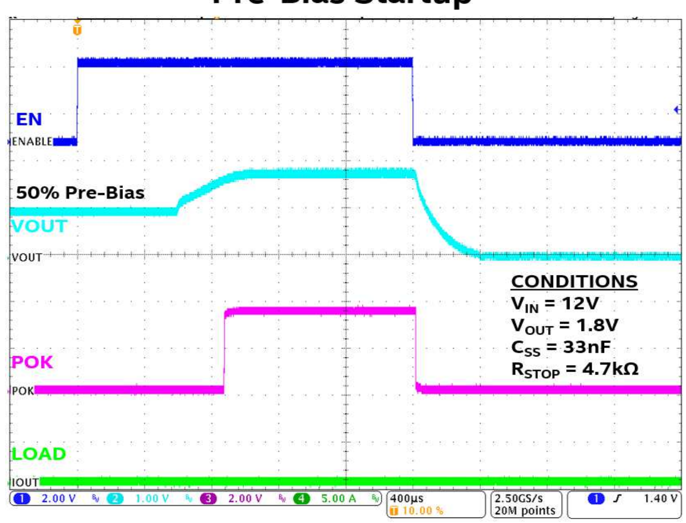
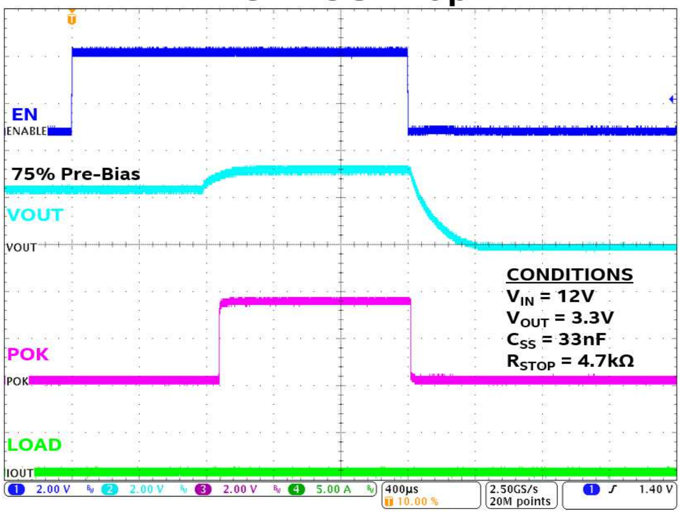


Pre-Bias Startup

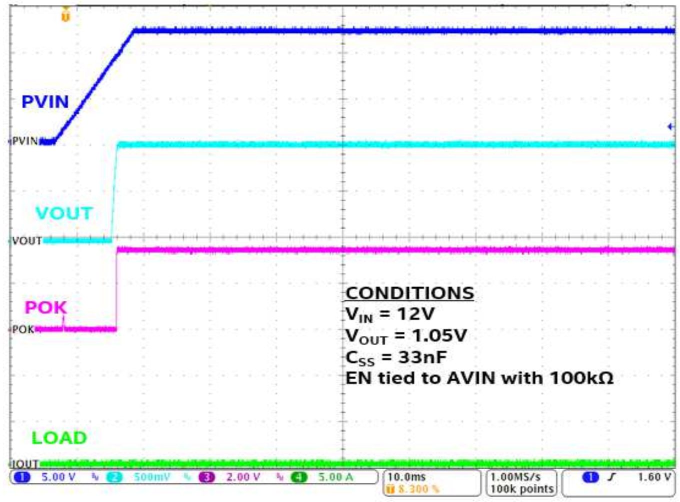


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

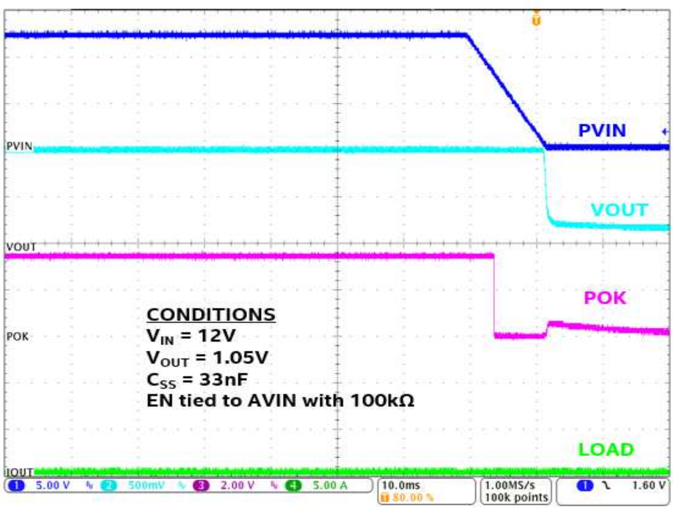
Pre-Bias Startup



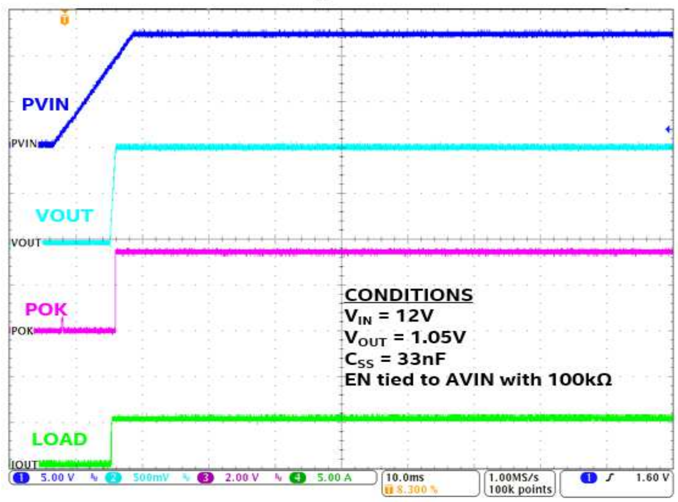
VIN Startup at No Load



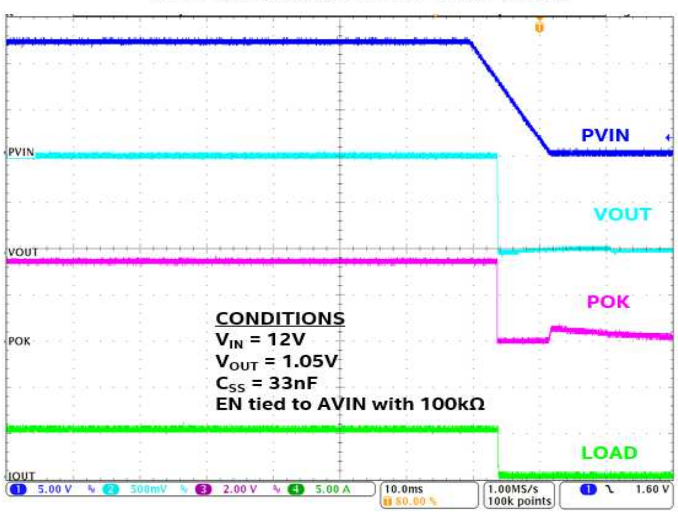
VIN Shutdown at No Load



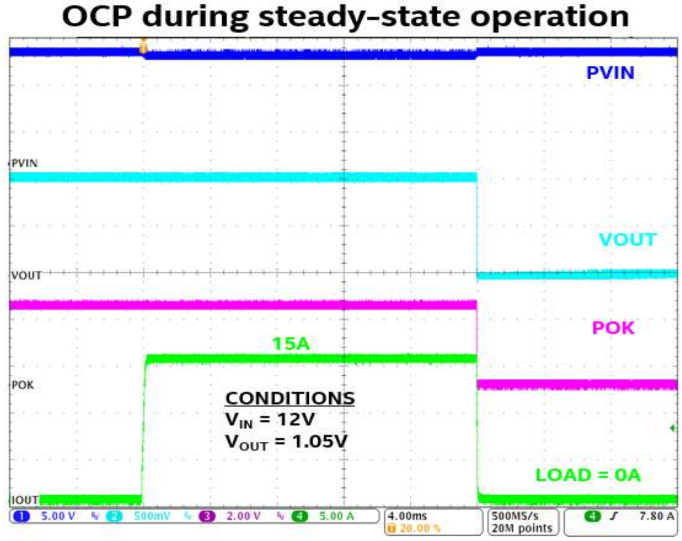
VIN Startup at 5A Load



VIN Shutdown at 5A Load

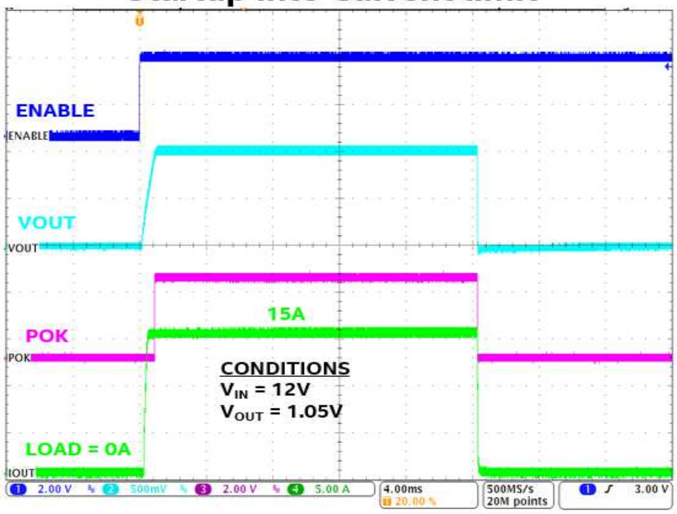


OCP during steady-state operation

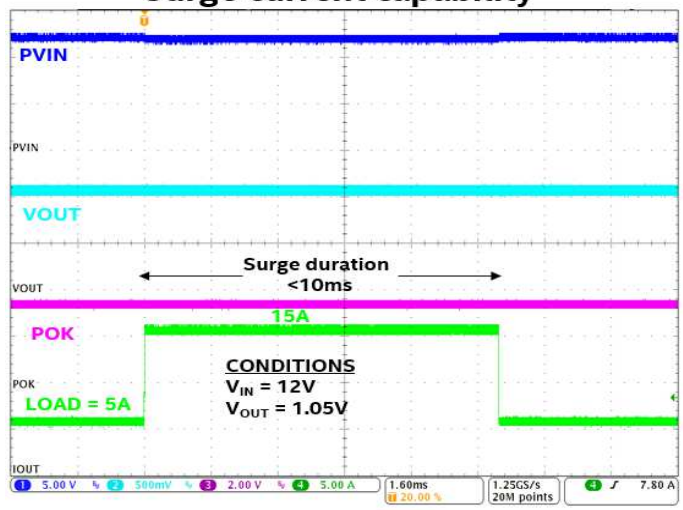


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

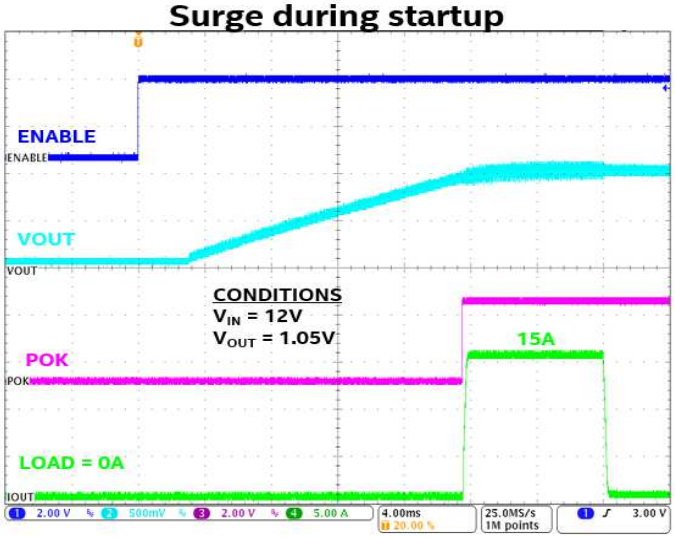
Startup into Current limit



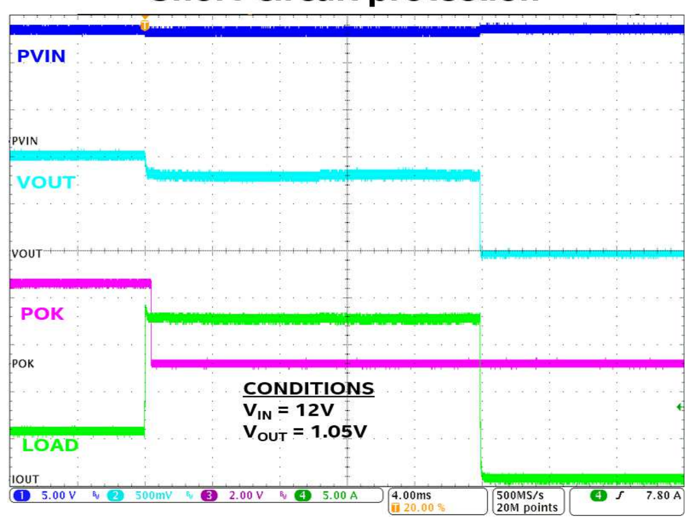
Surge current capability



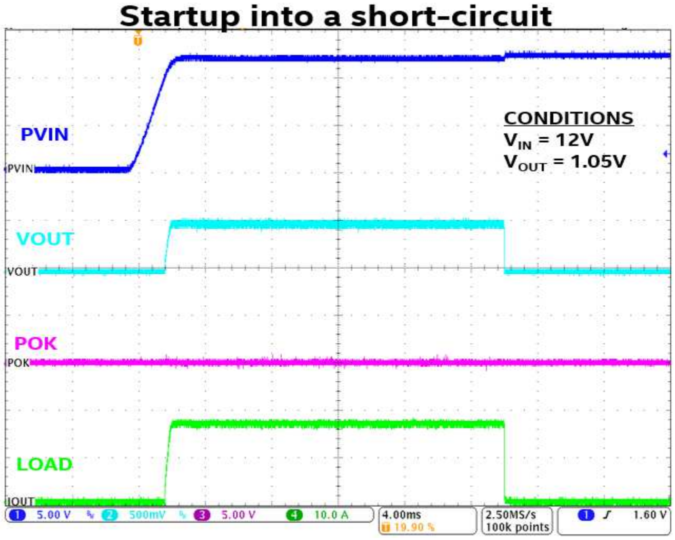
Surge during startup



Short-circuit protection

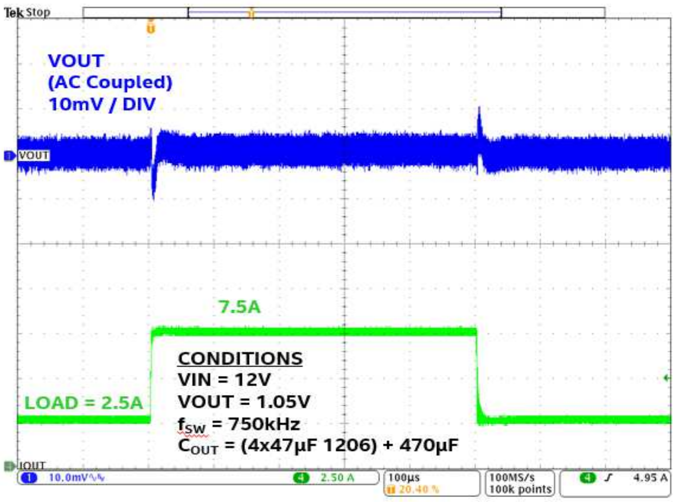


Startup into a short-circuit

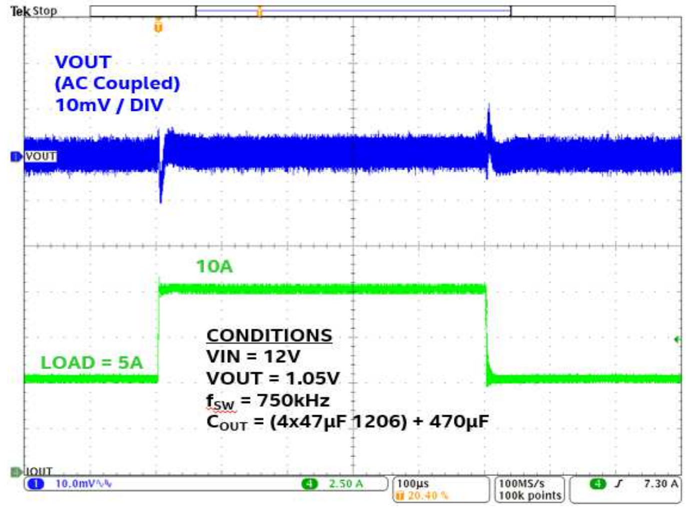


TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

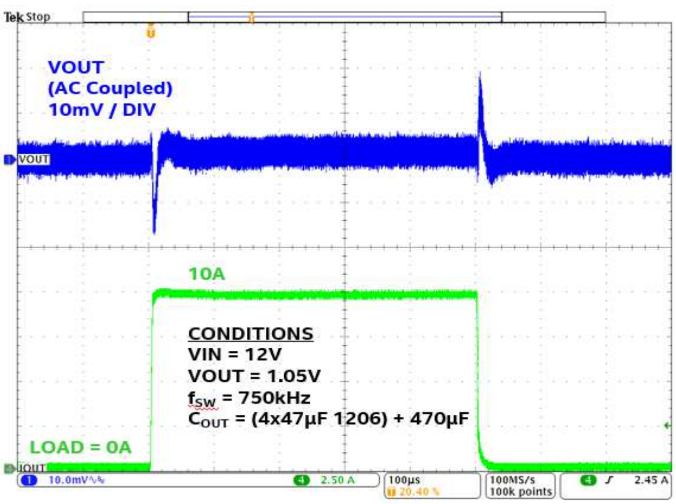
Load Transient 2.5 to 7.5A



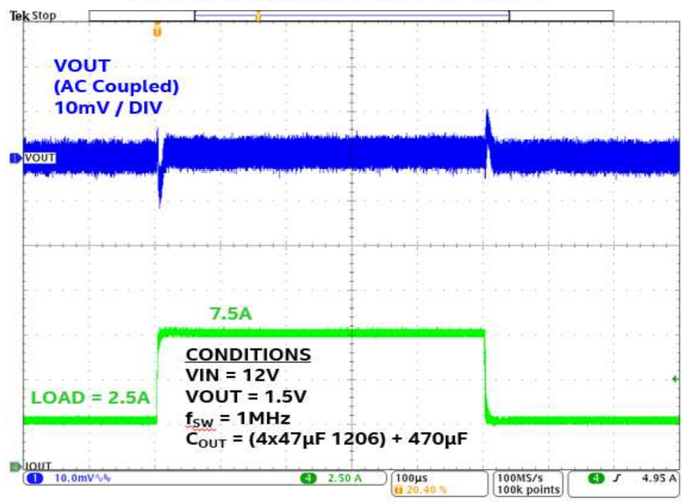
Load Transient 5 to 10A



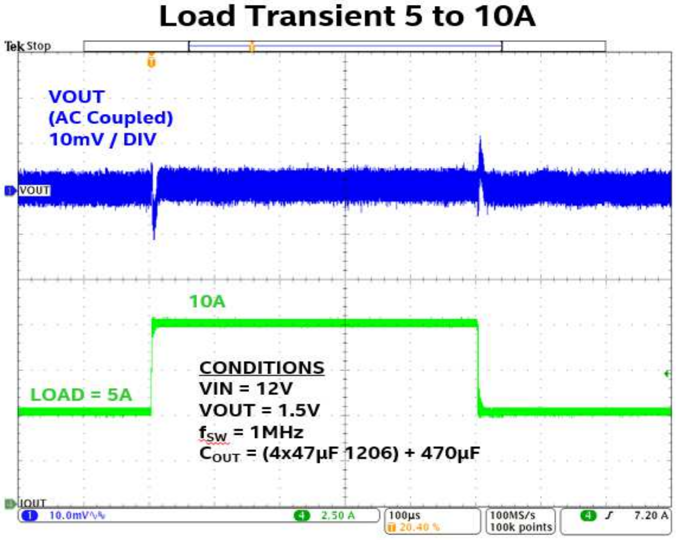
Load Transient 0 to 10A



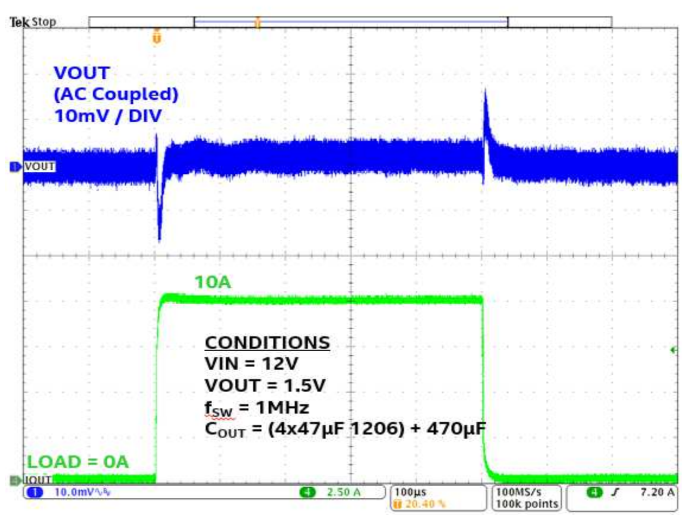
Load Transient 2.5 to 7.5A



Load Transient 5 to 10A



Load Transient 0 to 10A



FUNCTIONAL BLOCK DIAGRAM

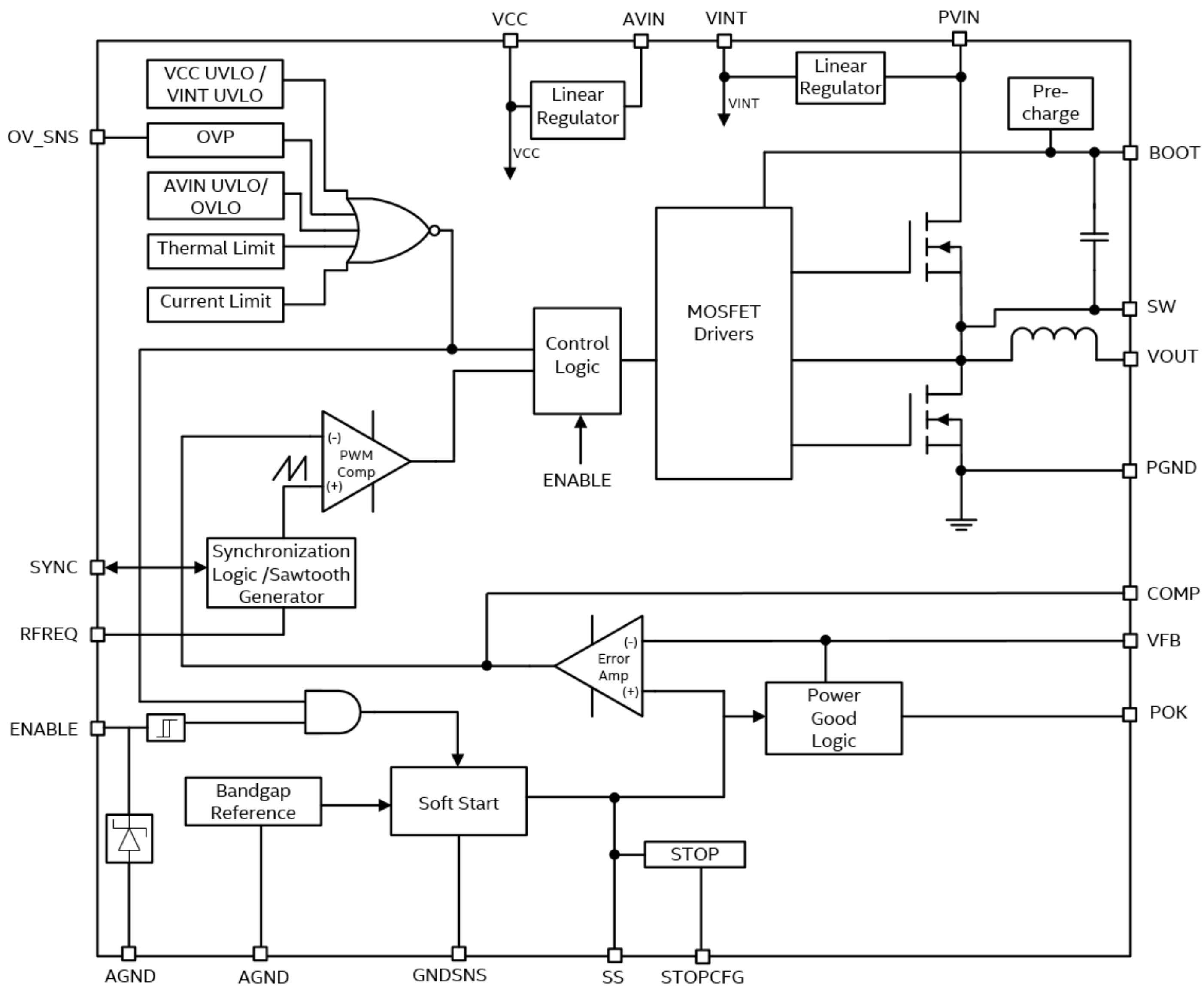


Figure 4: Functional Block Diagram

FUNCTIONAL DESCRIPTION

Synchronous Buck Module

The EN29A0QI is a highly integrated synchronous, buck converter with integrated controller, power MOSFET switches and integrated inductor. The nominal input voltage (PVIN) range is 9V to 16V and can support up to 10A of continuous output current. The output voltage is programmed using an external resistor divider network. The feedback control loop is customizable through external components. Type III or Type IV voltage mode control may be implemented to maximize control loop bandwidth and to maintain excellent phase margin to improve transient performance. The operating switching frequency is between 0.45MHz and 2MHz and enables the use of small-size input and output capacitors.

Operational Features:

- Precision enable circuit with tight threshold range
- Soft-start circuit allowing controlled startup when the converter is initially powered up
- Power OK circuit indicating the output voltage is greater than 92% of programmed value
- Resistor programmable switching frequency
- Bidirectional frequency synchronization pin

Protection Features:

- Over-current protection from excessive load current
- Thermal shutdown with hysteresis to prevent over temperature stress
- Output voltage pre-bias startup protection for smooth monotonic startup
- Output over-voltage protection
- Input under-voltage protection
- Input over-voltage protection

Precision Enable Operation

The enable (EN) pin provides a mean to start up or to shut down the device. When the EN pin is asserted high, the device will undergo a normal soft-start where the output will rise monotonically into regulation. Asserting a logic low on this pin will deactivate the device by turning off the internal power switches and the POK flag will also be pulled low. The output will tri-state or go through a soft-shutdown when EN goes low depending on the resistor connected to STOPCFG pin (refer to the section on soft-shutdown operation for more details). The EN threshold is a precision analog voltage rather than a digital logic threshold. The EN pin may be connected to AVIN through a resistor (typically 100kΩ) or be controlled by a 3.3V/1.8V logic signal. The maximum input current on the EN pin when tied to AVIN through a resistor should not exceed 200µA. A precision voltage reference and a comparator circuit are kept powered up even when EN is de-asserted. The narrow voltage gap between EN Logic Low and EN Logic High allows the device to turn on at a precise enable voltage level. With the enable threshold pinpointed, a proper choice of soft-start capacitor helps to accurately sequence multiple power supplies in a system as desired. There is an Enable lockout time of 12.5ms that prevents the device from re-enabling immediately after it is disabled.

Soft-Start Operation

The SS pin in conjunction with a small external capacitor between this pin and GNDSNS provides a soft-start function to limit in-rush current during device power-up. When the part is initially powered up, the output voltage is gradually ramped to its final value. The gradual output ramp is achieved by increasing the reference voltage to the error amplifier. A constant current flowing into the soft-start capacitor provides the reference voltage ramp. When the voltage on the soft-start capacitor reaches 0.60V, the output has reached its programmed voltage. The output rise time can be controlled by the choice of soft-start capacitor value.

The rise time is defined as the time from when the enable signal crosses the threshold and the input voltage crosses the upper UVLO threshold to the time when the output voltage reaches 95% of the programmed value. The rise time (t_{RISE}) is given by the following equation:

$$t_{RISE}\ [ms] = C_{ss}\ [nF] \times 0.03$$

With a 33nF soft-start capacitance on the SS pin, the soft-start rise time will be set to 0.99ms. The recommended range for the value of the SS capacitor is between 3.3nF and 680nF. Note that excessive bulk capacitance on the output can cause an over current event on startup if the soft-start time is too low. The minimum soft-start time for a given output voltage and output capacitance is given by:

$$t_{RISE,\ min} = 0.1 \times V_{OUT} \times C_{OUT}$$

Soft-Shutdown Operation

The EN29A0 has a programmable soft-shutdown, controlled by a resistor, R_{STOP}, on the STOPCFG pin. When the ENABLE pin goes low, internal circuitry detects the presence of a resistor on the STOPCFG pin. This resistor forms a RC circuit with the soft-start capacitor to determine the output decay time. If STOPCFG pin is left open, the output tri-states when the part is disabled. The soft-shutdown time is calculated as

$$t_{STOP}\ [\mu s] = 3 \times C_{ss}\ [nF] \times R_{STOP}\ [k\Omega]$$

The recommended range for the value for R_{STOP} is between 1kΩ and 100kΩ. To prevent the output voltage from undershooting on shutdown, the minimum recommended R_{STOP} for a given combination of V_{OUT}, C_{OUT} and C_{SS} is given by

$$R_{STOP} = \frac{\pi\ C_{OUT}\ V_{OUT}}{10\ C_{SS}}$$

Note that R_{STOP} must be configured before the device is powered on. The maximum soft-shutdown time is limited by the EN lockout time (t_{ENLO}) found in the Electrical Characteristics Table. If t_{STOP} is greater than t_{ENLO}, then the output will soft-shutdown till it reaches t_{ENLO} after which it will tri-state. The soft-shutdown mode is available only when EN is pulled low during normal operation – in the event of a fault, the output will tri-state regardless of the presence of a resistor on the STOPCFG pin. Note that excessive bulk capacitance on the output can cause an over-current event on shutdown if the soft-shutdown time is too low. For a given output voltage and output capacitance the minimum soft-shutdown time to prevent an over-current event on shutdown is given by:

$$t_{STOP,\ min} = 0.1 \times V_{OUT} \times C_{OUT}$$

POK Operation

The POK signal is an open drain signal (requires a pull up resistor to VCC or similar voltage) from the converter indicating the output voltage is within the specified range. Typically, a 100kΩ or lower resistance is used as the pull-up resistor. The POK signal will be logic high when the rising output voltage crosses 93.8% (nominal) of the programmed voltage level. If the output voltage falls below the falling threshold, the POK signal will be de-asserted. POK is also logic low if any of the conditions are met: 1) the input voltage is below V_{UVLOR}, 2) EN is pulled low, 3) any other faults are present in the system. The POK signal can be used to sequence down-stream converters by tying to their enable pins.

Resistor Programmable Frequency

The operation of the EN29A0QI can be optimized by proper choice of the R_{FREQ} resistor. The frequency can be tuned to optimize dynamic performance and efficiency. The corresponding R_{FREQ} values may be obtained from the f_{SW} vs R_{FREQ} characteristic curve. Table 7 provides a list of recommended frequencies for some common output voltage settings at V_{IN} = 12V.

A reduced frequency may be desired in some applications to achieve better efficiency. However, note that at lower frequencies the average OCP current magnitude is also reduced proportionally due to an increase in the inductor peak-peak ripple current. The relationship between OCP magnitude, I_{OCP}, and the switching frequency, f_{SW}, is given by:

$$\Delta I_{OCP}\ [A] \propto 1/(2 \times \Delta f_{SW}\ [MHz])$$

where ΔI_{OCP} is the change in OCP level from the nominal OCP level for a change in frequency of Δf_{SW}.

Table 7

VOUT (V)	Minimum frequency		Recommended frequency		Maximum frequency	
	Frequency (MHz)	R_{FREQ} (kΩ)	Frequency (MHz)	R_{FREQ} (kΩ)	Frequency (MHz)	R_{FREQ} (kΩ)
0.75	0.45	68.1	0.5	60.4	0.75	40.2
1	0.5	60.4	0.75	40.2	1	30.1
1.2	0.6	51.1	0.85	35.7	1.25	23.2
1.5	0.7	43.2	1	30.1	1.55	18.2
1.8	0.8	38.3	1.25	23.3	1.85	14.7
2.5	1	30.1	1.6	17.4	2	13.7
3.3	1.25	23.3	2	13.7	2	13.7

Frequency Synchronization and Master/ Slave operation

The EN29A0QI's switching frequency may be synchronized to an external clock signal through the bidirectional SYNC pin, provided the external synchronization frequency is higher than the frequency set by the frequency adjust resistor, R_{FREQ}. When a clock signal is present at SYNC, an activity detector detects the leading edge of the clock signal and the internal oscillator phase locks to the external clock. Refer to the Electrical Characteristics Table for specifications to ensure synchronization.

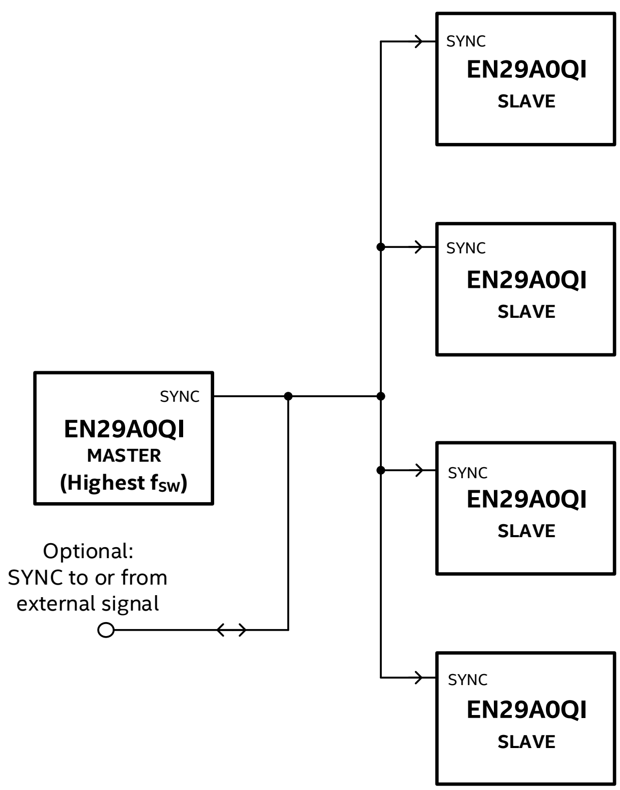


Figure 5: Frequency synchronization

Multiple EN29A0QI devices may be connected in a Master/Slave configuration. The device set at the highest free-running frequency is automatically placed in Master mode and becomes the SYNC master. In Master mode, a version of the internal switching oscillator signal is output on the SYNC pin. This PWM signal from the Master is fed to the Slave device at its SYNC pin. The slave device's PWM frequency synchronizes to the PWM frequency on its SYNC pin. The Master device's switching clock may be phase-locked to an external clock source of higher frequency to move the entire system frequency away from sensitive frequencies, in which case all devices are synchronized to the external clock. Additional Slave devices may be synchronized with the Master by connecting the SYNC of the Master to the SYNC of all other Slave devices. Refer to Figure 5 for details. To guarantee a particular device is set as the Master device, set its free-running switching frequency 1% or more higher than that of the remaining devices, after accounting for the tolerance of the R_{FREQ} resistors.

The SYNC pin may be left floating when the frequency synchronization feature is not used.

Over-Current Protection (OCP)

The EN29A0QI monitors current in the high side and low side MOSFET switches, both sinking and sourcing, to provide comprehensive current monitoring and protection. A proprietary dual threshold current limit scheme is employed. When the peak current exceeds the upper limit threshold, the high-side MOSFET is turned off, the low-side MOSFET is turned on, and PWM is ignored. Once the current ramps down below the lower threshold, the device will respond to PWM once again. This approach guarantees the device will stay within the inductor and MOSFET safe operating area versus a cycle by cycle limit where inductor current can get into a run-away condition. The OCP fault is determined by two timers working in conjunction: an OCP Timer (counting up to 20ms nominally) and an OCP Reset Timer (counting up to 10ms nominally). The OCP Timer is triggered during the first switch cycle that the output current exceeds the OCP trip level, and it starts counting up to 20ms. OCP Timer will count to 20ms and then latch the unit off unless OCP Reset Timer intervenes and resets the count. OCP Reset Timer counts up to 10ms when there is no current limiting. If current limiting occurs it is reset back to zero. Each time the OCP Reset Timer counts up to 10ms it resets the OCP Timer back to zero. Each cycle that the current limit is exceeded, the device will limit the output current by ignoring the PWM command until the current drops below the OCP level or OCP Timer is exceeded. If OCP Timer is exceeded the device will immediately set the shut-down latch: output will tristate and POK will go low. The OCP latch is reset by toggling the enable pin or cycling input power. Note that the OCP magnitude depends on switching frequency and duty ratio. Refer to the Resistor Programmable Frequency section for details on its dependence on switching frequency.

Over-Temperature Protection (OTP)

When the junction temperature exceeds the thermal shutdown temperature, sensing circuits in the converter will cause the device to set the shut-down latch: output will tristate and POK will go low. The part will exit the OTP latch and restart with a normal soft-start and resume normal operation after the junction temperature drops to a safe operating level if the enable pin is toggled or input power is cycled. The thermal shutdown temperature and hysteresis values can be found in the Thermal Characteristics table.

Input Under-Voltage Lock-Out (UVLO)

When the input voltage is below a required voltage level (V_{UVLOR}) for normal operation, the converter switching is inhibited. The lock-out threshold has hysteresis to prevent chatter. When the device is operating normally, if the input voltage falls below the lower threshold (V_{UVLOF}) the output will tri-state and POK will go low. Once a UVLO fault has occurred and the shut-down latch is set, the part will restart with a normal soft-start and resume normal operation if 1) Enable is toggled after the input voltage has gone back up above the upper threshold (V_{UVLOR}), or 2) The device's input power is toggled.

Input Over-Voltage Lock-Out (OVLO)

When the input voltage exceeds nominal voltage level (V_{OVLO}) for normal operation, the output will tri-state and POK goes low. The lock-out threshold has hysteresis to prevent chatter. Once an OVLO fault has occurred and the shut-down latch is set, the part will restart with a normal soft-start and resume normal operation if 1) Enable is toggled and the input voltage has fallen back below the lower threshold (V_{OVLOF}), or 2) The device's input power is toggled.

Output Over-Voltage Protection (OVP)

If the same resistor divider ratio as the feedback resistor divider ratio is used for the OV_SNS pin, the nominal overvoltage trip point is set 10% higher than the nominal set voltage. The OV_SNS pin may also be directly connected to the VFB pin to avoid redundancy. The over-voltage trip point is set nominally to 10% higher than the programmed output voltage when OV_SNS is tied to the VFB pin. When using an external resistor divider, the overvoltage trip point is set by the divider ratio which can be computed using the following equation:

$$R_{B1} = \frac{0.66\ X\ R_{A1}}{V_{OVERVOLTAGE} - 0.66}$$

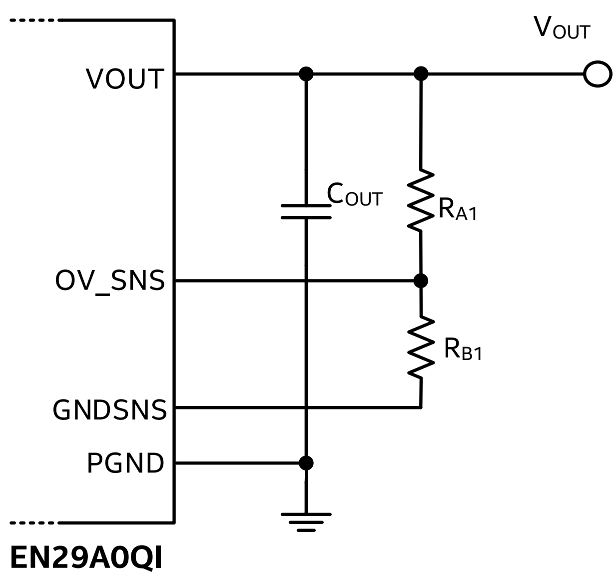


Figure 6: OVP trip-point external resistor divider

When the over-voltage trip point is exceeded the output will tri-state and POK goes low. Once an OVP fault has occurred and the shut-down latch is set, the part will restart with a normal soft-start and resume normal operation if 1) Enable is toggled after the fault is cleared, or 2) The device's input power is cycled.

Connecting the OV_SNS pin to AGND disables the output over-voltage protection feature.

Pre-Bias Startup Protection

A pre-biased condition can exist for a number of reasons. Rails with large bulk capacitance which may have insufficient time to discharge, leakage paths from one rail to another, dual/redundant supplies, etc. For pre-bias conditions where the output is below the target voltage the device shall attempt to start switching and regulate the output to the target Vout. The output rate of rise for this condition shall be monotonic within +/-

2% of the rising voltage trajectory. For voltages greater than the target voltage the device shall not respond to the ENABLE signal and will not startup. POK will remain low.

Note that when soft-shutdown is active, the part will pull the pre-bias rail low on shut-down till the Enable lockout time (t_{ENLO}) has expired. For applications where this is not desired, it is recommended to leave the STOPCFG open.

Fault Response Summary

Table 8

Fault condition	Output Response	Other Responses
Vin Under Voltage Lock Out; Vin Falling. (UVLO during VIN rising is not a fault condition, but does ignore the EN pin until VIN crosses the UVLO rising threshold.)	Tristate	Latch off (1) POK goes low Discharge SS pin
Vin Over Voltage Lock Out	Tristate	Latch off (1) POK goes low Discharge SS pin
Over Temperature Protection	Tristate	Latch off (1) POK goes low Discharge SS pin
Vout Over Voltage Protection	Tristate	Latch off (1) POK goes low Discharge SS pin
Over Current Protection (subject to OCP Timer and OCP Reset Timer functionality)	Tristate	Latch off (1) POK goes low Discharge SS pin

(1) Requires enable pin toggle or input power cycle to clear fault after fault condition is removed.

APPLICATION INFORMATION

Output Voltage Setting

The EN29A0QI output voltage is programmed using a simple resistor divider network (R_A and R_B). Figure 7 shows the resistor divider configuration.

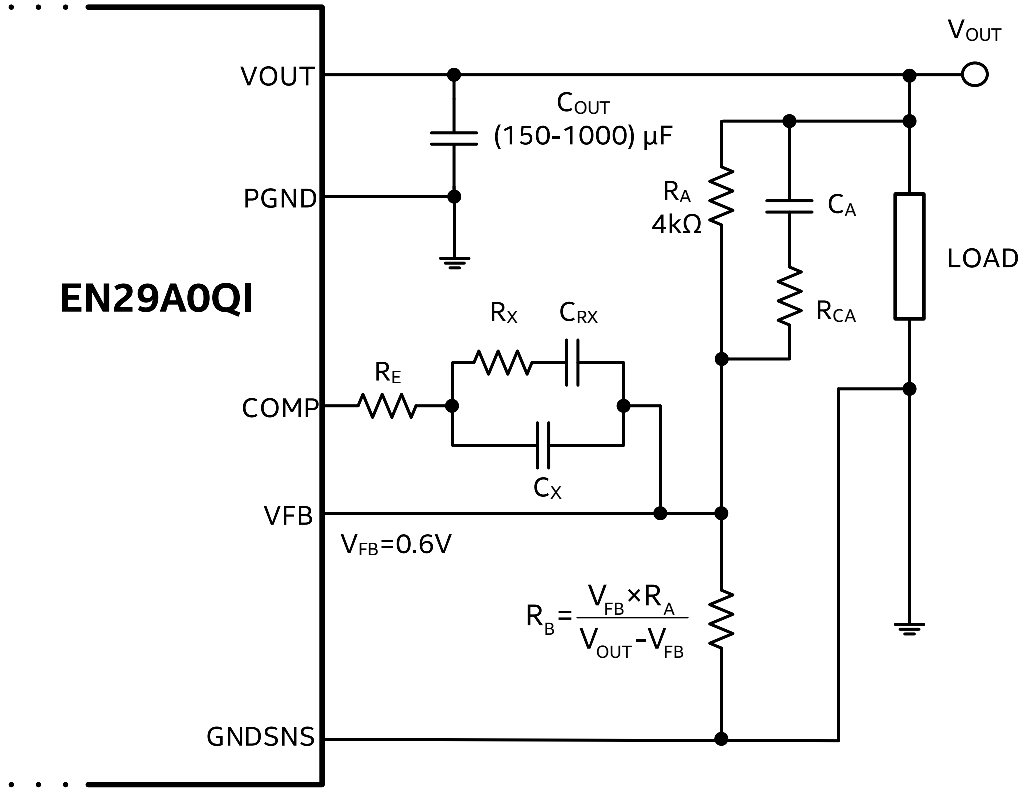


Figure 7: VOUT Resistor Divider & Compensation Network

The recommended R_A resistor value is 4kΩ and the feedback voltage is typically 0.6V. Depending on the output voltage (V_{OUT}), the R_B resistor value may be calculated as shown in Figure 7. Since the accuracy of the output voltage setting is dependent upon the feedback voltage and the external resistors, 1% or better resistors are recommended. The external compensation capacitor (C_A) and resistor (R_{CA}) is also required in parallel with R_A. Table 9 shows external compensation recommendations for a minimum footprint solution and for optimized transient response for different output voltages at V_{IN} = 12V.

Table 9: External Compensation Recommendations

CONFIGURATION	VOUT (V)	R_A (kΩ)	C_A (pF)	R_{CA} (Ω)	R_X (kΩ)	C_X (pF)	C_{RX} (pF)	C_{OUT} (µF)
Minimum size	$0.75 \leq V_{OUT} \leq 3.3$	4	680	150	4	10	1000	3 x 47 (1206)
Optimized transient response	$0.75 \leq V_{OUT} \leq 1.5$	4	470	150	10	10	1000	4 x 47 (1206) + 470
	$1.5 < V_{OUT} \leq 2.5$	4	330	150	10	10	1000	4 x 47 (1206) + 470
	$2.5 < V_{OUT} \leq 3.3$	4	330	150	15	10	1000	4 x 47 (1206) + 470