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Enpirion EV1320QI 2A Sink/Source DDR Termination Converter Evaluation Board

Introduction

Thank you for choosing Altera Enpirion power products!

Along with this document you will also need the latest device datasheet.

- The EV1320QI operates by charging a pair of capacitors in series and connecting them in parallel to generate an output voltage which is nearly one half the input voltage. There is no feedback control, and the output voltage is not regulated. The output voltage is directly proportional to the input voltage and is also affected by the load.
- The division by two property makes the EV1320 a suitable part for VTT applications for up to 2A of load current.
- The capacitor configuration around the EV1320 package determines how the device operates. For this evaluation board, the capacitors around the device have been chosen to minimize the output voltage droop as a function of load current. Please see Figure 1.

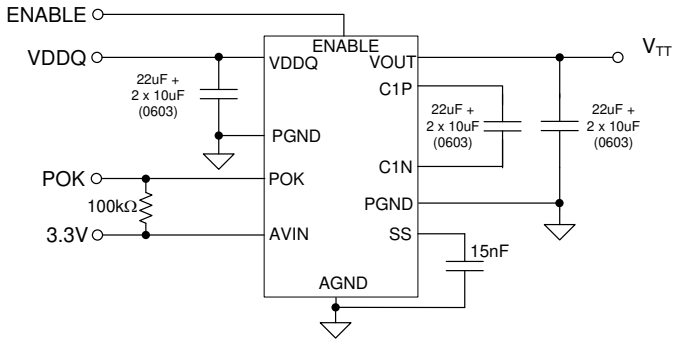


Figure 1: EV1320 Simplified Application Schematic

Quick Start Guide

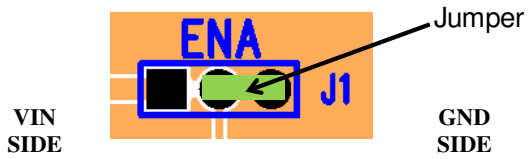


Figure 2: J2 allows control of the Enable pin.

The jumper on Enable pin as shown in Figure 2 is in disable mode. When jumper is between the middle and right pins the signal pin is connected to ground or logic low. When the jumper is between the left and middle pins, the signal pin is connected to AVIN or logic High.

WARNING: complete steps 1 through 4 before applying power to the EV1320QI evaluation board.

STEP 1: Set the "ENA" jumper to the Disable Position. See Figure 2 above.

STEP 2: With the AVIN power supply off, connect it to the input connectors AVIN (TP14) and PGND (TP16) as indicated in Figure 3 and set the power supply to the desired voltage (3.3V nominal).

STEP 3: With the VDDQ power supply off, connect it to the input power connectors VDDQ (TP12) and PGND (TP17) as indicated in Figure 3, and set the power supply to the desired voltage (1.2V–1.8V).

CAUTION: Be mindful of the polarity and magnitude. This evaluation board has no reverse polarity or voltage clamping protection on it.

STEP 4: Connect the load to the output connectors VOUT (TP13) and PGND (TP15), as indicated in Figure 3.

STEP 5: Power up the board by turning on the AVIN power supply first and then the VDDQ supply. Next, move the ENA jumper to the enabled position. The EV1320QI is now powered up and VOUT should be half of VDDQ. You can now make Efficiency, Ripple, Line/Load Regulation, Load transient, Power OK, and temperature related measurements.

STEP 6: Power Up/Down Behavior – Remove ENA jumper and connect a pulse generator (output disabled) signal to the middle pin of ENA and Ground. Set the pulse amplitude to swing from 0 to 2.5 volts. Set the pulse period to 10msec, duty cycle to 50% and fast transition (<1usec.) Hook up oscilloscope probes to ENA, POK and V_{OUT} with clean ground

returns. Turn on pulse generator output. Observe the V_{OUT} voltage ramps as ENA goes high and again as ENA goes low.

STEP 7: You can also operate the board by leaving the ENA jumper in the high position. Then apply AVIN to the board. Next, turn on the VDDQ supply. The output will ramp up and down as half of VDDQ all the time.

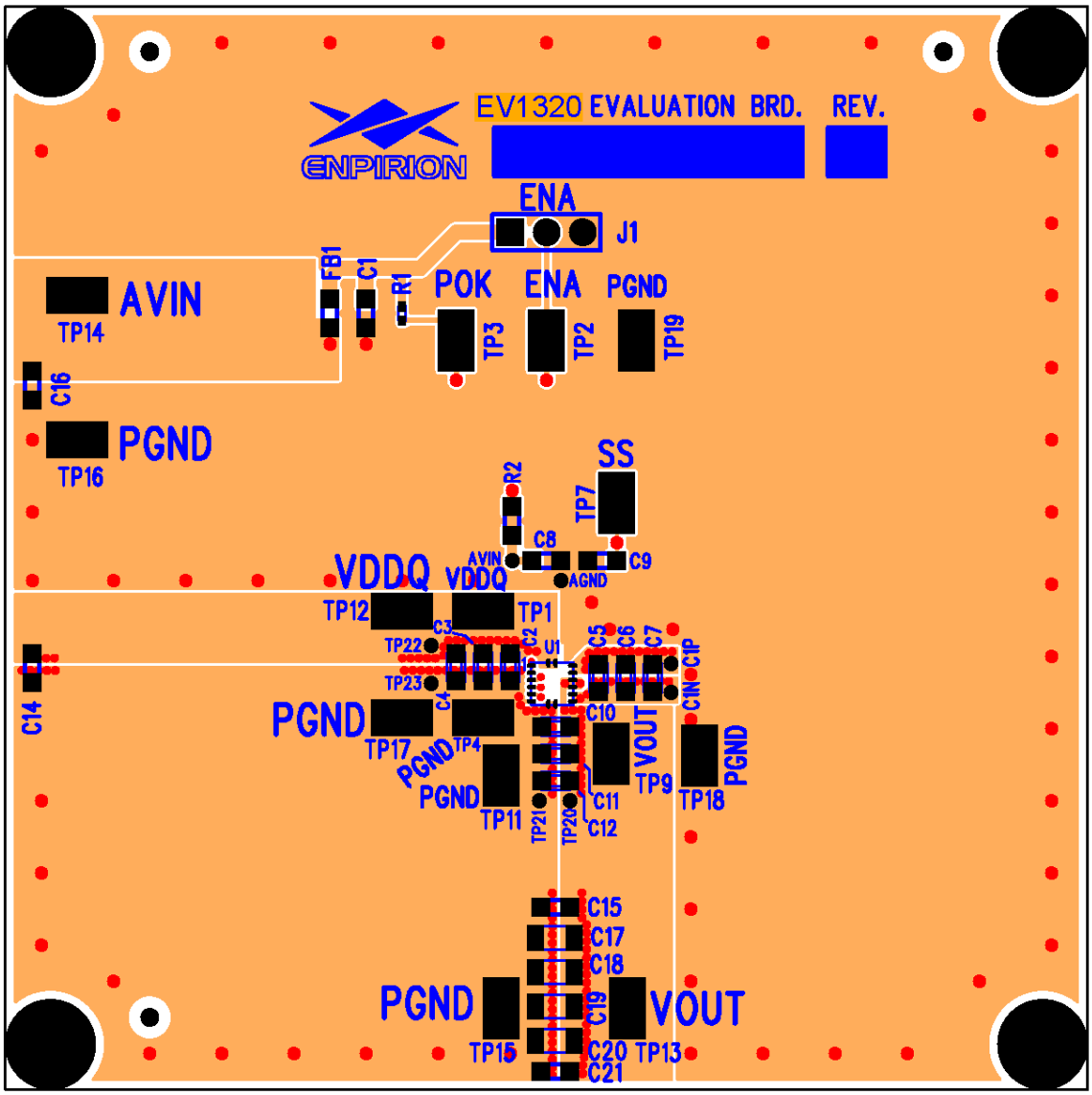


Figure 3: Evaluation Board Top Side Assembly and Copper Layers

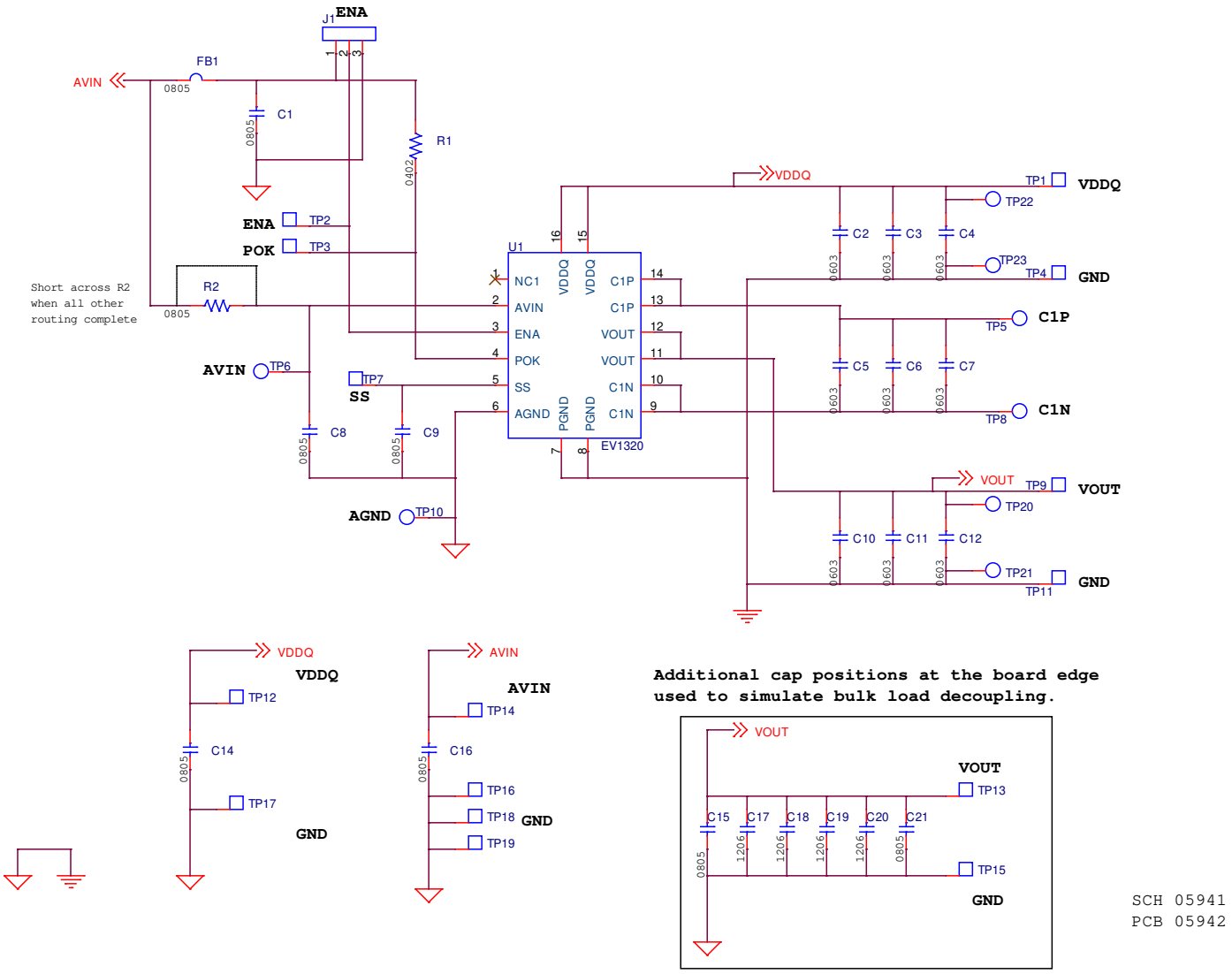
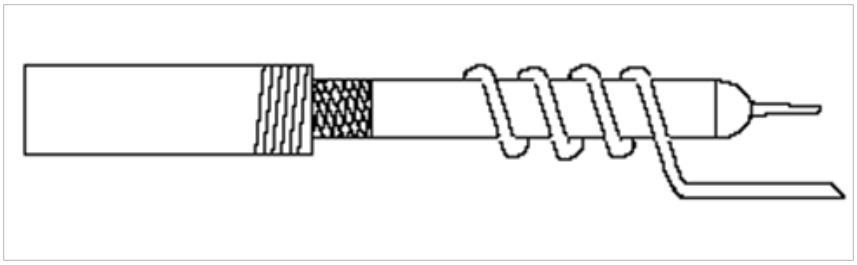


Figure 4: Evaluation Board Schematic

Test Recommendations

To guarantee measurement accuracy, the following precautions should be observed:

1. Make all input and output voltage measurements at the board using the surface mount test points provided (TP1 & TP4 for VDDQ, and TP9 & TP11 for VOUT). This will eliminate voltage drop across the line and load cables that can produce false readings.
2. Measure input and output current with calibrated series ammeters or accurate shunt resistors. This is especially important for measuring efficiency.
3. Use a low-loop-inductance probe tip similar to the one shown below to measure V_{OUT} ripple and switching signals to avoid noise coupling into the probe ground lead. Output ripple and load transient deviations can either be measured right after the device output capacitors, or at the board edge.
   Depending on the application, V_{OUT} ripple may not meet the customer requirement next to the last output capacitor C12. This may not matter so much because the critical spot to meet ripple requirements is at the load. This evaluation board comes with capacitors at the board edge which emulate bulk load decoupling. The ripple at the board edge is therefore significantly lower than next to the device. For more accurate ripple measurement techniques, please refer to Enpirion Output Ripple Measurement Methods Application Note (www.altera.com/enpirion). You can modify the board edge capacitor configuration as needed to match your specific load decoupling.



4. The board includes a pull-up for the POK signal and ready to monitor the power OK status.
5. A soft-start capacitor is populated on the board to provide a reasonable soft-start time. It can be changed as needed.

ALWAYS power down device before changing any board level components!

Bill of Materials

Designator	Qty	Description
C1, C14, C16	3	CAP, 10uF X7R 10V 0805 10%
C2, C5, C10	3	CAP, 22UF X5R 4V 0603 20%
C3, C4, C6, C7,C11, C12	6	CAP, 10UF X5R 4V 0603 20%
C9	1	CAP, 15000PF X7R 50V 0805 10%
C15, C17-C21	6	CAP, 22UF X5R 6.3V 0805 20%
C8, R2	2	NOT USED
FB1	1	SMT FERRITE BEAD 4A 0805, WURTH ELECTRONIK 742792012
J1	1	CONN HEADER, VERTICAL, 3 POSITION, 0.100", TIN
R1	1	RES 100K OHM 1/16W 1% 0402 SMD
TP1-TP4, TP7, TP9, TP11-TP19	15	TEST POINT SURFACE MOUNT, KEYSTONE 5016
U1	1	EV1320QI QFN 2A

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