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EVB-LAN9355
Evaluation Board
User's Guide

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949

Object of Declaration: EVB-LAN9355

EU Declaration of Conformity
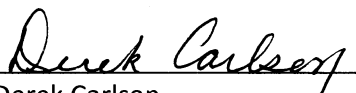
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Derek Carlson
VP Development Tools

16-July-2013
Date

NOTES:

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Preface

NOTICE TO CUSTOMERS

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Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9355. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9355 Evaluation Board as a development tool for the LAN9355 three-port 10/100 managed Ethernet switch. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9355 Evaluation Board.
- **Chapter 2. "Getting Started"** – Includes instructions on how to get started with the EVB-LAN9355 Evaluation Board.
- **Chapter 3. "Board Configuration"** – Provides information about the EVB-LAN9355 Evaluation Board battery charging features.
- **Appendix A. "EVB-LAN9355 Evaluation Board"** – This appendix shows the EVB-LAN9355 Evaluation Board.
- **Appendix B. "EVB-LAN9355 Evaluation Board Schematics"** – This appendix shows the EVB-LAN9355 Evaluation Board schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9355 Evaluation Board Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	`file`.o, where `file` can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (July 2015)

• Initial Release of this Document.

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9355 is a fully featured, three-port 10/100 managed Ethernet switch designed for industrial and embedded applications where performance, flexibility, ease of integration and system cost control are required.

The LAN9355 combines all the functions of a 10/100 switch system, including the switch fabric, packet buffers, buffer manager, media access controllers (MACs), PHY transceivers, and serial management. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hard-ware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks.

The LAN9355 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

100BASE-FX is supported via an external fiber transceiver and cable diagnostics (open and length) is included on the internal twisted pair copper interface.

The EVB-LAN9355 is an Evaluation Board (EVB) that utilizes the LAN9355 to provide a fully-functional three-port Ethernet switch with Dual MII/RMII/TurboMII. The EVB9355 provides one fully integrated MAC/PHY internet ports (Ports 2) via on-board RJ45 connectors. Port 0 and Port 1 provides two MII port connectors which support the following:

• An external Dual MII/RMII/Turbo MII –Capable MAC (with LAN9355 in PHY mode), via the on-board 40-pin male MII connector
• An external Dual MII/RMII/Turbo MII –Capable PHY (with LAN9355 in MAC mode), via the on-board 40-pin female MII connector

Power is supplied to the board via a +5V external wall mount power supply.

The EVB-LAN9355 includes a 64K x 8 I2C EEPROM that may be used to automatically load configuration settings from the EEPROM into the device at reset. An I2C host adapter interface header (10-pin, 2x5) is provided to simplify I2C based configuration. A simplified block diagram of the EVB LAN9355 can be seen in Figure 1-1.

FIGURE 1-1:   EVB-LAN9355 BLOCK DIAGRAM
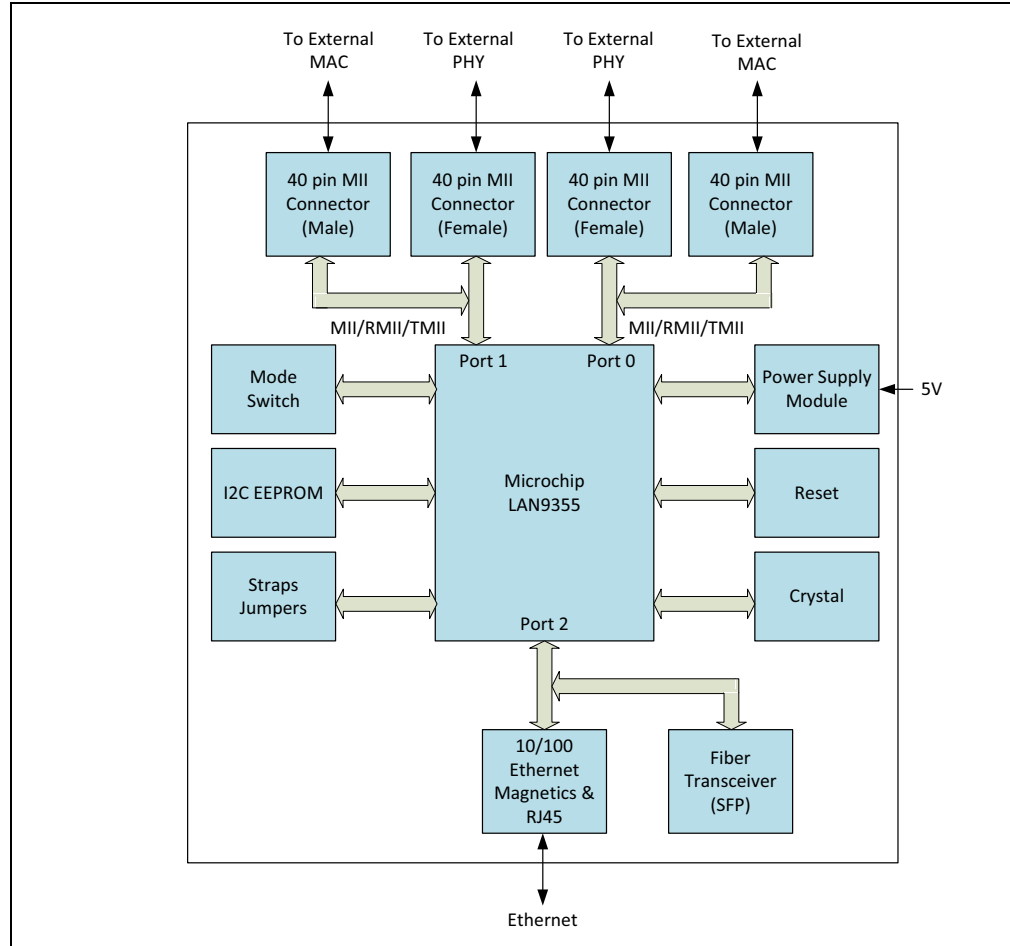
1.1.1   References

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

Document	Location
LAN9355 datasheet	Visit www.microchip.com
AN8-13 Suggested Magnetics	http://www.microchip.com/wwwAppNotes/AppNotes.aspx?appnote=en562793
EVB-LAN9355 Evaluation Board Schematic	Visit www.microchip.com

1.1.2 Terms and Abbreviations

- **EVB** - Evaluation Board
- **DNP** - Do Not Populate
- **100BASE-TX** - 100 Mbps Fast Ethernet, IEEE802.3u Compliant
- **GPIO** - General Purpose I/O
- **MII** - Media Independent Interface
- **RMII** - Reduced Media Independent Interface
- **EEE** - Energy-Efficient Ethernet
- **SFP** - Small Form-factor Pluggable
- **SFF** - Small Form Factor
- **SMI** - Serial Management Interface

Chapter 2. Board Details

2.1   BOARD DETAILS

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the EVB-LAN9355 is shown in Figure 2-1.

FIGURE 2-1:   **LAN9355 BOARD REV-A**
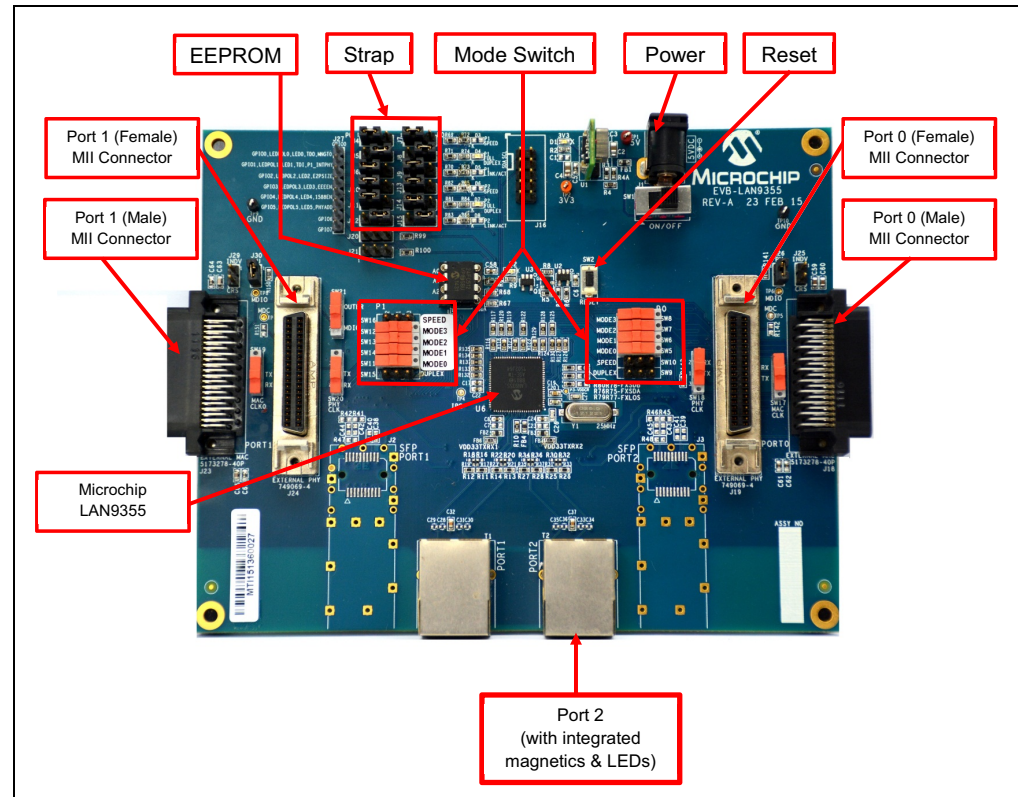
2.1.1   Power

DC 5V is applied through (J1) DC Socket, powered by a +5V external wall adapter switch (SW1) need to be ON position for the 5V to reach the 3.3V regulator. Glowing of Green LED (D1) indicates successful generation of 3.3V o/p. This Power is supplied to the LAN9355 and it has internal 1.2 V regulator which supplies power to the internal core logic.

2.1.2   Power-on Reset

A power-on reset occurs whenever power is initially applied to the LAN9355 or if the power is removed and reapplied to the LAN9355. This event resets all circuitry within the LAN9355. After initial power-on, the LAN9355 can be reset by pressing the reset switch (SW2). The reset LED D2 will assert (red) when the LAN9355 is in reset condition.

For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.1.3   Clock

The LAN9355 requires a fixed-frequency 25 MHz clock (±50 ppm) source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25 MHz crystal to the OSCI and OSCO pins. Optionally, this clock can be provided by driving the OSCI input pin with a single-ended 25 MHz clock source.

Chapter 3. Board Configuration

3.1   STRAP OPTIONS

The following tables describe the default settings and jumper descriptions for the EVB-LAN9355. These defaults are the recommended configurations for evaluation of the LAN9355. These settings may be changed as needed, however, any deviation from the defaults settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

3.1.1   Jumpers J4:J15

Jumpers J4 through J15 set various functions of the LAN9355. They can also be used as GPIOs, LED drivers. When used as LED drivers, as they are on the EVB-LAN9355, they are connected a specific way to set the strap value to a "1", and another way to set the strap value to a "0". Figure 3-1 illustrates the schematics connections with the D3 circuit as a pull-up, and the D4 circuit as a pull-down. To illuminate D3, the LAN9355 will drive the cathode of the D3 low. To illuminate D4, the LAN9355 will drive the cathode of the D4 high.

The J4 - J15 jumpers must be configured in pairs to identical settings in order to realize the D3 circuit or the D4 circuit. The pairings are as follows:

- J4 & J7
- J6 & J9
- J5 & J8
- J11 & J14
- J10 & J13
- J12 & J15

The following subsections detail the jumper pair settings, their associated strap settings, and the functional effects of setting the straps. All strap values are read during power-up and on the rising edge of nRST signal. Once the strap value is set, the LAN9355 will drive the LED's high or low for illumination according the strap value. For other designs which may use these pins as GPIOs refer to LAN9355 datasheet for additional information. In those cases, internal default straps must be changed by an I2C or SMI master or through EEPROM fields.

FIGURE 3-1: **LED STRAP CIRCUIT**
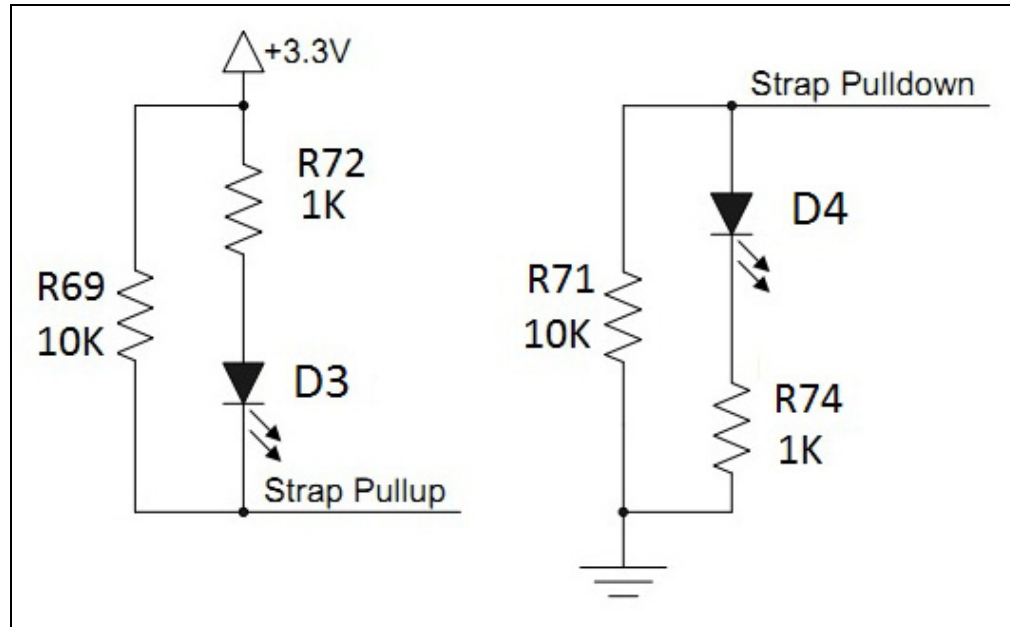
3.1.1.1   GPIO/LED POL/LED CONFIGURATIONS:

GPIO/LED POL/LED configuration straps are used to configure the default polarity of LEDs, GPIOs through jumpers as shown below in Table 3-1.

TABLE 3-1: **GPIO/LED POL/LED CONFIGURATIONS**

Header	Pin Settings	Signal Name	Strap Value	Description
J4 & J7	1-2(default)	LEDPOL0 /GPIO0 /LED0	1	The LED (D3) is set as active LOW.
	2 -3		0	The LED (D3) is set as active HIGH.
J5 & J8	1-2(default)	LEDPOL1 /GPIO1 /LED1	1	The LED (D4) is set as active LOW.
	2 -3		0	The LED (D4) is set as active HIGH.
J6 & J9	1-2(default)	LEDPOL2 /GPIO2 /LED2	1	The LED (D5) is set as active LOW.
	2 -3		0	The LED (D5) is set as active HIGH.
J10 & J13	1-2(default)	LEDPOL3 /GPIO3 /LED3	1	The LED (D6) is set as active LOW.
	2 -3		0	The LED (D6) is set as active HIGH.

TABLE 3-1:   GPIO/LED POL/LED CONFIGURATIONS (CONTINUED)

Header	Pin Settings	Signal Name	Strap Value	Description
J11 & J14	1-2(default)	LEDPOL4 /GPIO4 /LED4	1	The LED (D7) is set as active LOW.
	2 -3		0	The LED (D7) is set as active HIGH.
J12 & J15	1-2(default)	LEDPOL5 /GPIO5 /LED5	1	The LED (D8) is set as active LOW.
	2 -3		0	The LED (D8) is set as active HIGH.

3.1.1.2   SERIAL MANAGEMENT MODE CONFIGURATION

Serial Management Mode selection strap (MNGT0) is used to configure the default value of the Serial Management Mode Strap hard-strap (serial_mngt_mode_strap) through jumpers as shown below in Table 3-2.

TABLE 3-2:   SERIAL MANAGEMENT MODE CONFIGURATION

Header	Pin Settings	serial_mngt_mode_ strap	Description
J4 & J7	2-3	0	SMI Managed Mode
J4 & J7	1-2 (default)	1	I2C Managed Mode

3.1.1.3   EEPROM SIZE CONFIGURATION:

The EEPROM size configuration strap (J6 & J9) determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512 as shown below in Table 3-3.

TABLE 3-3:   EEPROM SIZE CONFIGURATION

Header	Pin Settings	eeprom_size_strap Value	Description
J6 & J9	1-2 (default)	1	EEPROM size = 32K bits (4k x 8) through 512K bits (64K x 8)
	2 -3	0	EEPROM size = 1K bits (128 x 8) through 16K bits (2K x 8)

3.1.1.4   ENERGY-EFFICIENT ETHERNET CONFIGURATION

EEEEEE_ENEN configuration strap is used to configure the default value of the EEE Enable 2-1 soft-straps (EEE_enable_strap_[2:1]) through jumpers as shown below in Table 3-4.

> **Note:**   "EEE_enable_strap_1" strap is used for the LAN9355 when in Port 1 internal PHY mode.

TABLE 3-4:   EEE_EN CONFIGURATION

Header	Pin Settings	EEE_enable_strap_[2:1] Value	Description
J10 & J13	1-2(default)	1	EEE Enable
	2 -3	0	EEE Disable

3.1.1.5   1588 ENABLE CONFIGURATION

Energy Efficient Ethernet configuration strap is used to configure the default value of the 1588 Enable soft-strap (1588_enable_strap) through jumpers as shown below in Table 3-5.

TABLE 3-5:   1588 ENABLE CONFIGURATION

Header	Pin Settings	1588_enable_strap Value	Description
J11 & J14	1-2 (default)	1	1588 Enable
	2 -3	0	1588 Disable

3.1.1.6   PHY ADDRESS CONFIGURATION

PHY Address selection strap is used to configure the default value of the Switch PHY Address Select soft-strap (phy_addr_sel_strap) through jumpers as shown below in Table 3-6.

TABLE 3-6:   PHY ADDRESSING

Header	Pin Settings	PHY_ADDR_SEL_STRAP Value	VIRTUAL PHY 0 AND 1 DEFAULT ADDRESS VALUE	PHY A DEFAULT ADDRESS VALUE	PHY B DEFAULT ADDRESS VALUE
J12 & J15	1-2	1	1	2	3
	2-3 (default)	0	0	1	2

3.1.2   GPIO 6 & GPIO 7 Input and Output Configurations

GPIO 6 & 7 configuration straps are used to configure the default input value of the GPIO 6 and 7 through jumpers as shown below in Table 3-7 and Table 3-8.

TABLE 3-7:   GPIO 6 & 7 INPUT CONFIGURATION

Header	Pin Settings	Input	Signal Name
J20	1-2	1	GPIO6
	2-3	0	
J21	1-2	1	GPIO7
	2-3	0	

TABLE 3-8:   GPIO 6 & 7 OUTPUT CONFIGURATION

Header	Pin	Output	Signal Name
J20	2	Push Pull	GPIO6
J21	2	Push Pull	GPIO7

Note: By default, the jumpers settings for J20 & J21 will be OPEN.

3.1.3   Link Partner Duplex/Speed Configurations

The "duplex_strap_0" strap from SW9 is used to determine the link partners duplex ability when in Port 0 MII MAC and RMII MAC modes.

The "speed_strap_0" strap from SW10 is used to determine the link partners speed ability and to determine the parallel detect speed when in Port 0 MII MAC and RMII MAC modes, as shown below in Table 3-9.

TABLE 3-9:   EMULATED LINK PARTNER DEFAULT ADVERTISED ABILITY FOR PORT 0

SW9 (P0_DUPLEX)	SW10 (P0_SPEED)	duplex_strap_0	speed_strap_0	ADVERTISED LINK PARTNER ABILITY
1-2	1-3	1	0	10BASE-T full-duplex (0010)
1-2	1-2	1	1	100BASE-X full-duplex (1000)
1-3	1-3	0	0	10BASE-T half-duplex (0001) (Default)
1-3	1-2	0	1	100BASE-X half-duplex (0100)

Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

The "duplex_strap_1" strap from SW15 is used to determine the link partners duplex ability when in Port 1 MII MAC and RMII MAC modes.

The "speed_strap_1" strap from SW16 is used to determine the link partners speed ability and to determine the parallel detect speed when in Port 1 MII MAC and RMII MAC modes, as shown below in Table 3-10.

TABLE 3-10:   EMULATED LINK PARTNER DEFAULT ADVERTISED ABILITY FOR PORT 1

SW15 (P1_DUPLEX)	SW16 (P1_SPEED)	duplex_strap_0	speed_strap_0	ADVERTISED LINK PARTNER ABILITY
1-2	1-3	1	0	10BASE-T full-duplex (0010)
1-2	1-2	1	1	100BASE-X full-duplex (1000)
1-3	1-3	0	0	10BASE-T half-duplex (0001) (Default)
1-3	1-2	0	1	100BASE-X half-duplex (0100)

Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

3.1.4   Port 0/Port 1 Mode Configurations

Port 0 Mode configuration straps (SW5, SW6, SW7 & SW8) are used to configure the hard-straps such as Switch Port 0 Mode Strap (P0_mode_strap[1:0]), Switch Port 0 RMII Clock Direction Strap (P0_rmii_clock_dir_strap) and Switch Port 0 Clock Strength Strap (P0_clock_strength_strap) as shown below in Table 3-11.

TABLE 3-11:   PORT 0 MODE STRAP MAPPING

P0_MODE3 (SW8)	P0_MODE2 (SW7)	P0_MODE1 (SW6)	P0_MODE0 (SW5)	MODE
1-3	1-3	X	X	MII MAC (default)
1-3	1-2	1-3	X	MII PHY
1-3	1-2	1-2	1-3	Turbo MII PHY 12 ma
1-3	1-2	1-2	1-2	Turbo MII PHY 16 ma
1-2	1-3	1-3	X	RMII MAC clock in
1-2	1-3	1-2	1-3	RMII MAC clock out 12ma
1-2	1-3	1-2	1-2	RMII MAC clock out 16ma
1-2	1-2	1-3	X	RMII PHY clock in
1-2	1-2	1-2	1-3	RMII PHY clock out 12ma
1-2	1-2	1-2	1-2	RMII PHY clock out 16ma

Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

Port 1 Mode configuration straps (SW11, SW14, SW13 & SW12) are used to configure the hard-straps such as Switch Port 1 Mode Strap (P1_mode_strap[1:0]), Switch Port 1 RMII Clock Direction Strap (P1_rmii_clock_dir_strap) and Switch Port 1 Clock Strength Strap (P1_clock_strength_strap) as shown below in Table 3-12.

TABLE 3-12:   PORT 1 MODE STRAP MAPPING

P1_INTPHY (J5 & J8)	P1_MODE3 (SW12)	P1_MODE2 (SW13)	P1_MODE1 (SW14)	P1_MODE0 (SW11)	MODE
2-3	1-3	1-3	X	X	MII MAC (default)
2-3	1-3	1-2	1-3	X	MII PHY
2-3	1-3	1-2	1-2	1-3	Turbo MII PHY 12 ma
2-3	1-3	1-2	1-2	1-2	Turbo MII PHY 16 ma
2-3	1-2	1-3	1-3	X	RMII MAC clock in
2-3	1-2	1-3	1-2	1-3	RMII MAC clock out 12ma
2-3	1-2	1-3	1-2	1-2	RMII MAC clock out 16ma
2-3	1-2	1-2	1-3	X	RMII PHY clock in
2-3	1-2	1-2	1-2	1-3	RMII PHY clock out 12ma
2-3	1-2	1-2	1-2	1-2	RMII PHY clock out 16ma
1-2	X	X	X	X	Internal PHY

Note: For Switches to short 1-3, Knob Position should be at 1-2 and vice versa.

3.1.5 RMII RX Clock Configurations

When LAN9355 is in MAC/PHY mode the reference clock routed either through TX or RX Clock as shown in Table 3-13.

TABLE 3-13: RX CLOCK CONFIGURATIONS FOR PORT 0

Switch Settings	DESCRIPTION	Mode
SW19 (1-3) (Default)	TX Clock used as a Reference Clock	RMII MAC
SW19 (1-2)	RX Clock used as a Reference Clock	RMII MAC
SW20 (1-3) (Default)	Reference clock used as a TX clock	RMII PHY
SW20 (1-2)	Reference clock used as a RX clock	RMII PHY

3.1.6 GPIO Header

J27 connector is used for GPIO header. Respective pin details are given below in Table 3-14.

TABLE 3-14: PIN NAMES FOR GPIO HEADER

Signal Name	Pin Number
GPIO0	J27.1
GPIO1	J27.2
GPIO2	J27.3
GPIO3	J27.4
GPIO4	J27.5
GPIO5	J27.6
GPIO6	J27.7
GPIO7	J27.8

3.1.7 I2C Aardvark® Header

J16 connector is used for I2C Aardvark header. Respective pin details are given below in Table 3-15.

TABLE 3-15: PIN NAMES FOR I2C AARDVARK HEADER

Signal Name	Pin Number
I2C2_SCL	J16.1
I2C2_SDA	J16.3
GND	J16.2 & J16.10

3.1.8 Copper and Fiber Mode Selections

The LAN9355 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) in SFP mode. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must to be configured.

> **Note:** Vendor part number for SFP Transceiver: Finisar/FTLF1217P2.

3.1.8.1 COPPER MODE

The EVB-LAN9355 is set to Copper Mode by default. Table 3-16 details the required strap resistors settings for Copper Mode operation.

TABLE 3-16: COPPER MODE STRAP RESISTORS

Resistors	Signal Names	Description
R79 (10K)	FXLOSEN	Copper twisted pair for ports A and B further determined by FXSDENA and FXSDENB
R76, R80 (10K)	FXSDA/FXSDB	Configures Port 0 and Port 1 to Copper Mode

> **Note:** R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-17 must be assembled for Copper Mode operation.

TABLE 3-17: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19, R21, R23	Port 0 Copper mode is Enabled
R31, R33, R35, R37	Port 1 Copper mode is Enabled

> **Note:** R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

3.1.8.2 FIBER MODE

The LAN9355 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resisters must be configured.

> **Note:** Copper Mode related resistors must be DNP while Fiber Mode is active (See **Section 3.1.8.1 "Copper Mode"**).

Table 3-18 details the required strap resistor settings for Fiber Mode operation.

TABLE 3-18: FIBER MODE STRAP RESISTORS

Resistors	Description
R77 (10K)	Configures Port 0 & 1 to FX_LOS Mode
R75, R78 (10K)	Configures Port 0 & 1 to Fiber mode, respectively

> **Note:** R76, R79, and R80 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-19 must be assembled for Fiber Mode operation.

TABLE 3-19:   FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 0 Fiber mode Enabled
R30, R32, R34, R36	Port 1 Fiber mode Enabled

> **Note:**   R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

3.1.8.3   FX-LOS FIBER MODE STRAP

FX-LOS strap details are shown in Table 3-20. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 3-20:   FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (v)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port 1
Populate	Populate	1.5	A level of 1.5V selects FX-LOS for Port 0 and FX-SD / Copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / Copper twisted pair for Ports 0 and 1, further determined by FXSDA, FXSDB

> **Note:**   The above strap details describe the LAN9355 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

3.2   LEDS

Table 3-21 describes the different LED references and their corresponding colors and indications.

TABLE 3-21:   LEDS

Reference	Color	Indication
D1	Green	3.3V Power active
D2	Red	LAN9355 is in reset condition
D4	Green	Full-duplex / Collision Port 1
D6	Green	Full-duplex / Collision Port 2

> **Note:**   Assumes the LED_FUN field of the LED_CFG register is 00b.

3.3   TEST POINTS

Table 3-22 describes the different test points and their corresponding connections.

TABLE 3-22:   TEST POINTS

Test Points	Description	Connection
TP1	Single pin populated 5V	5V_EXT
TP2	Single pin populated 3V3	3V3
TP3	Single pin unpopulated VDDCR	VDDCR

TABLE 3-22:   TEST POINTS

Test Points	Description	Connection
TP4	Single pin unpopulated IRQ	IRQ
TP5	Single pin unpopulated P0_MDC	P0_MDC
TP6	Single pin unpopulated P0_MDIO	P0_MDIO
TP7	Single pin unpopulated P1_MDC	P1_MDC
TP8	Single pin unpopulated P1_MDIO	P1_MDIO
TP9	Single pin populated GND	GND
TP10	Single pin populated GND	GND

3.4   MECHANICALS

Figure 3-2 displays details for EVB-LAN9355 mechanical dimensions. Dimensions are in mm.

FIGURE 3-2:   LAN9355 EVB MECHANICAL DIMENSIONS