

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts, Customers Priority, Honest Operation, and Considerate Service", our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip, ALPS, ROHM, Xilinx, Pulse, ON, Everlight and Freescale. Main products comprise IC, Modules, Potentiometer, IC Socket, Relay, Connector. Our parts cover such applications as commercial, industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China









RT9081AGQZA Linear Regulator Evaluation Board

Purpose

The The RT9081A is a high performance positive voltage regulator with separated bias voltage (V_{BIAS}), designed for applications requiring low input voltage and ultra low dropout voltage, output current up to 500mA. This document explains the function and use of the RT9081A evaluation board (EVB), and provides information to enable operation, modification of the evaluation board and circuit to suit individual requirements.

Table of Contents

Purpose	1
ntroduction	
Key Performance Summary Table	2
Bench Test Setup Conditions	3
Schematic, Bill of Materials & Board Layout	5
PCB Layout	6
More Information	7
moortant Notice for Richtek Evaluation Board	7



Introduction

General Product Information

The RT9081A is a high performance positive voltage regulator with separated bias voltage (V_{BIAS}), designed for applications requiring low input voltage and ultra low dropout voltage, output current up to 500mA. The feature of ultra low dropout voltage is ideal for applications where output voltage is very close to input voltage. The input voltage can be as low as 0.8V and the output voltage is adjustable by an external resistive divider. The RT9081A features very low quiescent current consumption for portable applications. The device is available in the ZADFN-6L 1.2x1.2 package.

Product Feature

Input Voltage Range: 0.8V to 5.5V
Bias Voltage Range: 2.4V to 5.5V
1.5% Output Voltage Accuracy @ 25°C

• Ultra Low Dropout Voltage: 140mV at 500mA

Low Bias Input Current :
 ▶ 80µA in Operating Mode
 ▶ 0.5µA in Disable Mode

• Enable Control

• Active Discharge Function

• Stable with a 1µF Output Ceramic Capacitor

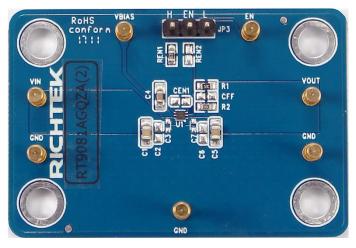
Key Performance Summary Table

Key Features Evaluation Board Number: PCB087_V1		
Default Input Voltage	V _{OUT} (N _{ormal}) + 0.3V < V _{IN} < 5.5V, V _{OUT} + 1.6V < V _{BIAS} < 5.5V	
Max Output Current	500mA	
Default Output Voltage	1.2V	
Default Marking & Package Type	RT9081AGQZA(2), ZADFN-6L 1.2x1.2	



Bench Test Setup Conditions

Headers Description and Placement



Carefully inspect all the components used in the EVB according to the following Bill of Materials table, and then make sure all the components are undamaged and correctly installed. If there is any missing or damaged component, which may occur during transportation, please contact our distributors or e-mail us at evb-service@richtek.com.

Test Points

The EVB is provided with the test points and pin names listed in the table below.

Test point/ Pin name	Signal	Comment (expected waveforms or voltage levels on test points)		
VIN	Input voltage	Power input for the LDO.		
EN	Enable test point	LDO enable signal input.		
GND	Ground	Ground.		
VBIAS	Power input for the internal control circuit	Supply voltage for the LDO control circuit. Mandatory to power up $V_{\mbox{\footnotesize{BIAS}}}$ before EN and VIN.		
VOUT	Output voltage	Power output for the LDO.		



Power-up & Measurement Procedure

- 1. Connect input power ($V_{VOUT} + 0.3V < V_{IN} < 5.5V$, $V_{OUT} + 1.6V < V_{BIAS} < 5.5V$) and input ground to VIN/VBIAS and GND test pins respectively.
- 2. Connect positive end and negative terminals of load to VOUT and GND test pins respectively.
- 3. There is a 3-pin header "EN" for enable control. To use a jumper at "H" option to tie EN test pin to input power VIN for enabling the device. Inversely, to use a jumper at "L" option to tie EN test pin and ground GND for disabling the device.
- 4. Verify the output voltage (approximately 1.2V) between VOUT and GND.
- 5. Connect an external load up to 500mA to the VOUT and GND terminals and verify the output voltage and current.

Output Voltage Setting

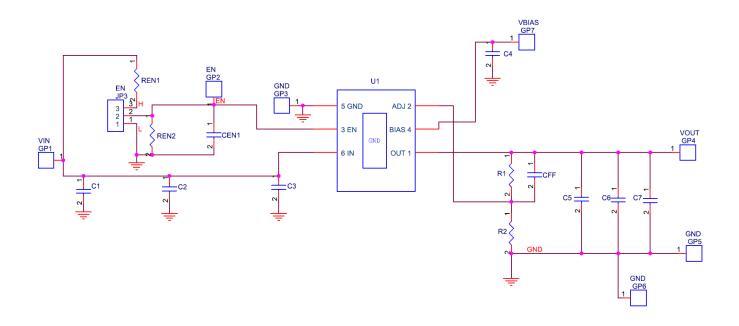
Set the output voltage with the resistive divider (R1, R2) between VOUT and GND with the midpoint connected to FB. The output is set by the following formula:

$$V_{VOUT} = 0.8V \times \left(1 + \frac{R1}{R2}\right)$$



Schematic, Bill of Materials & Board Layout

EVB Schematic Diagram

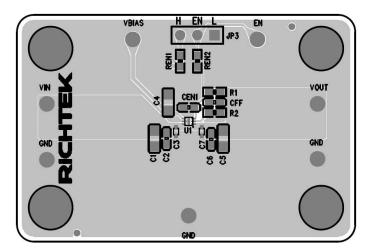


Bill of Materials

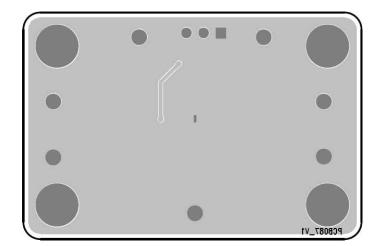
Reference	Qty	Part number	Description	Package	Manufacture
U1	1	RT9081AGQZA(2)	Linear Regulator	ZADFN-6L 1.2x1.2	RICHTEK
C1, C5	2	C2012X7R1E105KT	1μF/25V/X7R	C-0805	TDK
C4	1	C1608X7R1H104K080AA	0.1μF/50V/X7R	C-0603	TDK
R1	1	RTT033322FTP	33.2k	R-0603	旺詮
R2	1	WR06X6652FTL	66.5k	R-0603	WALSIN
REN1	1	WR06X1003FTL	100k	R-0603	WALSIN



PCB Layout



PCB Layout—Top View



PCB Layout—Bottom View



More Information

For more information, please find the related datasheet or application notes from Richtek website http://www.richtek.com.

Important Notice for Richtek Evaluation Board

THIS DOCUMENT IS FOR REFERENCE ONLY, NOTHING CONTAINED IN THIS DOCUMENT SHALL BE CONSTRUED AS RICHTEK'S WARRANTY, EXPRESS OR IMPLIED, UNDER CONTRACT, TORT OR STATUTORY, WITH RESPECT TO THE PRESENTATION HEREIN. IN NO EVENT SHALL RICHTEK BE LIABLE TO BUYER OR USER FOR ANY AND ALL DAMAGES INCLUDING WITHOUT LIMITATION TO DIRECT, INDIRECT, SPECIAL, PUNITIVE OR CONSEQUENTIAL DAMAGES.