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USB3503

USB 2.0 HSIC High-Speed Hub Controller Optimized for Portable Applications

PRODUCT FEATURES

Datasheet

Features

- Integrated USB 2.0 Compatible 3-Port Hub.
- HSIC Upstream Port
- Advanced power saving features
  - 1 µA Typical Standby Current
  - Port goes into power saving state when no devices are connected downstream
  - Port is shutdown when port is disabled.
  - Digital core shut down in Standby Mode
- Supports either Single-TT or Multi-TT configurations for Full-Speed and Low-Speed connections.
- Enhanced configuration options available through serial I2C Slave Port
  - VID/PID/DID
  - String Descriptors
  - Configuration options for Hub.
- Internal Default configuration option when serial I2C host not available.
- MultiTRAK™
  - Dedicated Transaction Translator per port.
- PortMap
  - Configurable port mapping and disable sequencing.
- PortSwap
  - Configurable differential intra-pair signal swapping.
- PHYBoost™
  - Programmable USB transceiver drive strength for recovering signal integrity
- VariSense™
  - Programmable USB receiver sensitivity
- flexPWR® Technology
  - Low current design ideal for battery powered applications
  - Internal supply switching provides low power modes
- External 12, 19.2, 24, 25, 26, 27, 38.4, or 52 MHz clock input
- Internal 3.3V & 1.2V Voltage Regulators for single supply operation.
  - External VBAT and 1.8V dual supply input option
- Internal Short Circuit protection of USB differential signal pins.
- USB Port ESD Protection (**DP**/**DM**)
  - ±15kV (air and contact discharge)
  - IEC 61000-4-2 level 4 ESD protection without external devices
- 25-pin WLCS (1.97mm x 1.97mm Wafer Level Chip Scale) Package - 0.4mm ball pitch

Applications

The USB3503 is targeted for applications where more than one USB port is required. As mobile devices add more features and the systems become more complex it is necessary to have more than one USB port to take communicate with the internal and peripheral devices.

- Mobile Phones
- Tablet Computers
- Ultra Mobile PCs
- Digital Still Cameras
- Digital Video Camcorders
- Gaming Consoles
- PDAs
- Portable Media Players
- GPS Personal Navigation Devices
- Media Players/Viewers

Order Number(s):

ORDER NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	REEL SIZE
USB3503A-1-GL-TR	0C to 70C	25-Ball WLCSP	3000 pieces
USB3503AI-1-GL-TR	-40C to 85C	25-Ball WLCSP	3000 pieces

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

Please contact your SMSC sales representative for additional documentation related to this product such as application notes, anomaly sheets, and design guidelines.

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Chapter 1 General Description

The SMSC USB3503 is a low-power, USB 2.0 hub controller with HSIC upstream connectivity and three USB 2.0 downtream ports. The USB3503 operates as a hi-speed hub and supports low-speed, full-speed, and hi-speed downstream devices on all of the enabled downstream ports.

The USB3503 has been specifically optimized for mobile embedded applications. The pin-count has been reduced by optimizing the USB3503 for mobile battery-powered embedded systems where power consumption, small package size, and minimal BOM are critical design requirements. Standby mode power has been minimized. Instead of a dedicated crystal, reference clock inputs are aligned to mobile applications. Flexible integrated power regulators ease integration into battery powered devices. All required resistors on the USB ports are integrated into the hub. This includes all series termination resistors on D+ and D– pins and all required pull-down resistors on D+ and D– pins.

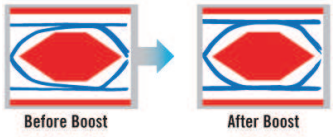
The USB3503 includes programmable features such as:

MultiTRAK™ Technology, which utilizes a dedicated Transaction Translator (TT) per port to maintain consistent full-speed data throughput regardless of the number of active downstream connections. MultiTRAK™ outperforms conventional USB 2.0 hubs with a single TT in USB full-speed data transfers.

PortMap, which provides flexible port mapping and disable sequences. The downstream ports of a USB3503 hub can be reordered or disabled in any sequence to support multiple platform designs with minimum effort. For any port that is disabled, the USB3503 hub controllers automatically reorder the remaining ports to match the USB host controller's port numbering scheme.

PortSwap, which adds per-port programmability to USB differential-pair pin locations. PortSwap allows direct alignment of USB signals (D+/D-) to connectors to avoid uneven trace length or crossing of the USB differential signals on the PCB.

PHYBoost, which provides programmable levels of Hi-Speed USB signal drive strength in the downstream port transceivers. PHYBoost attempts to restore USB signal integrity in a compromised system environment. The graphic on the right shows an example of Hi-Speed USB eye diagrams before and after PHYBoost signal integrity restoration.



VariSense, which controls the USB receiver sensitivity enabling programmable levels of USB signal receive sensitivity. This capability allows operation in a sub-optimal system environment, such as when a captive USB cable is used.

1.1 Customer Selectable Features

A default configuration is available in the USB3503 following a reset. This configuration may be sufficient for most applications. The USB3503 hub may also be configured by an external microcontroller. When using the microcontroller interface, the hub appears as an I^2C slave device.

The USB3503 hub supports customer selectable features including:

- Optional customer configuration via I^2C.
- Supports compound devices on a port-by-port basis.
- Customizable vendor ID, product ID, and device ID.
- Configurable downstream port power-on time reported to the host.
- Supports indication of the maximum current that the hub consumes from the USB upstream port.
- Supports Indication of the maximum current required for the hub controller.
- Configurable as a either a Self-Powered or Bus-Powered Hub
- Supports custom string descriptors (up to 30 characters):
  - Product string
  - Manufacturer string
  - Serial number string
- When available, I^2C configurable options for default configuration may include:
  - Downstream ports as non-removable ports
  - Downstream ports as disabled ports
  - USB signal drive strength
  - USB receiver sensitivity
  - USB differential pair pin location

1.1.1 Block Diagram

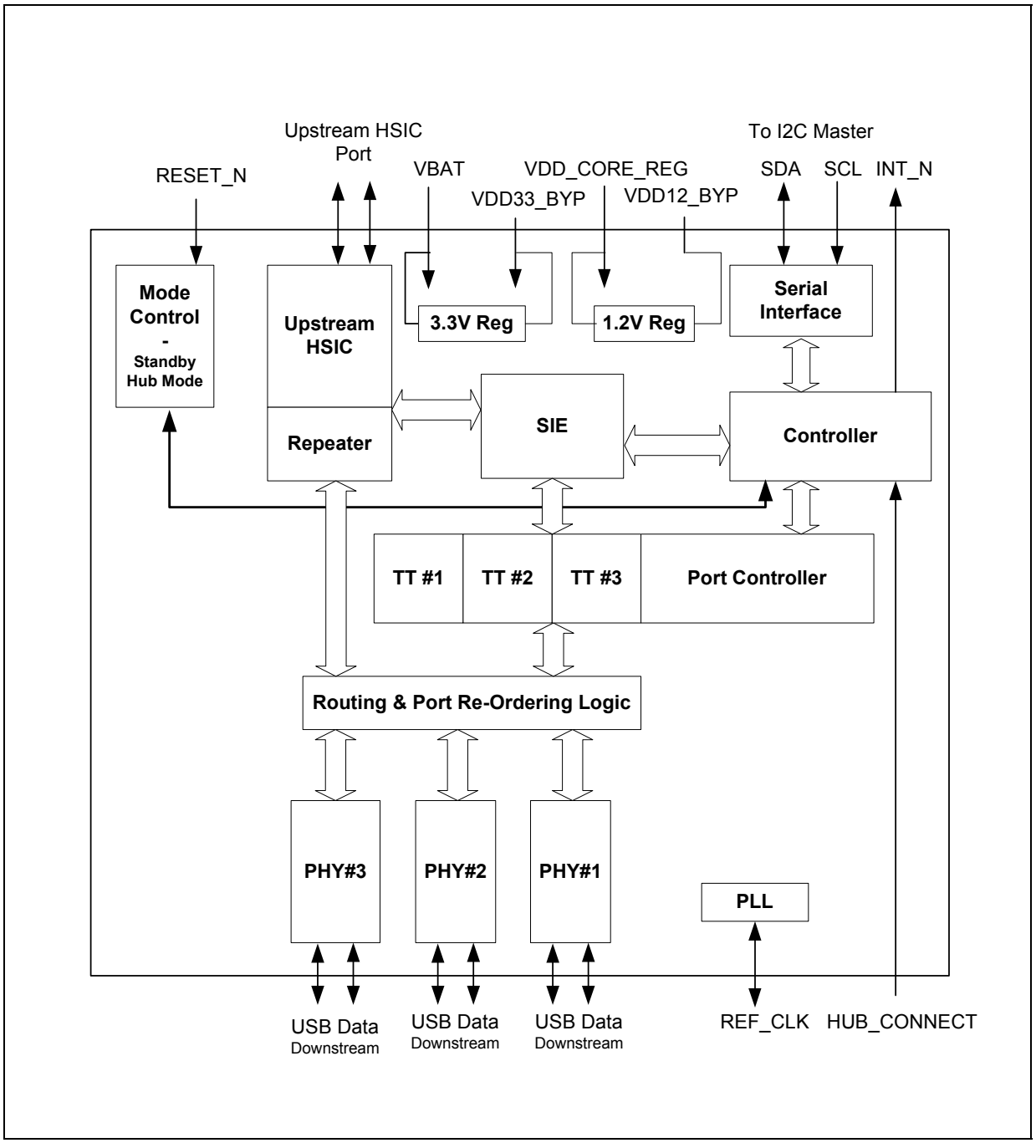


Figure 1.1 USB3503 Block Diagram

Chapter 2 Acronyms and Definitions

2.1 Acronyms

EP: Endpoint

FS: Full-Speed

HS: Hi-Speed

I²C®: Inter-Integrated Circuit[1]

LS: Low-Speed

HSIC: High-Speed Inter-Chip

2.2 Reference Documents

1. USB Engineering Change Notice dated December 29th, 2004, *UNICODE UTF-16LE For String Descriptors*.
2. *Universal Serial Bus Specification*, Revision 2.0, Dated April 27th, 2000.
3. *Battery Charging Specification*, Revision 1.1, Release Candidate 10, Dated Sept. 22, 2008
4. *High-Speed Inter-Chip USB Electrical Specification*, Version 1.0, Dated Sept. 23, 2007

1. I²C is a registered trademark of Philips Corporation.

Chapter 3 USB3503 Pin Definitions

3.1 Pin Configuration

The illustration below shows the package diagram.

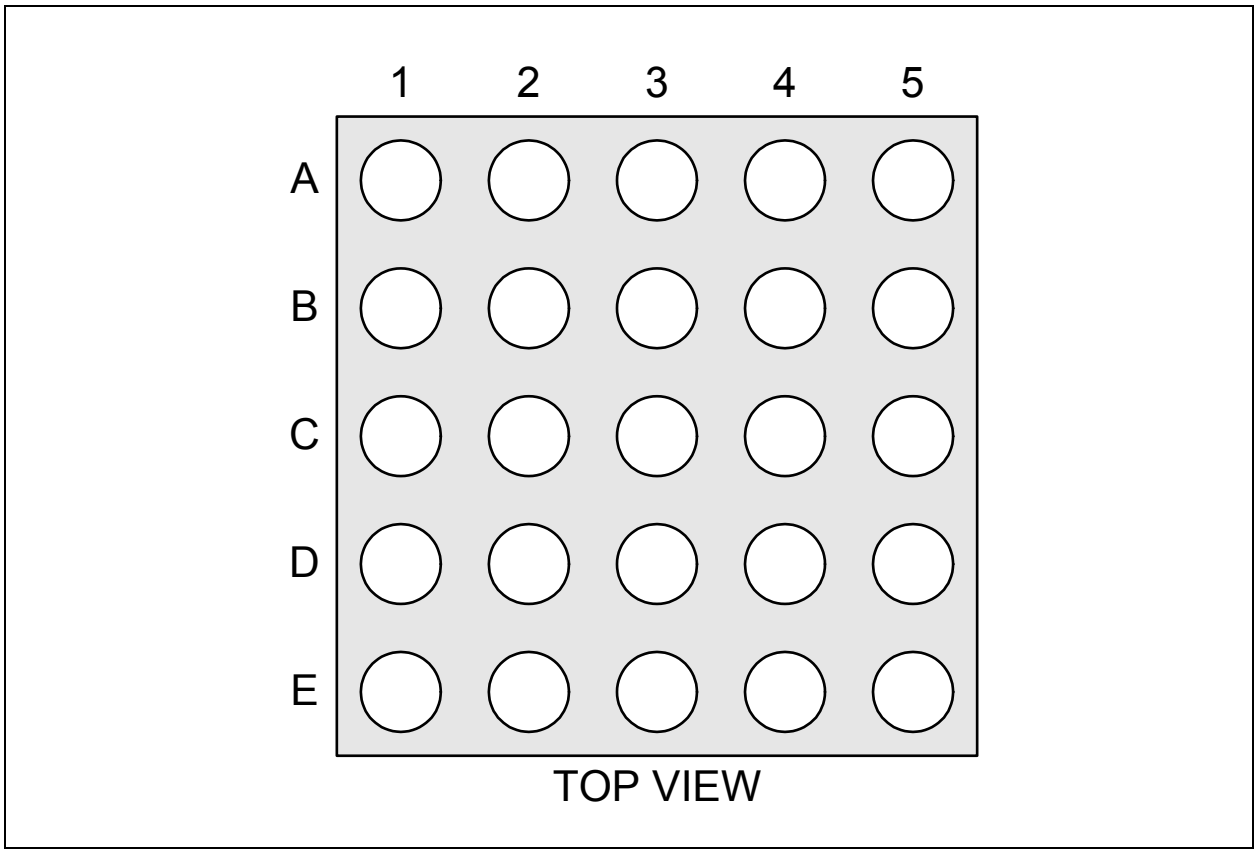


Figure 3.1 USB3503 25-Ball Package

3.2 Signal Definitions

WLCSP PIN	NAME	DESCRIPTION
E2	DATA	Upstream HSIC DATA pin of the USB Interface
E1	STROBE	Upstream HSIC STROBE pin of the USB Interface
A5	VDD33_BYP	3.3 V Regulator Bypass
C4	PRTPWR	Port Power Control Output
B4	OCS_N	Over Current Sense Input
A1	USBDN1_DP	USB downstream Port 1 D+ data pin

WLCSP PIN	NAME	DESCRIPTION
B1	USBDN1_DM	USB downstream Port 1 D- data pin
C2	USBDN2_DP	USB downstream Port 2 D+ data pin
D2	USBDN2_DM	USB downstream Port 2 D- data pin
C1	USBDN3_DP	USB downstream Port 3 D+ data pin
D1	USBDN3_DM	USB downstream Port 3 D- data pin
E5	SCL	I^2C clock input
D5	SDA	I^2C bi-directional data pin
E3	RESET_N	Active low reset signal
B5	HUB_CONNECT	Hub Connect
C5	INT_N	Active low interrupt signal
D4	REF_SEL1	Reference Clock Select 1 input
E4	REF_SEL0	Reference Clock Select 0 input
B3	REFCLK	Reference Clock input
A4	RBIAS	Bias Resistor pin
D3	VDD12_BYP	1.2 V Regulator
A2	VDD33_BYP	3.3 V Regulator
B2	VBAT	Voltage input from the battery supply
A3	VDD_CORE_REG	Power supply input to 1.2V regulator for digital logic core
C3	VSS	Ground

3.3 Pin Descriptions

This section provides a detailed description of each signal. The signals are arranged in functional groups according to their associated interface.

The terms assertion and negation are used. This is done to avoid confusion when working with a mixture of “active low” and “active high” signal. The term “assert”, or “assertion” indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term “negate”, or “negation” indicates that a signal is inactive.

3.3.1 Pin Definition

Table 3.1 Pin Descriptions

NAME	SYMBOL	TYPE	DESCRIPTION
UPSTREAM HIGH SPEED INTER-CHIP INTERFACE			
HSIC Clock/Strobe	STROBE	I/O	HSIC Upstream Hub Strobe pin
HSIC Data	DATA	I/O	HSIC Upstream Hub Data pin
High-Speed USB Data & Port Disable Strap Option	USBDN_DP[2:1] & USBDN_DM[2:1]	A-I/O	These pins connect to the downstream USB peripheral devices attached to the hub’s ports
			Downstream Port Disable Strap option: This pin will be sampled at RESET_N negation to determine if the port is disabled. Both USB data pins for the corresponding port must be tied to VDD33_BYP to disable the associated downstream port.
HS USB Data	USBDN_DP[3] & USBDN_DM[3]	A-I/O	These pins connect to the downstream USB peripheral devices attached to the hub’s ports.
			There is no downstream Port Disable Strap option on these ports.
SERIAL PORT INTERFACE			
Serial Data	SDA	I/OD	I^2C Serial Data
Serial Clock	SCL	I	Serial Clock (SCL)

Table 3.1 Pin Descriptions (continued)

NAME	SYMBOL	TYPE	DESCRIPTION
Interrupt	INT_N	OD	Interrupt The function of this pin is determined by the setting in the CFGP.INTSUSP configuration register. When CFGP.INTSUSP = 0 (General Interrupt) A transition from high to low identifies when one of the interrupt enabled status registers has been updated. SOC must update the Serial Port Interrupt Status Register to reset the interrupt pin high. When CFGP.INTSUSP = 1 (Suspend Interrupt) Indicates USB state of the hub. 'Asserted' low = Unconfigured or configured and in USB Suspend 'Negated' high = Hub is configured, and is active (i.e., not in suspend) If unused, this pin must be tied to **VDD33_BYP**.
Over Current Sense	OCS_N	I	Over Current Sense - Input from external current monitor indicating an over-current condition on port 3 or on ganged supply. Negated High = No over current fault detected Asserted Low = Over Current Fault Reported
Port Power	PRTPWR	OD	Port Power Control- Enables power to USB peripheral devices downstream on port 3 or on ganged supply. Asserted High = External Device should provide power for port(s). Negated Low = External Device should disable power to port(s).
MISC			
Reference Clock Input	REFCLK	I	Reference clock input.
Reference Clock Select	REF_SEL[1:0]	I	The reference select input must be set to correspond to the frequency applied to the REFCLK input. The customer should tie these pins to ground or VDD33_BYP. This input is latched during HUB.Init stage. Selects input reference clock frequency per Table 3.3.

Table 3.1 Pin Descriptions (continued)

NAME	SYMBOL	TYPE	DESCRIPTION
RESET Input	RESET_N	I	This active low signal is used by the system to reset the chip and hold the chip in low power STANDBY MODE.
USB Transceiver Bias	RBIAS	A-I/O	A 12.0kΩ (+/- 1%) resistor is attached from ground to this pin to set the transceiver's internal bias settings.
Hub Connect	HUB_CONNECT	I	Hub will transition to the Hub Communication Stage when this pin is asserted high. It can be used in three different ways: Tied to Ground - Hub will not transition to the Hub Communication Stage until connect_n bit of the SP_ILOCK register is negated. Tied to **VDD33_BYP** - Hub will automatically transition to the Hub Communication Stage regardless of the setting of the connect_n bit and without pausing for the SOC to reference status registers. Transition from low to high - Hub will transition to the Hub Communication Stage after this pin transitions from low to high. HUB_CONNECT should never be driven high when USB3503 is in Standby Mode.
POWER			
1.2V VDD Power	VDD12_BYP	Power	1.2 V Regulator. A 1.0 µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3503.
3.3V VDD Power	VDD33_BYP	Power	3.3V Regulator. A 4.7µF (<1 Ω ESR) capacitor to ground is required for regulator stability. The capacitor should be placed as close as possible to the USB3503.
Core Power Supply Input	VDD_CORE_REG	Power	Power supply to 1.2V regulator. This power pin should be connected to VDD33_BYP for single supply applications. Refer to Chapter 9 for power supply configuration options.
Battery Power Supply Input	VBAT	Power	Battery power supply. Refer to Chapter 9 for power supply configuration options.
VSS	VSS	Ground	Ground

3.3.2 I/O Type Descriptions

Table 3.2 USB3503 I/O Type Descriptions

I/O TYPE	DESCRIPTION
I	Digital Input.
OD	Digital Output. Open Drain.
I/O	Digital Input or Output.
A-I/O	Analog Input or Output.
Power	DC input or Output.
Ground	Ground.

3.3.3 Reference Clock

The REFCLK input is can be driven with a square wave from 0 V to VDD33_BYP. The USB3503 only uses the positive edge of the clock. The duty cycle is not critical.

The USB3503 is tolerant to jitter on the reference clock. The REFCLK jitter should be limited to a peak to peak jitter of less than 1 ns over a 10 µs time interval. If this level of jitter is exceeded the USB3503 high speed eye diagram may be degraded.

To select the REFCLK input frequency, the REF_SEL pins must be set according to Table 3.3 and Table 3.4. To select the primary REFCLK frequencies defined in Table 3.3, INT_N must be sampled high during the Hub.Init stage. If the INT_N pin is not used, the INT_N pin should be tied to VDD33_BYP. To select the secondary REFCLK frequencies defined in Table 3.4, INT_N must be sampled low during the Hub.Init stage. If the INT_N pin is not used, the INT_N pin should be tied to ground. Since the INT_N pin is open-drain during normal function, selecting the secondary REFCLK frequencies requires that the INT_N pin be driven low from an external source during Hub.Init and then, after startup, that external source must turn into an input to receive the INT_N signal.

Table 3.3 USB3503 Primary Reference Clock Frequencies

REF_SEL[1:0]	FREQUENCY (MHz)
‘00’	38.4
‘01’	26.0
‘10’	19.2
‘11’	12.0

Table 3.4 USB3503 Secondary Reference Clock Frequencies

REF_SEL[1:0]	FREQUENCY (MHz)
‘00’	24.0
‘01’	27.0
‘10’	25.0
‘11’	50.0

3.3.4 Interrupt

The general interrupt pin (INT_N) is intended to communicate a condition change within the hub. The conditions that may cause an interrupt are captured within a register mapped to the serial port (Register E8h: Serial Port Interrupt Status - INT_STATUS). The conditions that cause the interrupt to assert can be controlled through use of an interrupt mask register (Register E9h: Serial Port Interrupt Mask - INT_MASK).

The general interrupt and all interrupt conditions are functionally latched and event driven. Once the interrupt or any of the conditions have asserted, the status bit will remain asserted until the SOC negates the bit using the serial port. The bits will then remain negated until a new event condition occurs. The latching nature of the register causes the status to remain even if the condition that caused the interrupt ceases to be active. The event driven nature of the register causes the interrupt to only occur when a new event occurs- when a condition is removed and then is applied again.

The function of the interrupt and the associated status and masking registers are illustrated in Figure 3.2. Registers & Register bits shown in the figure are defined in Table 5.2, “Serial Interface Registers,” on page 26.

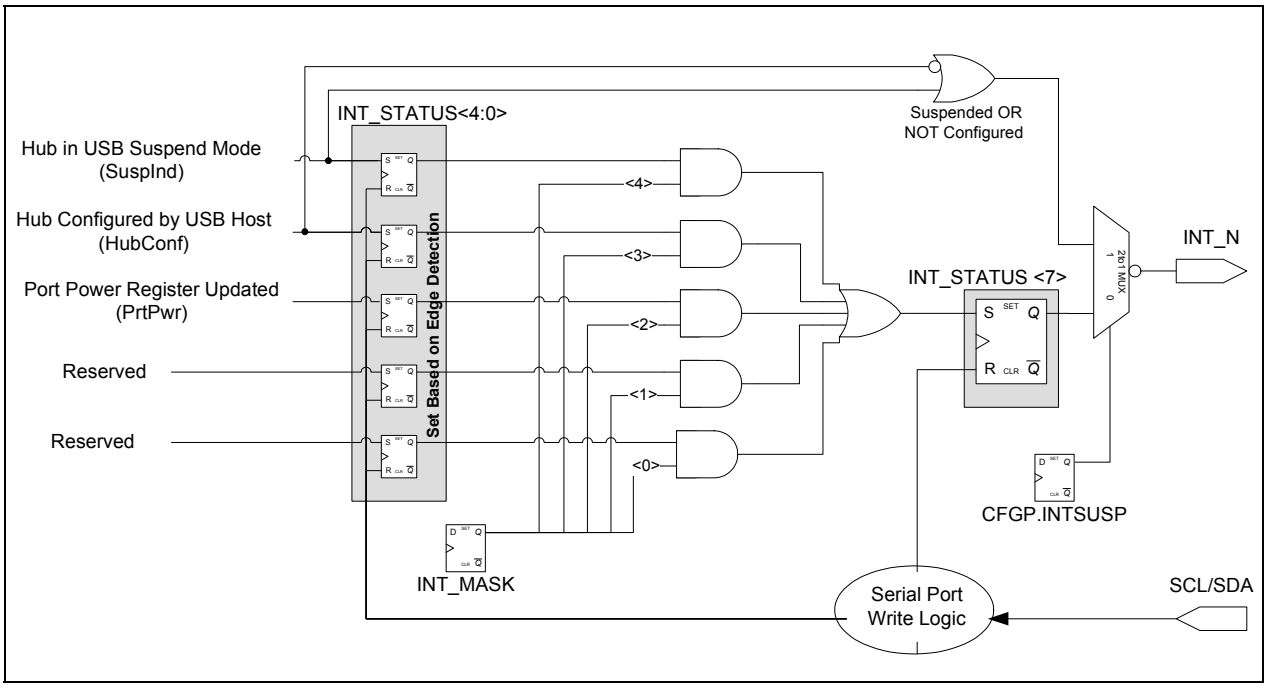


Figure 3.2 INT_N Operation

Figure 3.2 also shows an alternate configuration option (CFGP.INTSUSP) for a suspend interrupt. This option allows the user to change the behavior of the INT_N pin to become a direct level indication of configuration and suspend status.

When selected, the INT_N indicates that the entire hub has entered the USB suspend state.

NOTE: Because INT_N is driven low when active, care must be taken when selecting the external pullup resistor value for this open drain output. A sufficiently large resistor must be selected to insure suspend current requirements can be satisfied for the system.

Chapter 4 Modes of Operation

The USB3503 provides two modes of operation - Standby Mode and Hub Mode - which balance power consumption with functionality. The operating mode of the USB3503 is selected by setting values on primary inputs according to the table below.

Table 4.1 Controlling Modes of Operation

RESET_N INPUT	RESULTING MODE	SUMMARY
0	Standby	Lowest Power Mode – no function other than monitoring RESET_N input to move to higher states. All regulators are powered off.
1	Hub	Full Feature Mode - Operates as a configurable USB hub. Power consumption based on how many ports are active, at what speeds they are running and amount of data transferred.

4.1 Operational Mode Flowchart

The flowchart in Figure 4.1 shows the modes of operation. It also shows how the USB3503 traverses through the Hub mode stages (shown in bold.) The flow of control is dictated by control register bits shown in Italics as well as other events such as availability of reference clock. Refer to Section 5.3, "Serial Interface Register Definitions," on page 28 for the detailed definition of the control register bits. In this specification register bits are referenced using the syntax <Register>.<RegisterBit>. A summary of all registers can be found in Table 5.2, “Serial Interface Registers,” on page 26.

The remaining sections in this chapter provide more detail on each stage and mode of operation.

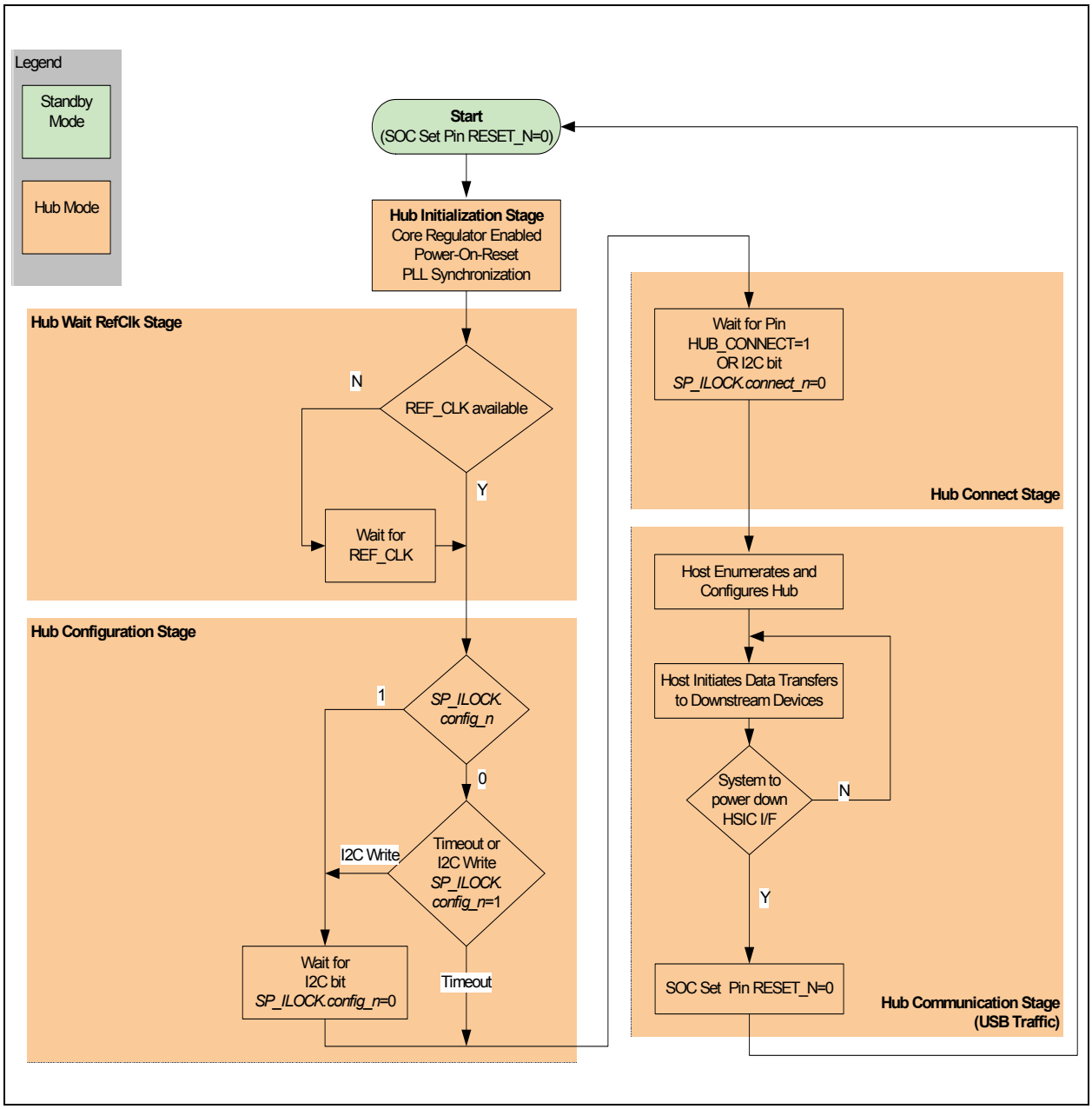


Figure 4.1 Modes of Operation Flowchart

4.2 Standby Mode

Standby Mode provides a very low power state for maximum power efficiency when no signaling is required. This is the lowest power state. In Standby Mode all internal regulators are powered off, the PLL is not running, and core logic is powered down in order to reduce power. Because core logic is powered off, no configuration settings are retained in this mode and must be re-initialized after RESET_N is negated high.

4.2.1 External Hardware RESET_N

A valid hardware reset is defined as an assertion of RESET_N low for a minimum of 100us after all power supplies are within operating range. While reset is asserted, the Hub (and its associated external circuitry) enters STANDBY MODE and consumes extremely low current as defined in Table 10.3 and Table 10.4.

Assertion of RESET_N (external pin) causes the following:

- All downstream ports are disabled.
- All transactions immediately terminate; no states are saved.
- All internal registers return to the default state.
- The PLL is halted.

After RESET_N is negated high in the Hub.Init stage, the Hub reads customer-specific data from the ROM.

4.3 Hub Mode

Hub Mode provides functions of configuration and high speed USB hub operation including connection and communication. Upon entering Hub Mode and initializing internal logic, the device passes through several sequential stages based on a fixed time interval.

4.3.1 Hub Initialization Stage (Hub.Init)

The first stage is the initialization stage and occurs when Hub mode is entered based on the conditions in Table 4.1. In this stage the 1.2V regulator is enabled and stabilizes, internal logic is reset, and the PLL locks if a valid REFCLK is supplied. Configuration registers are initialized to their default state and REF_SEL[1:0] input values are latched. The USB3503 will complete initialization and automatically enter the next stage after $T_{hubinit}$. Because the digital logic within the device is not yet stable, no communication with the device using the serial port is possible. Configuration registers are initialized to their default state.

4.3.2 Hub Wait RefClk Stage (Hub.WaitRef)

During this stage the serial port is not functional.

If the reference clock is provided before entering hub mode, the USB3503 will transition to the Hub Configuration stage without pausing in the Hub Wait RefClk stage. Otherwise, the USB3503 will transition to the Hub configuration stage once a valid reference clock is supplied and the PLL has locked.

4.3.3 Hub Configuration Stage (Hub.Config)

In this stage, the SOC has an opportunity to control the configuration of the USB3503 and modify any of the default configuration settings specified in the integrated ROM. These settings include USB

device descriptors, port electrical settings such as PHY BOOST, and control features. The SOC implements the changes using the serial slave port interface to write configuration & control registers.

See Section 5.3.29, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 37 for definition of SP_ILOCK register and how it controls progress through hub stages. If the SP_ILOCK.config_n bit has its default asserted low and the bit is not written by the serial port, then the USB3503 completes configuration without any I2C intervention.

If the SP_ILOCK.config_n bit has its default negated high or the SOC negates the bit high using the serial port during $T_{hubconfig}$, the USB3503 will remain in the Hub Configuration Stage indefinitely. This will allow the SOC to update other configuration and control registers without any remaining time-out restrictions. Once the SP_ILOCK.config_n bit is asserted low by the SOC the device will transition to the next stage.

4.3.4 Hub Connect Stage (Hub.Connect)

Next, the USB3503 enters the Hub Connect Stage. See Section 5.3.32, "Register EEh: Configure Portable Hub - CFGP," on page 39 and Section 5.3.29, "Register E7h: Serial Port Interlock Control - SP_ILOCK," on page 37 for definition of control registers which affect how the device transitions through the hub stages.

By using the appropriate controls, the USB3503 can be set to immediately transition, or instead to remain in the Hub Connect Stage indefinitely until one of the SOC handshake events occur. When set to wait on the handshake, the SOC may read or update any of the serial port registers. Once the SOC finishes accessing registers and is ready for USB communication to start, it can perform one of the selected handshakes which that cause the USB3503 to connect within $T_{hubconnect}$ and transition to the Hub Communication Stage.

4.3.5 Hub Communication Stage (Hub.Com)

Once it exits the Hub Connect Stage, the USB3503 enters Hub Communication Stage. In this stage full USB operation is supported under control of the USB Host on the upstream port. The USB3503 will remain in the Hub Communication Stage until the operating mode is changed by the system asserting RESET_N low.

While in the Hub Communication Stage, communication over the serial port is no longer supported and the resulting behavior of the serial port if accessed is undefined. In order to re-enable the serial port interface, the device must exit Hub Communication Stage. Exiting this stage is only possible by entering Standby mode.

4.3.6 Hub Mode Timing Diagram

The following timing diagram shows the progression through the stages of Hub Mode and the associated timing parameters.

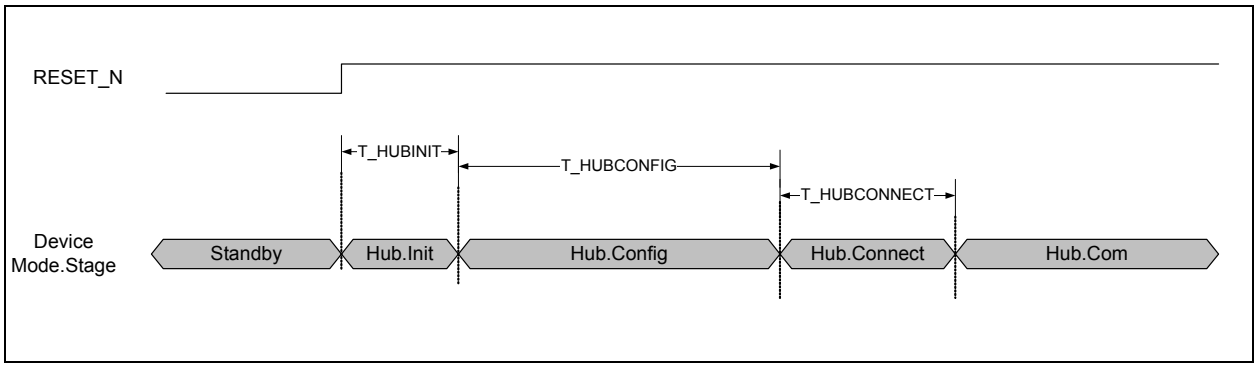


Figure 4.2 Timing Diagram for Hub Stages

The following table lists the timing parameters associated with the stages of the Hub Mode.

Table 4.2 Timing Parameters for Hub Stages

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Hub Initialization Time	$T_{HUBINIT}$		3	4	ms	
Hub Configuration Time-out	$T_{HUBCONFIG}$	94	95	96	ms	
Hub Connect Time	$T_{HUBCONNECT}$	0	1	10	us	

Chapter 5 Configuration Options

5.1 Hub Configuration Options

The SMSC Hub supports a number of features (some are mutually exclusive), and must be configured in order to correctly function when attached to a USB host controller. There are two principal ways to configure the hub: by writing to configuration registers using the serial slave port, or by internal default settings. Any configuration registers which are not written by the serial slave retain their default settings.

5.1.1 Multi/Single TT

SMSC's USB 2.0 Hub is fully specification compliant to the Universal Serial Bus Specification Revision 2.0 April 27,2000 (12/7/2000 and 5/28/2002 Errata). Please reference Chapter 11 (Hub Specification) for general details regarding Hub operation and functionality.

For performance reasons, the Hub provides 1 Transaction Translator (TT) per port (defined as Multi-TT configuration), and each TT has 1512 bytes of periodic buffer space and 272 Bytes of non- periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for each Transaction Translator.

When configured as a Single-TT Hub (required by USB 2.0 Specification), the Single Transaction Translator will have 1512 bytes of periodic buffer space and 272 bytes of non-periodic buffer space (divided into 4 non-periodic buffers per TT), for a total of 1784 bytes of buffer space for the entire Transaction Translator. **Each Transaction Translator's buffer is divided as shown in** Table 5.1, "Transaction Translator Buffer Chart".

Table 5.1 Transaction Translator Buffer Chart

Periodic Start-Split Descriptors	256 Bytes
Periodic Start-Split Data	752 Bytes
Periodic Complete-Split Descriptors	128 Bytes
Periodic Complete-Split Data	376 Bytes
Non-Periodic Descriptors	16 Bytes
Non-Periodic Data	256 Bytes
Total for each Transaction Translator	1784 Bytes

5.2 Default Serial Interface Register Memory Map

The Serial Interface Registers are used to customize the USB3503 for specific applications. Reserved registers or reserved bits within a defined register should not be written to non-default values or undefined behavior may result.