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MLX83100 Automotive 2-Phase DC Pre-Driver

Datasheet

1. Features and Benefits

- 2-phase DC gate driver
  - Level shifting between MCU PWM outputs and 2 external half-bridges
  - Compatible with 3.3V-5V microcontrollers
- Supported supply voltage range
  - Absolute maximum rating: 45V
  - Operating range: 4.5V-28V
  - 12V-28V Battery systems
  - Automotive qualified for 12V
  - Sleep mode with current <30µA
- Two charge pump configuration modes for
  - Low voltage operation
  - Reverse polarity N-FET protection
- High-side gate drivers with bootstrap circuits
  - Integrated 12V voltage regulator
  - Supports 6x 350nC N-FETs at 20kHz PWM
  - Supports 100% PWM operation
- Integrated current sense amplifier
  - Low offset and low offset drift
  - Fast settling time < 1µs
  - Programmable gain: 8x-48x
- Extensive diagnostics
  - Under/over voltage detection
  - Over temperature warning
  - Programmable V_{DS} monitoring
  - V_{GS} monitoring
- Serial, PWM diagnostics interface
  - Configurable diagnostics
  - Full diagnostic feedback
- Customer configurable EEPROM
  - Driver configuration
  - Diagnostics configuration
- Small package
  - 28-pin TSSOP-EP, AEC-Q100 grade 0 qualification (T_J=175˚C)

2. Application Examples

- Automotive 12V DC applications
  - Water pump / Oil pump / Fuel pump
  - Engine Cooling fan
  - HVAC blower / compressor
  - Wiper
  - Sunroof
  - EPS
- Industrial DC motor drivers up to 28V
  - Pumps
  - Fans
  - Blowers
  - Compressors

3. Ordering Information

Product	Temperature	Package	Option Code	Packing Form
MLX83100	L(-40°C to 150°C)	GO (TSSOP28-EP 4.4x9.8mm)	DBA-000	RE (Reel)

Ordering Example: *“MLX83100LGO-DBA-000-RE”.*

Melexis
INSPIRED ENGINEERING

4. Functional Diagram

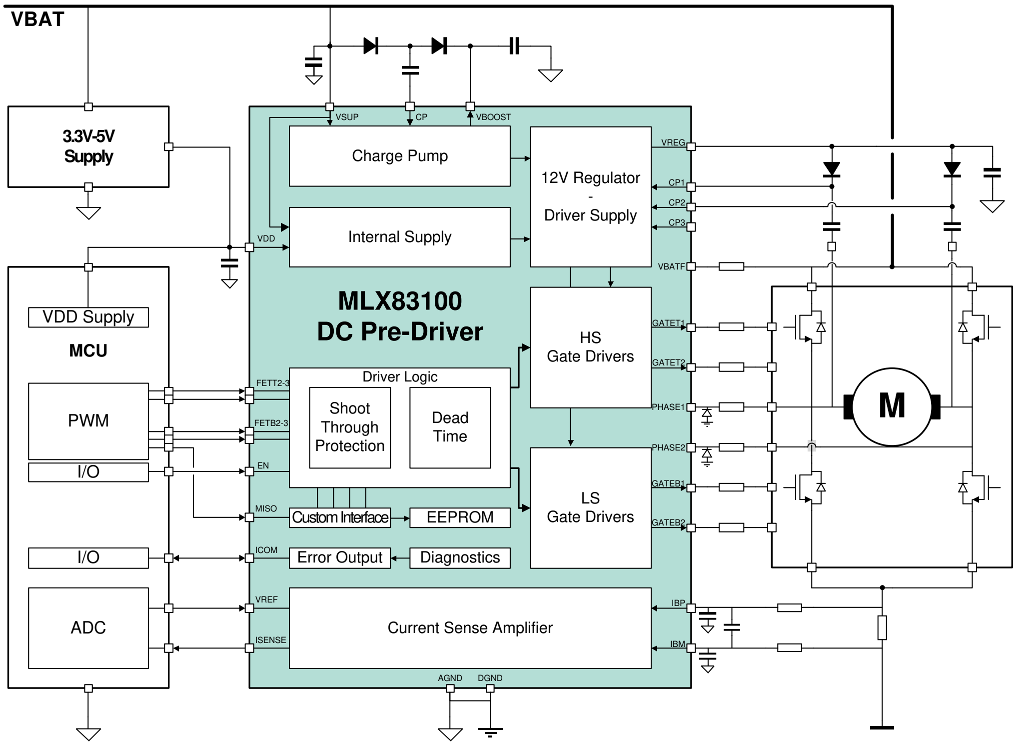

Figure 4-1 Typical application diagram

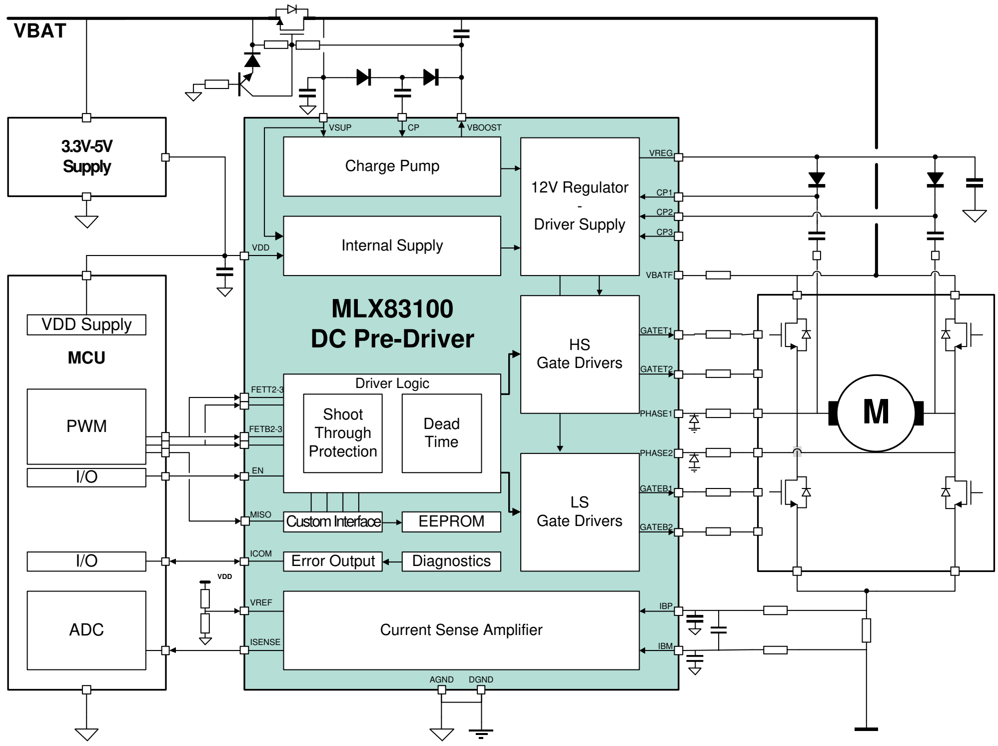

Figure 4-2 Alternative application diagram with reverse polarity N-FET

5. General Description

The MLX83100 is a two phase pre-driver (also called ‘bridge’ or ‘gate’ driver) IC with integrated current sense amplifier. This device is used to drive brushed DC motors in combination with a microcontroller and four discrete power N-FETs.

The device is able to control four external N-FETs for full H-bridge control in the supply range from 4.5V to 28V, by means of the integrated charge pump. The high side gate drivers are supplied via bootstrap circuits. The trickle charge pump allows 100% PWM operation despite the use of bootstrap capacitors. The bootstrap voltage regulator is optimized for gate charges up to 500nC per FET at 20 kHz PWM.

The device comprises various monitoring and protection functions, including under voltage and over voltage detection at multiple internal voltage nodes, over temperature detection, drain-source and gate-source voltage monitoring of the external N-FETs. In case of fault detection, the ICOM diagnostics interface will inform the microcontroller with a PWM signal, where the duty cycle indicates the nature of the error.

An integrated fast, high-bandwidth, low offset current sense amplifier allows for precise torque control, with programmable gain selection.

The MLX83100 provides an EEPROM for configurability, avoiding the need for a high pin-count package. The configuration allows the customer to optimize the pre-driver’s operation for different applications.

6. Contents

7. Pin Configuration & Definition

7.1. Pin Configuration

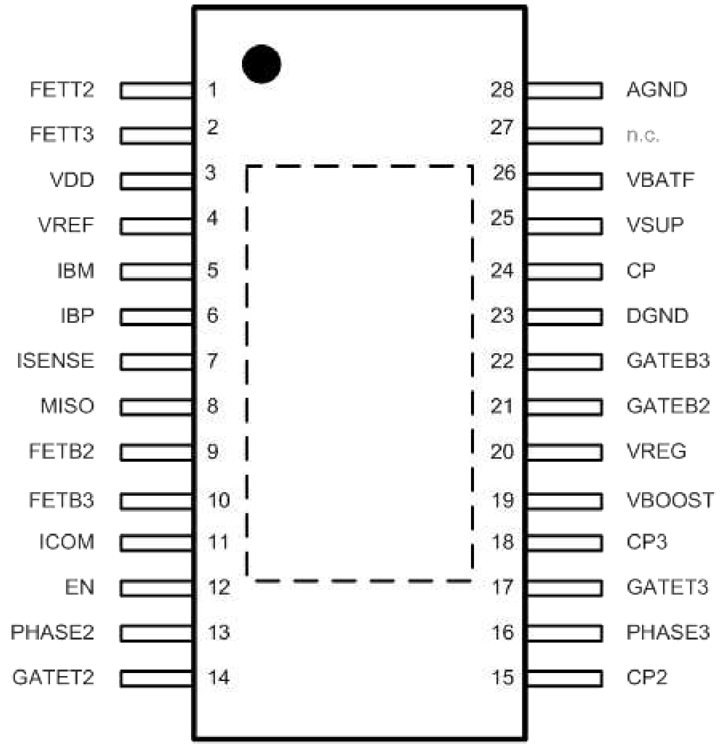

Figure 7-1 Pin configuration

7.2. Pin Definition

Pin #	Name	Description
1	FETT2	High-side FET2 PWM control input (active high)
2	FETT3	High-side FET3 PWM control input (active high)
3	VDD	Digital supply for IO's and current sense amplifier
4	VREF	Current sense amplifier reference input
5	IBM	Current sense amplifier negative input
6	IBP	Current sense amplifier positive input
7	ISENSE	Current sense amplifier output
8	MISO	MISO output for SPI
9	FETB2	Low-side FET2 PWM control input (active low) CLK input for SPI
10	FETB3	Low-side FET3 PWM control input (active low) MOSI input for SPI
11	ICOM	Bidirectional, serial diagnostics interface CSB input for SPI
12	EN	Enable input for gate driver outputs (active high)
13	PHASE2	Motor phase 2
14	GATET2	High-side FET2 gate driver output
15	CP2	High-side FET2 bootstrap capacitor
16	PHASE3	Motor phase 3
17	GATET3	High-side FET3 gate driver output
18	CP3	High-side FET3 bootstrap capacitor
19	VBOOST	Charge pump boosted supply output
20	VREG	Driver supply output for bootstrap capacitors
21	GATEB2	Low-side FET2 gate driver output
22	GATEB3	Low-side FET3 gate driver output
23	DGND	Driver ground
24	CP	Charge pump floating capacitor
25	VSUP	Power supply input (Battery input)
26	VBATF	Battery voltage connection for VDS-monitoring
27	n.c.	Not connected
28	AGND	Analog ground
29	PAD	Exposed pad

Table 7-1 Pin definition

8. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power supply voltage	V_{VSUP}, V_{BATF}	-0.3	-	45	V	t < 500ms (during load dump)
Power supply voltage	V_{VSUP}, V_{BATF}	-0.3	-	28	V	Permanent (functional)
Negative input current	I_{VSUP}	-15	-	-	mA	
Negative input current	I_{VBATF}	-10	-	-	mA	Defines with max. reverse polarity voltage the R_{VBATF}
Digital supply voltage	V_{VDD}	-0.3	-	5.5	V	
Analog input voltage	$V_{VREF,}$ V_{IBM},V_{IBF}	-0.3	-	V_{DD}+0.3	V	
Analog output voltage	V_{ISENSE}	-0.3	-	V_{DD}+0.3	V	
Digital input voltage	V_{FETBx}, V_{FETTx}, V_{EN}	-0.3	-	V_{DD}+0.3	V	
Digital input current		-10	-	10	mA	
Digital output voltage	V_{ICOM}	-0.3	-	V_{DD}+0.3	V	
Output voltage	$V_{GATEBx,}$ V_{REG}	-0.3	-	17	V	
Output voltage	V_{GATETx}	-0.3	-	V_{REG}+35	V	
Input voltage on CPx pins	V_{CPx}	-0.3	-	V_{REG}+35	V	
Input voltage on PHASEx pins	V_{PHASEx}	-0.7	-	45	V	
Maximum latch-up free current at any pin	I_{LATCH}	-100	-	100	mA	According to JEDEC JESD78, AEC-Q100-004
ESD capability	ESD	-2	-	+2	kV	Human Body Model
Storage temperature	T_{stg}	-55	-	150	˚C	
Junction temperature	T_J	-40	-	175	˚C	
Thermal resistance SOIC-16	R_{th-JA}	-	37	-	K/W	In free air on multilayer PCB (JEDEC 1s2p)
Thermal resistance SOIC-16	R_{th-JC}	-	10	-	K/W	Referring center of exposed pac

Table 8-1 Absolute maximum ratings

Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

9. Operating Range

Parameter	Symbol	Min	Typ	Max	Unit	Condition
Power supply voltage range	V_{VSUP}	4.5	-	28	V	Full functionality
Digital supply voltage range	V_{VDD}	3	-	5.5	V	CP discharged, power FETs off
Ambient temperature	T_A	-40	-	150	˚C	
Junction temperature	T_J	-40	-	175	˚C	

Table 9-1 Operating range

10. General Electrical Specifications

	Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
	Power Supply VSUP						
No.1	Supply voltage range	V_{SUP}	Functional	7	-	18	V
No.2	Supply voltage extended range low	V_{SUP_ERL}	Functional w. decreased gate drive voltage	4.5	-	7	V
No.3	Supply voltage extended range high	V_{SUP_ERH}		18	-	28	V
No.4	Quiescent current from V_{SUP}	I_{SUP_SLEEP}	V_{DD} = Low	-	-	30	µA
No.5	Operating current from V_{SUP}	I_{SUP_INT}	Pre-driver operation 25kHz PWM, no load	-	-	5	mA
No.6	Supply over voltage high	V_{SUP_OVH}	Warning on ICOM	-	-	35	V
No.7	Supply over voltage low	V_{SUP_OVL}	ICOM released	30	-	-	V
No.8	Supply over voltage hysteresis	V_{SUP_OVHY}		0.4	-	1	V
No.9	Supply over voltage debounce time	$V_{SUP\_OV\_DEB}$		-	-	2	µs
No.10	Supply under voltage high	V_{SUP_UVH}	ICOM released	-	-	6	V
No.11	Supply under voltage low	V_{SUP_UVL}	Warning on ICOM	5	-	-	V
No.12	Supply under voltage hysteresis	V_{SUP_UVHY}		0.2	-	0.5	V
No.13	Supply under voltage debounce time	$V_{SUP\_UV\_DEB}$		-	-	10	µs
No.14	Power on reset level	V_{POR}	Reset released on rising edge V_{SUP} when V_{DD}=high	2.6	-	4.5	V
	VVBATF						
No.15	Leakage from V_{BATF} to GND	R_{VBATF_LEAK}	Pre-driver not in sleep	-	-	30	µA
	Temperature Warning						
No.16	Over temperature high	OVT_H	Warning on ICOM	-	185	-	℃
No.17	Over temperature low	OVT_L	ICOM released	-	168	-	℃
	On-Chip Oscillator						
No.18	Oscillator frequency	f_{OSC}	Internal Oscillator	6.8	8	9.2	MHz

	Charge Pump CP, VBOOST						
No.19	Output slew rate	V_{CP}		-	100	-	V/µs
No.20	Charge pump frequency	f_{CP}		170	200	230	kHz
No.21	Reverse polarity N-FET gate-source voltage (V_{BOOST}-V_{SUP})	V_{GS_RPFET}	▪ CP Mode 1 ▪ V_{SUP} > 7V ▪ I_{REG} < 20mA	5	12	13	V
No.22	Resistive load from V_{BOOST} to GND	R_{BOOST_LEAK}	▪ R_{Typ} at room temperature ▪ R_{Min} at 150°C T_J ▪ (excl. R_{VREG_LEAK})	6	8	-	MOhm
No.23	V_{BOOST} under voltage high	V_{BOOST_UVH}	COM released ▪ CP Mode 0 (V_{BOOST}) ▪ CP Mode 1 (V_{BOOST}-V_{SUP})	6.1	-	7.2	V
No.24	V_{BOOST} under voltage low	V_{BOOST_UVL}	Warning on ICOM ▪ CP Mode 0 (V_{BOOST}) ▪ CP Mode 1 (V_{BOOST}-V_{SUP})	5.6	-	6.7	V
No.25	V_{BOOST} discharge stop	$V_{BOOST\_DISSTOP}$	▪ CP Mode 1 (V_{BOOST}-V_{SUP}) ▪ Discharge activated by V_{SUP_OV} and topped by $V_{BOOST\_DIS\_STOP}$	V_{SUP}-0.2	-	V_{SUP}+0.8	V
No.26	V_{BOOST} discharge current	I_{BOOST_DIS}	▪ CP Mode 1 (V_{BOOST}-V_{SUP}) ▪ From V_{BOOST} to DGND	25	-	90	mA

	Driver Supply VREG						
No.27	Load current on V_{REG}	$I_{REG\_CPMODE0}$	▪ V_{REG} > 11V ▪ CP Mode 0, EN_CP = 1	-	-	40	mA
		$I_{REG\_CPMODE1}$	▪ V_{REG} > 11V ▪ CP Mode 1, EN_CP = 1	-	-	20	mA
No.28	Output voltage V_{REG}	V_{REG}	▪ CP Mode 0, EN_CP = 1 ▪ V_{SUP} > 8V ▪ I_{REG} < 40mA	11	12	13	V
			▪ CP Mode 0, EN_CP = 1 ▪ 7V< V_{SUP} < 8V ▪ I_{REG} < 40mA	10	-	13	V
			▪ CP Mode 1, EN_CP = 1 ▪ V_{SUP} > 8V ▪ I_{REG} < 20mA	11	12	13	V
No.29	Internal resistive load from V_{REG} to GND	R_{VREG_LEAK}	▪ R_{Typ} at room temperature ▪ R_{Min} at 150°C T_J	0.3	0.4	-	MOhm
No.30	V_{REG} over voltage high	V_{REG_OVH}	▪ Warning on ICOM	14.2	-	16.5	V
No.31	V_{REG} over voltage low	V_{REG_OVL}	▪ ICOM released	13.5	-	15.8	V
No.32	V_{REG} over voltage hysteresis	V_{REG_OVHY}		0.65	-	1.5	V
No.33	V_{REG} under voltage high	V_{REG_UVH}	▪ ICOM released	7.2	-	8.1	V
No.34	V_{REG} under voltage low	V_{REG_UVL}	▪ Warning on ICOM	6.9	-	7.8	V
No.35	V_{REG} under voltage hysteresis	V_{REG_UVHY}		0.3	-	0.7	V
	Digital Supply VDD						
No.36	V_{DD} operating current	I_{DD}	▪ Incl. ICOM current sourcing	4	-	7	mA
No.37	V_{DD} pull down resistance	V_{DD_RPD}		200	300	370	kOhm
No.38	V_{DD} input voltage	V_{DD}	▪ V_{DD} = 3.3V or 5V	3	-	5.5	V
No.39	V_{DD} under voltage high	V_{DD_UVH}	▪ ICOM released	2.55	-	2.95	V
No.40	V_{DD} under voltage low	V_{DD_UVL}	▪ Warning on ICOM	2.45	-	2.85	V
No.41	V_{DD} under voltage hysteresis	V_{DD_UVHY}		0.08	0.10	0.14	V
No.42	V_{DD} sleep voltage high	V_{DD_SLEEPH}	▪ Out of sleep	2.1	-	2.7	V
No.43	V_{DD} sleep voltage low	V_{DD_SLEEPL}	▪ Go to sleep	1.6	-	2.1	V
No.44	V_{DD} sleep voltage hysteresis	$V_{DD\_SLEEPHY}$		0.45	0.58	0.80	V

	Gate Drivers						
No.45	Rise time	t_r	C_{LOAD} = 1nF, 20% to 80%	6	7	15	ns
No.46	Fall time	t_f	C_{LOAD} = 1nF, 80% to 20%	4	7	15	ns
No.47	Pull-up ON resistance low-side pre-driver	R_{ON_UP}	V_{SUP} > 7V -10mA, T_J = -40°C -10mA, T_J = 175°C	10	-	30	Ohm
	Pull-up ON resistance high-side pre-driver			15	-	30	Ohm
No.48	Pull-down ON resistance low-side pre-driver	R_{ON_DN}	V_{SUP} > 7V 10mA, T_J = -40°C 10mA, T_J = 175°C	10	-	30	Ohm
	Pull-down ON resistance high-side pre-driver			15	-	30	Ohm
No.49	Turn-on gate drive peak current (sourcing)	I_{GON}	V_{GS} = 0V, V_{SUP} > 7V		-	-1.4 (-0.45)	A
No.50	Turn-off gate drive peak current (sinking)	I_{GOFF}	V_{GS} = 12V, V_{SUP} > 7V		-	1.6 (0.45)	A
No.51	Propagation delay	t_{PDDRV}	From logic input threshold to 2V V_{GS} drive output at no load	20	-	120[1]	ns
No.52	Propagation delay matching	t_{PDDRVM}	Transitions at the different phases at no load condition	-20	-	20	ns
No.53	Programmable dead time : asynchronous internal delay between high-side and low-side pre-driver of one half bridge	t_{DEAD}	DEAD_TIME [2:0] = 000 001 010 011 100 101 110 111	-25%	0.00 0.51 0.80 1.10 1.67 2.30 3.40 6.90	+25%	µs
No.54	Dead time matching between different channels	t_{DEAD_TOL}		-15	-	15	%

[1] *For bare it is specified to 200ns max due measurement accuracy at wafer level*

No.55	Programmable drain-source voltage for monitoring of external N-FETs	V_{VDS_MON}	VDSMON[2:0] = 000 001 010 011 100 101 110 111	 0.40 0.60 0.85 1.05 1.25 1.50 1.70	Disabled 0.50 0.75 1.00 1.25 1.50 1.75 2.00	 0.60 0.90 1.15 1.45 1.75 2.00 2.30	V
No.56	Programmable drain-source monitor blanking time: Delay between gate high and enabling corresponding V_{DS} monitor	t_{VDS_BL}	VDS_BLANK_TIME[1:0] = 00 01 10 11	0.60 1.28 2.55 5.10	0.80 1.70 3.40 6.80	1.00 2.13 4.25 8.50	µs
No.57	Sleep gate discharge resistor	Rsgd	Internal resistance between FET gate-source pins to switch-off FET. V_{DD} = 0V (sleep mode) V_{GS} = 0.5V	-	-	1	kOhm
No.58	Trickle charge pump current capability	I_{TCP}	V_{SUP} > 12V PHASEx = V_{SUP} CPx = PHASEx + 6.5V $I_{TCP,max}$ @150C T_J $I_{TCP,min}$ @-40C T_J	-160	-	-25	µA
No.59	V_{GS} under voltage threshold high	V_{GS_UVH}	ICOM released	42	-	70	%V_{REG}
No.60	V_{GS} under voltage threshold low	V_{GS_UVL}	Warning on ICOM	36	-	63	%V_{REG}
No.61	PWM frequency	f_{DR_PWM}		-	20	100	kHz
No.62	Leakage from CPx - PHASEx	R_{CP_LEAK}	R_{Typ} at room temperature R_{Min} at 150°C T_J	0.5	1	-	MOhm
No.63	V_{CPx} discharge current	I_{BOOST_DIS}	Activated by V_{SUP_OVH} event From V_{CPx} to V_{PHASEx}	8	-	40	mA
	Logic IO's - FET inputs, MISO						
No.64	Digital input high voltage	$V_{IN\_DIG\_H}$	Min. voltage logical high	80	-	-	%V_{DD}
No.65	Digital input low voltage	$V_{IN\_DIG\_L}$	Max. voltage logical low	-	-	20	%V_{DD}
No.66	Input pull-up resistance	$R_{IN\_DIG\_PU}$	FETBx	90	-	410	kOhm
No.67	Input pull-down resistance	$R_{IN\_DIG\_PD}$	FETTx	90	-	410	kOhm

	Logic IO's - EN input						
No.68	Input pull-down resistance	$R_{\_EN\_PD}$	▪ EN	90	-	410	kOhm
No.69	Bridge disable propagation delay	EN_{PR_DEL}	▪ From bridge disable $EN<0.2V_{DD}$ to $V_{GS} < 0.5V$, $C_{LOAD} = 1nF$	-	-	1	µs
	Logic IO's - ICOM						
No.70	Pull-up current	$ICOM_{PU}$	▪ $V_{ICOM} = 0V$	-2.2	-	-5.0	mA
No.71	Pull-down current	$ICOM_{PD}$	▪ $V_{ICOM} = V_{DD}$	5.0	-	2.6	mA
No.72	ICOM PWM frequency fast	f_{ICOMF}		85	100	115	kHz
No.73	ICOM PWM frequency slow	f_{ICOMS}		10.6	12.5	14.4	kHz
No.74	SPI start-up pulse duration on ICOM to enter SPI mode	t_{SPI_SU}	▪ EN = Low ▪ FETTx = Low, FETBx = High	2048/ f_{OSC}	-	4096/ f_{OSC}	s
	SPI Timing						
No.75	SPI initial setup time	t_{SPI_ISU}		2	-	-	µs
No.76	SPI clock frequency	f_{SPI}		-	-	500	kHz
No.77	Rise/fall times	t_{SPI_RF}	▪ CLK, CSB, MISO, MOSI	-	-	200	ns
No.78	CSB setup time	t_{CSB_SU}		1	-	-	µs
No.79	CSB high time	t_{CSB_H}		2	-	-	µs
No.80	Clock high time	t_{CLK_H}		1	-	-	µs
No.81	Clock low time	t_{CLK_L}		1	-	-	µs
No.82	Data in setup time	t_{DI_SU}		1	-	-	µs
No.83	Data in hold time	t_{DI_H}		500	-		ns
No.84	Data out ready delay	t_{DO_R}	▪ C_{LOAD} at FETB1 < 50pF	-	500	-	ns
No.85	EEPROM read delay	t_{EE_RD}	▪ EE_RD = 1	6	-		µs
No.86	EEPROM write delay	t_{EE_WR}	▪ EE_WR = 1	12	-	-	ms
No.87	Temperature for EEPROM read	$T_{J\_EE\_RD}$	▪ Junction temperature	-40	-	150	°C
No.88	Temperature for EEPROM write	$T_{J\_EE\_WR}$	▪ Junction temperature	-40	-	150	°C

	Current Sense Amplifier						
No.89	Input offset voltage	V_{IS_IO}	Input differential voltage within ±100mV Common mode [-0.5, 1.0] V	-7.6	-	7.6	mV
No.90	Input offset voltage thermal drift	$V_{IS\_IO\_TDRIFT}$		-10	-	10	µV/°C
No.91	Input common mode rejection ratio DC	IS_{CMRR_DC}		60	-	-	dB
No.92	Input common mode rejection ratio 1MHz	IS_{CMRR_AC}		40	-	-	dB
No.93	Input power supply rejection ratio DC for V_{DD} supply	IS_{PSRR_DC}		60	-	-	dB
No.94	Input power supply rejection ratio 1MHz for V_{DD} supply	IS_{PSRR_AC}		40	-	-	dB
No.95	Closed loop gain	IS_{GAIN}	Current sense gain = 000 001 010 011 100 101 110 111	-3%	8.0 10.3 13.3 17.2 22.2 28.7 37.0 47.8	+3%	
No.96	Output settling time	IS_{SET}	Amplified output to 99% of final value after input change	-	-	1.0	µs
No.97	Output voltage range high	V_{ISENSE_MAX}	ISENSE output max level	V_{DD}-0.02	-	V_{DD}	V
No.98	Output voltage range low	V_{ISENSE_MIN}	ISENSE output min level	GND	-	GND+0.02	V
No.99	Output short circuit current to ground	I_{ISENSE_SC}	Output current saturation level	-	1.4	-	mA
No.10	Gain bandwidth (GBW)	IS_{GBW}		6	-	-	MHz
No.10	Output slew rate	IS_{SR}		–	8	-	V/µs
No.10	CM spike recovery	IS_{CM_REC}	CM spike = ±1.5V, t=250ns	-	-	730	ns
No.10	VREF voltage input	V_{REF}		0	-	50	%V_{DD}

Table 10-1 General Electrical Specifications

10.1. MLX83100 Typical Performance Graphs

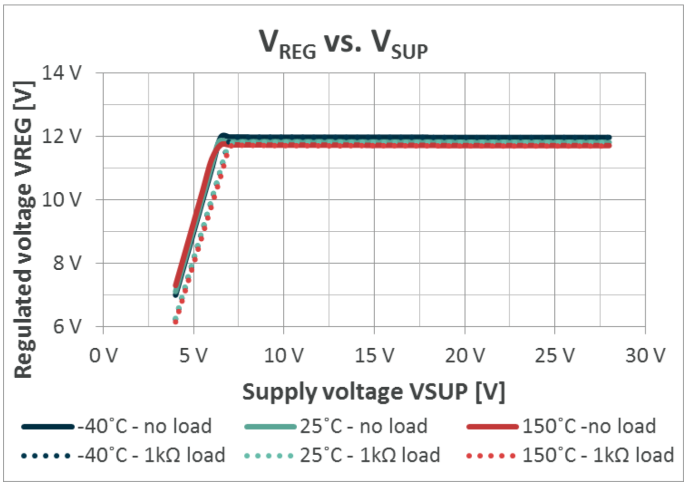

Figure 10-1 MLX83100 Regulated output voltage vs. supply voltage

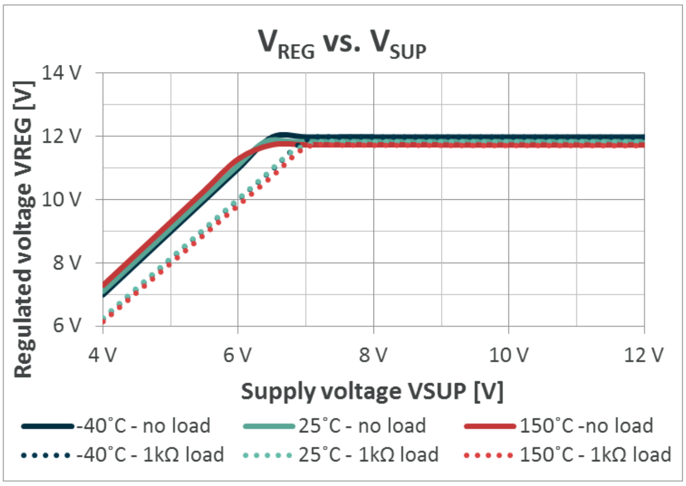

Figure 10-2 MLX83100 Regulated output voltage vs. supply voltage

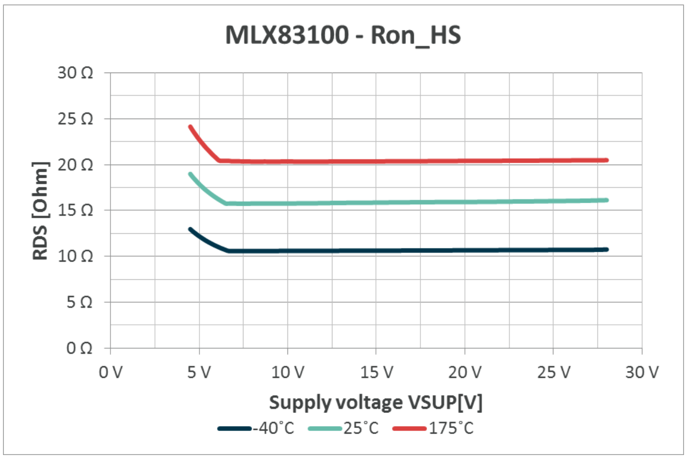

Figure 10-3 MLX83100 High-side driver FET R_{ON} resistance vs. supply voltage

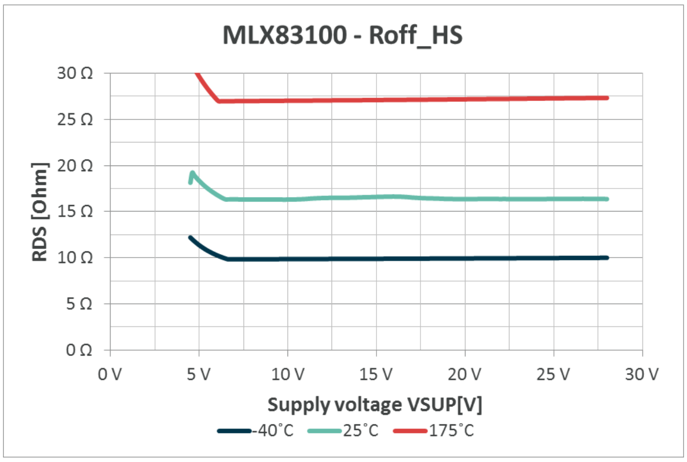

Figure 10-4 MLX83100 High-side driver FET R_{OFF} resistance vs. supply voltage

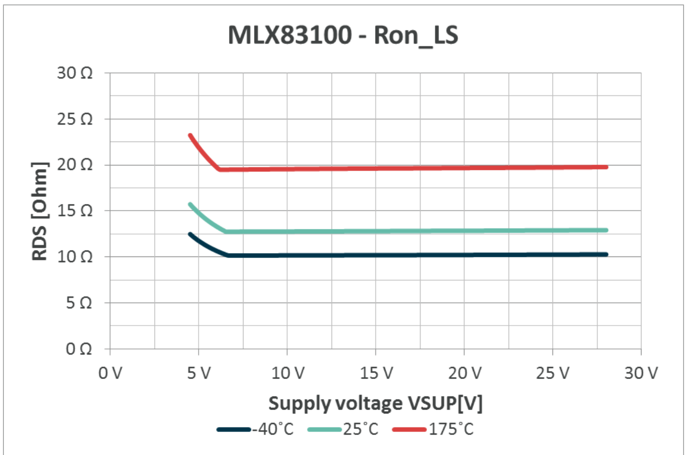

Figure 10-5 MLX83100 Low-side driver FET R_{ON} resistance vs. supply voltage

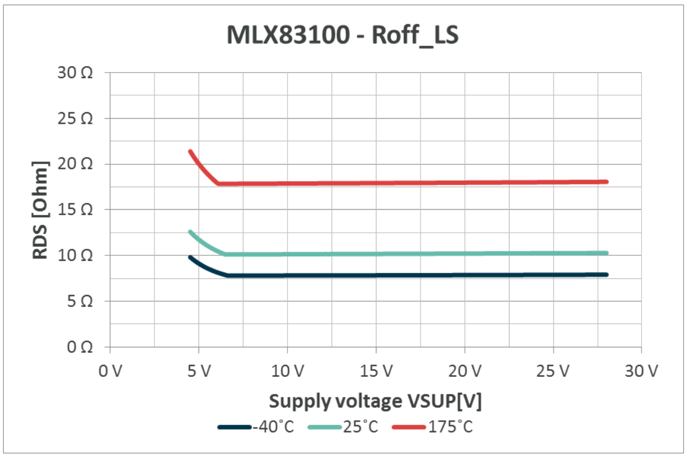

Figure 10-6 MLX83100 Low-side driver FET R_{OFF} resistance vs. supply voltage

11. Block Diagram

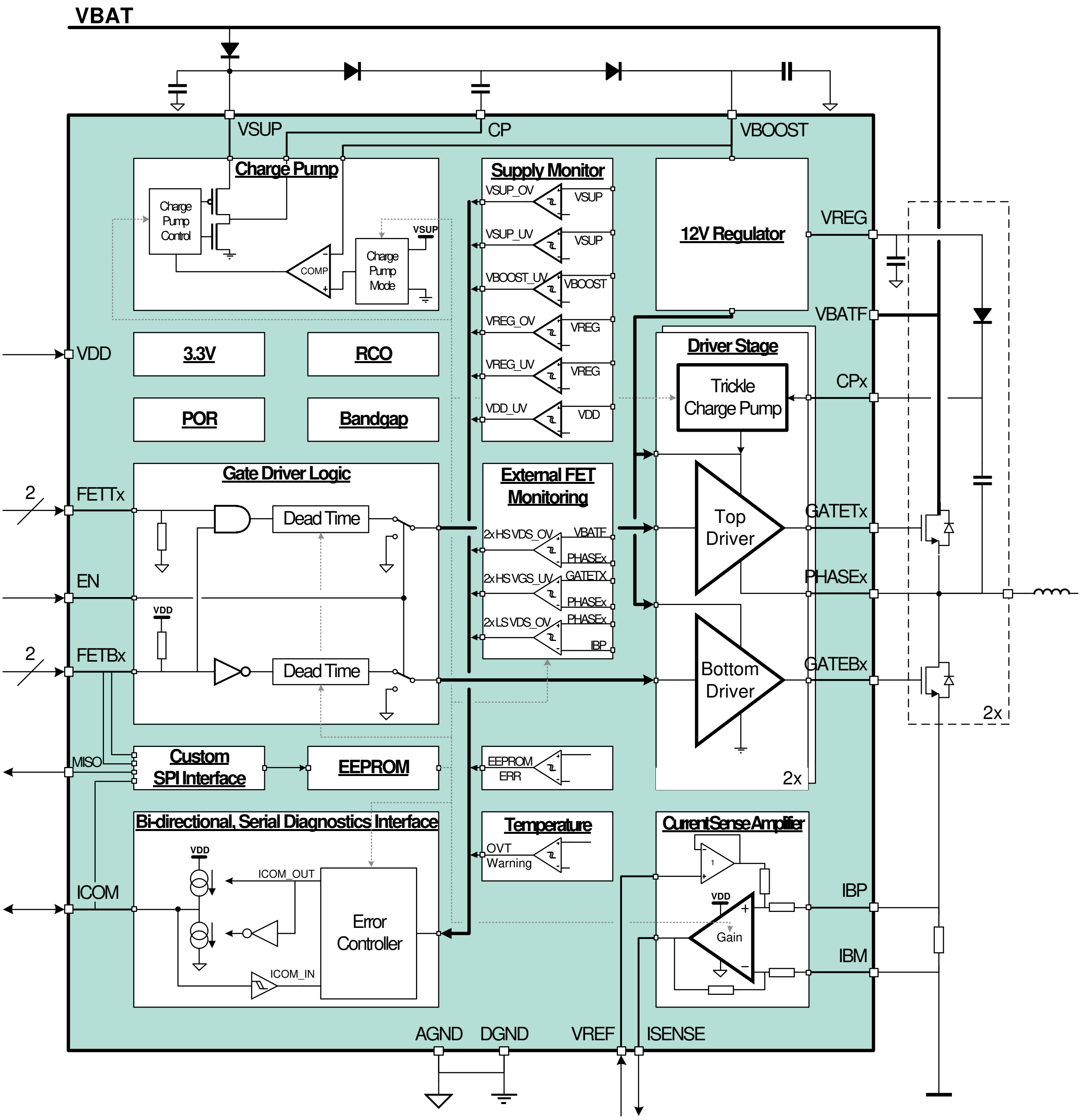

Figure 11-1 Block diagram

12. Functional Description

12.1. Supply System

The MLX83100 is supplied via pins VSUP and VDD. The power supply VSUP supplies the internal operation of the pre-driver, the charge pump and the voltage regulator used for the bootstrap based architecture. The digital supply VDD supplies the IO's and the current sense amplifier.

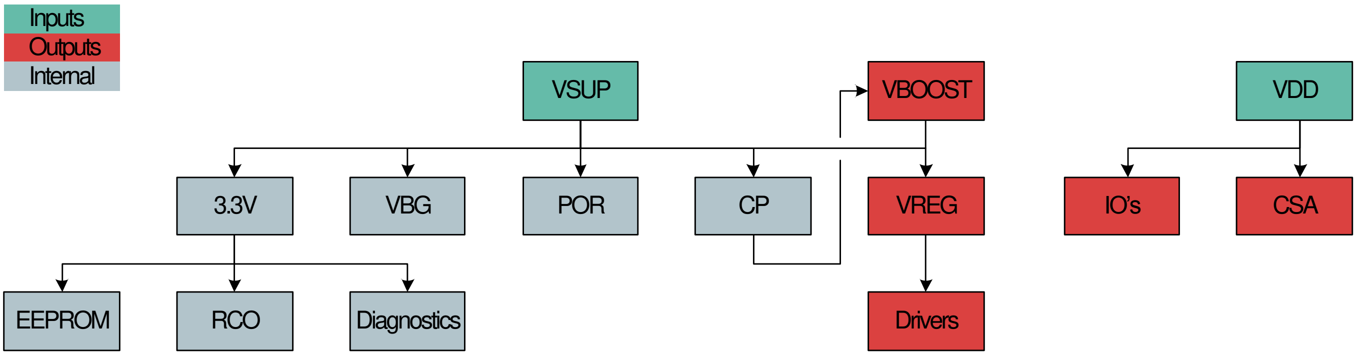

Figure 12-1 Principle organization of the supply system

12.1.1. Power Supply - VSUP

The internal operation of the pre-driver is supplied from the power supply input pin VSUP. It supplies the bandgap reference, power-on-reset system and internal 3.3V regulator. This 3.3V regulator in turn supplies the EEPROM, RC-oscillator and diagnostics. For safety reasons the pre-driver provides integrated under voltage and over voltage detection on VSUP.

12.1.2. Charge Pump - VBOOST

The IC comprises a charge pump, supplied from VSUP, which allows full device operation down to 4.5V. The charge pump boosted output voltage is available on VBOOST. This boosted voltage powers the voltage regulator VREG used to supply the low-side drivers directly, and high-side drivers via the bootstrap architecture. See Figure 4-1 for the standard charge pump configuration where VBOOST is regulated relative to ground. The charge pump will not be switching when $V_{SUP} > V_{REG} + 2xV_{f,\ diode}$.

An alternative mode of operation for the charge pump supports the use of an external low drop N-FET for reverse polarity protection. In this mode the charge pump boosts the output voltage relative to the supply voltage instead of relative to ground, see application diagram in Figure 4-2. The disadvantage is an additional amount of dissipation inside the driver to regulate VREG.

The charge pump architecture is a supply voltage doubler with feedback loop for stable output voltage generation, as shown in Figure 12-2. It can be configured in EEPROM to either regulate the boosted output voltage VBOOST relative to ground or relative to the supply voltage, see Figure 12-3 for the typical output voltage. Furthermore the EEPROM configuration allows disabling the charge pump for applications not requiring the low voltage operation, in order to reduce the overall power consumption.

For safety reasons the pre-driver provides integrated under voltage detection on VBOOST. In addition the charge pump comprises a discharge switch in order to keep VBOOST output voltage in a safe operating area in case of over voltage on the supply input pin. The discharge switch is activated as soon as the supply voltage VSUP exceeds the V_{SUP_OVH} threshold level and is deactivated when it drops below the V_{SUP_OVL} threshold. At the same time the charge pump is deactivated.

EN_CP	CPMODE	Charge pump configuration
0	x	Charge pump disabled
1	0	Charge pump configured to regulate VBOOST relative to ground, to support low voltage operation
1	1	Charge pump configured to regulate VBOOST relative to the supply, to support the use of a reverse polarity N-FET

Table 12-1 Charge pump configuration options

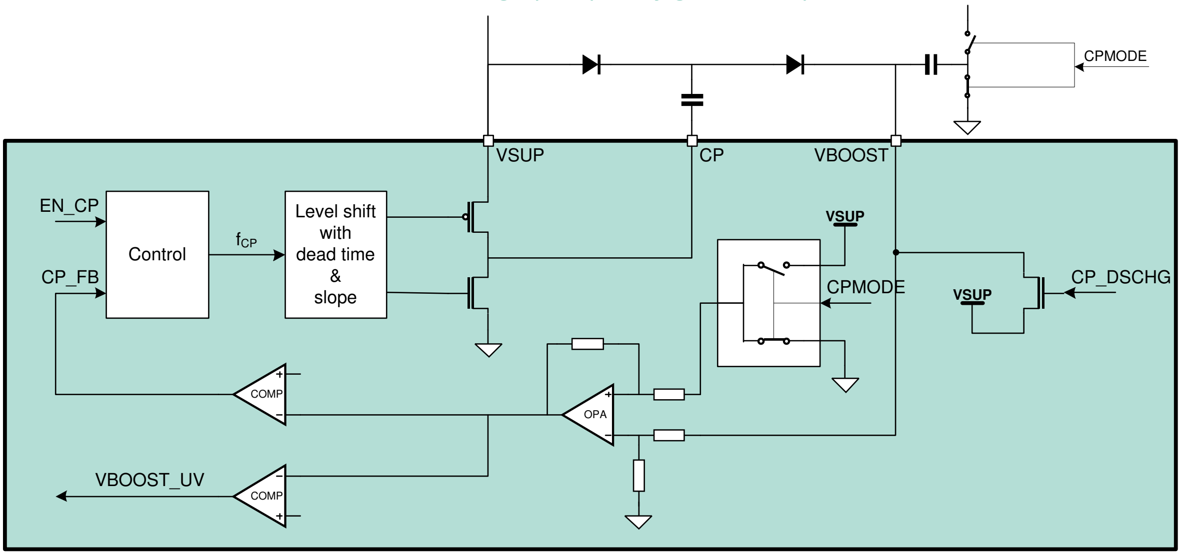

Figure 12-2 Charge pump principle schematic

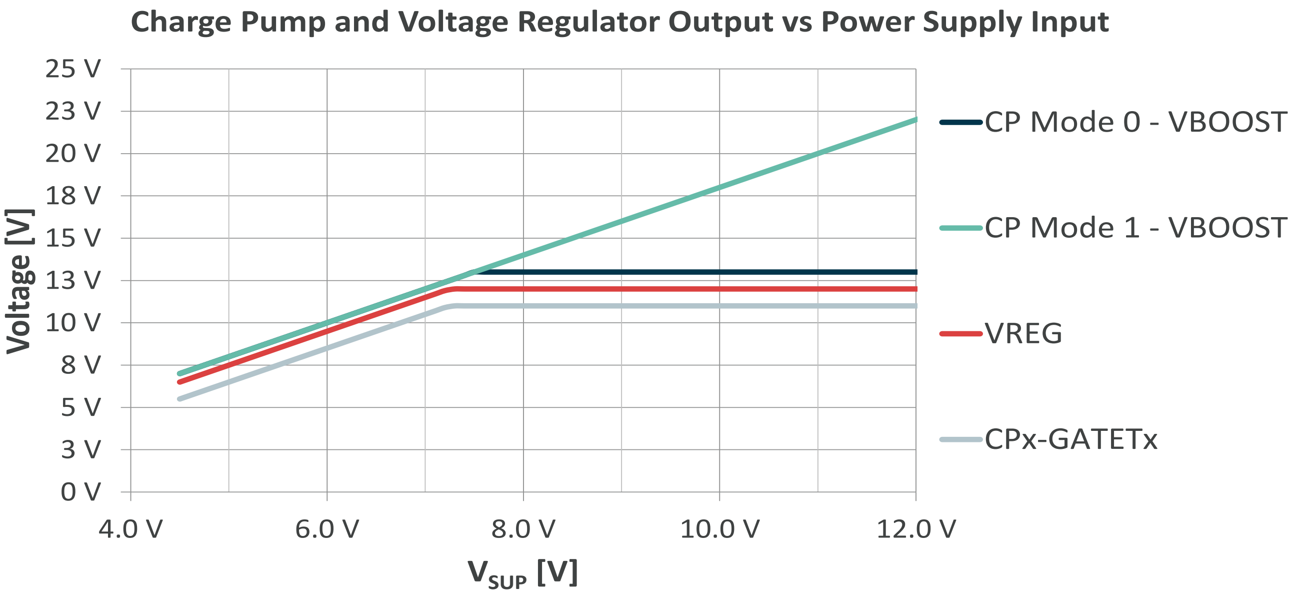

Figure 12-3 Charge pump output and driver supply

12.1.3. Voltage Regulator - VREG

The voltage regulator regulates the power supply down to 12V, in order to supply the low-side gate drivers and switch the external low-side N-FETs without gate-source over voltage at high battery voltages. The regulated output voltage VREG further provides the bootstrap voltage for driving the high-side N-FETs.

For safety reasons the pre-driver provides integrated under voltage and over voltage detection on VREG.

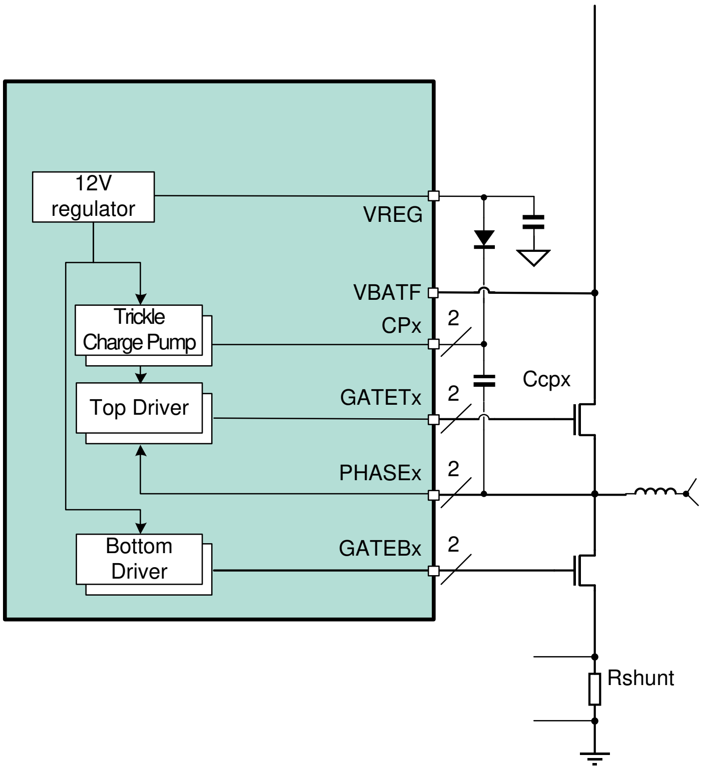

Figure 12-4 Voltage regulator for driver supply – VREG

12.1.4. Digital Supply - VDD

The MLX83100 comprises a current sense amplifier. The current sense amplifier and IO's are supplied from the digital supply VDD.

For safety reasons the pre-driver provides integrated under voltage detection on VDD.

Note:
When supplying VDD with a limited output impedance (e.g. from a microcontroller IO) the performance of the amplifier may be affected.

12.1.5. Sleep Mode

Sleep mode is activated when the digital supply input VDD is pulled below "VVDD sleep voltage threshold low". In sleep mode the charge pump is disabled and the current consumption on VSUP is reduced. All gate drivers are switched off via sleep gate discharge resistors R_{SGD}. The pre-driver will wake-up as soon as the voltage level on VDD rises above "VVDD sleep voltage threshold high".

Pin Name	State in sleep mode
CP	The charge pump is disabled.
VBOOST	Since the charge pump is disabled VBOOST is pulled to the supply voltage via the external charge pump diodes.
GATEBx	In sleep mode, gate-discharge resistors (R_{SGD}) between GATEBx and DGND are activated, ensuring all low-side gate drivers are switched off
GATETx	In sleep mode, gate-discharge resistors (R_{SGD}) between GATETx and PHASEx are activated, ensuring all high-side gate drivers are switched off
PHASEx	Phases are kept low with GATETx through the internal body diode of the pre-driver
VREG	Voltage regulator is disabled
CPx	Any charge that remains after VREG is disabled will leak to ground
ISENSE	Current sense amplifier is supplied from VDD, and thus not active
FETBx, FETTx EN, ICOM, MISO	All IO's are supplied from VDD, and thus not active

Table 12-2 Drivers in Sleep Mode

Notes:

1. In case any of the digital input pins are externally pulled high while VDD is low, current will flow into VDD via internal ESD protection diodes. This condition is not allowed.
2. When VDD is pulled low, also ICOM will go low. This should not be interpreted as a diagnostic interrupt.

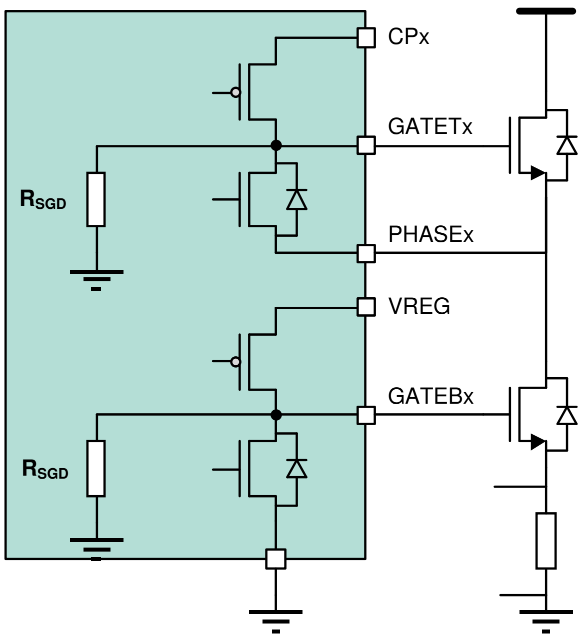

Figure 13-1-5 Drivers in Sleep Mode

12.2. Gate Drivers

12.2.1. PWM Input Control Logic – FETBx & FETTx

Each of the 4 external N-FETs can be controlled independently via the 4 digital PWM input pins: FETBx and FETTx. However, the digital logic provides the option to control the 2 external half bridges with only 2 control signals, by shorting high-side and low-side PWM input pins for each half bridge.

The IC provides internal shoot through protection since the digital logic prevents simultaneous activation of both high-side and low-side driver of one half bridge. A configurable dead time ensures the high-side (low-side) N-FET is fully switched off, before switching on the complementary low-side (high-side) N-FET.

For safety reasons the pre-driver provides integrated drain-source and gate-source monitoring for each of the 4 external N-FETs.

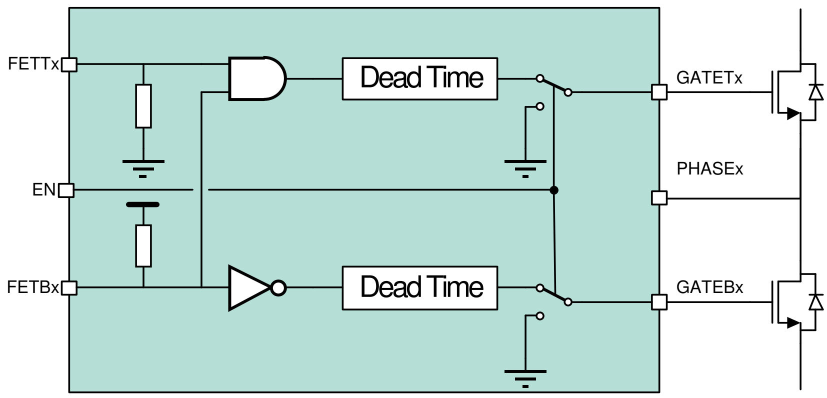

Figure 12-5 Input control logic of the driver stage

12.2.2. Enable Input EN

The enable input pin EN enables the gate driver outputs when set high. When reset, all gate driver outputs are switched to the low state, switching off all external N-FETs. This is performed by pulling all gate drivers to ground via the pull-down on-resistances. The enable pin can be used by the microcontroller to disable all drivers in case of any fault detection.

While EN is low, the programming of the EEPROM via SPI can be initiated by pulling ICOM low for the SPI start-up time specified by t_{SPI_SU}.

12.2.3. Gate Driver Supply and Bootstrap Architecture – VREG & CPx

The voltage regulator regulates the power supply voltage down to 12V. The regulated voltage is used to directly supply the low-side drivers. To provide sufficient supply voltage for the high-side drivers a bootstrap architecture is used. When the low-side N-FET is switched on, the phase voltage will be pulled low and the bootstrap capacitor is charged from the VREG buffer capacitor through the bootstrap diode. Afterwards, if the low-side N-FET is switched off and the high-side N-FET is switched on, the charge of the bootstrap capacitor is used to supply sufficient gate drive voltage to the high-side N-FET. The integrated trickle charge pump assures the bootstrap capacitor will not be discharged, and allows 100% PWM operation.

12.3. Integrated Current Sense Amplifier

The IC comprises an integrated fast, high-bandwidth, low offset current sense amplifier.

The current sense amplifier is supplied from the digital supply. It senses the voltage over the low-side shunt, amplifies it with the gain programmed in EEPROM and adds the offset provided on VREF. The output of the amplifier is available on ISENSE.

$$ISENSE = Current \times Shunt \times Gain_{EEPROM} + V_{VREF}$$

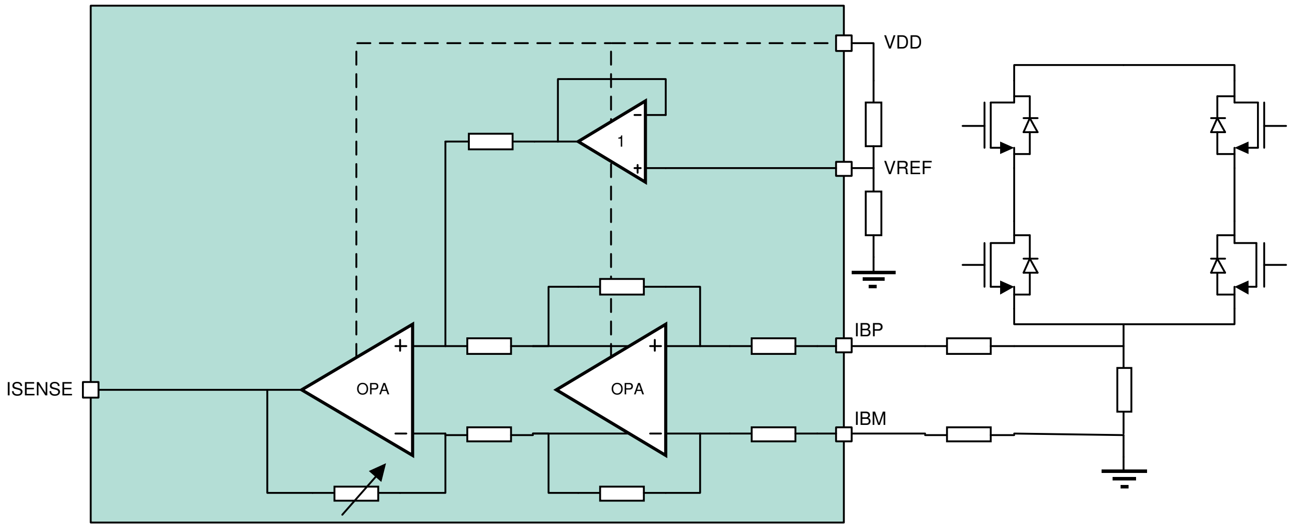

Figure 12-6 Current Sense Amplifier

12.4. Protection and Diagnostic Functions

12.4.1. Power Supply Over Voltage Shutdown (VSUP_OV)

The pre-driver has an integrated VSUP over voltage shut down to prevent destruction of the IC at high supply voltages.

12.4.2. Power Supply Under Voltage Warning (VSUP_UV)

The pre-driver has an integrated VSUP under voltage detection. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable operation.

12.4.3. Digital Supply Under Voltage Warning (VDD_UV)

The pre-driver has an integrated VDD under voltage detection. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable communication between microcontroller and pre-driver.

12.4.4. VBOOST Under Voltage Warning (VBOOST_UV)

The integrated charge pump boosts the supply voltage in low voltage operation on the VBOOST output. There is an under voltage detection on VBOOST to warn the microcontroller the charge pump is not ready. It is the responsibility of the microcontroller to take action in order to ensure reliable motor operation.

12.4.5. Gate Driver Supply Over Voltage Warning/Shutdown (VREG_OV)

The MLX83100 comprises an integrated VREG over voltage detection. The reaction of the pre-driver on this VREG_OV event depends on the status of the Bridge Feedback bit in EEPROM. If this VREG_OV_BF_EN bit is set the pre-driver will disable all gate drivers, switching off all external N-FETs. If the bit is reset it will just give a warning to the microcontroller.

VREG_OV_BF_EN	Pre-driver reaction VREG_OV event
0	VREG_OV is reported on ICOM, but the drivers remain active
1	VREG_OV is reported on ICOM and the drivers are disabled

Table 12-3 EEPROM Configuration for VREG over voltage detection

12.4.6. Gate Driver Supply Under Voltage Warning (VREG_UV)

The pre-driver detects when the regulated voltage drops below the under voltage threshold. The diagnostics interface will give a warning to the microcontroller. It is the responsibility of the microcontroller to take action in order to ensure reliable switching of the external N-FETs, since the VREG voltage directly supplies the low-side gate drivers.

12.4.7. Gate Source Voltage Monitoring Warning (VGS_UV)

In order to ensure reliable switching of the high-side N-FETs, the MLX83100 comprises gate-source monitors for each of the high-side N-FETs. In case of an under voltage, the diagnostics interface will give a warning to the microcontroller, if the gate-source comparators are enabled in EEPROM. It is the responsibility of the microcontroller to take action in order to ensure reliable switching of the high-side gate drivers.

12.4.8. Over Temperature Warning (OVT)

If the junction temperature exceeds the specified threshold, a warning will be communicated to the microcontroller. The pre-driver will continue in normal operation. It is the responsibility of the microcontroller to protect the IC against over temperature destruction.

12.4.9. Shoot Through Protection and Dead Time

The pre-drivers' internal implementation guarantees that low-side and high-side N-FET of the same external half bridge cannot be conducting at the same time, preventing a short between the supply and ground. In addition the pre-driver provides a programmable dead time in EEPROM. The dead time sets the delay between the moment when the high-side (low-side) N-FET is switched off, and the moment when the complementary low-side (high-side) N-FET can be switched on.

12.4.10. Drain-Source Voltage Monitoring Warning/Shutdown (VDS_ERR)

The MLX83100 provides a drain-source voltage monitoring feature for each external N-FET to protect against short circuits to ground or supply. For the high-sides the drain-source voltage are sensed via the VBATF –and PHASEx-pins. For the low-sides the PHASEx –and IBP-pins are used. The drain-source voltage comparator can be enabled or disabled in EEPROM.

The drain-source voltage monitor for a certain external N-FET is activated when the corresponding input is switched on and the dead time has passed. An additional blanking time can be programmed in EEPROM. If the drain-source voltage remains higher than the VDS monitor threshold voltage, the VDS error is raised. The threshold voltage is configurable in EEPROM.

The reaction of the pre-driver on a VDS error can be configured in EEPROM with the Bridge Feedback bit. If this bit is set the pre-driver automatically disables the drivers when a VDS error is detected. If the bit is reset, the drivers remain active. In both cases the VDS error will be reported to the microcontroller.

VDS_COMP_EN	VDS_BF_EN	Pre-driver reaction on VDS-error event
0	x	Any VDS error is ignored and no error is reported on ICOM
1	0	VDS_ERR is reported on ICOM, but the drivers remain active
1	1	VDS_ERR is reported on ICOM and the drivers are disabled

Table 12-4 EEPROM Configuration for drain-source error detection