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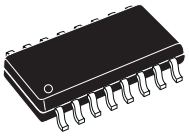
L6566B

Multi-mode controller for SMPS

Features

- Selectable multi-mode operation: fixed frequency or quasi-resonant
- On-board 700 V high-voltage start-up
- Advanced light load management
- Low quiescent current (< 3 mA)
- Adaptive UVLO
- Line feedforward for constant power capability vs mains voltage
- Pulse-by-pulse OCP, shutdown on overload (latched or autorestart)
- Transformer saturation detection
- Programmable frequency modulation for EMI reduction
- Latched or autorestart OVP
- Brownout protection
- -600/+800 mA totem pole gate driver with active pull-down during UVLO
- SO16N package

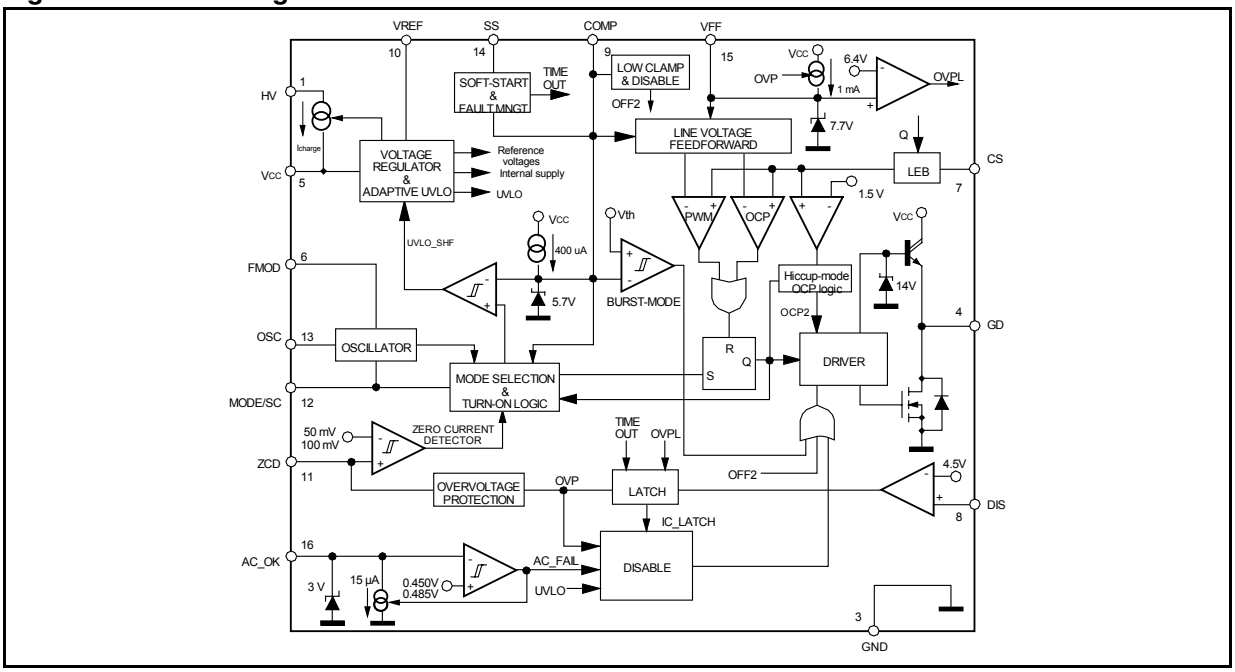


SO16N

Applications

- Hi-end AC-DC adapter/charger
- LCD TV/monitor, PDP
- digital consumer, IT equipment
- single-stage PFC

Figure 1. Block diagram



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1 Description

The L6566B is an extremely versatile current-mode primary controller ICs, specifically designed for high-performance offline flyback converters. It is also suited for single-stage single-switch input-current-shaping converters (single-stage PFC) for applications supposed to comply with EN61000-3-2 or JEITA-MITI regulations.

Both fixed-frequency (FF) and quasi-resonant (QR) operation are supported. The user can pick either of the two depending on application needs. The device features an externally programmable oscillator: it defines converter's switching frequency in FF mode and the maximum allowed switching frequency in QR mode.

When FF operation is selected, the ICs work like a standard current-mode controller with a maximum duty cycle limited at 70 % min. The oscillator frequency can be modulated to mitigate EMI emissions.

QR operation, when selected, occurs at heavy load and is achieved through a transformer demagnetization sensing input that triggers MOSFET's turn-on. Under some conditions, ZVS (zero-voltage switching) can be achieved. Converter's power capability rise with the mains voltage is compensated by line voltage feedforward. At medium and light load, as the QR operating frequency equals the oscillator frequency, a function (valley skipping) is activated to prevent further frequency rise and keep the operation as close to ZVS as possible.

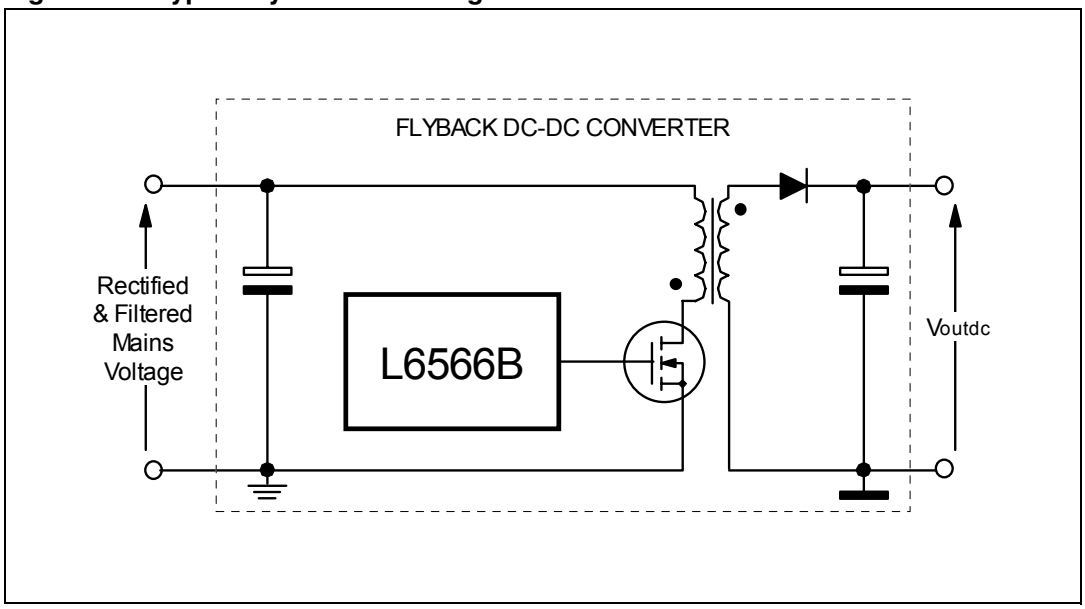
With either FF or QR operation, at very light load the ICs enter a controlled burst-mode operation that, along with the built-in non-dissipative high-voltage start-up circuit and the low quiescent current, helps keep low the consumption from the mains and meet energy saving recommendations.

An innovative adaptive UVLO helps minimize the issues related to the fluctuations of the self-supply voltage due to transformer's parasites.

The protection functions included in this device are: not-latched input undervoltage (brownout), output OVP (auto-restart or latch-mode selectable), a first-level OCP with delayed shutdown to protect the system during overload or short circuit conditions (auto-restart or latch-mode selectable) and a second-level OCP that is invoked when the transformer saturates or the secondary diode fails short. A latched disable input allows easy implementation of OTP with an external NTC, while an internal thermal shutdown prevents IC overheating.

Programmable soft-start, leading-edge blanking on the current sense input for greater noise immunity, slope compensation (in FF mode only), and a shutdown function for externally controlled burst-mode operation or remote ON/OFF control complete the equipment of this device.

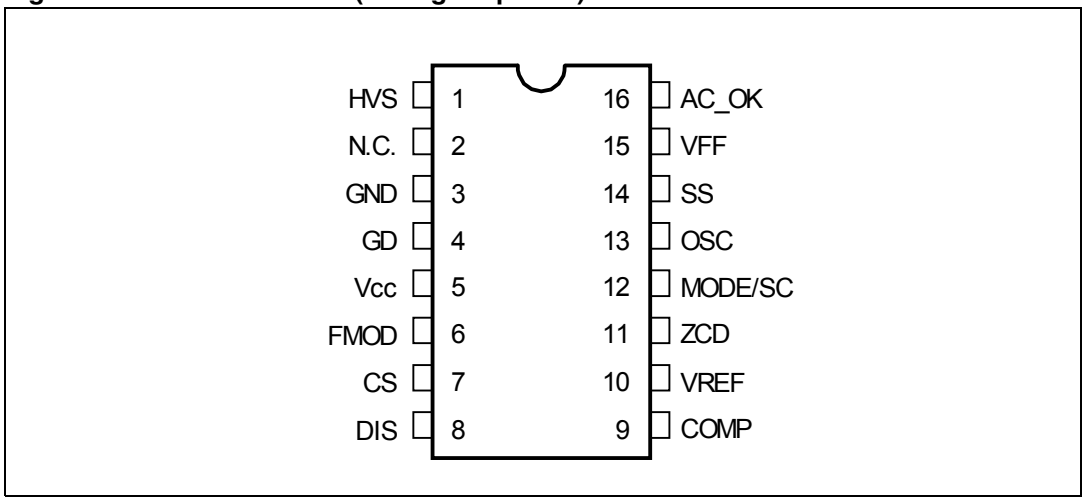
Figure 2. Typical system block diagram



2 Pin settings

2.1 Connections

Figure 3. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	HVS	High-voltage start-up. The pin, able to withstand 700 V, is to be tied directly to the rectified mains voltage. A 1 mA internal current source charges the capacitor connected between Vcc pin (5) and GND pin (3) until the voltage on the Vcc pin reaches the turn-on threshold, then it is shut down. Normally, the generator is re-enabled when the Vcc voltage falls below 5 V to ensure a low power throughput during short circuit. Otherwise, when a latched protection is tripped the generator is re-enabled 0.5 V below the turn-on threshold, to keep the latch supplied; or, when the IC is turned off by pin COMP (9) pulled low the generator is active just below the UVLO threshold to allow a faster restart.
2	N.C.	Not internally connected. Provision for clearance on the PCB to meet safety requirements.
3	GND	Ground. Current return for both the signal part of the IC and the gate drive. All of the ground connections of the bias components should be tied to a track going to this pin and kept separate from any pulsed current return.
4	GD	Gate driver output. The totem pole output stage is able to drive power MOSFET's and IGBT's with a peak current capability of 800 mA source/sink.

Table 1. Pin functions (continued)

N°	Pin	Function
5	Vcc	Supply voltage of both the signal part of the IC and the gate driver. The internal high voltage generator charges an electrolytic capacitor connected between this pin and GND (pin 3) as long as the voltage on the pin is below the turn-on threshold of the IC, after that it is disabled and the chip is turned on. The IC is disabled as the voltage on the pin falls below the UVLO threshold. This threshold is reduced at light load to counteract the natural reduction of the self-supply voltage. Sometimes a small bypass capacitor (0.1 µF typ.) to GND might be useful to get a clean bias voltage for the signal part of the IC.
6	FMOD	Frequency modulation input. When FF mode operation is selected, a capacitor connected from this pin to GND (pin 3) is alternately charged and discharged by internal current sources. As a result, the voltage on the pin is a symmetrical triangular waveform with the frequency related to the capacitance value. By connecting a resistor from this pin to pin 13 (OSC) it is possible to modulate the current sourced by the OSC pin and then the oscillator frequency. This modulation is to reduce the peak value of EMI emissions by means of a spread-spectrum action. If the function is not used, the pin will be left open.
7	CS	Input to the PWM comparator. The current flowing in the MOSFET is sensed through a resistor, the resulting voltage is applied to this pin and compared with an internal reference to determine MOSFET's turn-off. The pin is equipped with 150 ns min. blanking time after the gate-drive output goes high for improved noise immunity. A second comparison level located at 1.5 V latches the device off and reduces its consumption in case of transformer saturation or secondary diode short circuit. The information is latched until the voltage on the Vcc pin (5) goes below the UVLO threshold, hence resulting in intermittent operation. A logic circuit improves sensitivity to temporary disturbances.
8	DIS	IC's latched disable input. Internally the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V, latches off the IC and brings its consumption to a lower value. The latch is cleared as the voltage on the Vcc pin (5) goes below the UVLO threshold, but the HV generator keeps the Vcc voltage high (see pin 1 description). It is then necessary to recycle the input power to restart the IC. For a quick restart pull pin 16 (AC_OK) below the disable threshold (see pin 16 description). Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Ground the pin if the function is not used.
9	COMP	Control input for loop regulation. The pin will be driven by the phototransistor (emitter-grounded) of an optocoupler to modulate its voltage by modulating the current sunk. A capacitor placed between the pin and GND (3), as close to the IC as possible to reduce noise pick-up, sets a pole in the output-to-control transfer function. The dynamics of the pin is in the 2.5 to 5 V range. A voltage below an internally defined threshold activates burst-mode operation. The voltage at the pin is bottom-clamped at about 2 V. If the clamp is externally overridden and the voltage is pulled below 1.4 V the IC will shut down.
10	VREF	An internal generator furnishes an accurate voltage reference (5 V ± 2 %) that can be used to supply few mA to an external circuit. A small film capacitor (0.1 µF typ.), connected between this pin and GND (3), is recommended to ensure the stability of the generator and to prevent noise from affecting the reference. This reference is internally monitored by a separate auxiliary reference and any failure or drift will cause the IC to latch off.

Table 1. Pin functions (continued)

N°	Pin	Function
11	ZCD	Transformer demagnetization sensing input for quasi-resonant operation and OVP input. The pin is externally connected to the transformer's auxiliary winding through a resistor divider. A negative-going edge triggers MOSFET's turn-on if QR mode is selected. A voltage exceeding 5 V shuts the IC down and brings its consumption to a lower value (OVP). Latch-off or auto-restart mode is selectable externally. This function is strobed and digitally filtered to increase noise immunity.
12	MODE/SC	Operating mode selection. If the pin is connected to the VREF pin (7) quasi-resonant operation is selected, the oscillator (pin 13, OSC) determines the maximum allowed operating frequency. Fixed-frequency operation is selected if the pin is not tied to VREF, in which case the oscillator determines the actual operating frequency, the maximum allowed duty cycle is set at 70 % min. and the pin delivers a voltage ramp synchronized to the oscillator when the gate-drive output is high; the voltage delivered is zero while the gate-drive output is low. The pin is to be connected to pin CS (7) via a resistor for slope compensation.
13	OSC	Oscillator pin. The pin is an accurate 1 V voltage source, and a resistor connected from the pin to GND (pin 3) defines a current. This current is internally used to set the oscillator frequency that defines the maximum allowed switching frequency of the L6566B, if working in QR mode, or the operating switching frequency if working in FF mode.
14	SS	Soft-start current source. At start-up a capacitor Css between this pin and GND (pin 3) is charged with an internal current generator. During the ramp, the internal reference clamp on the current sense pin (7, CS) rises linearly starting from zero to its final value, thus causing the duty cycle to increase progressively starting from zero as well. During soft-start the adaptive UVLO function and all functions monitoring pin COMP are disabled. The soft-start capacitor is discharged whenever the supply voltage of the IC falls below the UVLO threshold. The same capacitor is used to delay IC's shutdown (latch-off or auto-restart mode selectable) after detecting an overload condition (OLP).
15	VFF	Line voltage feedforward input. The information on the converter's input voltage is fed into the pin through a resistor divider and is used to change the setpoint of the pulse-by-pulse current limitation (the higher the voltage, the lower the setpoint). The linear dynamics of the pin ranges from 0 to 3 V. A voltage higher than 3 V makes the IC stop switching. If feedforward is not desired, tie the pin to GND (pin 3) directly if a latch-mode OVP is not required (see pin 11, ZCD) or through a 10 kΩ min. resistor if a latch-mode OVP is required. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up.
16	AC_OK	Brownout protection input. A voltage below 0.45 V shuts down (not latched) the IC, lowers its consumption and clears the latch set by latched protections (DIS > 4.5 V, SS > 6.4 V, VFF > 6.4 V). IC's operation is re-enabled as the voltage exceeds 0.45 V. The comparator is provided with current hysteresis: an internal 15 µA current generator is ON as long as the voltage on the pin is below 0.45 V and is OFF if this value is exceeded. Bypass the pin with a capacitor to GND (pin 3) to reduce noise pick-up. Tie to Vcc with a 220 to 680 kΩ resistor if the function is not used.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Value	Unit
V_{HVS}	1	Voltage range (referred to ground)	-0.3 to 700	V
I_{HVS}	1	Output current	Self-limited	
V_{CC}	5	IC supply voltage (Icc = 20 mA)	Self-limited	
V_{FMOD}	6	Voltage range	-0.3 to 2	V
V_{max}	7, 8, 10, 14	Analog inputs and outputs	-0.3 to 7	V
V_{max}	9, 15, 16	Maximum pin voltage (Ipin ≤ 1 mA)	Self-limited	
I_{ZCD}	11	Zero current detector max. current	±5	mA
$V_{MODE/SC}$	12	Voltage range	-0.3 to 5.3	V
V_{OSC}	13	Voltage range	-0.3 to 3.3	V
P_{TOT}		Power dissipation @T_A = 50 °C	0.75	W
T_{STG}		Storage temperature	-55 to 150	°C
T_J		Junction operating temperature range	-40 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	120	°C/W

4 Electrical characteristics

(T_J = -25 to 125°C, V_{CC} = 12, C_O = 1 nF; MODE/SC = V_{REF}, R_T = 20 kΩ from OSC to GND, unless otherwise specified).

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Supply voltage						
Vcc	Operating range after turn-on	$V_{COMP} > V_{COMPL}$	10.6		23	V
		$V_{COMP} = V_{COMPO}$	8		23	
Vcc_{On}	Turn-on threshold	(1)	13	14	15	V
Vcc_{Off}	Turn-off threshold	(1) $V_{COMP} > V_{COMPL}$	9.4	10	10.6	V
		(1) $V_{COMP} = V_{COMPO}$	7.2	7.6	8.0	
Hys	Hysteresis	$V_{COMP} > V_{COMPL}$		4		V
V_Z	Zener voltage	Icc = 20 mA, IC disabled	23	25	27	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 13 V		200	250	µA
I_q	Quiescent current	After turn-on, $V_{ZCD} = V_{CS}$ = 1 V		2.6	2.8	mA
Icc	Operating supply current	MODE/SC open		4	4.6	mA
I_{qdis}	Quiescent current	IC disabled (2)	330		2500	µA
		IC latched off		440	500	
High-voltage start-up generator						
V_{HV}	Breakdown voltage	I_{HV} < 100 µA	700			V
$V_{HVstart}$	Start voltage	I_{Vcc} < 100 µA	65	80	100	V
I_{charge}	Vcc charge current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V	0.55	0.85	1	mA
$I_{HV, ON}$	ON-state current	$V_{HV} > V_{Hvstart}$, Vcc > 3 V			1.6	mA
		$V_{HV} > V_{Hvstart}$, Vcc = 0			0.8	
$I_{HV, OFF}$	OFF-state leakage current	V_{HV} = 400 V			40	µA
$V_{CCrestart}$	Vcc restart voltage	Vcc falling	4.4	5	5.6	V
		(1) IC latched off	12.5	13.5	14.5	
		(1) Disabled by $V_{COMP} < V_{COMPOFF}$	9.4	10	10.6	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Reference voltage						
V_{REF}	Output voltage	(1) T_J = 25 °C; I_{REF} = 1 mA	4.95	5	5.05	V
V_{REF}	Total variation	I_{REF} = 1 to 5 mA, Vcc = 10.6 to 23 V	4.9		5.1	V
I_{REF}	Short circuit current	V_{REF} = 0	10		30	mA
	Sink capability in UVLO	Vcc = 6 V; Isink = 0.5 mA		0.2	0.5	V
V_{OV}	Overvoltage threshold		5.3	5.7		V
Internal oscillator						
f_{sw}	Oscillation frequency	Operating range	10		300	kHz
		T_J = 25 °C, V_{ZCD} = 0, MODE/SC = open	95	100	105	
		Vcc =12 to 23 V, V_{ZCD} = 0, MODE/SC = open	93	100	107	
V_{OSC}	Voltage reference	(3)	0.97	1	1.03	V
D_{max}	Maximum duty cycle	MODE/SC = open, V_{COMP} = 5 V	70		75	%
Brownout protection						
Vth	Threshold voltage	Voltage falling (turn-off)	0.432	0.450	0.468	V
		Voltage rising (turn-on)	0.452	0.485	0.518	V
I_{Hys}	Current hysteresis	Vcc > 5 V, V_{VFF} = 0.3 V	12	15	18	µA
$V_{AC\_OK\_CL}$	Clamp level	(1) I_{AC_OK} = 100 µA	3	3.15	3.3	V
Line voltage feedforward						
I_{VFF}	Input bias current	V_{VFF} = 0 to 3 V, V_{ZCD} < V_{ZCDth}			-1	µA
		V_{ZCD} > V_{ZCDth}	-0.7	-1		mA
V_{VFF}	Linear operation range			0 to 3		V
V_{OFF}	IC disable voltage		3	3.15	3.3	V
$V_{VFFlatch}$	Latch-off/clamp level	V_{ZCD} > V_{ZCDth}		6.4		V
Kc	Control voltage gain (3)	V_{VFF} = 1 V, V_{COMP} = 4 V		0.4		V/V
K_{FF}	Feedforward gain (3)	V_{VFF} = 1 V, V_{COMP} = 4 V		0.04		V/V

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Current sense comparator						
I_{CS}	Input bias current	V_{CS} = 0			-1	µA
t_{LEB}	Leading edge blanking		150	250	300	ns
$td_{(H-L)}$	Delay to output				100	ns
V_{CSx}	Overcurrent setpoint	$V_{COMP} = V_{COMPHI}$, V_{VFF} = 0 V	0.92	1	1.08	V
		$V_{COMP} = V_{COMPHI}$, V_{VFF} = 1.5 V	0.45	0.5	0.55	
		$V_{COMP} = V_{COMPHI}$, V_{VFF} = 3.0 V		0	0.1	
V_{CSdis}	Hiccup-mode OCP level	(1)	1.4	1.5	1.6	V
PWM control						
V_{COMPHI}	Upper clamp voltage	I_{COMP} = 0		5.7		V
V_{COMPLO}	Lower clamp voltage	I_{SOURCE} = -1 mA		2.0		V
V_{COMPSH}	Linear dynamics upper limit	(1) V_{VFF} = 0 V	4.8	5	5.2	V
I_{COMP}	Max. source current	V_{COMP} = 3.3 V	320	400	480	µA
R_{COMP}	Dynamic resistance	V_{COMP} = 2.6 to 4.8 V		25		kΩ
V_{COMPBM}	Burst-mode threshold	(1)	2.52	2.65	2.78	V
		(1) MODE/SC = open	2.7	2.85	3	
Hys	Burst-mode hysteresis			20		mV
I_{CLAMPL}	Lower clamp capability	V_{COMP} = 2 V	-3.5		-1.5	mA
$V_{COMPOFF}$	Disable threshold	Voltage falling		1.4		V
V_{COMPO}	Level for lower UVLO off threshold (voltage falling)	(3)	2.61	2.75	2.89	V
		(3) MODE/SC = open	3.02	3.15	3.28	
V_{COMPL}	Level for higher UVLO off threshold (voltage rising)	(3)	2.9	3.05	3.2	V
		(3) MODE/SC = open	3.41	3.55	3.69	

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
Zero current detector/ overvoltage protection						
V_{ZCDH}	Upper clamp voltage	I_{ZCD} = 3 mA	5.4	5.7	6	V
V_{ZCDL}	Lower clamp voltage	I_{ZCD} = - 3 mA		-0.4		V
V_{ZCDA}	Arming voltage	(1) positive-going edge	85	100	115	mV
V_{ZCDT}	Triggering voltage	(1) negative-going edge	30	50	70	mV
I_{ZCD}	Internal pull-up	$V_{COMP} < V_{COMPSH}$			-1	µA
		V_{ZCD} < 2 V, $V_{COMP} = V_{COMPHI}$	-130	-100	-70	
I_{ZCDsrc}	Source current capability	$V_{ZCD} = V_{ZCDL}$	-3			mA
I_{ZCDsnk}	Sink current capability	$V_{ZCD} = V_{ZCDH}$	3			mA
T_{BLANK1}	Turn-on inhibit time	After gate-drive going low		2.5		µs
V_{ZCDth}	OVP threshold		4.85	5	5.15	V
T_{BLANK2}	OVP strobe delay	After gate-drive going low		2		µs
Latched shutdown function						
I_{OTP}	Input bias current	V_{DIS} = 0 to V_{OTP}			-1	µA
V_{OTP}	Disable threshold	(1)	4.32	4.5	4.68	V
Thermal shutdown						
Vth	Shutdown threshold			160		°C
Hys	Hysteresis			50		°C
External oscillator (frequency modulation)						
f_{FMOD}	Oscillation frequency	C_{MOD} = 0.1 µF	600	750	900	Hz
---	Usable frequency range		0.05		15	kHz
V_{pk}	Peak voltage	(3)		1.5		V
V_{vy}	Valley voltage			0.5		V
I_{FMOD}	Charge/discharge current			150		µA
Mode selection / slope compensation						
$MODE_{th}$	Threshold for QR operation			3		V
SC_{pk}	Ramp peak (MODE/SC = open)	R_{S-COMP} = 3 kΩ to GND, GD pin high, V_{COMP} = 5 V		1.7		V
SC_{vy}	Ramp starting value (MODE/SC = open)	R_{S-COMP} = 3 kΩ to GND, GD pin high		0.3		V
	Ramp voltage (MODE/SC = open)	GD pin low		0		V
	Source capability (MODE/SC = open)	$V_{S-COMP} = V_{S-COMPpk}$	0.8			mA

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Soft-start						
I_{SS1}	Charge current	T_J = 25 °C, V_{SS} < 2 V, V_{COMP} = 4 V	14	20	26	µA
I_{SS2}		T_J = 25 °C, V_{SS} > 2 V, V_{COMP} = V_{COMPHi}	3.5	5	6.5	
I_{SSdis}	Discharge current	V_{SS} > 2 V	3.5	5	6.5	µA
$V_{SSclamp}$	High saturation voltage	V_{COMP} = 4 V		2		V
V_{SSDIS}	Disable level	(1) V_{COMP} = V_{COMPHi}	4.85	5	5.15	V
V_{SSLAT}	Latch-off level	V_{COMP} = V_{COMPHi}		6.4		V
Gate driver						
V_{GDH}	Output high voltage	$I_{GDsource}$ = 5 mA, Vcc = 12 V	9.8	11		V
V_{GDL}	Output low voltage	I_{GDsink} = 100 mA		0.75		V
$I_{sourcepk}$	Output source peak current		-0.6			A
I_{sinkpk}	Output sink peak current		0.8			A
t_f	Fall time			40		ns
t_r	Rise time			50		ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; Vcc = 20 V	10	11.3	15	V
	UVLO saturation	Vcc = 0 to Vccon, I_{sink} = 1 mA		0.9	1.1	V

1. Parameters tracking one another.
2. See *Table 6 on page 41* and *Table 7 on page 42*
3. The voltage feedforward block output is given by: $V_{cs} = Kc\left(V_{COMP} - 2.5\right) - K_{FF}V_{VFF}$

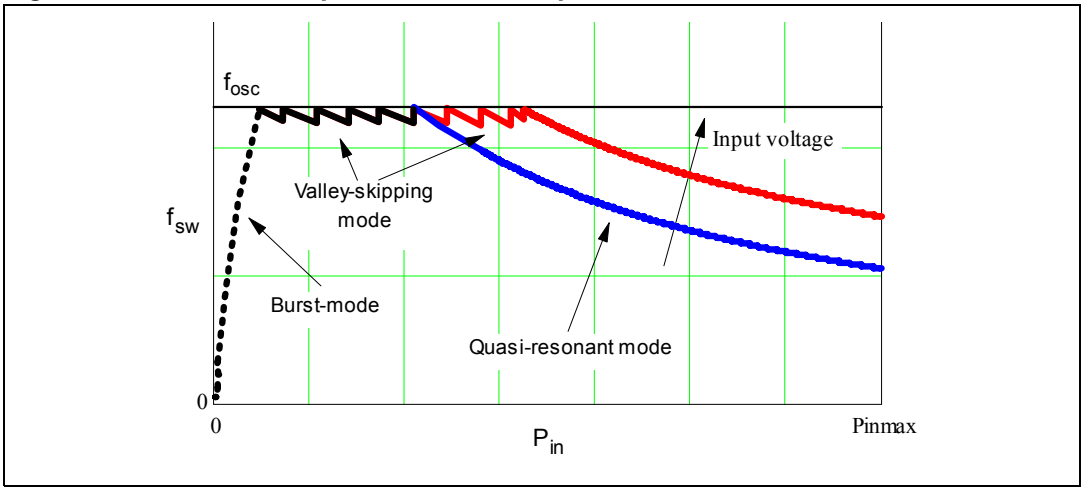
5 Application information

The L6566B is a versatile peak-current-mode PWM controller specific for offline flyback converters. The device allows either fixed-frequency (FF) or quasi-resonant (QR) operation, selectable with the pin MODE/SC (12): forcing the voltage on the pin over 3 V (e.g. by tying it to the 5 V reference externally available at pin VREF, 10) will activate QR operation, otherwise the device will be FF-operated.

Irrespective of the operating option selected by pin 12, the device is able to work in different modes, depending on the converter's load conditions. If QR operation is selected (see *Figure 4*):

1. QR mode at heavy load. Quasi-resonant operation lies in synchronizing MOSFET's turn-on to the transformer's demagnetization by detecting the resulting negative-going edge of the voltage across any winding of the transformer. Then the system works close to the boundary between discontinuous (DCM) and continuous conduction (CCM) of the transformer. As a result, the switching frequency will be different for different line/load conditions (see the hyperbolic-like portion of the curves in *Figure 4*). Minimum turn-on losses, low EMI emission and safe behavior in short circuit are the main benefits of this kind of operation.
2. Valley-skipping mode at medium/ light load. The externally programmable oscillator of the L6566B, synchronized to MOSFET's turn-on, enables the designer to define the maximum operating frequency of the converter. As the load is reduced MOSFET's turn-on will not any more occur on the first valley but on the second one, the third one and so on. In this way the switching frequency will no longer increase (piecewise linear portion in *Figure 4*).
3. Burst-mode with no or very light load. When the load is extremely light or disconnected, the converter will enter a controlled on/off operation with constant peak current. Decreasing the load will then result in frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations or recommendations. Being the peak current very low, no issue of audible noise arises.

Figure 4. Multi-mode operation with QR option active



If FF operation is selected:

1. FF mode from heavy to light load. The system operates exactly like a standard current mode control, at a frequency f_{sw} determined by the externally programmable oscillator: both DCM and CCM transformer operation are possible, depending on whether the power that it processes is greater or less than:

Equation 1

$$Pin_T = \frac{\left(\frac{Vin\ V_R}{Vin + V_R}\right)^2}{2 f_{sw} Lp}$$

where Vin is the input voltage to the converter, V_R the reflected voltage (i.e. the regulated output voltage times the primary-to-secondary turn ratio) and Lp the inductance of the primary winding. Pin_T is the power level that marks the transition from continuous to discontinuous operation mode of the transformer.

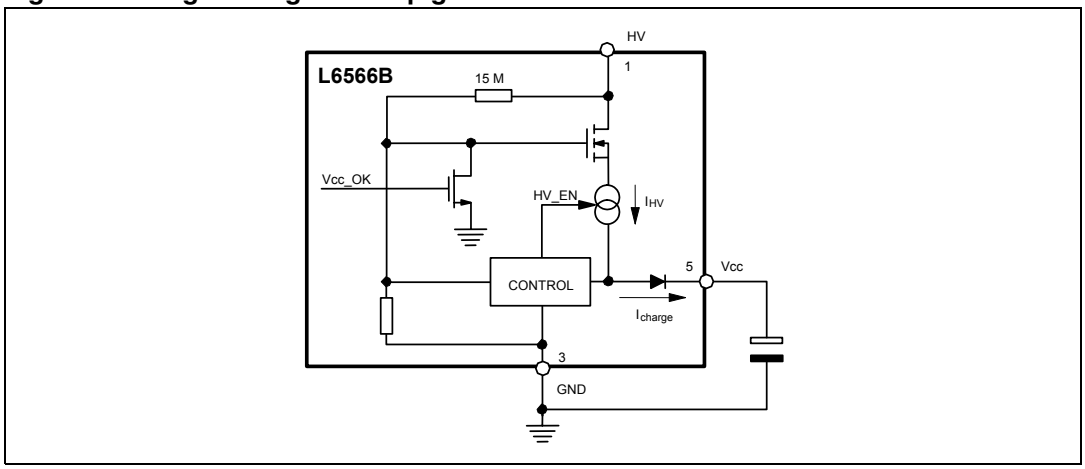
2. Burst-mode with no or very light load. This kind of operation is activated in the same way and results in the same behavior as previously described for QR operation.

The L6566B is specifically designed for applications with no PFC front-end; pin 6 (FMOD) features an auxiliary oscillator that can modulate the switching frequency (when FF operation is selected) in order to mitigate EMI emissions by a spread-spectrum action.

5.1 High-voltage start-up generator

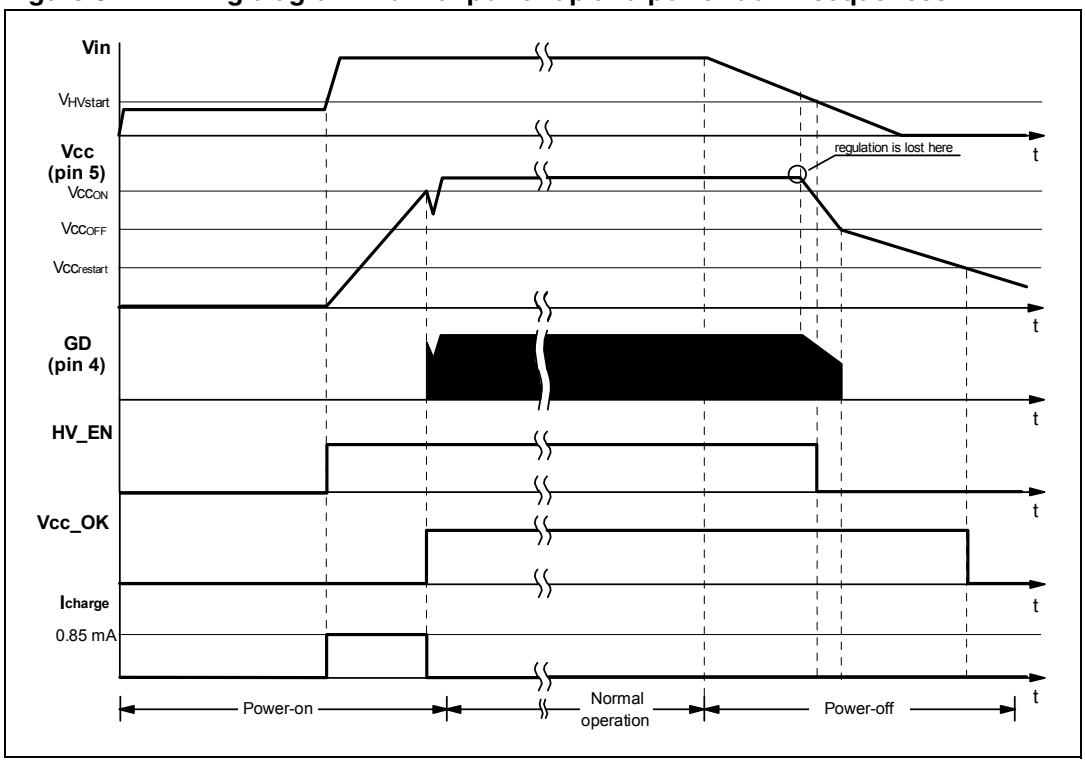
Figure 5 shows the internal schematic of the high-voltage start-up generator (HV generator). It is made up of a high-voltage N-channel FET, whose gate is biased by a 15 MΩ resistor, with a temperature-compensated current generator connected to its source.

Figure 5. High-voltage start-up generator: internal schematic



With reference to the timing diagram of *Figure 6*, when power is first applied to the converter the voltage on the bulk capacitor (Vin) builds up and, at about 80 V, the HV generator is enabled to operate (HV_EN is pulled high) so that it draws about 1 mA. This current, minus the device's consumption, charges the bypass capacitor connected from pin Vcc (5) to ground and makes its voltage rise almost linearly.

Figure 6. Timing diagram: normal power-up and power-down sequences



As the Vcc voltage reaches the turn-on threshold (14 V typ.) the device starts operating and the HV generator is cut off by the Vcc_OK signal asserted high. The device is powered by the energy stored in the Vcc capacitor until the self-supply circuit (typically an auxiliary winding of the transformer and a steering diode) develops a voltage high enough to sustain the operation. The residual consumption of this circuit is just the one on the 15 MΩ resistor (≈10 mW at 400 Vdc), typically 50-70 times lower, under the same conditions, as compared to a standard start-up circuit made with external dropping resistors.

At converter power-down the system will lose regulation as soon as the input voltage is so low that either peak current or maximum duty cycle limitation is tripped. Vcc will then drop and stop IC activity as it falls below the UVLO threshold (10 V typ.). The Vcc_OK signal is de-asserted as the Vcc voltage goes below a threshold VCC_{rest} located at about 5V. The HV generator can now restart. However, if Vin < Vin_{start}, as illustrated in *Figure 6*, HV_EN is de-asserted too and the HV generator is disabled. This prevents converter's restart attempts and ensures monotonic output voltage decay at power-down in systems where brownout protection (see the relevant section) is not used.

The low restart threshold VCC_{rest} ensures that, during short circuits, the restart attempts of the device will have a very low repetition rate, as shown in the timing diagram of *Figure 7 on page 20*, and that the converter will work safely with extremely low power throughput.

Figure 7. Timing diagram showing short-circuit behavior (SS pin clamped at 5 V)

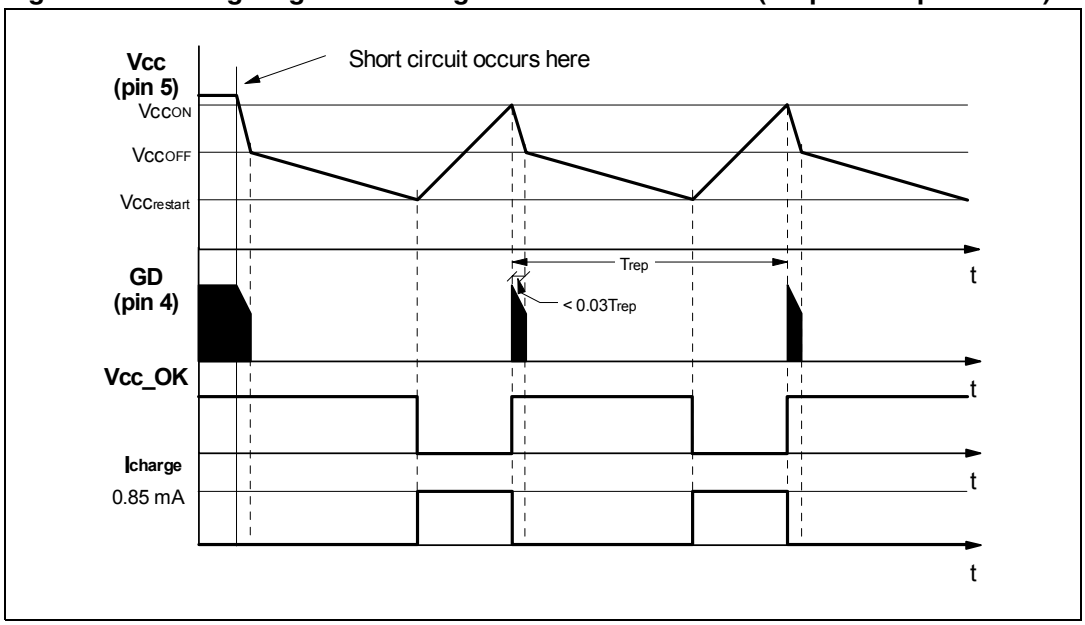
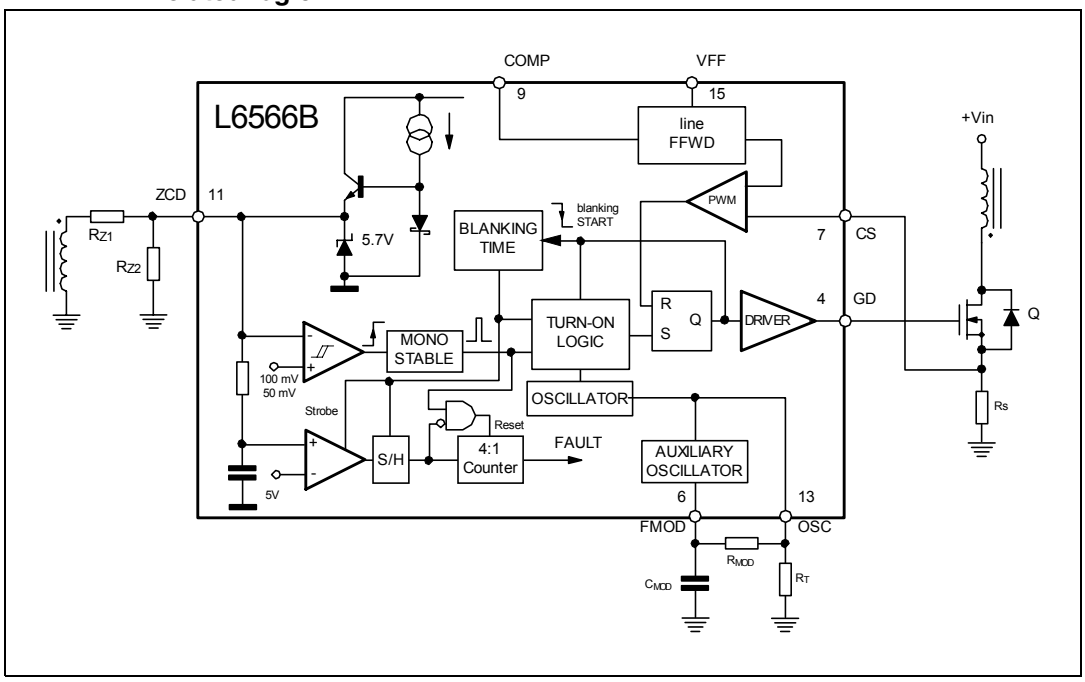


Figure 8. Zero current detection block, triggering block, oscillator block and related logic



5.2 Zero current detection and triggering block; oscillator block

The zero current detection (ZCD) and triggering blocks switch on the external MOSFET if a negative-going edge falling below 50 mV is applied to the input (pin 11, ZCD). To do so the triggering block must be previously armed by a positive-going edge exceeding 100 mV.

This feature is typically used to detect transformer demagnetization for QR operation, where the signal for the ZCD input is obtained from the transformer's auxiliary winding used also to supply the L6566B. The triggering block is blanked for T_{BLANK} = 2.5 µs after MOSFET's turn-off to prevent any negative-going edge that follows leakage inductance demagnetization from triggering the ZCD circuit erroneously.

The voltage at the pin is both top and bottom limited by a double clamp, as illustrated in the internal diagram of the ZCD block of *Figure 8 on page 20*. The upper clamp is typically located at 5.7 V, while the lower clamp is located at -0.4 V. The interface between the pin and the auxiliary winding will be a resistor divider. Its resistance ratio will be properly chosen (see *Section 5.11: OVP block on page 35*) and the individual resistance values (R_{Z1}, R_{Z2}) will be such that the current sourced and sunk by the pin be within the rated capability of the internal clamps (± 3 mA).

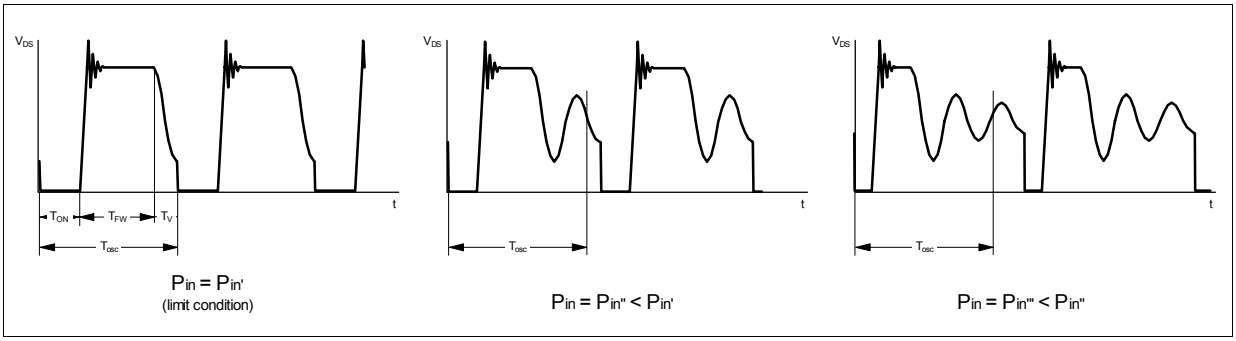
At converter power-up, when no signal is coming from the ZCD pin, the oscillator starts up the system. The oscillator is programmed externally by means of a resistor (R_T) connected from pin OSC (13) to ground. With good approximation the oscillation frequency f_{osc} will be:

Equation 2

$$f_{osc} \approx \frac{2 \cdot 10^3}{R_T}$$

(with f_{osc} in kHz and R_T in kΩ). As the device is turned on, the oscillator starts immediately; at the end of the first oscillator cycle, being zero the voltage on the ZCD pin, the MOSFET will be turned on, thus starting the first switching cycle right at the beginning of the second oscillator cycle. At any switching cycle, the MOSFET is turned off as the voltage on the current sense pin (CS, 7) hits an internal reference set by the line feedforward block, and the transformer starts demagnetization. If this completes (hence a negative-going edge appears on the ZCD pin) after a time exceeding one oscillation period $T_{osc} = 1/f_{osc}$ from the previous turn-on, the MOSFET will be turned on again - with some delay to ensure minimum voltage at turn-on – and the oscillator ramp will be reset. If, instead, the negative-going edge appears before T_{osc} has elapsed, it will be ignored and only the first negative-going edge after T_{osc} will turn-on the MOSFET and synchronize the oscillator. In this way one or more drain ringing cycles will be skipped ("valley-skipping mode", *Figure 9*) and the switching frequency will be prevented from exceeding f_{osc}.

Figure 9. Drain ringing cycle skipping as the load is gradually reduced



Note: When the system operates in valley skipping-mode, uneven switching cycles may be observed under some line/load conditions, due to the fact that the OFF-time of the MOSFET is allowed to change with discrete steps of one ringing cycle, while the OFF-time needed for cycle-by-cycle energy balance may fall in between. Thus one or more longer switching cycles will be compensated by one or more shorter cycles and vice versa. However, this mechanism is absolutely normal and there is no appreciable effect on the performance of the converter or on its output voltage.

If the MOSFET is enabled to turn on but the amplitude of the signal on the ZCD pin is smaller than the arming threshold for some reason (e.g. a heavy damping of drain oscillations, like in some single-stage PFC topologies, or when a turn-off snubber is used), MOSFET's turn-on cannot be triggered. This case is identical to what happens at start-up: at the end of the next oscillator cycle the MOSFET will be turned on, and a new switching cycle will take place after skipping no more than one oscillator cycle.

The operation described so far does not consider the blanking time T_{BLANK} after MOSFET's turn off, and actually T_{BLANK} does not come into play as long as the following condition is met:

Equation 3

$$D \leq 1 - \frac{T_{BLANK}}{T_{osc}}$$

where D is the MOSFET duty cycle. If this condition is not met, things do not change substantially: the time during which MOSFET's turn-on is inhibited is extended beyond T_{osc} by a fraction of T_{BLANK}. As a consequence, the maximum switching frequency will be a little lower than the programmed value f_{osc} and valley-skipping mode may take place slightly earlier than expected. However this is quite unusual: setting f_{osc} = 150 kHz, the phenomenon can be observed at duty cycles higher than 60 %. See *Section 5.11: OVP block on page 35* for further implications of T_{BLANK}.

If the voltage on the COMP pin (9) saturates high, which reveals an open control loop, an internal pull-up keeps the ZCD pin close to 2 V during MOSFET's OFF-time to prevent noise from false triggering the detection block. When this pull-up is active, the ZCD pin might not be able to go below the triggering threshold, which would stop the converter. To allow auto-restart operation, however ensuring minimum operating frequency in these conditions, the oscillator frequency that retriggers MOSFET's turn-on is that of the external oscillator divided by 128. Additionally, to prevent malfunction at converter's start-up, the pull-up is disabled during the initial soft-start (see the relevant section). However, to ensure a correct

start-up, at the end of the soft-start phase the output voltage of the converter must meet the condition:

Equation 4

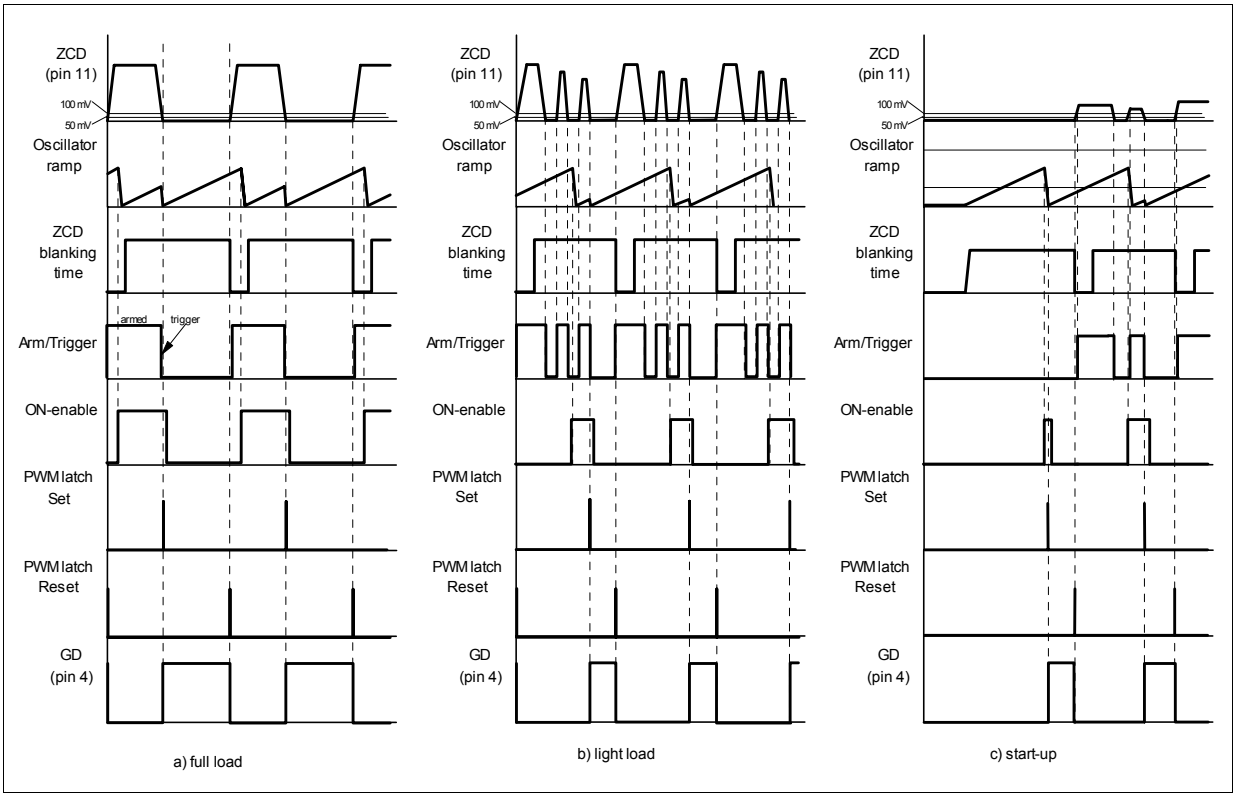
$$Vout > \frac{Ns}{Naux} R_{Z1} I_{ZCD}$$

where Ns is the turn number of the secondary winding, Naux the turn number of the auxiliary winding and I_{ZCD} the maximum pull-up current (130 µA).

The operation described so far under different operating conditions for the converter is illustrated in the timing diagrams of *Figure 10*.

If the FF option is selected the operation will be exactly equal to that of a standard current-mode PWM controller. It will work at a frequency fsw = fosc; both DCM and CCM transformer's operation are possible, depending on the operating conditions (input voltage and output load) and on the design of the power stage. The MOSFET is turned on at the beginning of each oscillator cycle and is turned off as the voltage on the current sense pin reaches an internal reference set by the line feedforward block. The maximum duty cycle is limited at 70 % minimum. The signal on the ZCD pin in this case is used only for detecting feedback loop failures (see *Section 5.11: OVP block on page 35*).

Figure 10. Operation of ZCD, triggering and oscillator blocks (QR option active)



5.3 Burst-mode operation at no load or very light load

When the voltage at the COMP pin (9) falls 20 mV below a threshold fixed internally at a value, V_{COMPBM}, depending on the selected operating mode, the L6566B is disabled with the MOSFET kept in OFF state and its consumption reduced at a lower value to minimize Vcc capacitor discharge.

The control voltage now will increase as a result of the feedback reaction to the energy delivery stop (the output voltage will be slowly decaying), the threshold will be exceeded and the device will restart switching again. In this way the converter will work in burst-mode with a nearly constant peak current defined by the internal disable level. A load decrease will then cause a frequency reduction, which can go down even to few hundred hertz, thus minimizing all frequency-related losses and making it easier to comply with energy saving regulations. This kind of operation, shown in the timing diagrams of *Figure 11* along with the others previously described, is noise-free since the peak current is low.

If it is necessary to decrease the intervention threshold of the burst-mode operation, this can be done by adding a small DC offset on the current sense pin as shown in *Figure 12 on page 25*.

Note: The offset reduces the available dynamics of the current signal; thereby, the value of the sense resistor must be determined taking this offset into account.

Figure 11. Load-dependent operating modes: timing diagrams

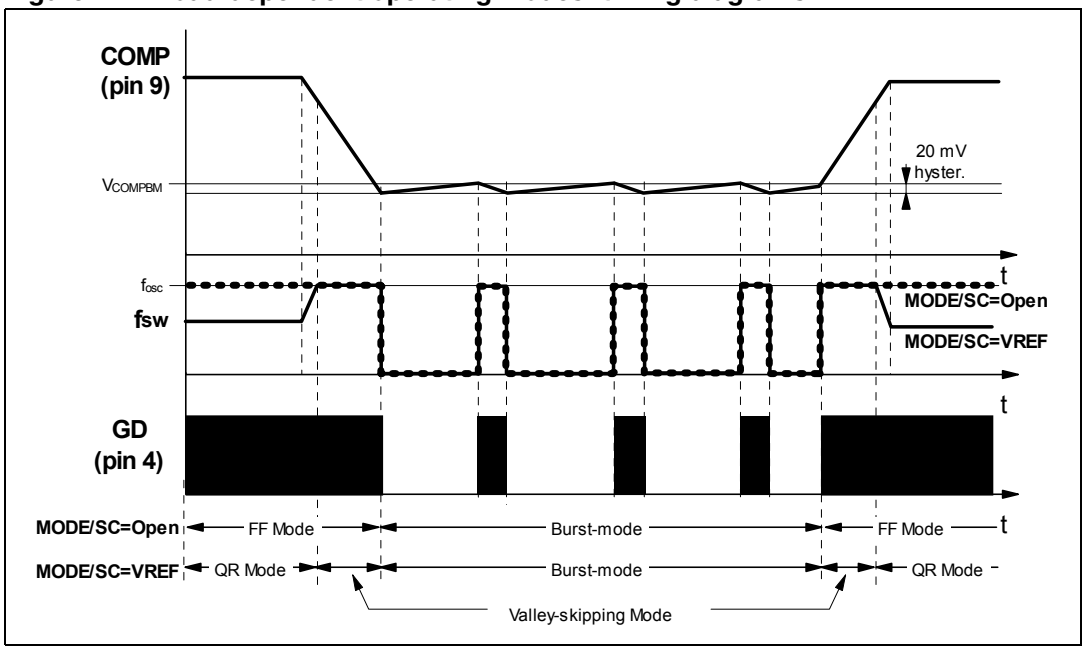
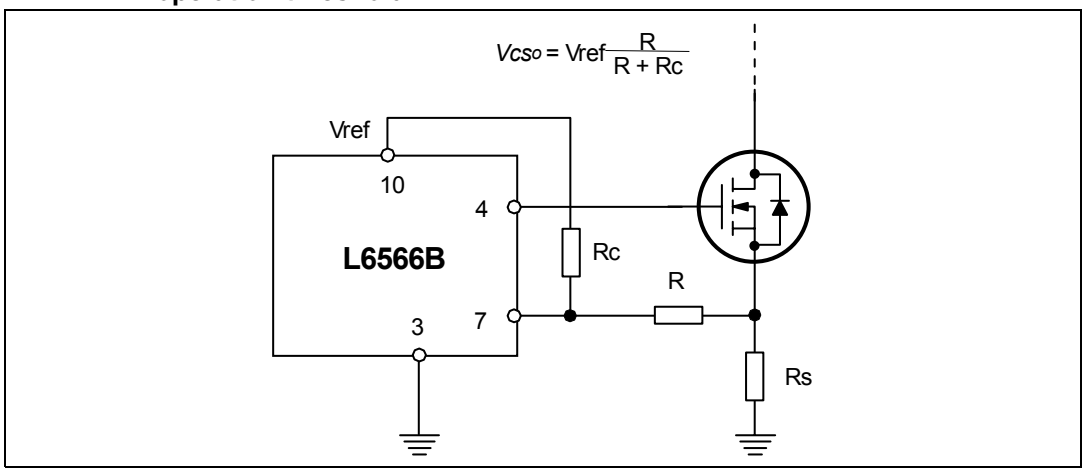


Figure 12. Addition of an offset to the current sense lowers the burst-mode operation threshold



5.4 Adaptive UVLO

A major problem when optimizing a converter for minimum no-load consumption is that the voltage generated by the auxiliary winding under these conditions falls considerably as compared even to a few mA load. This very often causes the supply voltage Vcc of the control IC to drop and go below the UVLO threshold so that the operation becomes intermittent, which is undesired. Furthermore, this must be traded off against the need of generating a voltage not exceeding the maximum allowed by the control IC at full load.

To help the designer overcome this problem, the device, besides reducing its own consumption during burst-mode operation, also features a proprietary adaptive UVLO function. It consists of shifting the UVLO threshold downwards at light load, namely when the voltage at pin COMP falls below a threshold V_{COMPO} internally fixed, so as to have more headroom. To prevent any malfunction during transients from minimum to maximum load the normal (higher) UVLO threshold is re-established when the voltage at pin COMP exceeds V_{COMPL} and Vcc has exceeded the normal UVLO threshold (see *Figure 13*). The normal UVLO threshold ensures that at full load the MOSFET will be driven with a proper gate-to-source voltage.

Figure 13. Adaptive UVLO block