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eX Family FPGAs

Leading Edge Performance

- 240 MHz System Performance
- 350 MHz Internal Performance
- 3.9 ns Clock-to-Out (Pad-to-Pad)

Specifications

- 3,000 to 12,000 Available System Gates
- Maximum 512 Flip-Flops (Using CC Macros)
- 0.22 μ m CMOS Process Technology
- Up to 132 User-Programmable I/O Pins

Features

- High-Performance, Low-Power Antifuse FPGA
- LP/Sleep Mode for Additional Power Savings
- Advanced Small-Footprint Packages
- Hot-Swap Compliant I/Os

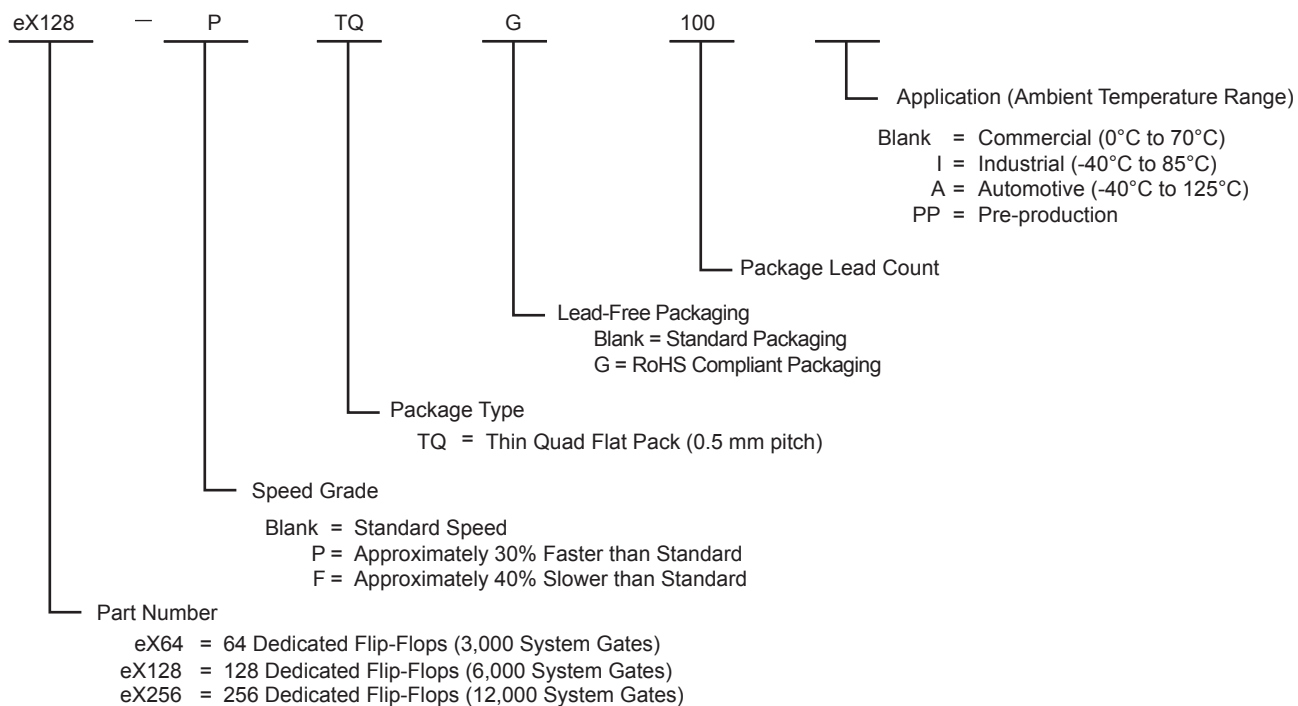
- Single-Chip Solution
- Nonvolatile
- Live on Power-Up
- No Power-Up/Down Sequence Required for Supply Voltages
- Configurable Weak-Resistor Pull-Up or Pull-Down for Tristated Outputs during Power-Up
- Individual Output Slew Rate Control
- 2.5 V, 3.3 V, and 5.0 V Mixed-Voltage Operation with 5.0V Input Tolerance and 5.0V Drive Strength
- Software Design Support with Microsemi Designer and Libero[®] Integrated Design Environment (IDE) Tools
- Up to 100% Resource Utilization with 100% Pin Locking
- Deterministic Timing
- Unique In-System Diagnostic and Verification Capability with Silicon Explorer II
- Boundary Scan Testing in Compliance with IEEE Standard 1149.1 (JTAG)
- Fuselock[™] Secure Programming Technology Designed to Prevent Reverse Engineering and Design Theft

Product Profile

Device	eX64	eX128	eX256
Capacity			
System Gates	3,000	6,000	12,000
Typical Gates	2,000	4,000	8,000
Register Cells			
Dedicated Flip-Flops	64	128	256
Maximum Flip-Flops	128	256	512
Combinatorial Cells	128	256	512
Maximum User I/Os	84	100	132
Global Clocks			
Hardwired	1	1	1
Routed	2	2	2
Speed Grades	-F, Std, -P	-F, Std, -P	-F, Std, -P
Temperature Grades*	C, I, A	C, I, A	C, I, A
Package (by pin count)			
TQ	64, 100	64, 100	100

Note: *Refer to the eX Automotive Family FPGAs datasheet for details on automotive temperature offerings.

Ordering Information



eX Device Status

eX Devices	Status
eX64	Production
eX128	Production
eX256	Production

Plastic Device Resources

Device	User I/Os (Including Clock Buffers)	
	TQ64	TQ100
eX64	41	56
eX128	46	70
eX256	—	81

Note: TQ = Thin Quad Flat Pack

Temperature Grade Offerings

Device\ Package	TQ64	TQ100
eX64	C, I, A	C, I, A
eX128	C, I, A	C, I, A
eX256	C, I, A	C, I, A

Note: C = Commercial

I = Industrial

A = Automotive

Speed Grade and Temperature Grade Matrix

	-F	Std	-P
C	✓	✓	✓
I		✓	✓
A		✓	

Note: P = Approximately 30% faster than Standard

-F = Approximately 40% slower than Standard

Refer to the [eX Automotive Family FPGAs datasheet](#) for details on automotive temperature offerings.

Contact your local Microsemi representative for device availability.

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1 – eX FPGA Architecture and Characteristics

General Description

The eX family of FPGAs is a low-cost solution for low-power, high-performance designs. The inherent low power attributes of the antifuse technology, coupled with an additional low static power mode, make these devices ideal for power-sensitive applications. Fabricated with an advanced 0.22 mm CMOS antifuse technology, these devices achieve high performance with no power penalty.

eX Family Architecture

Microsemi eX family is implemented on a high-voltage twin-well CMOS process using 0.22 μm design rules. The eX family architecture uses a “sea-of-modules” structure where the entire floor of the device is covered with a grid of logic modules with virtually no chip area lost to interconnect elements or routing. Interconnection among these logic modules is achieved using Microsemi patented metal-to-metal programmable antifuse interconnect elements. The antifuse interconnect is made up of a combination of amorphous silicon and dielectric material with barrier metals and has an “on” state resistance of 25Ω with a capacitance of 1.0fF for low-signal impedance. The antifuses are normally open circuit and, when programmed, form a permanent low-impedance connection. The eX family provides two types of logic modules, the register cell (R-cell) and the combinatorial cell (C-cell).

The R-cell contains a flip-flop featuring asynchronous clear, asynchronous preset, and clock enable (using the S0 and S1 lines) control signals (Figure 1-1). The R-cell registers feature programmable clock polarity selectable on a register-by-register basis. This provides additional flexibility while allowing mapping of synthesized functions into the eX FPGA. The clock source for the R-cell can be chosen from either the hard-wired clock or the routed clock.

The C-cell implements a range of combinatorial functions up to five inputs (Figure 1-2 on page 1-2). Inclusion of the DB input and its associated inverter function enables the implementation of more than 4,000 combinatorial functions in the eX architecture in a single module.

Two C-cells can be combined together to create a flip-flop to imitate an R-cell via the use of the CC macro. This is particularly useful when implementing non-timing-critical paths and when the design engineer is running out of R-cells. More information about the CC macro can be found in the [Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros](#) application note.

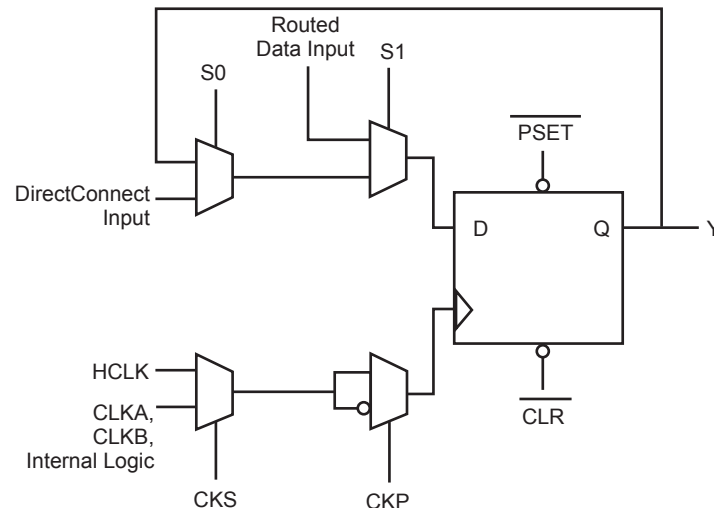


Figure 1-1 • R-Cell

Module Organization

C-cell and R-cell logic modules are arranged into horizontal banks called Clusters, each of which contains two C-cells and one R-cell in a C-R-C configuration.

Clusters are further organized into modules called SuperClusters for improved design efficiency and device performance, as shown in Figure 1-3. Each SuperCluster is a two-wide grouping of Clusters.

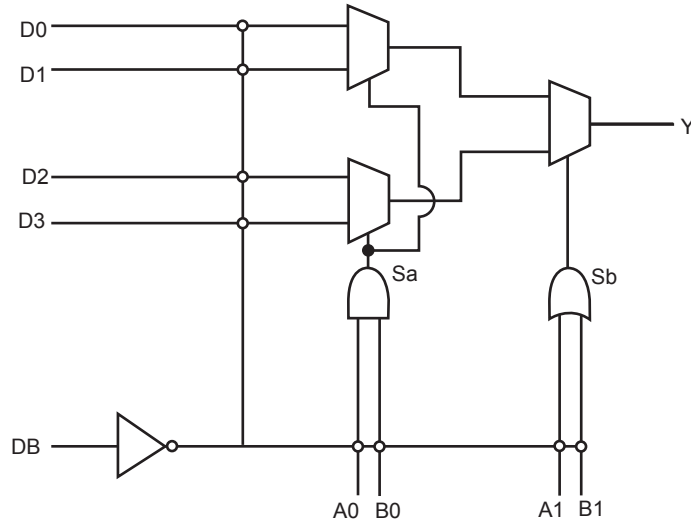


Figure 1-2 • C-Cell

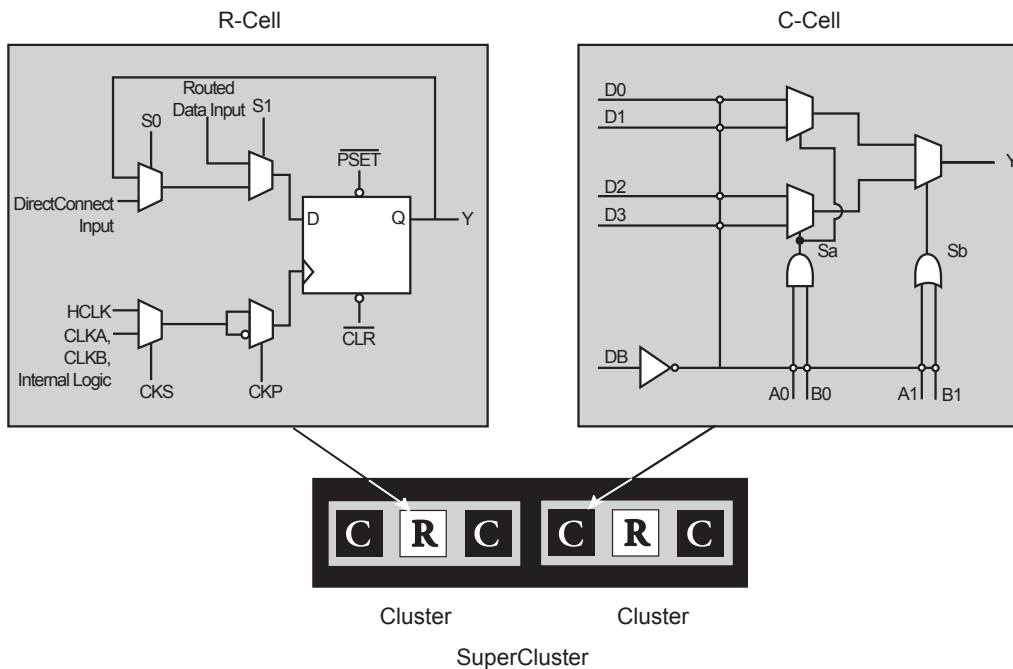


Figure 1-3 • Cluster Organization

Routing Resources

Clusters and SuperClusters can be connected through the use of two innovative local routing resources called FastConnect and DirectConnect, which enable extremely fast and predictable interconnection of modules within Clusters and SuperClusters (Figure 1-4). This routing architecture also dramatically reduces the number of antifuses required to complete a circuit, ensuring the highest possible performance.

DirectConnect is a horizontal routing resource that provides connections from a C-cell to its neighboring R-cell in a given SuperCluster. DirectConnect uses a hard-wired signal path requiring no programmable interconnection to achieve its fast signal propagation time of less than 0.1 ns (–P speed grade).

FastConnect enables horizontal routing between any two logic modules within a given SuperCluster and vertical routing with the SuperCluster immediately below it. Only one programmable connection is used in a FastConnect path, delivering maximum pin-to-pin propagation of 0.3 ns (–P speed grade).

In addition to DirectConnect and FastConnect, the architecture makes use of two globally oriented routing resources known as segmented routing and high-drive routing. The segmented routing structure of Microsemi provides a variety of track lengths for extremely fast routing between SuperClusters. The exact combination of track lengths and antifuses within each path is chosen by the fully automatic place-and-route software to minimize signal propagation delays.

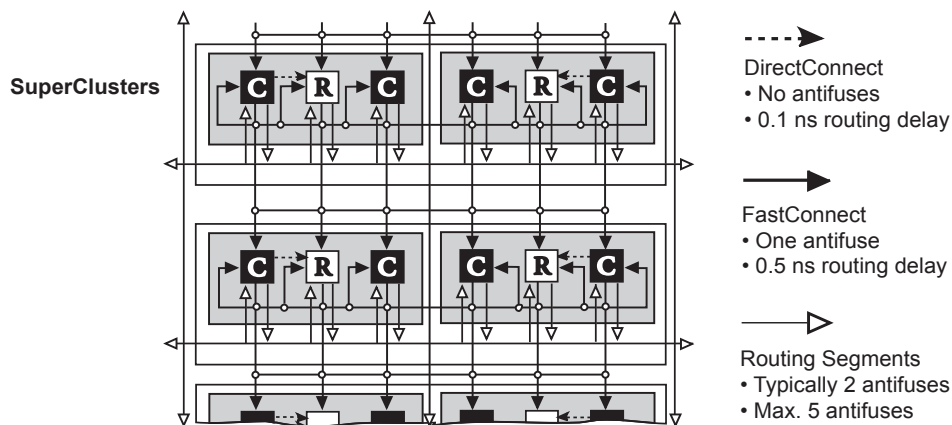


Figure 1-4 • DirectConnect and FastConnect for SuperClusters

Clock Resources

eX's high-drive routing structure provides three clock networks. The first clock, called HCLK, is hardwired from the HCLK buffer to the clock select MUX in each R-Cell. HCLK cannot be connected to combinational logic. This provides a fast propagation path for the clock signal, enabling the 3.9 ns clock-to-out (pad-to-pad) performance of the eX devices. The hard-wired clock is tuned to provide a clock skew of less than 0.1 ns worst case. If not used, the HCLK pin must be tied LOW or HIGH and must not be left floating. Figure 1-5 describes the clock circuit used for the constant load HCLK.

HCLK does not function until the fourth clock cycle each time the device is powered up to prevent false output levels due to any possible slow power-on-reset signal and fast start-up clock circuit. To activate HCLK from the first cycle, the TRST pin must be reserved in the Design software and the pin must be tied to GND on the board. (See the "TRST, I/O Boundary Scan Reset Pin" on page 1-32).

The remaining two clocks (CLKA, CLKB) are global routed clock networks that can be sourced from external pins or from internal logic signals (via the CLKINT routed clock buffer) within the eX device. CLKA and CLKB may be connected to sequential cells or to combinational logic. If CLKA or CLKB is sourced from internal logic signals, the external clock pin cannot be used for any other input and must be tied LOW or HIGH and must not float. Figure 1-6 describes the CLKA and CLKB circuit used in eX devices.

Table 1-1 describes the possible connections of the routed clock networks, CLKA and CLKB. Unused clock pins must not be left floating and must be tied to HIGH or LOW.

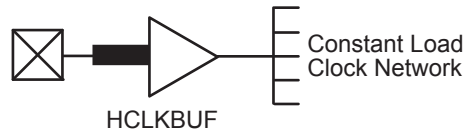


Figure 1-5 • eX HCLK Clock Pad

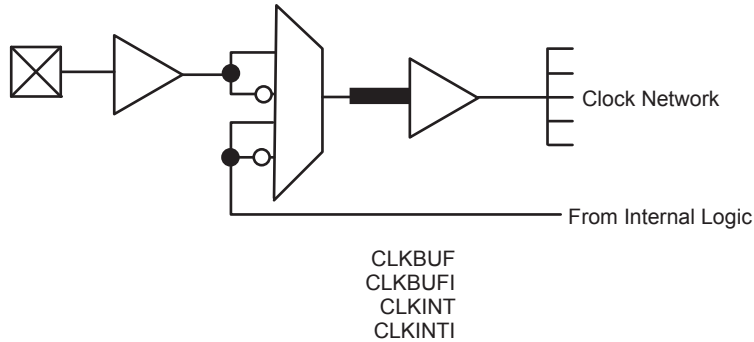


Figure 1-6 • eX Routed Clock Buffer

Table 1-1 • Connections of Routed Clock Networks, CLKA and CLKB

Module	Pins
C-Cell	A0, A1, B0 and B1
R-Cell	CLKA, CLKB, S0, S1, PSET, and CLR
I/O-Cell	EN

Other Architectural Features

Performance

The combination of architectural features described above enables eX devices to operate with internal clock frequencies exceeding 350 MHz for very fast execution of complex logic functions. The eX family is an optimal platform upon which the functionality previously contained in CPLDs can be integrated. eX devices meet the performance goals of gate arrays, and at the same time, present significant improvements in cost and time to market. Using timing-driven place-and-route tools, designers can achieve highly deterministic device performance.

User Security

Microsemi FuseLock advantage provides the highest level of protection in the FPGA industry against unauthorized modifications. In addition to the inherent strengths of the architecture, special security fuses that are intended to prevent internal probing and overwriting are hidden throughout the fabric of the device. They are located such that they cannot be accessed or bypassed without destroying the rest of the device, making Microsemi antifuse FPGAs highly resistant to both invasive and more subtle noninvasive attacks.

Look for this symbol to ensure your valuable IP is secure. The FuseLock Symbol on the FPGA ensures that the device is safeguarded to cryptographic attacks.



FuseLock

Figure 1-7 • Fuselock

For more information, refer to *Implementation of Security in Microsemi Antifuse FPGAs* application note.

I/O Modules

Each I/O on an eX device can be configured as an input, an output, a tristate output, or a bidirectional pin. Even without the inclusion of dedicated I/O registers, these I/Os, in combination with array registers, can achieve clock-to-out (pad-to-pad) timing as fast as 3.9 ns. I/O cells in eX devices do not contain embedded latches or flip-flops and can be inferred directly from HDL code. The device can easily interface with any other device in the system, which in turn enables parallel design of system components and reduces overall design time.

All unused I/Os are configured as tristate outputs by Microsemi's Designer software, for maximum flexibility when designing new boards or migrating existing designs. Each I/O module has an available pull-up or pull-down resistor of approximately 50 k Ω that can configure the I/O in a known state during power-up. Just shortly before V_{CCA} reaches 2.5 V, the resistors are disabled and the I/Os will be controlled by user logic.

Table 1-2 describes the I/O features of eX devices. For more information on I/Os, refer to [Microsemi eX, SX-A, and RT54SX-S I/Os application note](#).

Table 1-2 • I/O Features

Function	Description
Input Buffer Threshold Selection	<ul style="list-style-type: none"> • 5.0V TTL • 3.3V LVTTTL • 2.5V LVCMOS2
Nominal Output Drive	<ul style="list-style-type: none"> • 5.0V TTL/CMOS • 3.3V LVTTTL • 2.5V LVCMOS 2
Output Buffer	“Hot-Swap” Capability <ul style="list-style-type: none"> • I/O on an unpowered device does not sink current • Can be used for “cold sparing” Selectable on an individual I/O basis Individually selectable low-slew option
Power-Up	Individually selectable pull ups and pull downs during power-up (default is to power up in tristate) Enables deterministic power-up of device V_{CCA} and V_{CCI} can be powered in any order

The eX family supports mixed-voltage operation and is designed to tolerate 5.0 V inputs in each case. A detailed description of the I/O pins in eX devices can be found in ["Pin Description" on page 1-31](#).

Hot-Swapping

eX I/Os are configured to be hot-swappable. During power-up/down (or partial up/down), all I/Os are tristated, provided V_{CCA} ramps up within a diode drop of V_{CCI} . V_{CCA} and V_{CCI} do not have to be stable during power-up/down, and they do not require a specific power-up or power-down sequence in order to avoid damage to the eX devices. In addition, all outputs can be programmed to have a weak resistor pull-up or pull-down for output tristate at power-up. After the eX device is plugged into an electrically active system, the device will not degrade the reliability of or cause damage to the host system. The device's output pins are driven to a high impedance state until normal chip operating conditions are reached. Please see the application note, [Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications](#), which also applies to the eX devices, for more information on hot swapping.

Power Requirements

Power consumption is extremely low for the eX family due to the low capacitance of the antifuse interconnects. The antifuse architecture does not require active circuitry to hold a charge (as do SRAM or EPROM), making it the lowest-power FPGA architecture available today.

Low Power Mode

The eX family has been designed with a Low Power Mode. This feature, activated with setting the special LP pin to HIGH for a period longer than 800 ns, is particularly useful for battery-operated systems where battery life is a primary concern. In this mode, the core of the device is turned off and the device consumes minimal power with low standby current. In addition, all input buffers are turned off, and all outputs and bidirectional buffers are tristated when the device enters this mode. Since the core of the device is turned off, the states of the registers are lost. The device must be re-initialized when returning to normal operating mode. I/Os can be driven during LP mode. For details, refer to the [Design for Low Power in Microsemi Antifuse FPGAs](#) application note under the section Using the LP Mode Pin on eX Devices. Clock pins should be driven either HIGH or LOW and should not float; otherwise, they will draw current and burn power. The device must be re-initialized when exiting LP mode.

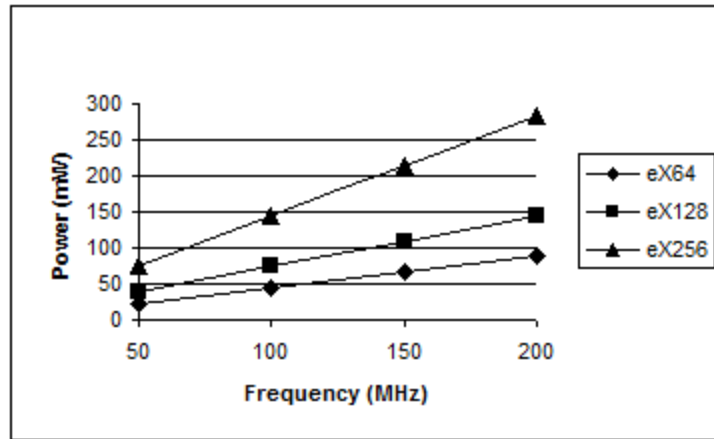
To exit the LP mode, the LP pin must be driven LOW for over 200 μ s to allow for the charge pumps to power-up and device initialization can begin.

Table 1-3 illustrates the standby current of eX devices in LP mode.

Table 1-3 • Standby Power of eX Devices in LP Mode Typical Conditions, V_{CCA} , $V_{CCI} = 2.5$ V, $T_J = 25^\circ$ C

Product	Low Power Standby Current	Units
eX64	100	μ A
eX128	111	μ A
eX256	134	μ A

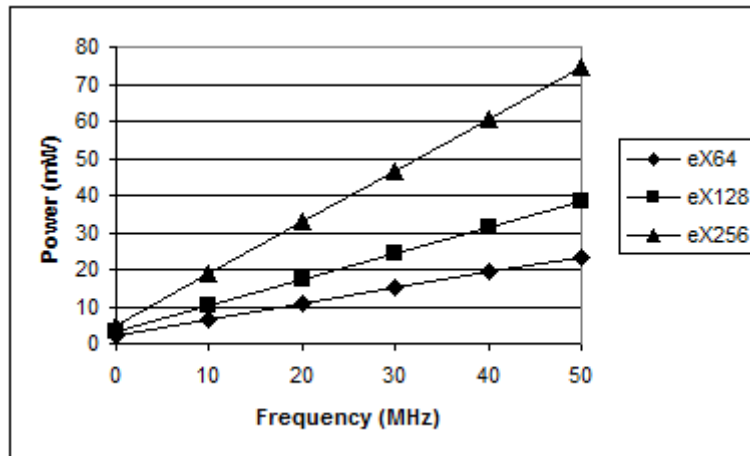
Figure 1-8 to Figure 1-11 on page 1-9 show some sample power characteristics of eX devices.



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-8 • eX Dynamic Power Consumption – High Frequency



Notes:

1. Device filled with 16-bit counters.
2. VCCA, VCCI = 2.7 V, device tested at room temperature.

Figure 1-9 • eX Dynamic Power Consumption – Low Frequency

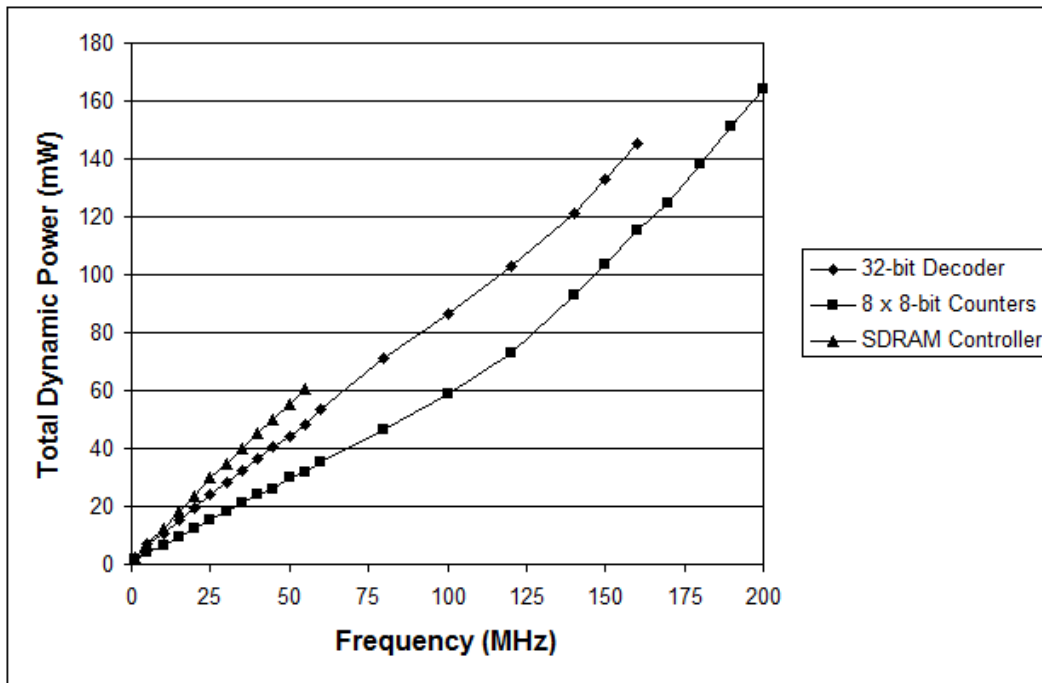


Figure 1-10 • Total Dynamic Power (mW)

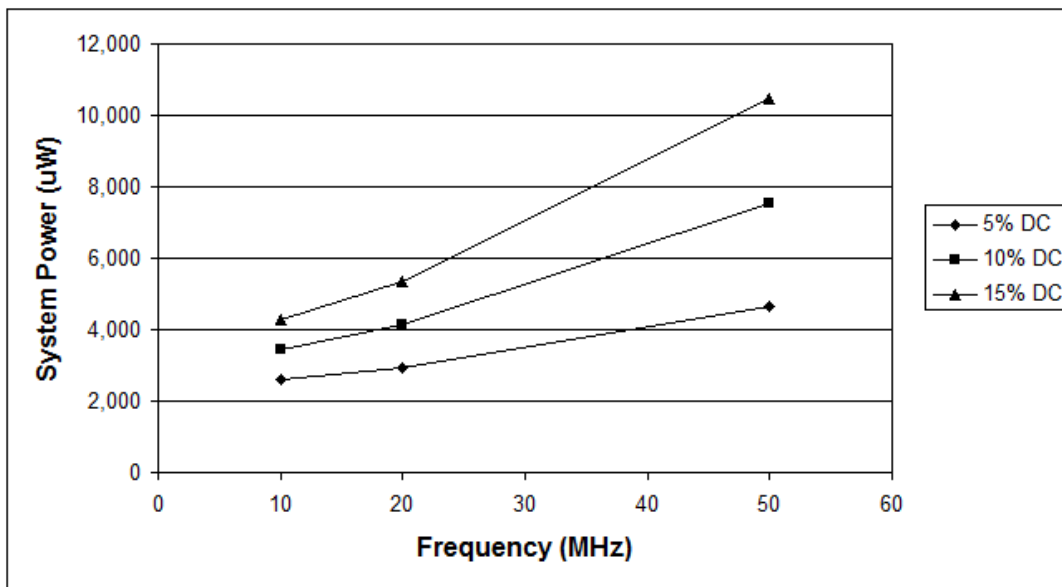


Figure 1-11 • System Power at 5%, 10%, and 15% Duty Cycle

Boundary Scan Testing (BST)

All eX devices are IEEE 1149.1 compliant. eX devices offer superior diagnostic and testing capabilities by providing Boundary Scan Testing (BST) and probing capabilities. These functions are controlled through the special test pins (TMS, TDI, TCK, TDO and TRST). The functionality of each pin is defined by two available modes: Dedicated and Flexible, and is described in [Table 1-4](#). In the dedicated test mode, TCK, TDI, and TDO are dedicated pins and cannot be used as regular I/Os. In flexible mode (default mode), TMS should be set HIGH through a pull-up resistor of 10 k Ω . TMS can be pulled LOW to initiate the test sequence.

Table 1-4 • Boundary Scan Pin Functionality

Dedicated Test Mode	Flexible Mode
TCK, TDI, TDO are dedicated BST pins	TCK, TDI, TDO are flexible and may be used as I/Os
No need for pull-up resistor for TMS and TDI	Use a pull-up resistor of 10 k Ω on TMS

Dedicated Test Mode

In Dedicated mode, all JTAG pins are reserved for BST; designers cannot use them as regular I/Os. An internal pull-up resistor is automatically enabled on both TMS and TDI pins, and the TMS pin will function as defined in the IEEE 1149.1 (JTAG) specification.

To select Dedicated mode, users need to reserve the JTAG pins in Microsemi's Designer software by checking the **Reserve JTAG** box in the Device Selection Wizard ([Figure 1-12](#)). JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O. Refer to the "3.3 V LVTTTL Electrical Specifications" section and "5.0 V TTL Electrical Specifications" section on [page 1-18](#) for detailed specifications.



Figure 1-12 • Device Selection Wizard

Flexible Mode

In Flexible Mode, TDI, TCK and TDO may be used as either user I/Os or as JTAG input pins. The internal resistors on the TMS and TDI pins are disabled in flexible JTAG mode, and an external 10 k Ω pull-resistor to V_{CC1} is required on the TMS pin.

To select the Flexible mode, users need to clear the check box for **Reserve JTAG** in the Device Selection Wizard in Microsemi's Designer software. The functionality of TDI, TCK, and TDO pins is controlled by the BST TAP controller. The TAP controller receives two control inputs, TMS and TCK. Upon power-up, the TAP controller enters the Test-Logic-Reset state. In this state, TDI, TCK, and TDO function as user I/Os. The TDI, TCK, and TDO pins are transformed from user I/Os into BST pins when the TMS pin is LOW at the first rising edge of TCK. The TDI, TCK, and TDO pins return to user I/Os when TMS is held HIGH for at least five TCK cycles.

Table 1-5 describes the different configuration requirements of BST pins and their functionality in different modes.

Table 1-5 • Boundary-Scan Pin Configurations and Functions

Mode	Designer "Reserve JTAG" Selection	TAP Controller State
Dedicated (JTAG)	Checked	Any
Flexible (User I/O)	Unchecked	Test-Logic-Reset
Flexible (JTAG)	Unchecked	Any EXCEPT Test-Logic-Reset

TRST Pin

The TRST pin functions as a dedicated Boundary-Scan Reset pin when the **Reserve JTAG Test Reset** option is selected, as shown in Figure 1-12. An internal pull-up resistor is permanently enabled on the TRST pin in this mode. It is recommended to connect this pin to GND in normal operation to keep the JTAG state controller in the Test-Logic-Reset state. When JTAG is being used, it can be left floating or be driven HIGH.

When the **Reserve JTAG Test Reset** option is not selected, this pin will function as a regular I/O. If unused as an I/O in the design, it will be configured as a tristated output.

JTAG Instructions

Table 1-6 lists the supported instructions with the corresponding IR codes for eX devices.

Table 1-6 • JTAG Instruction Code

Instructions (IR4: IR0)	Binary Code
EXTEST	00000
SAMPLE / PRELOAD	00001
INTEST	00010
USERCODE	00011
IDCODE	00100
HIGHZ	01110
CLAMP	01111
Diagnostic	10000
BYPASS	11111
Reserved	All others

Table 1-7 lists the codes returned after executing the IDCODE instruction for eX devices. Note that bit 0 is always "1." Bits 11-1 are always "02F", which is Microsemi SoC Products Group's manufacturer code.

Table 1-7 • IDCODE for eX Devices

Device	Revision	Bits 31-28	Bits 27-12
eX64	0	8	40B2, 42B2
eX128	0	9	40B0, 42B0
eX256	0	9	40B5, 42B5
eX64	1	A	40B2, 42B2
eX128	1	B	40B0, 42B0
eX256	1	B	40B5, 42B5

Programming

Device programming is supported through Silicon Sculptor series of programmers. In particular, Silicon Sculptor II is a compact, robust, single-site and multi-site device programmer for the PC.

With standalone software, Silicon Sculptor II allows concurrent programming of multiple units from the same PC, ensuring the fastest programming times possible. Each fuse is subsequently verified by Silicon Sculptor II to insure correct programming. In addition, integrity tests ensure that no extra fuses are programmed. Silicon Sculptor II also provides extensive hardware self-testing capability.

The procedure for programming an eX device using Silicon Sculptor II is as follows:

1. Load the *.AFM file
2. Select the device to be programmed
3. Begin programming

When the design is ready to go to production, Microsemi offers device volume-programming services either through distribution partners or via in-house programming from the factory.

For more details on programming eX devices, please refer to the [Programming Antifuse Devices](#) application note and the [Silicon Sculptor II User's Guide](#).

Probing Capabilities

eX devices provide internal probing capability that is accessed with the JTAG pins. The Silicon Explorer II Diagnostic hardware is used to control the TDI, TCK, TMS and TDO pins to select the desired nets for debugging. The user simply assigns the selected internal nets in the Silicon Explorer II software to the PRA/PRB output pins for observation. Probing functionality is activated when the BST pins are in JTAG mode and the TRST pin is driven HIGH or left floating. If the TRST pin is held LOW, the TAP controller will remain in the Test-Logic-Reset state so no probing can be performed. The Silicon Explorer II automatically places the device into JTAG mode, but the user must drive the TRST pin HIGH or allow the internal pull-up resistor to pull TRST HIGH.

When you select the **Reserve Probe Pin** box, as shown in [Figure 1-12 on page 1-10](#), the layout tool reserves the PRA and PRB pins as dedicated outputs for probing. This reserve option is merely a guideline. If the Layout tool requires that the PRA and PRB pins be user I/Os to achieve successful layout, the tool will use these pins for user I/Os. If you assign user I/Os to the PRA and PRB pins and select the **Reserve Probe Pin** option, Designer Layout will override the "Reserve Probe Pin" option and place your user I/Os on those pins.

To allow for probing capabilities, the security fuse must not be programmed. Programming the security fuse will disable the probe circuitry. [Table 1-8 on page 1-13](#) summarizes the possible device configurations for probing once the device leaves the Test-Logic-Reset JTAG state.

Silicon Explorer II Probe

Silicon Explorer II is an integrated hardware and software solution that, in conjunction with Microsemi Designer software tools, allow users to examine any of the internal nets of the device while it is operating in a prototype or a production system. The user can probe into an eX device via the PRA and PRB pins without changing the placement and routing of the design and without using any additional resources. Silicon Explorer II's noninvasive method does not alter timing or loading effects, thus shortening the debug cycle.

Silicon Explorer II does not require re-layout or additional MUXes to bring signals out to an external pin, which is necessary when using programmable logic devices from other suppliers.

Silicon Explorer II samples data at 100 MHz (asynchronous) or 66 MHz (synchronous). Silicon Explorer II attaches to a PC's standard COM port, turning the PC into a fully functional 18-channel logic analyzer. Silicon Explorer II allows designers to complete the design verification process at their desks and reduces verification time from several hours per cycle to a few seconds.

The Silicon Explorer II tool uses the boundary scan ports (TDI, TCK, TMS and TDO) to select the desired nets for verification. The selected internal nets are assigned to the PRA/PRB pins for observation. [Figure 1-13 on page 1-13](#) illustrates the interconnection between Silicon Explorer II and the eX device to perform in-circuit verification.

Design Considerations

The TDI, TCK, TDO, PRA, and PRB pins should not be used as input or bidirectional ports. Since these pins are active during probing, critical signals input through these pins are not available while probing. In addition, the Security Fuse should not be programmed because doing so disables the probe circuitry. It is recommended to use a series 70Ω termination resistor on every probe connector (TDI, TCK, TMS, TDO, PRA, PRB). The 70Ω series termination is used to prevent data transmission corruption during probing and reading back the checksum.

Table 1-8 • Device Configuration Options for Probe Capability (TRST pin reserved)

JTAG Mode	TRST ¹	Security Fuse Programmed	PRA, PRB ²	TDI, TCK, TDO ²
Dedicated	LOW	No	User I/O ³	Probing Unavailable
Flexible	LOW	No	User I/O ³	User I/O ³
Dedicated	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
Flexible	HIGH	No	Probe Circuit Outputs	Probe Circuit Inputs
–	–	Yes	Probe Circuit Secured	Probe Circuit Secured

Notes:

1. If TRST pin is not reserved, the device behaves according to TRST = HIGH in the table.
2. Avoid using the TDI, TCK, TDO, PRA, and PRB pins as input or bidirectional ports. Since these pins are active during probing, input signals will not pass through these pins and may cause contention.
3. If no user signal is assigned to these pins, they will behave as unused I/Os in this mode. Unused pins are automatically tristated by Microsemi Designer software.

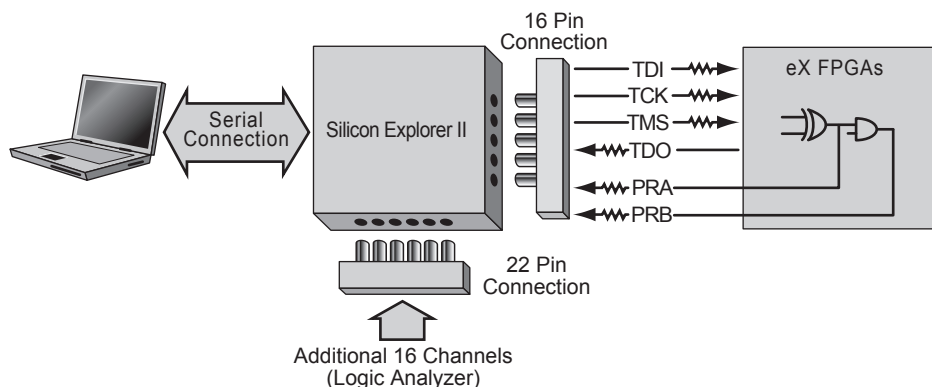


Figure 1-13 • Silicon Explorer II Probe Setup

Development Tool Support

The eX family of FPGAs is fully supported by both Libero® Integrated Design Environment and Designer FPGA Development software. Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment. Libero IDE includes Synplify® for Microsemi from Synplicity®, ViewDraw for Microsemi from Mentor Graphics, ModelSim® HDL Simulator from Mentor Graphics®, WaveFormer Lite™ from SynaptiCAD™, and Designer software from Microsemi. Refer to the [Libero IDE flow](#) (located on Microsemi SoC Product Group’s website) diagram for more information.

Designer software is a place-and-route tool and provides a comprehensive suite of backend support tools for FPGA development. The Designer software includes timing-driven place-and-route, and a world-class integrated static timing analyzer and constraints editor. With the Designer software, a user can lock his/her design pins before layout while minimally impacting the results of place-and-route. Additionally, the back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with Silicon Explorer II, Microsemi integrated verification and logic analysis tool. Another tool included in the Designer software is the SmartGen core generator, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design. Microsemi's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and UNIX operating systems.

Related Documents

Datasheet

eX Automotive Family FPGAs

www.microsemi.com/soc/documents/eX_Auto_DS.pdf

Application Notes

Maximizing Logic Utilization in eX, SX and SX-A FPGA Devices Using CC Macros

www.microsemi.com/soc/documents/CC_Macro_AN.pdf

Implementation of Security in Microsemi Antifuse FPGAs

www.microsemi.com/soc/documents/Antifuse_Security_AN.pdf

Microsemi eX, SX-A, and RT54SX-S I/Os

www.microsemi.com/soc/documents/antifuseIO_AN.pdf

Microsemi SX-A and RT54SX-S Devices in Hot-Swap and Cold-Sparing Applications

www.microsemi.com/soc/documents/HotSwapColdSparing_AN.pdf

Design For Low Power in Microsemi Antifuse FPGAs

www.microsemi.com/soc/documents/Low_Power_AN.pdf

Programming Antifuse Devices

www.microsemi.com/soc/documents/AntifuseProgram_AN.pdf

User Guides

Silicon Sculptor II User's Guide

www.microsemi.com/soc/documents/SiliSculptII_Sculpt3_ug.pdf

Miscellaneous

Libero IDE flow

www.microsemi.com/soc/products/tools/libero/flow.html

2.5 V / 3.3 V / 5.0 V Operating Conditions

Table 1-9 • Absolute Maximum Ratings*

Symbol	Parameter	Limits	Units
VCCI	DC Supply Voltage for I/Os	−0.3 to +6.0	V
VCCA	DC Supply Voltage for Array	−0.3 to +3.0	V
VI	Input Voltage	−0.5 to +5.75	V
VO	Output Voltage	−0.5 to +V _{CCL}	V
T _{STG}	Storage Temperature	−65 to +150	°C

Note: *Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

Table 1-10 • Recommended Operating Conditions

Parameter	Commercial	Industrial	Units
Temperature Range*	0 to +70	−40 to +85	°C
2.5V Power Supply Range (VCCA, VCCI)	2.3 to 2.7	2.3 to 2.7	V
3.3V Power Supply Range (VCCI)	3.0 to 3.6	3.0 to 3.6	V
5.0V Power Supply Range (VCCI)	4.75 to 5.25	4.75 to 5.25	V

Note: *Ambient temperature (T_A).

Table 1-11 • Typical eX Standby Current at 25°C

Product	VCCA = 2.5 V VCCI = 2.5 V	VCCA = 2.5 V VCCI = 3.3 V	VCCA = 2.5 V VCCI = 5.0 V
eX64	397 μA	497 μA	700 μA
eX128	696 μA	795 μA	1,000 μA
eX256	698 μA	796 μA	2,000 μA

2.5 V LVCMOS2 Electrical Specifications

Symbol	Parameter		Commercial		Industrial		Units
			Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL	(IOH = -100 mA)	2.1		2.1		V
	VCCI = MIN, VI = VIH or VIL	(IOH = -1 mA)	2.0		2.0		V
	VCCI = MIN, VI = VIH or VIL	(IOH = -2 mA)	1.7		1.7		V
VOL	VCCI = MIN, VI = VIH or VIL	(IOL = 100 mA)		0.2		0.2	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 1mA)		0.4		0.4	V
	VCCI = MIN, VI = VIH or VIL	(IOL = 2 mA)		0.7		0.7	V
VIL	Input Low Voltage, VOUT ≤ VOL (max.)		-0.3	0.7	-0.3	0.7	V
VIH	Input High Voltage, VOUT ≥ VOH (min.)		1.7	VCCI + 0.3	1.7	VCCI + 0.3	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND		-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND		-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time			10		10	ns
C _{IO}	I/O Capacitance			10		10	pF
ICC ^{3,4}	Standby Current			1.0		3.0	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .						

Notes:

1. t_R is the transition time from 0.7 V to 1.7 V.
2. t_F is the transition time from 1.7 V to 0.7 V.
3. I_{CC} max Commercial -F = 5.0 mA
4. $I_{CC} = I_{CCI} + I_{CCA}$

3.3 V LVTTTL Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL (IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL (IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage		0.8		0.8	V
VIH	Input High Voltage	2.0	VCCI + 0.5	2.0	VCCI + 0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND	-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND	-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time		10		10	ns
C _{IO}	I/O Capacitance		10		10	pF
ICC ^{3,4}	Standby Current		1.5		10	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .					

Notes:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F = 5.0 mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

5.0 V TTL Electrical Specifications

Symbol	Parameter	Commercial		Industrial		Units
		Min.	Max.	Min.	Max.	
VOH	VCCI = MIN, VI = VIH or VIL (IOH = -8 mA)	2.4		2.4		V
VOL	VCCI = MIN, VI = VIH or VIL (IOL = 12 mA)		0.4		0.4	V
VIL	Input Low Voltage		0.8		0.8	V
VIH	Input High Voltage	2.0	VCCI + 0.5	2.0	VCCI + 0.5	V
IIL/ IIH	Input Leakage Current, VIN = VCCI or GND	-10	10	-10	10	μA
IOZ	3-State Output Leakage Current, VOUT = VCCI or GND	-10	10	-10	10	μA
t _R , t _{F1,2}	Input Transition Time		10		10	ns
C _{IO}	I/O Capacitance		10		10	pF
ICC ^{3,4}	Standby Current		15		20	mA
IV Curve	Can be derived from the IBIS model at www.microsemi.com/soc/custsup/models/ibis.html .					

Note:

1. t_R is the transition time from 0.8 V to 2.0 V.
2. t_F is the transition time from 2.0 V to 0.8 V.
3. ICC max Commercial -F = 20 mA
4. ICC = ICCI + ICCA
5. JTAG pins comply with LVTTTL/TTL I/O specification regardless of whether they are used as a user I/O or a JTAG I/O.

Power Dissipation

Power consumption for eX devices can be divided into two components: static and dynamic.

Static Power Component

The power due to standby current is typically a small component of the overall power. Typical standby current for eX devices is listed in the [Table 1-11 on page 1-16](#). For example, the typical static power for eX128 at 3.3 V V_{CCI} is:

$$I_{CC} * V_{CCA} = 795 \mu A * 2.5 V = 1.99 mW$$

Dynamic Power Component

Power dissipation in CMOS devices is usually dominated by the dynamic power dissipation. This component is frequency-dependent and a function of the logic and the external I/O. Dynamic power dissipation results from charging internal chip capacitance due to PC board traces and load device inputs. An additional component of the dynamic power dissipation is the totem pole current in the CMOS transistor pairs. The net effect can be associated with an equivalent capacitance that can be combined with frequency and voltage to represent dynamic power dissipation.

$$\text{Dynamic power dissipation} = C_{EQ} * V_{CCA}^2 * F$$

where:

C_{EQ} = Equivalent capacitance

F = switching frequency

Equivalent capacitance is calculated by measuring I_{CCA} at a specified frequency and voltage for each circuit component of interest. Measurements have been made over a range of frequencies at a fixed value of VCC. Equivalent capacitance is frequency-independent, so the results can be used over a wide range of operating conditions. Equivalent capacitance values are shown below.

CEQ Values for eX Devices

Combinatorial modules (C_{eqcm})	1.70 pF
Sequential modules (C_{eqsm})	1.70 pF
Input buffers (C_{eqi})	1.30 pF
Output buffers (C_{eqo})	7.40 pF
Routed array clocks (C_{eqcr})	1.05 pF

The variable and fixed capacitance of other device components must also be taken into account when estimating the dynamic power dissipation.

[Table 1-12](#) shows the capacitance of the clock components of eX devices.

Table 1-12 • Capacitance of Clock Components of eX Devices

	eX64	eX128	eX256
Dedicated array clock – variable (C_{eqhv})	0.85 pF	0.85 pF	0.85 pF
Dedicated array clock – fixed (C_{eqhf})	18.00 pF	20.00 pF	25.00 pF
Routed array clock A (r1)	23.00 pF	28.00 pF	35.00 pF
Routed array clock B (r2)	23.00 pF	28.00 pF	35.00 pF

The estimation of the dynamic power dissipation is a piece-wise linear summation of the power dissipation of each component.

$$\begin{aligned} \text{Dynamic power dissipation} = & V_{CCA}^2 * [(m_c * C_{eqcm} * f_{mC})_{\text{Comb Modules}} + (m_s * C_{eqsm} * f_{mS})_{\text{Seq Modules}} \\ & + (n * C_{eqi} * f_n)_{\text{Input Buffers}} + (0.5 * (q1 * C_{eqcr} * f_{q1}) + (r1 * f_{q1}))_{\text{RCLKA}} + (0.5 * (q2 * C_{eqcr} * f_{q2}) \\ & + (r2 * f_{q2}))_{\text{RCLKB}} + (0.5 * (s1 * C_{eqhv} * f_{s1}) + (C_{eqhf} * f_{s1}))_{\text{HCLK}}] + V_{CCI}^2 * [(p * (C_{eqo} + C_L) \\ & * f_p)_{\text{Output Buffers}}] \end{aligned}$$

where:

- m_c = Number of combinatorial cells switching at frequency f_m , typically 20% of C-cells
- m_s = Number of sequential cells switching at frequency f_m , typically 20% of R-cells
- n = Number of input buffers switching at frequency f_n , typically number of inputs / 4
- p = Number of output buffers switching at frequency f_p , typically number of outputs / 4
- $q1$ = Number of R-cells driven by routed array clock A
- $q2$ = Number of R-cells driven by routed array clock B
- $r1$ = Fixed capacitance due to routed array clock A
- $r2$ = Fixed capacitance due to routed array clock B
- $s1$ = Number of R-cells driven by dedicated array clock
- C_{eqcm} = Equivalent capacitance of combinatorial modules
- C_{eqsm} = Equivalent capacitance of sequential modules
- C_{eqi} = Equivalent capacitance of input buffers
- C_{eqcr} = Equivalent capacitance of routed array clocks
- C_{eqhv} = Variable capacitance of dedicated array clock
- C_{eqhf} = Fixed capacitance of dedicated array clock
- C_{eqo} = Equivalent capacitance of output buffers
- C_L = Average output loading capacitance, typically 10 pF
- f_{mC} = Average C-cell switching frequency, typically $F/10$
- f_{mS} = Average R-cell switching frequency, typically $F/10$
- f_n = Average input buffer switching frequency, typically $F/5$
- f_p = Average output buffer switching frequency, typically $F/5$
- f_{q1} = Frequency of routed clock A
- f_{q2} = Frequency of routed clock B
- f_{s1} = Frequency of dedicated array clock

The eX, SX-A and RTSX-S Power Calculator can be used to estimate the total power dissipation (static and dynamic) of eX devices: www.microsemi.com/soc/techdocs/calculators.aspx.

Thermal Characteristics

The temperature variable in the Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because the heat generated from dynamic power consumption is usually hotter than the ambient temperature. EQ 1, shown below, can be used to calculate junction temperature.

EQ 1

$$\text{Junction Temperature} = \Delta T + T_a(1)$$

Where:

T_a = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient = $\theta_{ja} * P$

P = Power

θ_{ja} = Junction to ambient of package. θ_{ja} numbers are located in the "Package Thermal Characteristics" section below.

Package Thermal Characteristics

The device junction-to-case thermal characteristic is θ_{jc} , and the junction-to-ambient air characteristic is θ_{ja} . The thermal characteristics for θ_{ja} are shown with two different air flow rates. θ_{jc} is provided for reference. The maximum junction temperature is 150°C.

The maximum power dissipation allowed for eX devices is a function of θ_{ja} . A sample calculation of the absolute maximum power dissipation allowed for a TQFP 100-pin package at commercial temperature and still air is as follows:

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (}^\circ\text{C)} - \text{Max. ambient temp. (}^\circ\text{C)}}{\theta_{ja} (^\circ\text{C/W)}} = \frac{150^\circ\text{C} - 70^\circ\text{C}}{33.5^\circ\text{C/W}} = 2.39\text{W}$$

Package Type	Pin Count	θ_{jc}	θ_{ja}			Units
			Still Air	1.0 m/s 200 ft/min	2.5 m/s 500 ft/min	
Thin Quad Flat Pack (TQFP)	64	12.0	42.4	36.3	34.0	°C/W
Thin Quad Flat Pack (TQFP)	100	14.0	33.5	27.4	25.0	°C/W