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eZ80190 Development Kit

User Manual

PRELIMINARY

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eZ80190 Development Kit
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Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

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Introduction

The eZ80190 Development Kit provides a general-purpose platform for evaluating the capabilities and operation of ZiLOG's eZ80190 microprocessor. The eZ80F91 Development Kit features two primary boards: the eZ80® Development Platform and the eZ80190 Module. This arrangement provides a full development platform when using both boards. It can also provide a smaller-sized reference platform with the eZ80190 Module as a stand-alone development tool.

Kit Features

The key features of the eZ80190 Development Kit are:

- eZ80® Development Platform:
  - Up to 2MB fast SRAM (12ns access time)
  - Embedded Modem Socket with a U.S. Telephone Line Interface
  - I^2C EEPROM
  - I^2C Configuration Register
  - GPIO Port and Memory Headers
  - LEDs, including a 7x5 LED matrix
  - Jumpers
  - Two RS232 connectors—Console, Modem
  - 9VDC Power Connector
  - RS485 connector[1]
  - JTAG Debug Interface[1]
  - ZiLOG Debug Interface (ZDI)
  - ZiLOG Developer Studio II and the eZ80® C-Compiler

1. The eZ80® Development Platform's RS485 and JTAG functions are not supported on the eZ80190 device.

- eZ80190 Module:
  - eZ80190 device operating at 50MHz
  - 1MB Flash Memory
  - 512KB SRAM
  - 10BaseT Ethernet Interface
  - Real-Time Clock with Battery Back-Up
- ZPAKII Debug Interface Tool
- 4-port 10BaseT Ethernet hub
- eZ80® Software and Documentation CD-ROM

Hardware Specifications

Table 1 lists the specifications of the eZ80® Development Platform.

Table 1. eZ80® Development Platform Hardware Specifications

Operating Temperature:	20ºC ±5ºC
Operating Voltage:	9 VDC

eZ80® Development Platform Overview

The purpose of the eZ80190 Development Kit is to provide the developer with a set of tools for evaluating the features of the eZ80® family of devices, and to be able to develop a new application before building application hardware. The eZ80® Development Platform is designed to accept a number of application-specific modules and eZ80®-based add-on modules, including the eZ80190 Module, which features an Ethernet MAC, a Real-Time Clock, and the eZ80190 microprocessor with a fast Multiply-Accumulate unit.

When attached to the eZ80® Development Platform, the eZ80190 Module can operate in stand-alone mode with Flash memory, or interface via the ZPAK II debug interface tool to a host PC running ZiLOG Developer Studio II Integrated Development Environment (ZDS IDE) software. If the user's eZ80® application demands Internet connectivity and/or a network connection, the eZ80190 microprocessor can serve web pages over a TCP/IP network, allowing easy system monitoring and control, and effortless processor code updates.

The address bus, data bus, and all eZ80190 Module control signals are buffered on the eZ80® Development Platform to provide sufficient drive capability.

A block diagram of the eZ80® Development Platform and the eZ80190 Module is shown in Figure 1.

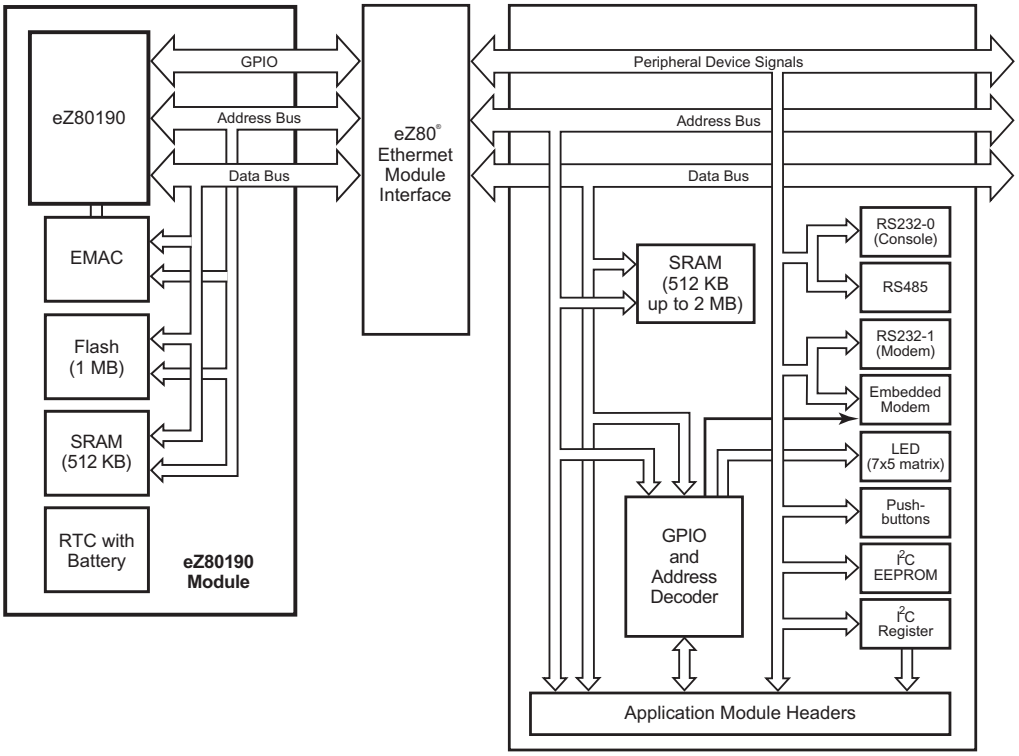
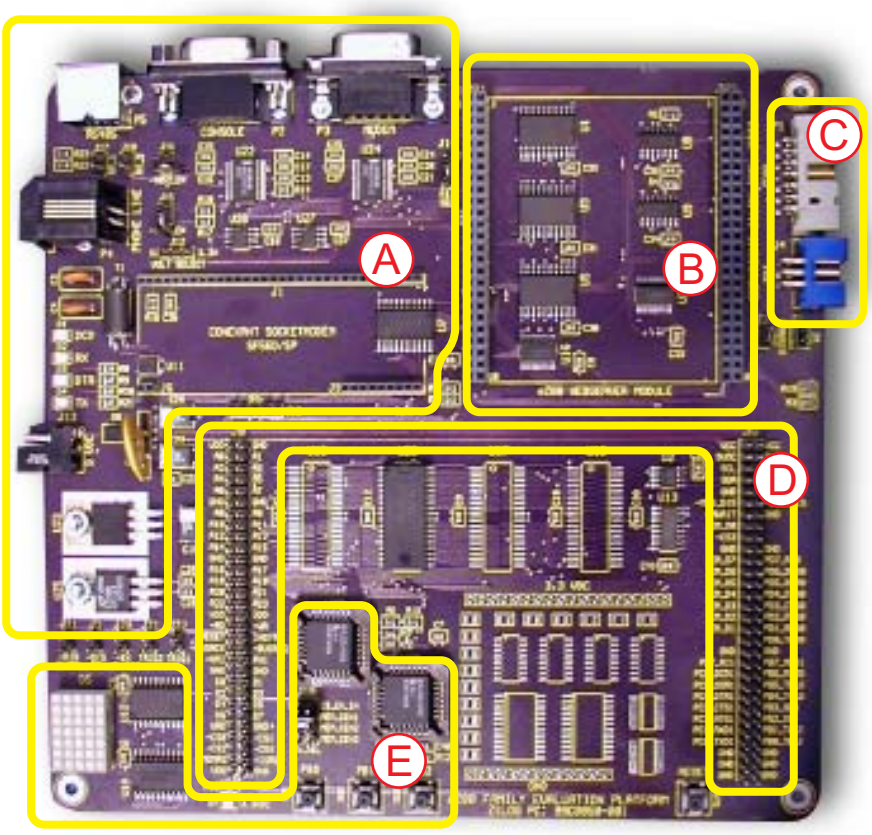


Figure 1. eZ80® Development Platform Block Diagram with eZ80190 Module

Figure 2 is a photographic representation of the eZ80® Development Platform segmented into its key blocks, as shown in the legend for the figure.

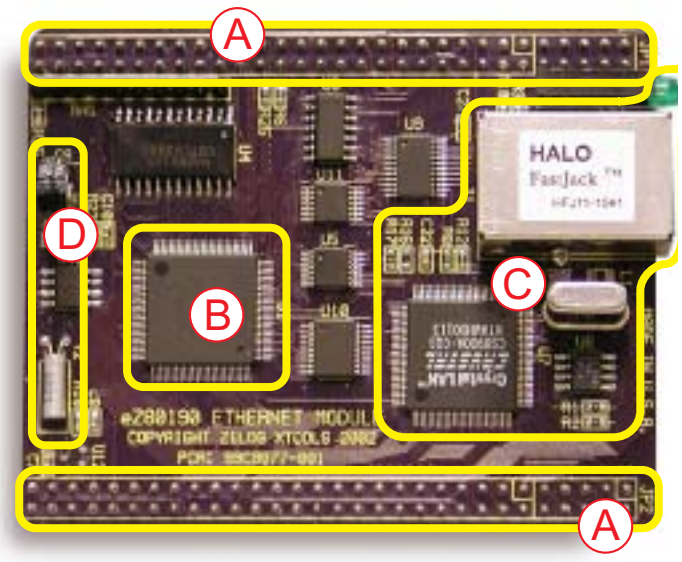


Key to blocks A–E:

A. Power and serial communications.
B. eZ80190 Module interface.
C. Debug interface.
D. Application module interfaces.
E. General-Purpose Port and LED with address decoder.

Figure 2. The eZ80® Development Platform

Figure 3 is a photographic representation of the eZ80190 Module segmented into its key blocks, as shown in the legend for the figure.



Note: Key to blocks A–D.
A. eZ80190 Module interfaces.
B. eZ80190 CPU.
C. 10/100 BaseT Ethernet Interface
D. IrDA transceiver.

Figure 3. The eZ80190 Module

The structures of the eZ80® Development Platform and the eZ80190 Module are illustrated in the Schematic Diagrams starting on page 61.

eZ80® Development Platform

This section describes the eZ80® Development Platform hardware, its key components and its interfaces, including detailed programmer interface information such as memory maps, register definitions, and interrupt usage.

Functional Description

The eZ80® Development Platform consists of seven major hardware blocks. These blocks, listed below, are diagrammed in Figure 4.

- eZ80190 Module interface (2 male headers)
- Power supply for the eZ80® Development Platform, the eZ80190 Module, and application modules
- Application Module interface (2 female headers)
- General-Purpose Port and LED matrix
- RS232 serial communications ports
- Embedded modem interface
- I^2C devices

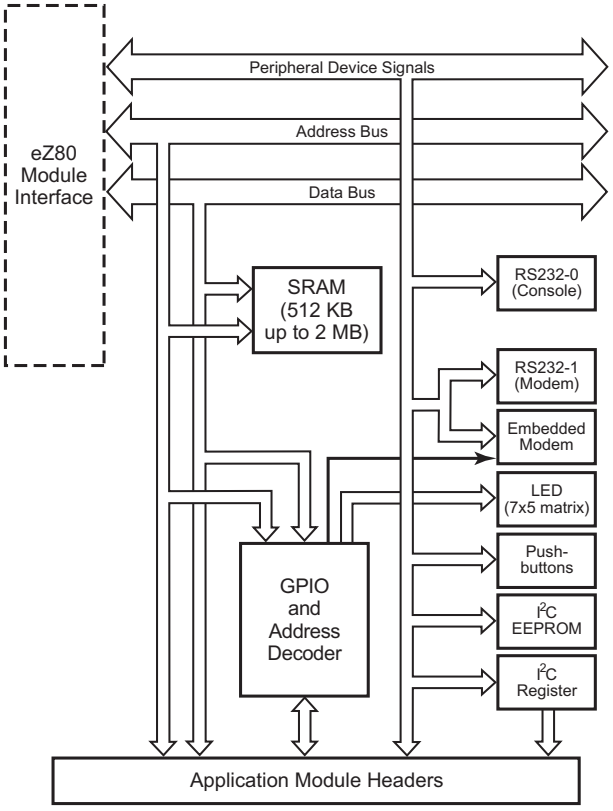


Figure 4. Basic eZ80® Development Platform Block Diagram

Physical Dimensions

The dimensions of the eZ80® Development Platform PCB is 177.8mm x 182.9mm. The overall height is 38.1mm. See Figure 5.

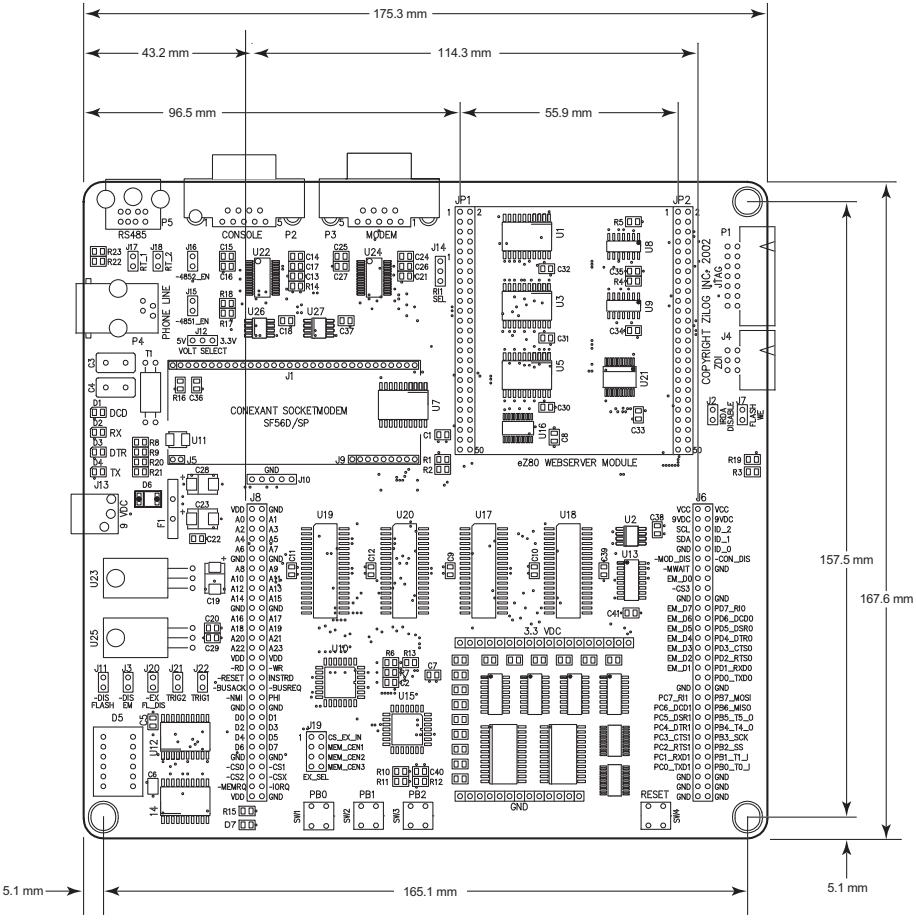


Figure 5. Physical Dimensions of the eZ80® Development Platform

Operational Description

The eZ80® Development Platform can accept any eZ80®-core-based modules, provided that the module interfaces correctly to the eZ80® Development Platform. The purpose of the eZ80® Development Platform is to provide the application developer with a tool to evaluate the features of the eZ80190 device and to develop an application without building additional hardware.

eZ80190 Module Interface

The eZ80190 Module interface provides easy an connection for the eZ80190 Module. This interface is designed to fit future eZ80® modules and user-developed modules using current eZ80® devices.

The eZ80190 Module interface consists of two 50-pin receptacles, JP1 and JP2, which are described in the next pages.

Peripheral Bus Connector (JP1)

Figure 6 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header, located at position JP1 on the eZ80® Development Platform. Table 2 describes the pins and their functions.

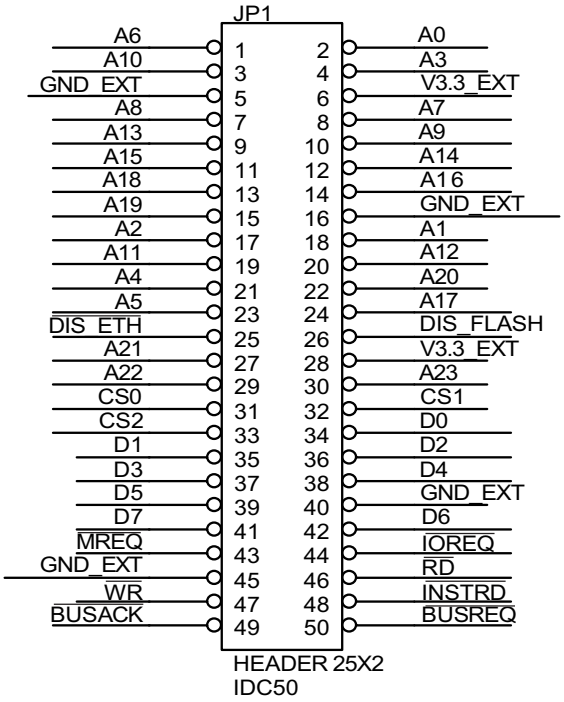


Figure 6. eZ80® Development Platform Peripheral Bus Connector Pin Configuration—JP1

Table 2. eZ80® Development Platform Peripheral Bus Connector Identification—JP1[1]

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V_{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.
2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

**Table 2. eZ80® Development Platform
Peripheral Bus Connector Identification—JP1[1] (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ801900100ZCO Signal[2]
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	$\overline{\text{DIS\_ETH}}$	Output	Low	No
26	$\overline{\text{DIS\_FLASH}}$	Output	Low	No
27	A21	Bidirectional		Yes
28	V_{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80190 Module Schematic Diagrams on pages 66 through 73.
2. The Power and Ground nets are connected directly to the eZ801900100ZCO device.

Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.