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eZ80190

Product Specification

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page Number
December 2008	14	Updated as per latest template and style guide changes. Removed preliminary.	All
March 2006	13	Added registered trademark to eZ80 and eZ80Acclaim	All
February 2004	12	Revised BRG divisor language, UART section	57
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Architectural Overview

General Description

Zilog's eZ80190 microprocessor is a high-speed single-cycle instruction-fetch microprocessor with a clock speed of up to 50 MHz. It is the first of a new set of products based upon Zilog's eZ80® CPU.

The eZ80 CPU is one of the fastest 8-bit CPUs available today, executing code up to four times faster with zero wait-state memory than a standard Z80® operating at the same frequency. This increased processing efficiency can be used to improve available bandwidth or to decrease power consumption.

Considering both the high clock speed and instruction pipeline efficiency, the eZ80 CPU's processing power rivals the performance of 16-bit microprocessors.

Features

The key features of eZ80190 microprocessor are as follows:

- Single-cycle instruction fetch, high-performance eZ80 CPU core[1]
- 16 x 16-bit Multiply and 40-bit Accumulate with 1 KB dual-port SRAM
- Four Chip Selects with individual Wait State generators
- Six Counter/Timers with prescalers
- Watchdog Timer (WDT)
- 2-channel Direct Memory Access (DMA) controller
- 8 KB high-speed data SRAM
- 2 Universal Zilog Interface (UZI) channels (I^2C, SPI, UART) with built-in Baud Rate Generator
- Fixed-priority vectored interrupts (32 external, 11 internal)
- 32 bits of General-Purpose Input/Output (GPIO)
- On-chip oscillator
- 3.0 V to 3.6 V supply voltage with 5 V tolerant inputs
- 100-pin LQFP package

1. For simplicity, the term *eZ80 CPU* is referred to as *CPU* for the bulk of this document.

- Up to 50 MHz clock speed
- Operating Temperature:
  - Standard Temperature Range: 0 ºC to +70 ºC
  - Extended Temperature Range: –40 ºC to +105 ºC
- Zilog Debug Interface (ZDI)

Note: *All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.*

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Block Diagram

Figure 1 on page 3 displays a block diagram of the eZ80190 processor.

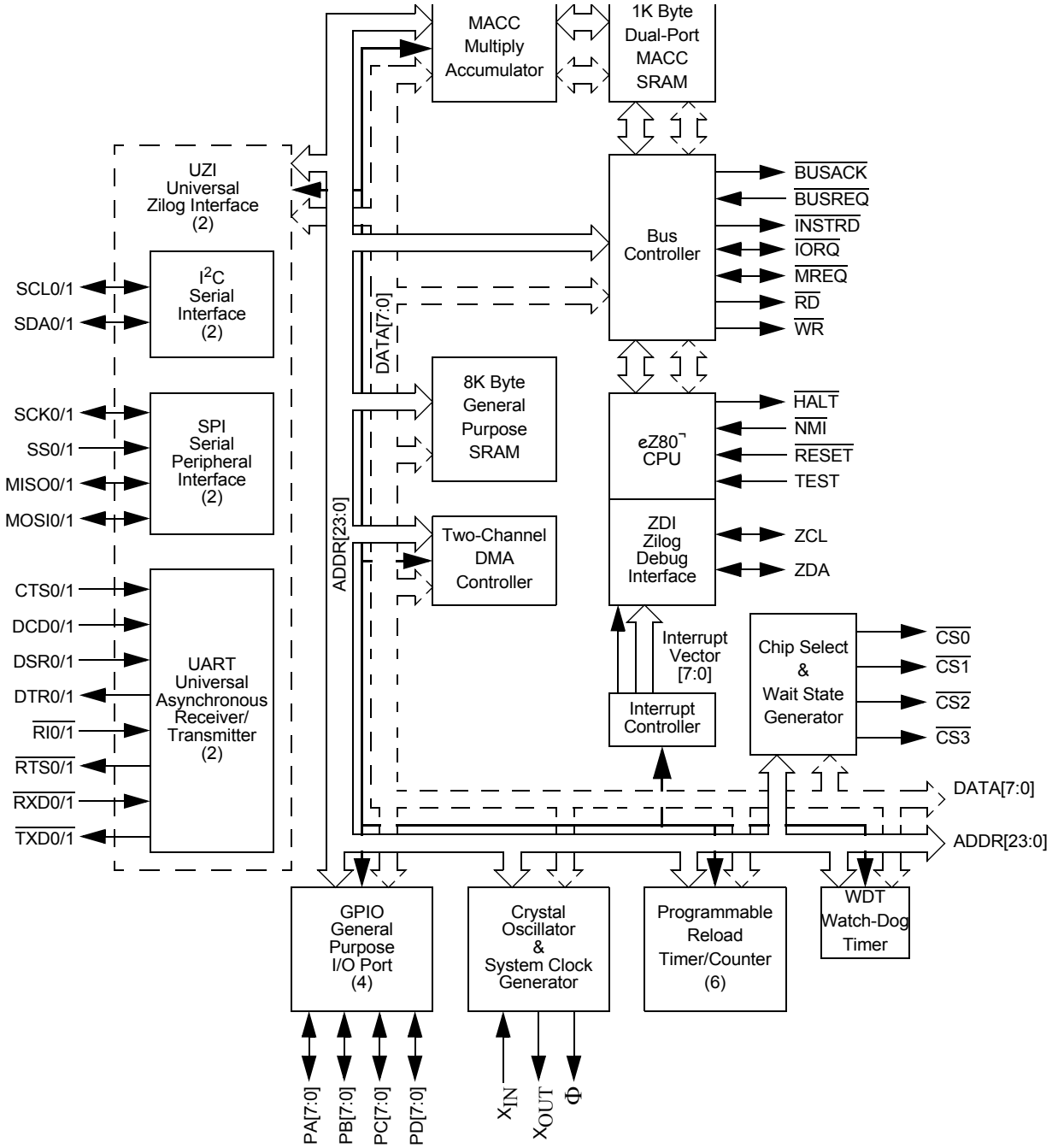

Figure 1. eZ80190 Block Diagram

Pin Description

Figure 2 displays the pin layout of the eZ80190 device in the 100-pin LQFP package. Table 1 on page 5 lists the pins and their functions.

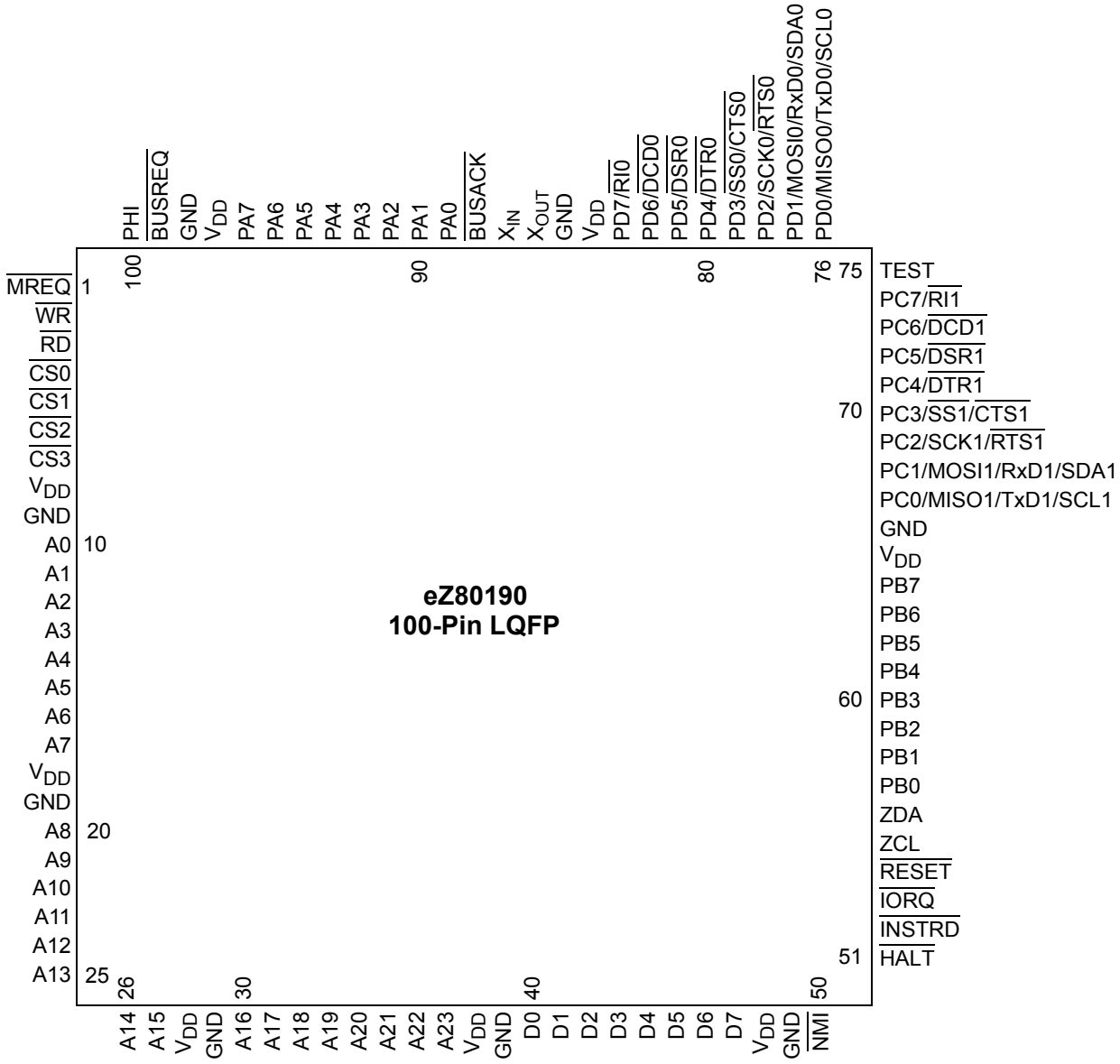

Figure 2. 100-Pin LQFP Configuration of the eZ80190 Device

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device

Pin No.	Symbol	Function	Signal Direction	Description
1	MREQ	Memory Request	Input/Output, Active Low	$\overline{MREQ}$ indicates the CPU is accessing a location in memory. The $\overline{RD}$, $\overline{WR}$, and $\overline{INSTRD}$ signals indicate the type of access. The eZ80190 device does not drive this line during Reset. It is an input in bus acknowledge cycles.
2	WR	Write	Output, Active Low	$\overline{WR}$ indicates the CPU is writing to the current address location. The device accessed is determined by the $\overline{IORQ}$ and $\overline{MREQ}$ pins. The $\overline{WR}$ pin is tristated during bus acknowledge cycles.
3	RD	Read	Output, Active Low	$\overline{RD}$ indicates the eZ80190 device is reading from the current address location. This pin is tristated during bus acknowledge cycles.
4	CS0	Chip Select 0	Output, Active Low	$\overline{CS0}$ indicates access in the defined $\overline{CS0}$ memory or I/O address space. This signal is still driven during bus acknowledge cycles and is generated from the address and control provided on the external pins.
5	CS1	Chip Select 1	Output, Active Low	$\overline{CS1}$ indicates access in the defined $\overline{CS1}$ memory or I/O address space. This signal is still driven during bus acknowledge cycles and is generated from the address and control provided on the external pins.
6	CS2	Chip Select 2	Output, Active Low	$\overline{CS2}$ indicates access in the defined $\overline{CS2}$ memory or I/O address space. This signal is still driven during bus acknowledge cycles and is generated from the address and control provided on the external pins.
7	CS3	Chip Select 3	Output, Active Low	$\overline{CS3}$ indicates access in the defined $\overline{CS3}$ memory or I/O address space. This signal is still driven during bus acknowledge cycles and is generated from the address and control provided on the external pins.
8	V_{DD}	Power Supply		Power Supply
9	GND	Ground		Ground

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
10	ADDR0	Address Bus	Input/Output	The ADDR0 is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
11	ADDR1	Address Bus	Input/Output	The ADDR1 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
12	ADDR2	Address Bus	Input/Output	The ADDR2 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
13	ADDR3	Address Bus	Input/Output	The ADDR3 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
14	ADDR4	Address Bus	Input/Output	The ADDR4 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
15	ADDR5	Address Bus	Input/Output	The ADDR5 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
16	ADDR6	Address Bus	Input/Output	The ADDR6 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
17	ADDR7	Address Bus	Input/Output	The ADDR7 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
18	V_{DD}	Power Supply		Power Supply
19	GND	Ground		Ground
20	ADDR8	Address Bus	Input/Output	The ADDR8 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
21	ADDR9	Address Bus	Input/Output	The ADDR9 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
22	ADDR10	Address Bus	Input/Output	The ADDR10 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
23	ADDR11	Address Bus	Input/Output	The ADDR11 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
24	ADDR12	Address Bus	Input/Output	The ADDR12 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
25	ADDR13	Address Bus	Input/Output	The ADDR13 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
26	ADDR14	Address Bus	Input/Output	The ADDR14 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
27	ADDR15	Address Bus	Input/Output	The ADDR15 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
28	V_{DD}	Power Supply		Power Supply
29	GND	Ground		Ground

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
30	ADDR16	Address Bus	Input/Output	The ADDR16 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
31	ADDR17	Address Bus	Input/Output	The ADDR17 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
32	ADDR18	Address Bus	Input/Output	The ADDR18 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
33	ADDR19	Address Bus	Input/Output	The ADDR19 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
34	ADDR20	Address Bus	Input/Output	The ADDR20 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
35	ADDR21	Address Bus	Input/Output	The ADDR21 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
36	ADDR22	Address Bus	Input/Output	The ADDR22 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
37	ADDR23	Address Bus	Input/Output	The ADDR23 pin is configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. This pin is configured as an input during bus acknowledge cycles. Drives the Chip Select/ Wait State Generator block to generate Chip Selects.
38	V_{DD}	Power Supply		Power Supply
39	GND	Ground		Ground
40	DATA0	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
41	DATA1	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
42	DATA2	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
43	DATA3	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
44	DATA4	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
45	DATA5	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
46	DATA6	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
47	DATA7	Data Bus	Bidirectional, tristate	The data bus transfers data to and from I/O and memory devices. The eZ80190 device drives these lines only during write cycles when the eZ80190 device is the bus master. The data bus is configured as an output in normal operation and as an input during bus acknowledge cycles.
48	V_{DD}	Power Supply		Power Supply
49	GND	Ground		Ground

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
50	NMI	Nonmaskable Interrupt	Schmitt Trigger Input, Active Low	The $\overline{\text{NMI}}$ input is prioritized higher than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external $\overline{\text{NMI}}$ signal is combined with an internal $\overline{\text{NMI}}$ signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU.
51	HALT	Halt	Output, Active Low	A Low on this pin indicates the CPU has stopped because a HALT instruction is executed.
52	INSTRD	Instruction READ	Output, Active Low, tristate	$\overline{\text{INSTRD}}$ (with $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$) indicates the eZ80190 device is fetching an instruction from code memory. The eZ80190 device does not drive this line during Reset or bus acknowledge cycles.
53	IORQ	Input/Output Request	Input/Output, Active Low	$\overline{\text{IORQ}}$ indicates the CPU is accessing a location in I/O space. $\overline{\text{RD}}$ and $\overline{\text{WR}}$ indicate the type of access. The eZ80190 device does not drive this line during Reset and is an input in bus acknowledge cycles.
54	RESET	Reset	Schmitt Trigger Input, Active Low	This signal is used to initialize the eZ80190 device. This input must be Low for a minimum of 3 system clock cycles, and must be held Low until the clock is stable. This input includes a Schmitt trigger to allow RC rise times.
55	ZCL	ZDI Clock	Input with Pull-up	The ZCL pin is used to clock the data between the Zilog Debug Interface and the eZ80190 device. This pin features an internal pull-up.
56	ZDA	ZDI Data	Input/Output, Open-Drain with Pull-up	The ZDA pin is used to transfer data between the Zilog Debug Interface and the eZ80190 device. This pin is open-drain and features an internal pull-up.
57	PB0	GPIO Port B	Input/Output	The PB0 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
58	PB1	GPIO Port B	Input/Output	The PB1 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
59	PB2	GPIO Port B	Input/Output	The PB2 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
60	PB3	GPIO Port B	Input/Output	The PB3 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
61	PB4	GPIO Port B	Input/Output	The PB4 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
62	PB5	GPIO Port B	Input/Output	The PB5 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
63	PB6	GPIO Port B	Input/Output	The PB6 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
64	PB7	GPIO Port B	Input/Output	The PB7 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port B pin, when programmed as an output, can be selected to be an open-drain or open-source output.
65	V_{DD}	Power Supply		Power Supply
66	GND	Ground		Ground
67	PC0	GPIO Port C	Input/Output	The PC0 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as an output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one channel of the UZI interface.
	MISO1	Master In Slave Out	Input/Output	The MISO line is configured as an input when the eZ80190 device is an SPI master device and as an output when eZ80190 device is an SPI slave device. This signal is multiplexed with PC0.
	SCL1	I^2C Serial Clock	Input/Output	The SCL1 pin is used to receive and transmit the I^2C clock. This signal is multiplexed with PC0.
	TxD1	Transmit Data	Output	The TxD1 pin is used by the UART to transmit asynchronous serial data. This signal is multiplexed with PC0.

Table 1. 100-Pin LQFP Pin Identification of the eZ80190 Device (Continued)

Pin No.	Symbol	Function	Signal Direction	Description
68	PC1	GPIO Port C	Input/Output	The PC1 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as an output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one channel of the UZI interface.
	MOSI1	Master Out Slave In	Input/Output	The MOSI line is configured as an output when the eZ80190 device is an SPI master device and as an input when the eZ80190 device is an SPI slave device. This signal is multiplexed with PC1.
	RxD1	Receive Data	Input	The RxD1 pin is used by the UART to receive asynchronous serial data. This signal is multiplexed with PC1.
	SDA1	I^2C Serial Data	Input/Output	The SDA1 pin carries the I^2C data signal. This signal is multiplexed with PC1.
69	PC2	GPIO Port C	Input/Output	The PC2 pin can be used for GPIO. It can be individually programmed as an input or output and can also be used individually as an interrupt input. Each Port C pin, when programmed as an output, can be selected to be an open-drain or open-source output. Port C is multiplexed with one channel of the UZI interface.
	SCK1	SPI Serial Clock	Input/Output	SPI serial clock. This signal is multiplexed with PC2.
	RTS1	Request to Send	Output, Active Low	The $\overline{\text{RTS1}}$ pin carries the modem-control signal from the UART. This signal is multiplexed with PC2.