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eZ80F91 Development Kit

User Manual

PRELIMINARY

UM014205-0203

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Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

Table of Contents

List of Figures

List of Tables

Introduction

The eZ80F91 Development Kit provides a general-purpose platform for evaluating the capabilities and operation of ZiLOG's eZ80F91 microcontroller. The eZ80F91 is a member of ZiLOG's eZ80Acclaim! product family, which offers on-chip Flash capability. The eZ80F91 Development Kit features two primary boards: the eZ80® Development Platform and the eZ80F91 Module. This arrangement provides a full development platform when using both boards. It can also provide a smaller-sized reference platform with the eZ80F91 Module as a stand-alone development tool.

Kit Features

The key features of the eZ80F91 Development Kit are:

- eZ80® Development Platform:
  - Up to 2MB fast SRAM (12ns access time; 1MB factory-installed, with 512KB on module, 512KB on platform)
  - Embedded modem socket with a U.S. telephone line interface
  - I^2C EEPROM
  - I^2C configuration register
  - GPIO, logic circuit, and memory headers
  - Supported by ZiLOG Developer Studio II and the eZ80® C-Compiler
  - LEDs, including a 7x5 LED matrix
  - Platform configuration jumpers
  - Two RS232 connectors—console, modem
  - RS485 connector with cable assembly
  - ZiLOG Debug Interface (ZDI)

  - JTAG Debug Interface
  - 9 VDC power connector
  - Telephone jack
- eZ80F91 Module:
  - eZ80F91 device operating at 50 MHz, with 256 KB of internal Flash memory and 8 KB of internal SRAM memory
  - 512 KB of off-chip SRAM memory
  - 1 MB of off-chip Flash memory (footprint)
  - On-chip Ethernet Media Access Controller (EMAC)
  - Ethernet port
  - IrDA port
  - Real-Time Clock with battery backup
  - Two headers compatible with the eZ80® Development Platform
- ZPAK II Debug Tool
- eZ80® Software and Documentation CD-ROM

Hardware Specifications

Table 1 lists the specifications of the eZ80® Development Platform.

Table 1. eZ80® Development Platform Hardware Specifications

Operating Temperature:	20ºC ±5ºC
Operating Voltage:	9 VDC

eZ80F91 Development Kit Overview

The purpose of the eZ80F91 Development Kit is to provide the developer with a set of tools for evaluating the features of the eZ80F91 microcontroller and to be able to develop a new application before building application hardware.

The eZ80® Development Platform is designed to accept a number of application-specific modules and eZ80®-based add-on modules, including the eZ80F91 Module featured in this kit.

The eZ80® Development Platform, together with its plugged-in eZ80F91 Module, can operate in stand-alone mode with Flash memory, or interface via the ZPAK II Debug Tool to a host PC running ZiLOG Developer Studio II Integrated Development Environment (ZDS IDE) software.

The address bus, data bus, and all eZ80F91 Module control signals are buffered on the eZ80® Development Platform to provide sufficient drive capability.

A block diagram of the eZ80® Development Platform and the eZ80F91 Module is shown in Figure 1.

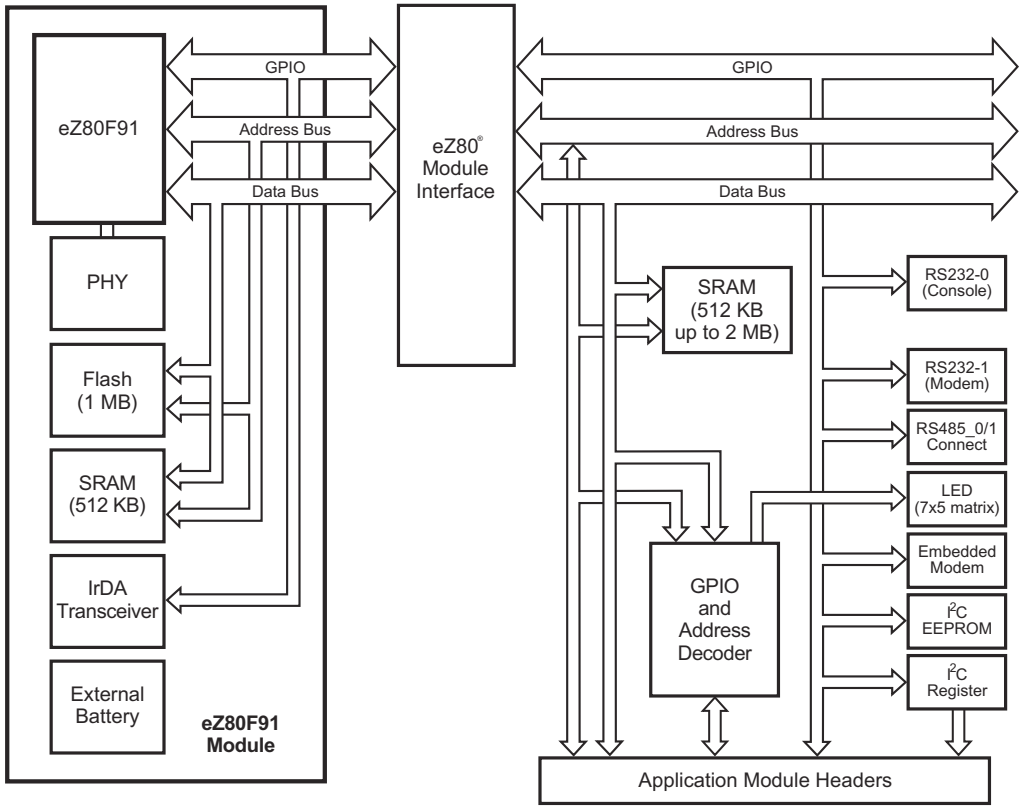
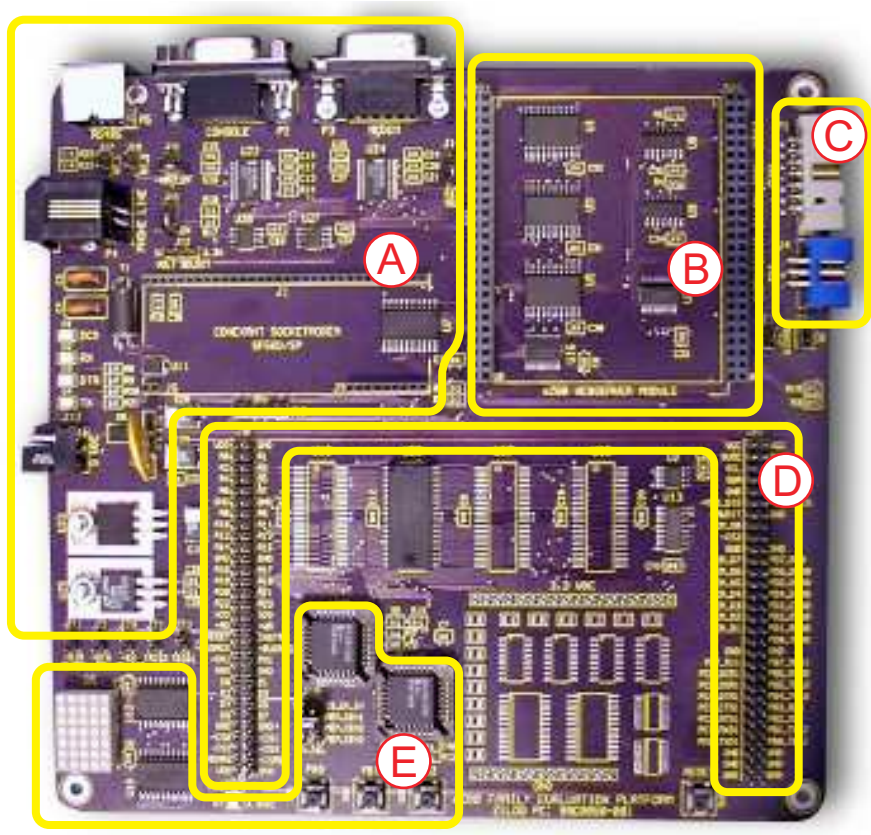


Figure 1. eZ80® Development Platform Block Diagram with eZ80F91 Module

Figure 2 is a photographic representation of the eZ80® Development Platform segmented into its key blocks, as shown in the legend for the figure.

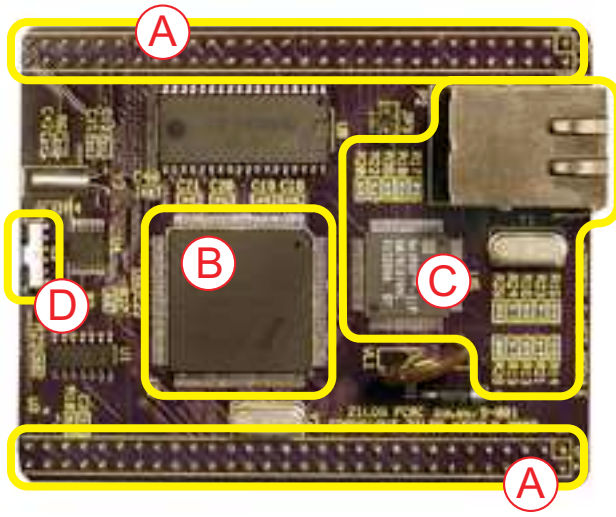


Note: Key to blocks A–E.

A. Power and serial communications.
B. eZ80F91 Module interface.
C. JTAG and ZDI debug interfaces.
D. Application module interfaces.
E. GPIO and LED with Address Decoder.

Figure 2. The eZ80® Development Platform

Figure 3 is a photographic representation of the eZ80F91 Module segmented into its key blocks, as shown in the legend for the figure.



Note: Key to blocks A–C.
A. eZ80F91 Module interfaces.
B. eZ80F91 CPU.
C. 10/100 BaseT Ethernet Interface
D. IrDA transceiver.

Figure 3. The eZ80F91 Module

The structures of the eZ80® Development Platform and the eZ80F91 Module are illustrated in the Schematic Diagrams starting on page 59.

eZ80® Development Platform

This section describes the eZ80® Development Platform hardware, its key components and its interfaces, including programming information such as memory maps and register definitions.

Functional Description

The eZ80® Development Platform consists of seven major hardware blocks. These blocks, listed below, are diagrammed in Figure 4.

- eZ80F91 Module interface (2 female headers)
- Power supply for the eZ80® Development Platform, the eZ80F91 Module, and application modules
- Application Module interface (2 male headers)
- GPIO and LED matrix
- Two RS232 serial communications ports
- Two RS485 ports
- Embedded modem interface
- I^2C devices

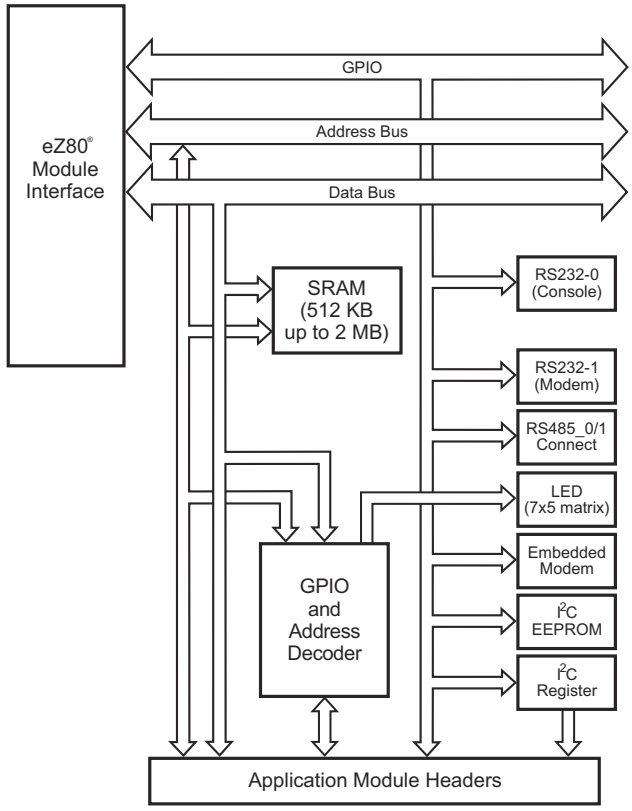


Figure 4. Basic eZ80® Development Platform Block Diagram

Physical Dimensions

The dimensions of the eZ80® Development Platform PCB is 177.8mm x182.9mm. The overall height is 38.1mm. See Figure 5.

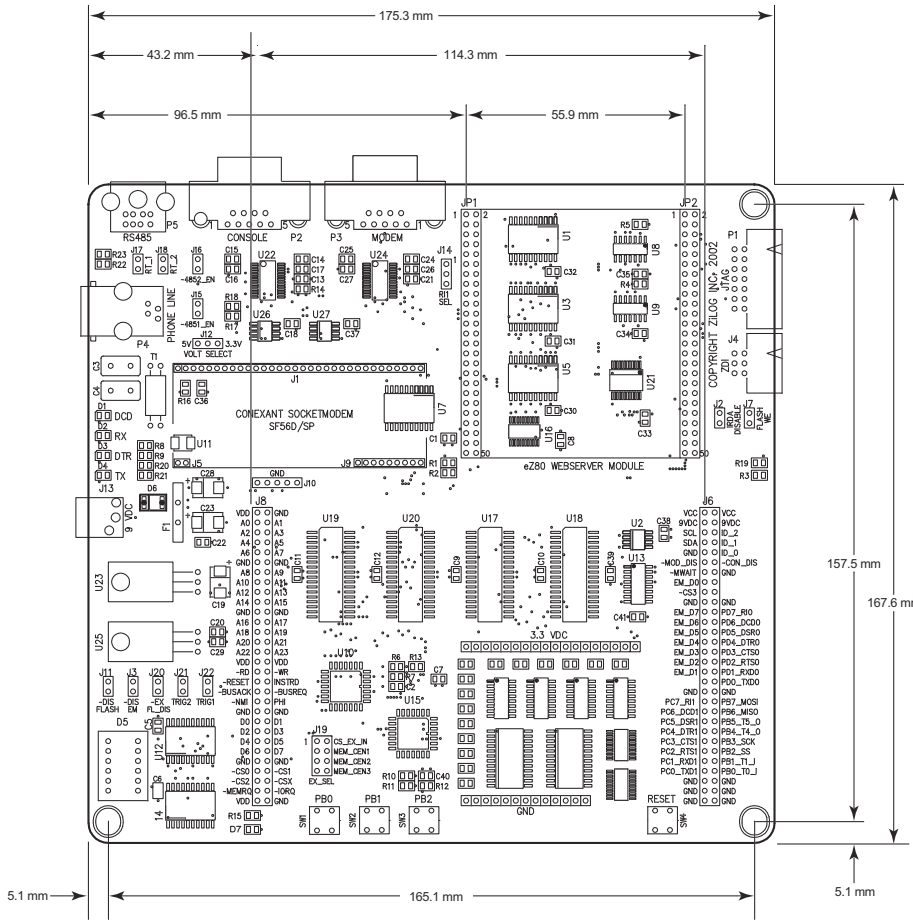


Figure 5. Physical Dimensions of the eZ80® Development Platform

Operational Description

The eZ80® Development Platform can accept any eZ80®-core-based modules, provided that the module interfaces correctly to the eZ80® Development Platform. The purpose of the eZ80® Development Platform is to provide the application developer with a tool to evaluate the features of the eZ80F91, and to develop an application without building additional hardware.

eZ80F91 Module Interface

The eZ80® Development Platform provides an easy interface for connecting each of the development modules in the eZ80® family, including the eZ80F91 Module. The eZ80F91 Module interface consists of two 50-pin receptacles, JP1 and JP2, as described in the pages that follow.

Almost all of these receptacles' signals are connected directly to the CPU. Five input signals, in particular, offer options to the application developer by disabling certain functions of the eZ80F91 Module.

These five input signals[1] are:

- Disable Flash ($\overline{\text{DIS\_Flash}}$)
- Flash Write Enable ($\overline{\text{FlashWE}}$)
- Disable IrDA ($\overline{\text{DIS\_IrDA}}$)
- $\overline{\text{F91\_WE}}$
- RTC_VDD

A description of these five signals follows.

Disable Flash. When active Low, the $\overline{\text{DIS\_Flash}}$ input signal disables the Flash chip on the eZ80F91 Module.

1. These input signals are only used if external Flash memory is present on the eZ80F91 Module. As shipped from the factory, external Flash is not installed.

Flash Write Enable. When active Low, the $\overline{\text{FlashWE}}$ input signal enables write operations on the Flash boot block of the eZ80F91 Module.

Disable IrDA. When the $\overline{\text{DIS\_IrDA}}$ input signal is pulled Low, the IrDA transceiver, located on the eZ80F91 Module, is disabled. As a result, UART0 can be used with the RS232 or the RS485 interfaces on the eZ80® Development Platform.

F91_WE. When the $\overline{\text{F91\_WE}}$ signal is active Low, internal Flash on the eZ80F91 Module is enabled for writing. This signal is inverted from the $\overline{\text{WP}}$ signal of on the eZ80F91 Module.

RTC_VDD. RTC_VDD is a test point for the Real Time Clock power supply.

Peripheral Bus Connector

Figure 6 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header, located at position JP1 on the eZ80® Development Platform. Table 2 identifies the pins and their functions.

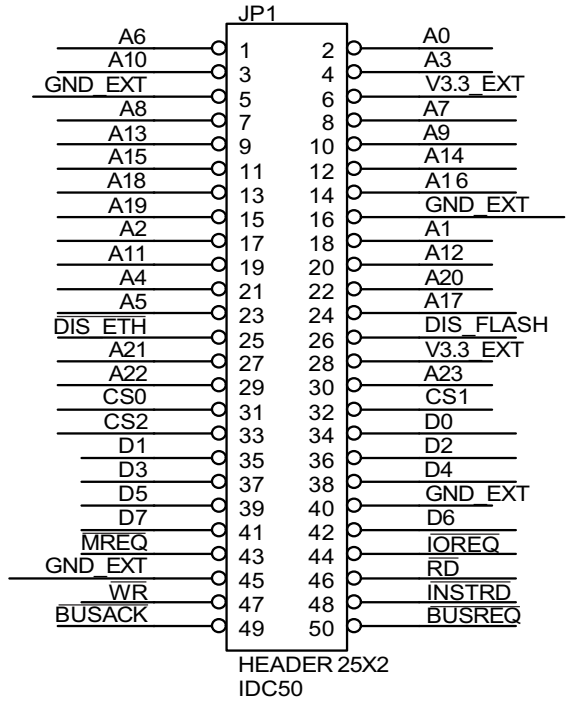


Figure 6. eZ80® Development Platform Peripheral Bus Connector Pin Configuration—JP1

Table 2. eZ80® Development Platform Peripheral Bus Connector Identification—JP1[1,3]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V_{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics on pages 64 through 66.
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Table 2. eZ80® Development Platform Peripheral Bus Connector Identification—JP1[1,3] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	$\overline{\text{DIS\_ETH}}$	Output	Low	No
26	$\overline{\text{DIS\_FLASH}}$	Output	Low	No
27	A21	Bidirectional		Yes
28	V_{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics on pages 64 through 66.
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

Table 2. eZ80® Development Platform Peripheral Bus Connector Identification—JP1[1,3] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
31	CS0	Input	Low	Yes
32	CS1	Input	Low	Yes
33	CS2	Input	Low	Yes
34	D0	Bidirectional		Yes
35	D1	Bidirectional		Yes
36	D2	Bidirectional		No
37	D3	Bidirectional		Yes
38	D4	Bidirectional		Yes
39	D5	Bidirectional		Yes
40	GND			
41	D7	Bidirectional		Yes
42	D6	Bidirectional		Yes
43	$\overline{\text{MREQ}}$	Bidirectional	Low	Yes
44	$\overline{\text{IORQ}}$	Bidirectional	Low	Yes
45	GND			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics on pages 64 through 66.
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on RD, WR, IORQ, MREQ, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80 CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.