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zilog

eZ80Acclaim!® Microcontrollers

eZ80F91 Development Kit

User Manual

UM014220-0508

Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page No
May 2008	20	Updated Figure 24 and Figure 25. Updated Zilog logo, Zilog text, Disclaimer section.	63 and 64
June 2007	19	Introduction, eZ80F91 Module, ZDS II. 9 VDC power supply replaced with 6 VDC power supply on later builds. Windows Vista added.	2, 1, 55
April 2007	18	No changes to content.	
April 2007	17	Introduction and Troubleshooting. Updated user interfaces for ZDS II and how to download code.	55, 56
June 2006	16	Introduction. Added section covering board hardware revision history.	2

Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: *Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).*

Table of Contents

Introduction

Zilog's eZ80F91 Development Kit provides a general-purpose platform for evaluating the capabilities and operation of eZ80F91 microcontroller. The eZ80F91 is a member of eZ80Acclaim!® product family, which offers on-chip Flash capability. The eZ80F91 Development Kit features two primary boards: the eZ80Acclaim! Development Kit and the eZ80F91 Module. This arrangement provides a full development platform when using both the boards. It can also provide a smaller-sized reference platform with the eZ80F91 Module as a stand-alone development tool.

Kit Features

The key features of the eZ80F91 Development Kit include:

- eZ80Acclaim! Development Kit:
  - Up to 2 MB fast SRAM (12 ns access time; 1 MB factory-installed, with 512 KB on module, 512 KB on platform)
  - Embedded modem socket with a U.S. telephone line interface
  - I^2C EEPROM
  - I^2C configuration register
  - GPIO, logic circuit, and memory headers
  - Supported by Zilog Developer Studio II and the eZ80® C-Compiler
  - LEDs, including a 7x5 LED matrix
  - Platform configuration jumpers
  - Two RS-232 connectors—console, modem
  - RS-485 connector with cable assembly
  - Zilog Debug Interface (ZDI)
  - JTAG Debug Interface

  - 9 VDC power connector
  - Telephone jack
- eZ80F91 Module:
  - eZ80F91 device operating at 50 MHz, with 256 KB of internal Flash memory and 8 KB of internal SRAM memory
  - 512 KB of off-chip SRAM memory
  - 1 MB of off-chip Flash memory (footprint)
  - On-chip Ethernet Media Access Controller (EMAC)
  - Ethernet port
  - IrDA port
  - Real-Time Clock with battery backup
  - Two headers compatible with the eZ80Acclaim!® Development Kit
- ZPAK II Debug Tool
- eZ80Acclaim! Software and Documentation CD-ROM

Hardware Specifications

Table 2 lists the specifications of the eZ80Acclaim! Development Kit.

Table 2. eZ80Acclaim!® Development Kit Hardware Specifications

Operating Temperature	20 ºC±5 ºC
Operating Voltage	9 VDC (on earlier builds supplied with a 9 VDC power supply) 6 VDC (on later builds supplied with 6 VDC power supply)

eZ80F91 Development Board Revision History

99C0858-001 Rev C or later

10/20/03—Updated layout and added reset fix.

05/30/06—The following components are not populated on the board:

- U11: Triac, SCR Phone Line D0-214
- U26 and U27: IC RS485, XCVR, Low PWR, 8-SOIC
- C3 and C4: CAP 1000 pF Ceramic Disc 1 KV
- D1 and D3: Diode LED Amber 0805 SMT
- T1: Inductor Ferrite Bead, 2x15 Turns
- J1: Conn HDR/Pin 1x32 2 mm socket
- J5: Conn HDR/Pin 1x2 2 mm socket
- J9: Conn HDR/Pin 1x9 2 mm socket
- P4: Conn RJ14 Jack 6-Pos 4-CKT
- P5: Conn 9-CKT Cir rt-angl PC Mount

eZ80F91 Development Kit Overview

The purpose of the eZ80F91 Development Kit is to provide a set of tools for evaluating the features of the eZ80F91 microcontroller and to be able to develop a new application before building application hardware.

The eZ80Acclaim!® Development Kit is designed to accept a number of application-specific modules and eZ80Acclaim!-based add-on modules, including the eZ80F91 Module featured in this kit.

The eZ80Acclaim! Development Kit, together with its plugged-in eZ80F91 Module, can operate in stand-alone mode with Flash memory, or interface via the ZPAK II Debug Tool or USB Smart Cable (ZUSBSC0100ZACG) to a host PC running Zilog Developer Studio II Integrated Development Environment (ZDS II IDE) software.

The address bus, data bus, and all eZ80F91 Module control signals are buffered on the eZ80Acclaim! Development Kit to provide sufficient drive capability.

A block diagram of the eZ80Acclaim! Development Kit and the eZ80F91 Module is shown in Figure 1.

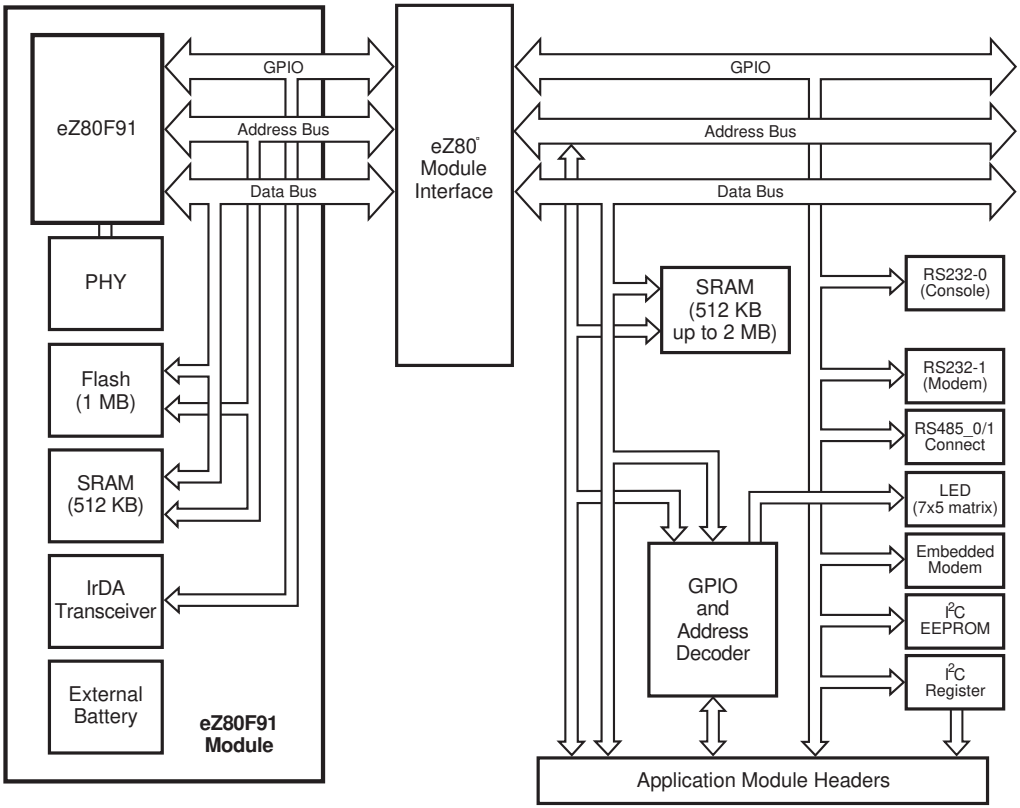
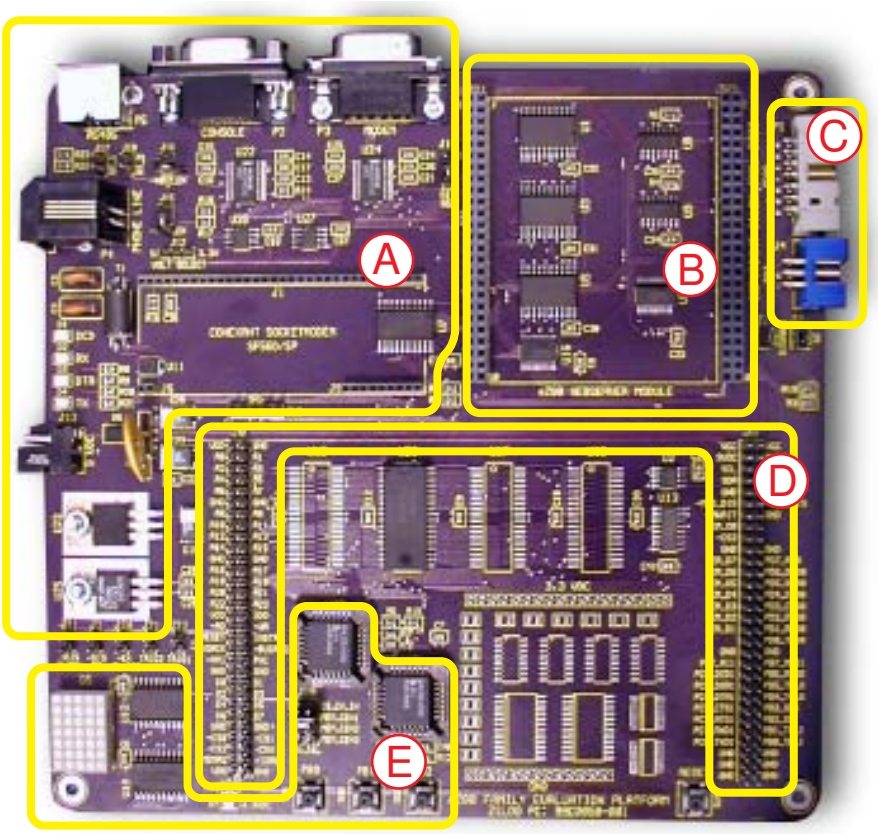


Figure 1. eZ80Acclaim!® Development Kit Block Diagram with eZ80F91 Module

Figure 2 on page 5 displays eZ80Acclaim!® Development Kit segmented into its key blocks, as shown in the legend for the figure.



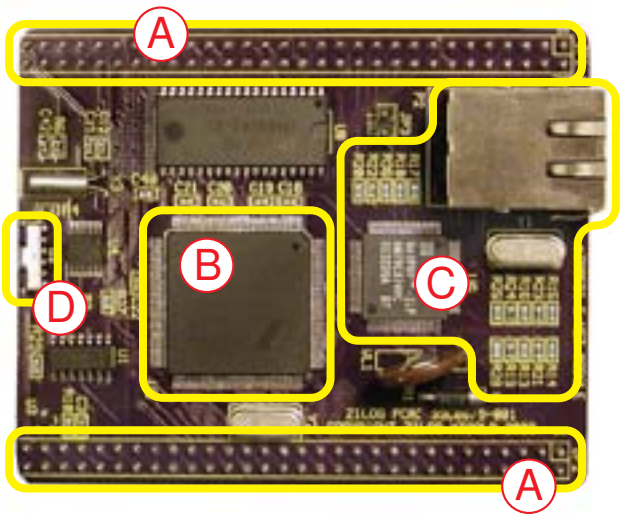
Note: The above is an example only and might have a different configuration. See Table 2.

Key to blocks A–E:

A. Power and serial communications
B. eZ80F91 Module interface
C. JTAG and ZDI debug interfaces
D. Application module interfaces
E. GPIO and LED with Address Decoder

Figure 2. The eZ80Acclaim!® Development Kit

Figure 3 displays the eZ80F91 Module segmented into its key blocks, as shown in the legend for the figure.



Note: Key to blocks A–C.
A. eZ80F91 Module interfaces.
B. eZ80F91 CPU.
C. 10/100 BaseT Ethernet Interface
D. IrDA transceiver.

Figure 3. The eZ80F91 Module

The structures of the eZ80Acclaim!® Development Kit and the eZ80F91 Module are displayed in the Schematics on page 57.

eZ80 Development Kit

This section describes the eZ80Acclaim!® Development Kit hardware, its key components and its interfaces, including programming information such as memory maps and register definitions.

Functional Description

The eZ80Acclaim! Development Kit consists of seven major hardware blocks. These blocks are listed below (see Figure 4 on page 8).

- eZ80F91 Module interface (2 female headers)
- Power supply for the eZ80Acclaim! Development Kit, the eZ80F91 Module, and application modules
- Application Module interface (2 male headers)
- GPIO and LED matrix
- Two RS-232 serial communications ports
- Two RS-485 ports
- Embedded modem interface
- I^2C devices

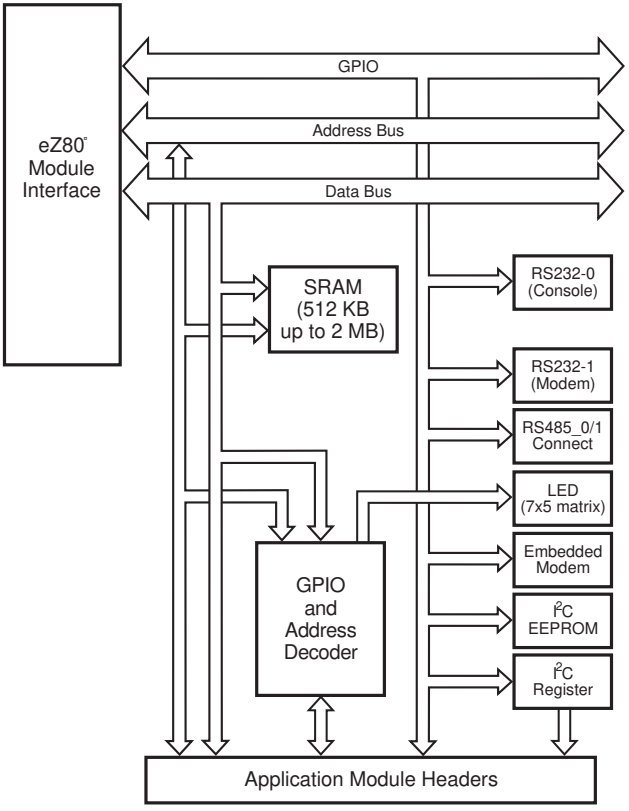


Figure 4. Basic eZ80Acclaim!® Development Kit Block Diagram

Physical Dimensions

The dimensions of the eZ80Acclaim!® Development Kit PCB is 177.8 mm x 182.9 mm. The overall height is 38.1 mm. See Figure 5.

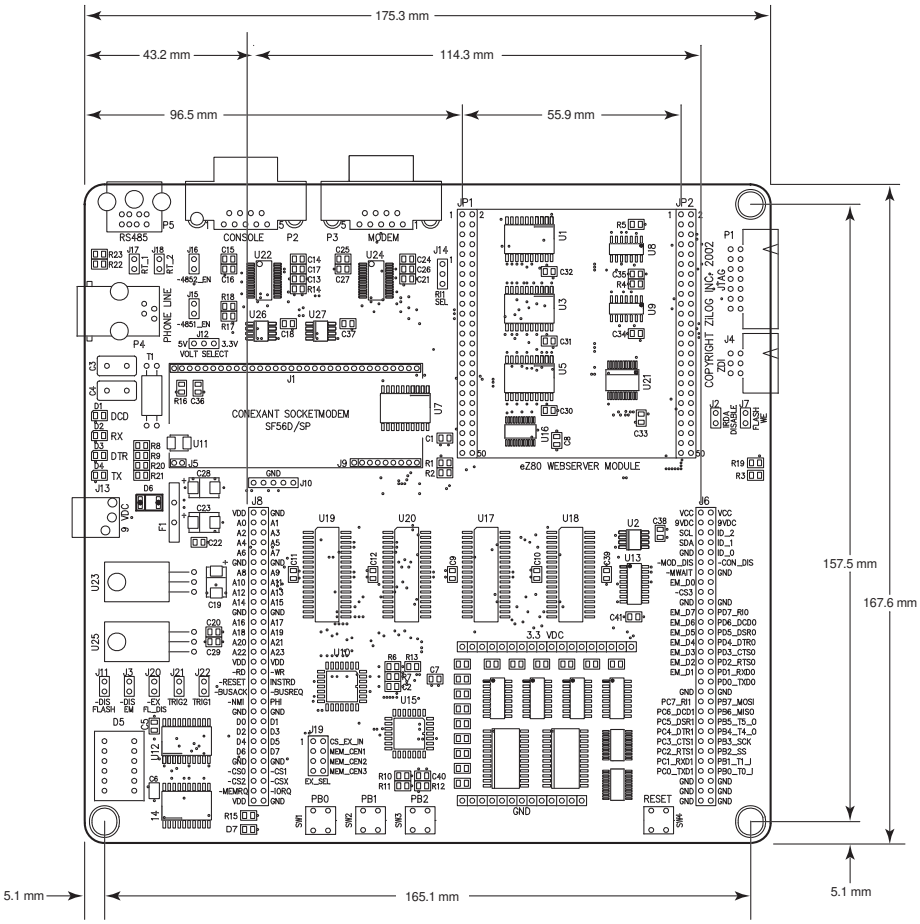


Figure 5. Physical Dimensions of the eZ80Acclaim!® Development Kit

Operational Description

The eZ80Acclaim!® Development Kit can accept any eZ80®-core-based modules, provided that the module interfaces correctly to the eZ80Acclaim! Development Kit. The purpose of the eZ80Acclaim! Development Kit is to provide you a tool to evaluate the features of the eZ80F91 device, and to develop an application without building additional hardware.

eZ80F91 Module Interface

The eZ80Acclaim! Development Kit provides an easy interface for connecting each of the development modules in the eZ80Acclaim! family, including the eZ80F91 Module. The eZ80F91 Module interface consists of two 50-pin receptacles, JP1 and JP2; a third receptacle, JP3, enables the programming of internal on-chip Flash memory.

Almost all these receptacles' signals are connected directly to the CPU. Five input signals, in particular, offer you options by disabling certain functions of the eZ80F91 Module.

These five input signals[1] are:

- Enable Flash ($\overline{\text{EN\_Flash}}$)
- Flash Write Enable ($\overline{\text{FlashWE}}$)
- Disable IrDA ($\overline{\text{DIS\_IrDA}}$)
- $\overline{\text{F91\_WE}}$
- RTC_V_{DD}

1. These input signals are only used if external Flash memory is present on the eZ80F91 Module. As shipped from the factory, external Flash is not installed.

The description of these five signals are provided below.

Enable Flash—When active Low, the $\overline{\text{EN\_Flash}}$ input signal enables the Flash chip on the eZ80F91 Module.

Flash Write Enable—When active Low, the $\overline{\text{FlashWE}}$ input signal enables write operations on the Flash boot block of the eZ80F91 Module.

Disable IrDA—When the $\overline{\text{DIS\_IrDA}}$ input signal is pulled Low, the IrDA transceiver, located on the eZ80F91 Module, is disabled. As a result, UART0 can be used with the RS-232 or the RS-485 interfaces on the eZ80Acclaim!® Development Kit.

F91_WE—When the $\overline{\text{F91\_WE}}$ signal is active Low, internal Flash on the eZ80F91 Module is enabled for writing. This signal is inverted from the $\overline{\text{WP}}$ signal of on the eZ80F91 Module.

RTC_V_{DD}—RTC_V_{DD} is a test point for the Real Time Clock power supply.

Peripheral Bus Connector

Figure 6 displays the pin layout of the Peripheral Bus Connector in the 50-pin header, located at position JP1 on the eZ80Acclaim! Development Kit. Table 3 on page 13 lists the pins and their functions.

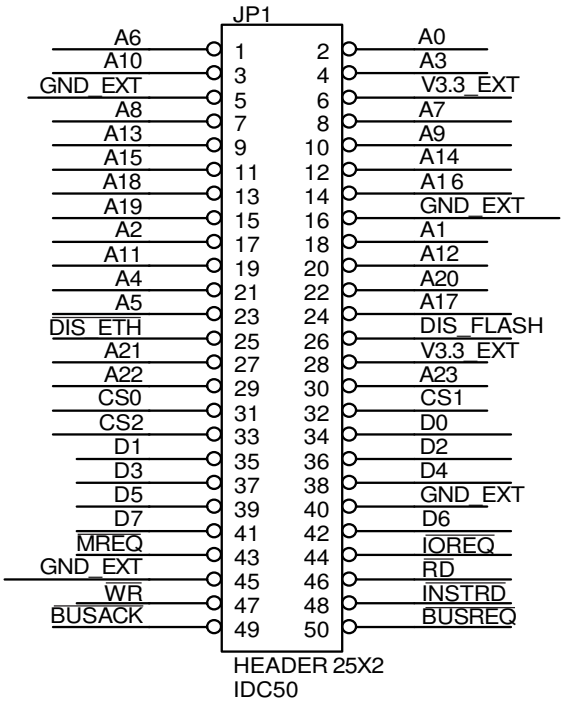


Figure 6. eZ80Acclaim!® Development Kit Peripheral Bus Connector Pin Configuration—JP1

Table 3. eZ80Acclaim!® Development Kit Peripheral Bus Connector Identification—JP1[1,3]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V_{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes

Table 3. eZ80Acclaim!® Development Kit Peripheral Bus Connector Identification—JP1[1,3] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	$\overline{\text{DIS\_ETH}}$	Output	Low	No
26	$\overline{\text{EN\_Flash}}$	Output	Low	No
27	A21	Bidirectional		Yes
28	V_{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes
31	CS0	Input	Low	Yes
32	CS1	Input	Low	Yes
33	CS2	Input	Low	Yes
34	D0	Bidirectional		Yes
35	D1	Bidirectional		Yes
36	D2	Bidirectional		No
37	D3	Bidirectional		Yes
38	D4	Bidirectional		Yes
39	D5	Bidirectional		Yes
40	GND			
41	D7	Bidirectional		Yes
42	D6	Bidirectional		Yes
43	$\overline{\text{MREQ}}$	Bidirectional	Low	Yes
44	$\overline{\text{IORQ}}$	Bidirectional	Low	Yes

Table 3. eZ80Acclaim!® Development Kit Peripheral Bus Connector Identification—JP1[1,3] (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
45	GND			
46	$\overline{RD}$	Bidirectional	Low	Yes
47	$\overline{WR}$	Bidirectional	Low	Yes
48	$\overline{INSTRD}$	Input	Low	Yes
49	$\overline{BUSACK}$	Input	Pull-Up 10 kΩ; Low	Yes
50	$\overline{BUSREQ}$	Output	Pull-Up 10 kΩ; Low	Yes

Notes

1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics, see Figure 23 through Figure 25.
2. The Power and Ground nets are connected directly to the eZ80F91 device.
3. Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91's Peripheral Power-Down Register.

I/O Connector

Figure 7 displays the pin layout of the I/O Connector in the 50-pin header, located at position JP2 on the eZ80Acclaim!® Development Kit. Table 4 on page 17 identifies the pins and their functions.

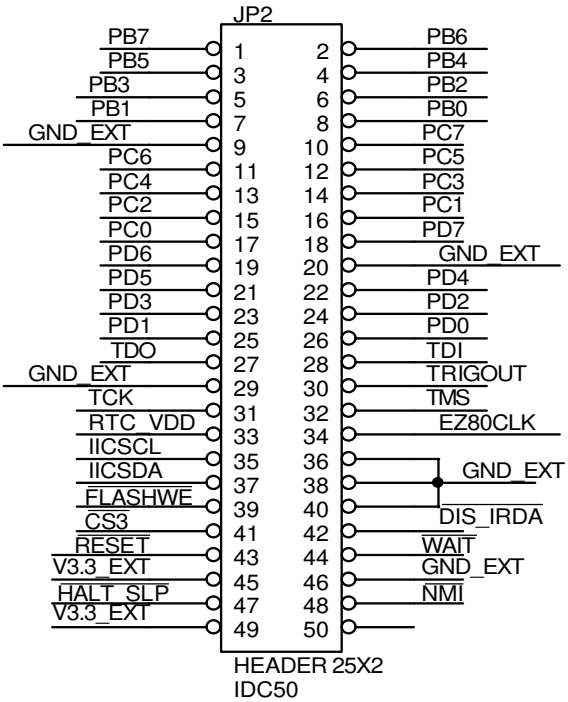


Figure 7. eZ80Acclaim!® Development Kit I/O Connector Pin Configuration—JP2

Table 4. eZ80Acclaim!® Development Kit I/O Connector Identification—JP2[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
1	PB7	Bidirectional		Yes
2	PB6	Bidirectional		Yes
3	PB5	Bidirectional		Yes
4	PB4	Bidirectional		Yes
5	PB3	Bidirectional		Yes
6	PB2	Bidirectional		Yes
7	PB1	Bidirectional		Yes
8	PB0	Bidirectional		Yes
9	GND			
10	PC7	Bidirectional		Yes
11	PC6	Bidirectional		Yes
12	PC5	Bidirectional		Yes
13	PC4	Bidirectional		Yes
14	PC3	Bidirectional		Yes
15	PC2	Bidirectional		Yes
16	PC1	Bidirectional		Yes
17	PC0	Bidirectional		Yes
18	PD7	Bidirectional		Yes
19	PD6	Bidirectional		
20	GND			
21	PD5	Bidirectional		Yes
22	PD4	Bidirectional		Yes
23	PD3	Bidirectional		Yes

Table 4. eZ80Acclaim!® Development Kit I/O Connector Identification—JP2[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
24	PD2	Bidirectional		Yes
25	PD1	Bidirectional		Yes
26	PD0	Bidirectional		Yes
27	TDO	Input		Yes
28	TDI/ZDA	Output		Yes
29	GND			
30	TRIGOUT	Input	High	
31	TCK/ZCL	Output		Yes
32	TMS	Output	High	Yes
33	RTC_V_{DD}			
34	EZ80CLK	Input		Yes
35	SCL	Bidirectional		Yes
36	GND			
37	SDA	Bidirectional		Yes
38	GND			
39	$\overline{\text{FlashWE}}$	Output	Low	No
40	GND			
41	$\overline{\text{CS3}}$	Input	Low	Yes
42	$\overline{\text{DIS\_IrDA}}$	Output	Low	No
43	$\overline{\text{RESET}}$	Bidirectional	Low	Yes
44	$\overline{\text{WAIT}}$	Output	Pull-Up 10 kΩ; Low	Yes
45	V_{DD}			
46	GND			

Table 4. eZ80Acclaim!® Development Kit I/O Connector Identification—JP2[1]

Pin #	Symbol	Signal Direction	Active Level	eZ80F91 Signal[2]
47	$\overline{\text{HALT\_SLP}}$	Input	Low	Yes
48	$\overline{\text{NMI}}$	Output	Low	Yes
49	V_{DD}			
50	Reserved			

Notes
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F91 Module Schematics, see Figure 23 through Figure 25.
2. The Power and Ground nets are connected directly to the eZ80F91 device.

Internal On-Chip Flash Memory

To program internal on-chip Flash memory, the JP3 shunt must be installed. Table 5 lists the setting for the JP3 jumper that is resident on the eZ80F91 Module.

Table 5. Jumper, eZ80F91 Module

Symbol	Jumper Name	Shunt Status	Function	Affected Device
JP3	Write Enable (WR_EN)	In	On-chip Flash is enabled for writing.	On-chip Flash
		Out	On-chip Flash memory is write-protected.	On-chip Flash

Application Module Interface

An Application Module Interface is provided to allow you to add an application-specific module to the eZ80Acclaim!® Development Kit. Zilog's

Thermostat Application Module (not provided in the kit) is an example of an application-specific module that demonstrates an HVAC control system. Implementing an application module with the Application Module Interface requires that the eZ80F91 Module also be mounted on the eZ80Acclaim! Development Kit, because the eZ80F91 device controls the application. To mount an application module, use the two male headers J6 and J8.

Connector J6 carries the General-Purpose Input/Output ports (GPIO), and connector J8 carries memory and control signals. To design an application module, you must be familiar with the architecture and features of the eZ80F91 Module currently installed. Table 6 and Table 7 list the signals and functions related to each of these connectors by pin. Power and ground signals are omitted for the sake of simplicity.

Table 6. GPIO Connector J6*

Signal	Pin #	Function	Direction	Notes
SCL	5	I^2C Clock	IN/OUT	
SDA	7	I^2C Data	IN/OUT	
MOD_DIS	9	Modem Disable	IN	If a shunt is installed between pins 6 and 9, the modem function on the eZ80Acclaim!® Development Kit is disabled.
MWAIT	13	WAIT signal for the CPU	IN	
EM_D0	15	Emulated, Bit 0	IN/OUT	
$\overline{CS3}$	17	Chip Select 3 of the CPU	OUT	This signal is also present on the J8.
EM_D[7:1]	21,23,25, 27,29,31, 33	Emulated, Bit [7:1]	IN/OUT	
Reserved	35			