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eZ80Acclaim!™/ eZ80Acclaim*Plus!*™ Ethernet Modules

Product Specification

PS030603-1013

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Revision History

Each instance in the following revision history table reflects a change to this document from its previous version. For more details, refer to the corresponding pages or appropriate links provided in the table.

Date	Revision Level	Description	Page Number
Oct 2013	03	Corrected erroneous part number listed f or the eZ80Acclaim*Plus!* Development Kit, Ordering Information chapter.	17
May 2013	02	Updated to include ordering information for the eZ80F915150MODG and eZ80F917150MODG parts.	17
Mar 2013	01	Original issue.	All

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eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Modules

Zilog's eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Modules are compact, high-performance devices specially designed for the rapid development and deployment of embedded systems requiring control and internet/intranet connectivity.

These expandable modules are powered by Zilog's power-efficient, optimized-pipeline-architecture eZ80F91 MCU, a member of Zilog's eZ80Acclaim*Plus!*™ family. The eZ80F91 MCU is a high-speed, single-cycle instruction-fetch microcontroller that operates with a clock speed of 50MHz. It can also operate in Z80®-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of these eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Modules make them suitable for a variety of applications, including industrial control, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Features

Zilog's eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Modules offer the following features:

- Factory-default operating clock frequency at 50MHz
- 10/100 Base-T Ethernet PHY with RJ45 connector
- 512KB off-chip fast SRAM
- 8MB off-chip NOR Flash memory
- 32Mbit serial Flash memory with SPI interface
- Battery for on-chip Real-Time Clock
- Input/Output connector (J2) which provides 32 general-purpose 5V-tolerant I/O pinouts
- Onboard connector provides I/O bus for external peripheral connections (IRQ, $\overline{CS}$, 24 address, 8 data)
- Low-cost connection to carrier board via two 2x30 pin headers
- Small footprint 63.5mm x 78.7mm
- 3.3V power supply
- Standard operating temperature range: 0ºC to +70ºC

eZ80Acclaim!™/eZ80AcclaimPlus!™ MCU Features

The eZ80Acclaim!™/eZ80AcclaimPlus!™ MCUs offer the following features:

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- 256 KB of Flash memory and 8 KB of SRAM
- 10/100 Mbps Ethernet MAC with 8 KB frame buffer
- Low power features including SLEEP Mode, HALT Mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators and support for 9-bit operation
- SPI with independent clock generator
- I^2C with independent clock generator
- Infrared data association (IrDA)-compliant infrared encoder/decoder
- New DMA-like eZ80 instructions for efficient block data transfer
- External interface with four chip selects, individual wait state generators, and an external WAIT input pin; supports Intel- and Motorola-style buses
- Flexible-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32 kHz oscillator, selectable 50/60 Hz input, and separate V_{DD} pin for battery backup
- Four 16-bit Counter/Timers with prescalers and direct input/output drive
- Watchdog Timer (WDT)
- 32 bits of general-purpose input/output (GPIO)
- JTAG and ZDI debug interfaces
- 144-pin BGA or 144-pin LQFP package
- Supply voltage of 3.0 V to 3.6 V with 5 V-tolerant inputs
- Standard operating temperature range: 0 ºC to +70 ºC

Block Diagram

Figure 1 presents a block diagram of the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module.

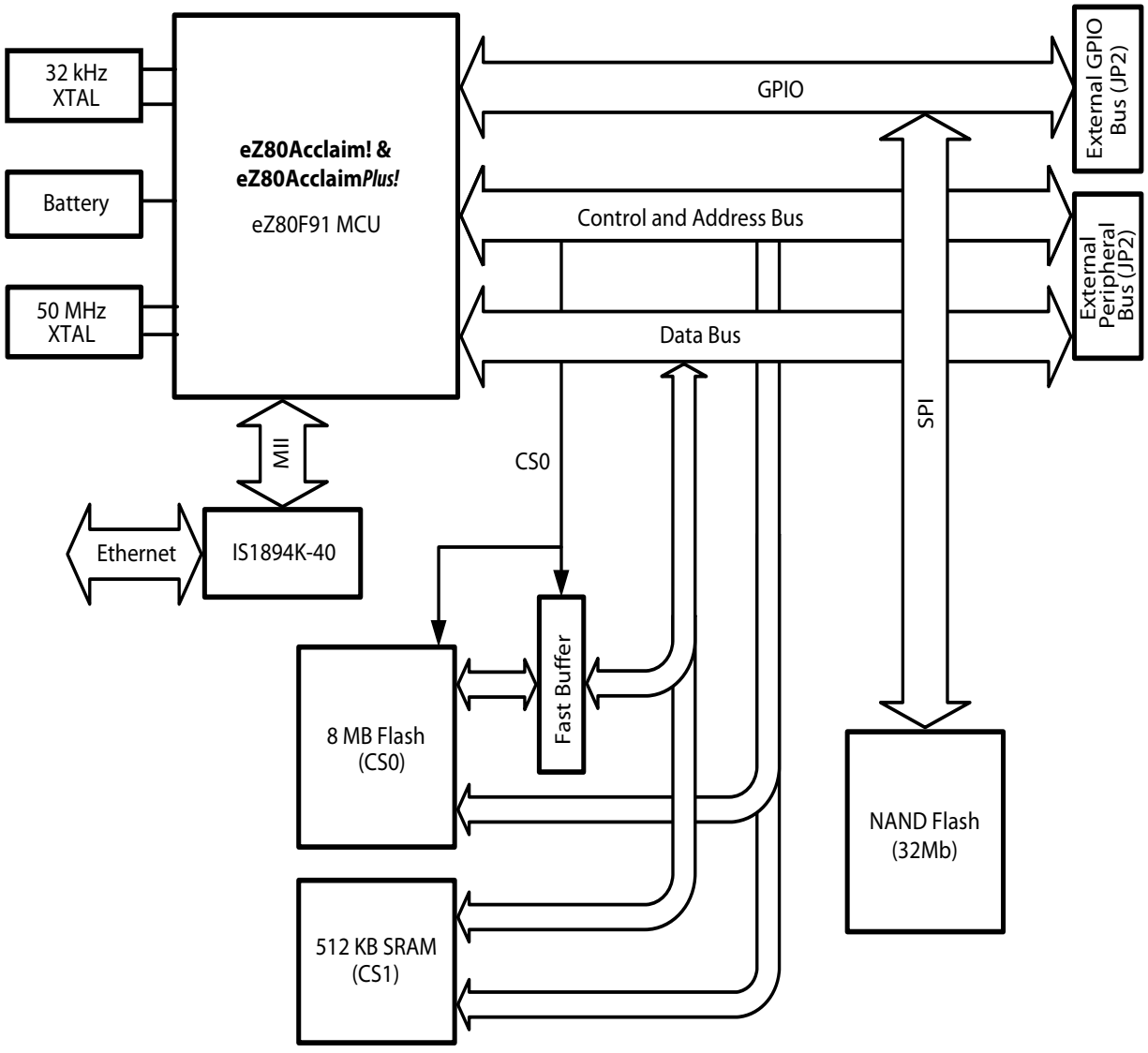

Figure 1. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Functional Block Diagram

Pin Description

This chapter describes each pin and its signal direction for each of the eZ80Acclaim!™/ eZ80AcclaimPlus!™ Ethernet Module's Peripheral Bus and GPIO connectors.

Peripheral Bus Connector

Figure 2 presents a pin layout of the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Modules' 60-pin Peripheral Bus Connector (J1). Table 1 lists the pins and their functions.

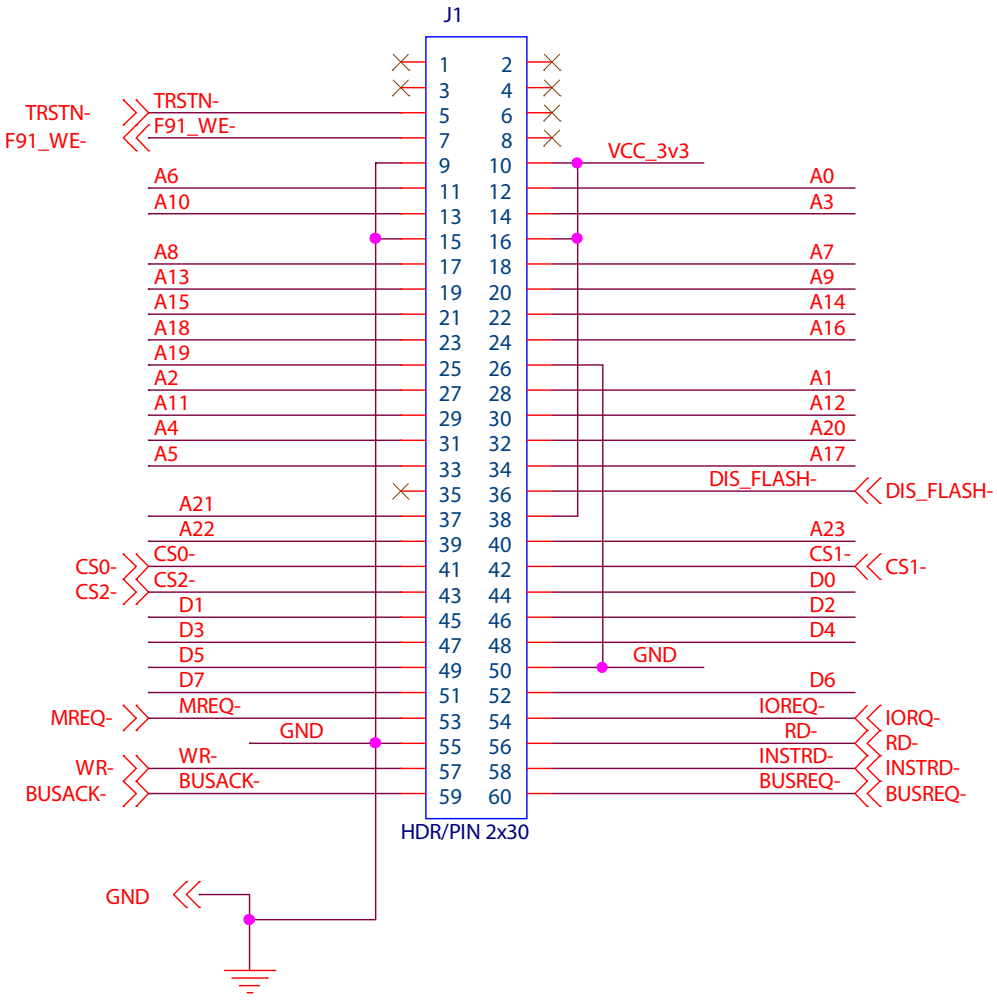

Figure 2. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Peripheral Bus Connector: J1 Pin Configuration

Note: All signals with an overline are active Low. For example, B/$\overline{W}$, in which WORD is active Low, and $\overline{B}$/W, in which BYTE is active Low.

Table 1. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Peripheral Bus: Connector Pin Identification

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
1	Reserved			
2	Reserved			
3	Reserved			
4	Reserved			
5	$\overline{TRSTN}$		Input	Reset for on-chip instrumentation (OCI).
6	Reserved			
7	$\overline{F91\_WE}$	PU 10kΩ	Input	A Low enables a write to on-chip Flash memory. If this pin is unconnected, on-chip Flash memory is write-protected.
8	Reserved			
9	GND			V_{SS}/Ground (0V).
10	V_{CC}			3.3V supply input pin.
11	A6		Bidirectional	
12	A0		Bidirectional	
13	A10		Bidirectional	
14	A3		Bidirectional	
15	GND			V_{SS}/Ground (0V).
16	V_{CC}			3.3V supply input pin.
17	A8		Bidirectional	
18	A7		Bidirectional	
19	A13		Bidirectional	
20	A9		Bidirectional	
21	A15		Bidirectional	
22	A14		Bidirectional	

Notes:
1. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7, and A0–A23 must be below 10pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3V (5V-tolerant), except where otherwise noted.

Table 1. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Peripheral Bus: Connector Pin Identification (Continued)

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
23	A18		Bidirectional	
24	A16		Bidirectional	
25	A19		Bidirectional	
26	GND			V_{SS}/Ground (0 V).
27	A2		Bidirectional	
28	A1		Bidirectional	
29	A11		Bidirectional	
30	A12		Bidirectional	
31	A4		Bidirectional	
32	A20		Bidirectional	
33	A5		Bidirectional	
34	A17		Bidirectional	
35	Reserved			
36	$\overline{\text{DIS\_FLASH}}$	PU 10 kΩ	Input	A Low disables onboard Flash memory. Flash is enabled if $\overline{\text{DIS\_FLASH}}$ is not connected; CMOS input 3.3 V (5 V-tolerant).
37	A21		Bidirectional	
38	V_{CC}			3.3 V supply input pin.
39	A22		Bidirectional	
40	A23		Bidirectional	
41	$\overline{\text{CS0}}$		Output	
42	$\overline{\text{CS1}}$		Output	
43	$\overline{\text{CS2}}$		Output	
44	D0	PU 4 kΩ	Bidirectional	
45	D1	PU 4 kΩ	Bidirectional	
46	D2	PU 4 kΩ	Bidirectional	
47	D3	PU 4 kΩ	Bidirectional	
48	D4	PU 4 kΩ	Bidirectional	

Notes:
1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3 V (5 V-tolerant), except where otherwise noted.

Table 1. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Peripheral Bus: Connector Pin Identification (Continued)

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
49	D5	PU 4kΩ	Bidirectional	
50	GND			V_{SS}/Ground (0V).
51	D7	PU 4kΩ	Bidirectional	
52	D6		Bidirectional	
53	$\overline{\text{MREQ}}$		Bidirectional	
54	$\overline{\text{IORQ}}$		Bidirectional	
55	GND			V_{SS}/Ground (0V).
56	$\overline{\text{RD}}$		Bidirectional	
57	$\overline{\text{WR}}$		Bidirectional	
58	$\overline{\text{INSTRD}}$		Output	
59	$\overline{\text{BUSACK}}$		Output	
60	$\overline{\text{BUSREQ}}$	PU 2kΩ	Input	

Notes:
1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3V (5V-tolerant), except where otherwise noted.

Input/Output Connector

Figure 3 presents a pin layout of the 60-pin I/O connector (J2) of the modules. However, the eZ80® Development Platform features a 50-pin connector. eZ80Acclaim!™/ eZ80AcclaimPlus!™ Ethernet Modules are designed to interface pin 60 of their J2 connectors to pin 50 of the eZ80 Development Platform's JP2 connector so that pins 1–10 of the Modules overlap the edge of the eZ80 development platform. Table 2 describes the pins.

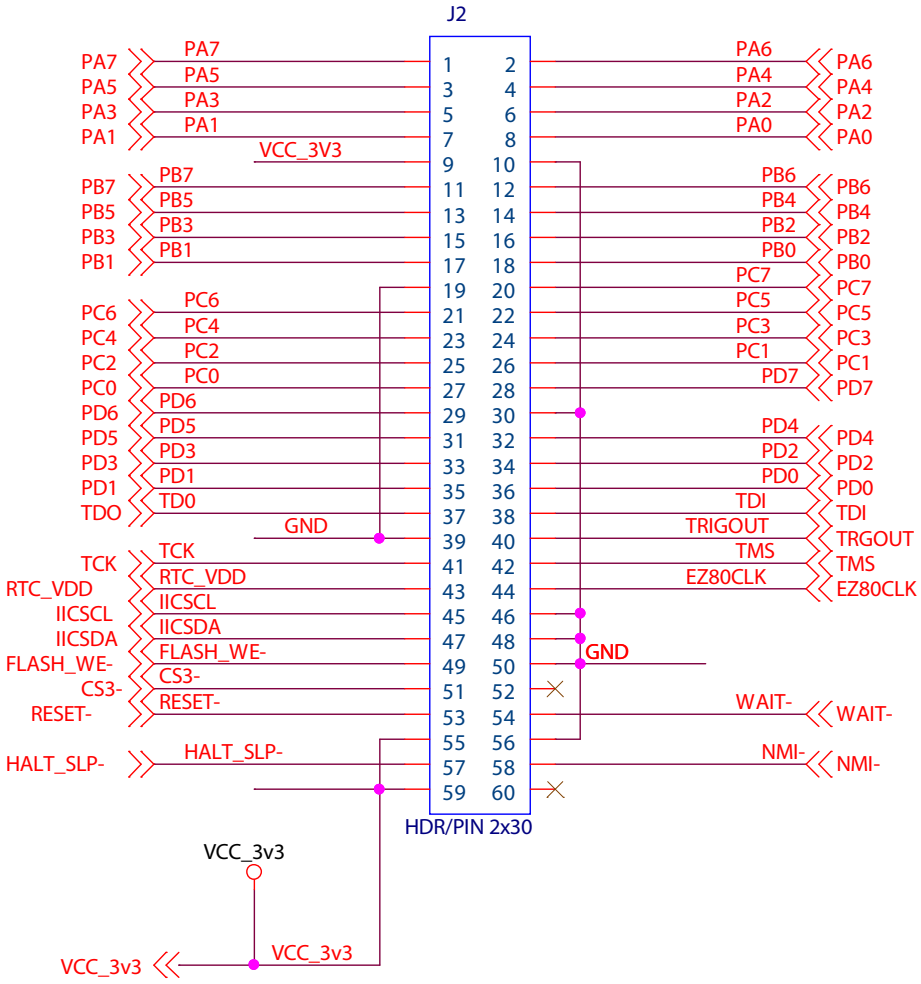

Figure 3. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Input/Output Connector: J2 Pin Configuration

Table 2. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Input/Output Connector: Pin Identification

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
1	PA7		Bidirectional	
2	PA6		Bidirectional	
3	PA5		Bidirectional	
4	PA4		Bidirectional	
5	PA3		Bidirectional	
6	PA2		Bidirectional	
7	PA1		Bidirectional	
8	PA0		Bidirectional	
9	V_{CC}			3.3 V supply input pin.
10	GND			V_{SS}/Ground (0 V).
11	PB7		Bidirectional	
12	PB6		Bidirectional	
13	PB5		Bidirectional	
14	PB4		Bidirectional	
15	PB3		Bidirectional	
16	PB2		Bidirectional	
17	PB1		Bidirectional	
18	PB0		Bidirectional	
19	GND			V_{SS}/Ground (0 V).
20	PC7		Bidirectional	
21	PC6		Bidirectional	
22	PC5		Bidirectional	
23	PC4		Bidirectional	
24	PC3		Bidirectional	
25	PC2		Bidirectional	
26	PC1		Bidirectional	
27	PC0		Bidirectional	

Notes:
1. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3 V (5 V-tolerant), except where otherwise noted.

Table 2. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Input/Output Connector: Pin Identification (Continued)

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
28	PD7		Bidirectional	
29	PD6		Bidirectional	
30	GND			V_{SS}/Ground (0 V).
31	PD5		Bidirectional	
32	PD4	PD 4kΩ	Bidirectional	
33	PD3		Bidirectional	
34	PD2		Bidirectional	
35	PD1		Bidirectional	
36	PD0		Bidirectional	
37	TDO		Output	JTAG Data Output pin.
38	TDI/ZDA		Input	JTAG Data Input pin.
39	GND			V_{SS}/Ground (0 V).
40	TRIGOUT		Output	Active High trigger event indicator.
41	TCK/ZCL	PU 10kΩ	Input	JTAG Input. High on reset enables ZDI Mode; Low on reset enables OCI debug.
42	TMS	PU 10kΩ	Input	JTAG Test Mode Select Input.
43	RTC_V_{DD}			RTC supply. For proper operation of the Modules, this pin must be connected to the same power source that powers the module (as it is done on the Zilog® development platform).
44	EZ80CLK		Output	Synchronous CPU clock output.
45	I^2C SCL	PU 4kΩ	Bidirectional	I^2C Bus Clock.
46	GND			V_{SS}/Ground (0 V).
47	I^2C SDA	PU 4kΩ	Bidirectional	I^2C Data Clock.
48	GND		Power	V_{SS}/Ground (0 V).
49	$\overline{\text{FLASHWE}}$	PU 10kΩ	Input	A Low enables a write to external Flash memory boot block area. If this pin is unconnected, the Flash memory boot block area is write-protected.
50	GND			V_{SS}/Ground (0 V).

Notes:
1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3 V (5 V-tolerant), except where otherwise noted.

Table 2. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module Input/Output Connector: Pin Identification (Continued)

Pin No	Symbol	Pull Up/ Down	Signal Direction	Comments
51	CS3		Output	Used on the eZ80190, eZ80L92, eZ80F92, eZ80F93 devices and connected to the CS8900 EMAC.
52	$\overline{\text{DIS\_IRDA}}$	PU 10kΩ	Input	A Low disables the onboard IRDA transceiver to use PC0/PC1 UART pins externally.
53	RESET	PU 2kΩ	Bidirectional	Reset Output from module or push-button reset.
54	WAIT	PU 2kΩ	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the CPU to provide additional clock cycles for an external peripheral or external memory to complete its read or write operation.
55	V_{CC}			3.3V supply input pin.
56	GND			V_{SS}/Ground (0V).
57	HALT_SLP		Output, Active Low	A Low on this pin indicates that the CPU enters either HALT or SLEEP Mode because of execution of either a HALT or SLP instruction.
58	NMI	PU 10kΩ	Schmitt-trigger Input, Active Low	The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt-trigger to allow RC rise times. This external $\overline{\text{NMI}}$ signal is combined with an internal $\overline{\text{NMI}}$ signal generated from the WDT block before being connected to the $\overline{\text{NMI}}$ input of the CPU.
59	V_{CC}			3.3V supply input pin.
60	Reserved		NC	Reserved; no connection.

Notes:
1. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7, and A0–A23 must be below 10 pF to satisfy timing requirements for the CPU.
2. All unused inputs must be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
3. All inputs are CMOS level 3.3V (5V-tolerant), except where otherwise noted.

Onboard Component Description

This chapter describes each individual component of the eZ80Acclaim!™/ eZ80AcclaimPlus!™ Ethernet Module.

Logic-Level Input/Outputs

The I/O connector features 32 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V-tolerant. Some of the general-purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs, and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information about the eZ80Acclaim!™ MCU, refer to the eZ80F91 MCU Product Specification (PS0192). To learn more about the eZ80Acclaim*Plus!*™ MCU, refer to the eZ80F91 ASSP Product Specification (PS0270).

Onboard Battery Backup

An onboard Panasonic ML2020 3V Lithium battery powers the 32kHz real-time clock when external power is removed. The battery is charged through diode D2 and resistor R17 when external power is applied to the board.

Ethernet PHY and RJ45 Connector

The Module is equipped with an RJ45 connector with integrated magnetics and two LEDs manufactured by IDT.

Ethernet LEDs

Ethernet activity is indicated by two LEDs located on the RJ45 connector. When the PHY is receiving data, the green LED is ON. When the PHY is transmitting data, the yellow LED is ON.

Fast Buffer (U6)

The eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module features a fast buffer (see Figure 1 on page 3) that is used to prevent bus contention that can occurs due to slow turn-off time of the module's external Flash memory, and the fast bus turn-around time of the

eZ80F91 MCU (i.e, a generic feature of the eZ80® family when it is used in NATIVE Mode).

When developing with the eZ80 family of products in NATIVE Mode, the challenge with bus contention occurs when two or more devices drive a common bus. The eZ80F91 MCU's CS0 drives the Flash CE. After accessing the Flash memory space, CS0 is driven High a maximum of 8.8ns after the next rising edge of the clock (refer to T6 in Figure 4). The Flash turn-off time (T_{OD}) is 25ns, which is the period from OE or CE going High to the Flash output drivers going into High-Z Mode. In essence, after the end of the MCU's read access to Flash, a period of 8.8ns + 25ns = 33.8ns must occur before Flash memory stops driving the data bus. At this point, the eZ80F91 device is already well into the next bus cycle.

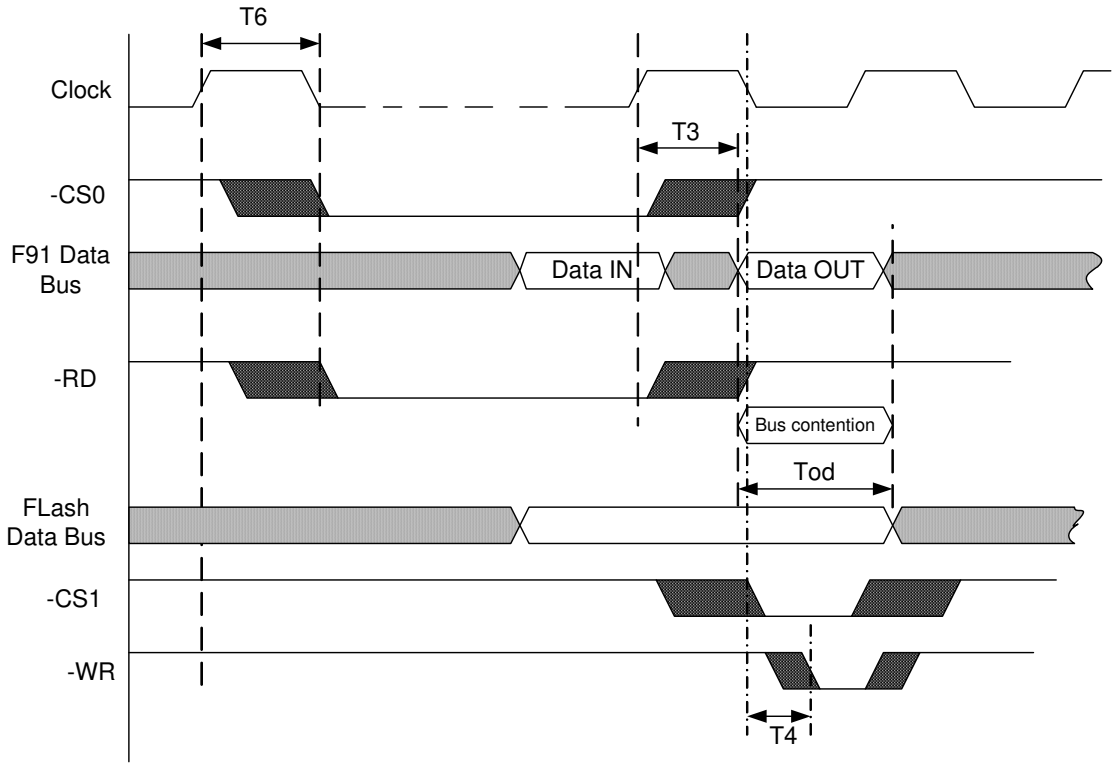

Figure 4. Bus Contention without the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module: Fast Buffer Feature

During a memory write cycle, data (output) from the eZ80F91 device is valid not later than T3 = 7.5ns, and the write pulse is asserted not later than 4.5ns after the falling edge of the Clock (14.5ns from the rising edge if Clock is 50MHz). The result is that during T_{CON} = (33.8ns – 7.5ns) = 26.3ns, two devices drive the common data bus: the eZ80F91 MCU itself, and Flash memory. In turn, data that is being written during the write opera-

tion could become corrupted. The part used to isolate a slow Flash data bus from a fast eZ80F91 bus has a 5.5ns turn-off time, which reduces the 25ns duration of the T_{CON} to 5.5ns. As a result, bus contention still occurs, but its duration is not 26.3ns, as described in the following equation:

Time of contention = (8.8ns – 7.5ns + 5.5ns = 6.8ns

Data being written is not corrupted because the write pulse is not yet asserted.

For more information about bus contention on the eZ80Acclaim!™ MCU, refer to the eZ80F91 MCU Product Specification (PS0192). To learn more about bus contention on the eZ80Acclaim*Plus!*™ MCU, refer to the eZ80F91 ASSP Product Specification (PS0270).

Memory

The Module's onboard memory consists of the following components:

- U4, CY7C1049: 512KB SRAM with a 10ns access time
- U5, S29GL064N: 8MB NOR Flash with 90ns access time
- U3, S25FL032: 32Mb NAND Flash with an SPI interface

The Module contains external Flash memory, and the eZ80F91 MCU contains internal Flash memory. To allow read/write access to Flash memory on the Module, there are two signals provided, on connectors J1 and J2. A jumper on the module, JP3, enables the programming of on-chip Flash. There is also a signal that duplicates the function of this JP3 jumper. Table 3 indicates the states of the signals and the status of the JP3 jumper for different modes.

Table 3. Flash Memory Programming Signals and Jumpers

Signal/Jumper	Function	State/Status
DIS_FLASH	Controls read/write access to the eZ80Acclaim!™/ eZ80AcclaimPlus!™ Ethernet Module for external Flash memory.	When Low, access is enabled
$\overline{\text{FLASHWE}}$	Controls write operations to the boot block of the eZ80Acclaim!™/ eZ80AcclaimPlus!™ Ethernet Module for external Flash memory.	When Low, write is enabled
JP3	Controls write access to eZ80F91 MCU on-chip Flash memory.	When IN, write is enabled
F91_WE	Controls write access to eZ80F91 MCU on-chip Flash memory.	When Low, write is enabled

The external Flash memory space of the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module has an access time of 90ns. At least five wait states must be added to the cycle when accessing external Flash at 50MHz clock speed. The eZ80F91 devices on-chip Flash

is faster; its minimum access time is 60ns, which requires only three wait states at 50MHz.

The Modules feature 512KB of fast SRAM. Access time is 10ns, which requires one-wait-state access. The eZ80F91 MCU's on-chip SRAM is used with zero wait states. An additional memory component on the Module is NAND Flash memory with an SPI interface. This 32Mb device is manufactured by Spansion.

Serial Interface Ports

The CPU contains two UARTs with programmable baud rate generators. UART0 is connected to GPIO PD[0:7] on the I/O connector. UART1 is connected to GPIO PC[0:7] on the I/O connector.

Note: Do not connect an RS-232 interface without level shifters. There are no RS-232 level shifters on the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module.

Physical Dimensions

The footprint of each Modules' PCB is 63.5**mm** x 78.7mm. With an RJ-45 Ethernet connector, the overall height is 25mm, see Figure 5.

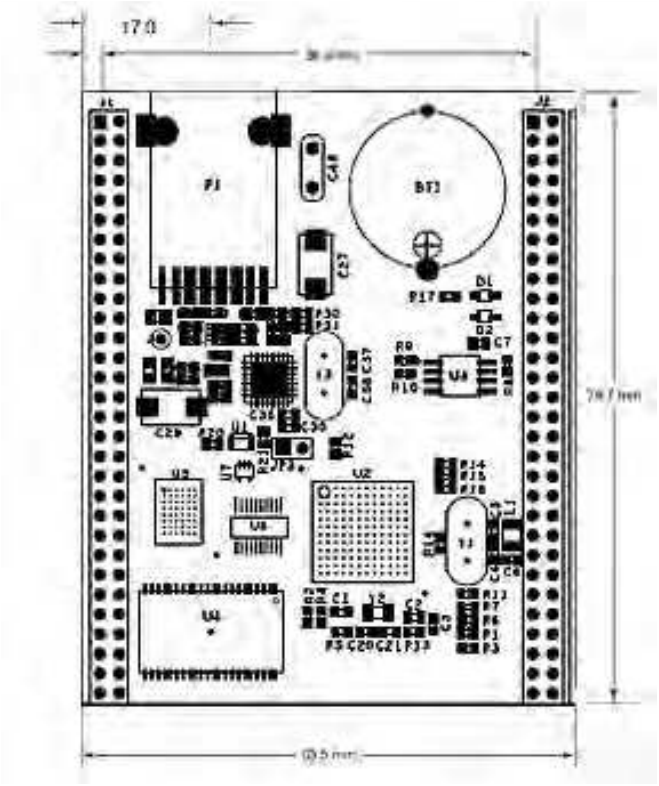

Figure 5. Physical Dimensions of the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module

Absolute Maximum Ratings

Stresses greater than those listed in Table 4 causes permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 4. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50 ºC)	25%	90%	
Operating Voltage	—	3.6	V

Ordering Information

You can order your eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module from Zilog or any of Zilog's authorized distributors using the following part numbers. For more information about ordering, please consult your local Zilog sales office. The Zilog website lists all regional offices and provides additional information about the ZMOTION® Detection Module II product line.

Part Numbers

Table 5 lists the part numbers for the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module products and kit, and briefly describes each part.

Table 5. Part Numbers

Part Number	Description
eZ80F915150MODG	eZ80Acclaim! Ethernet Module
eZ80F917150MODG	eZ80Acclaim*Plus!* Ethernet Module
eZ80F910300ZCOG	eZ80Acclaim*Plus!* Development Kit

Schematic Diagrams

Figures 6 through Figure 10 displays the layout of the eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet Module.

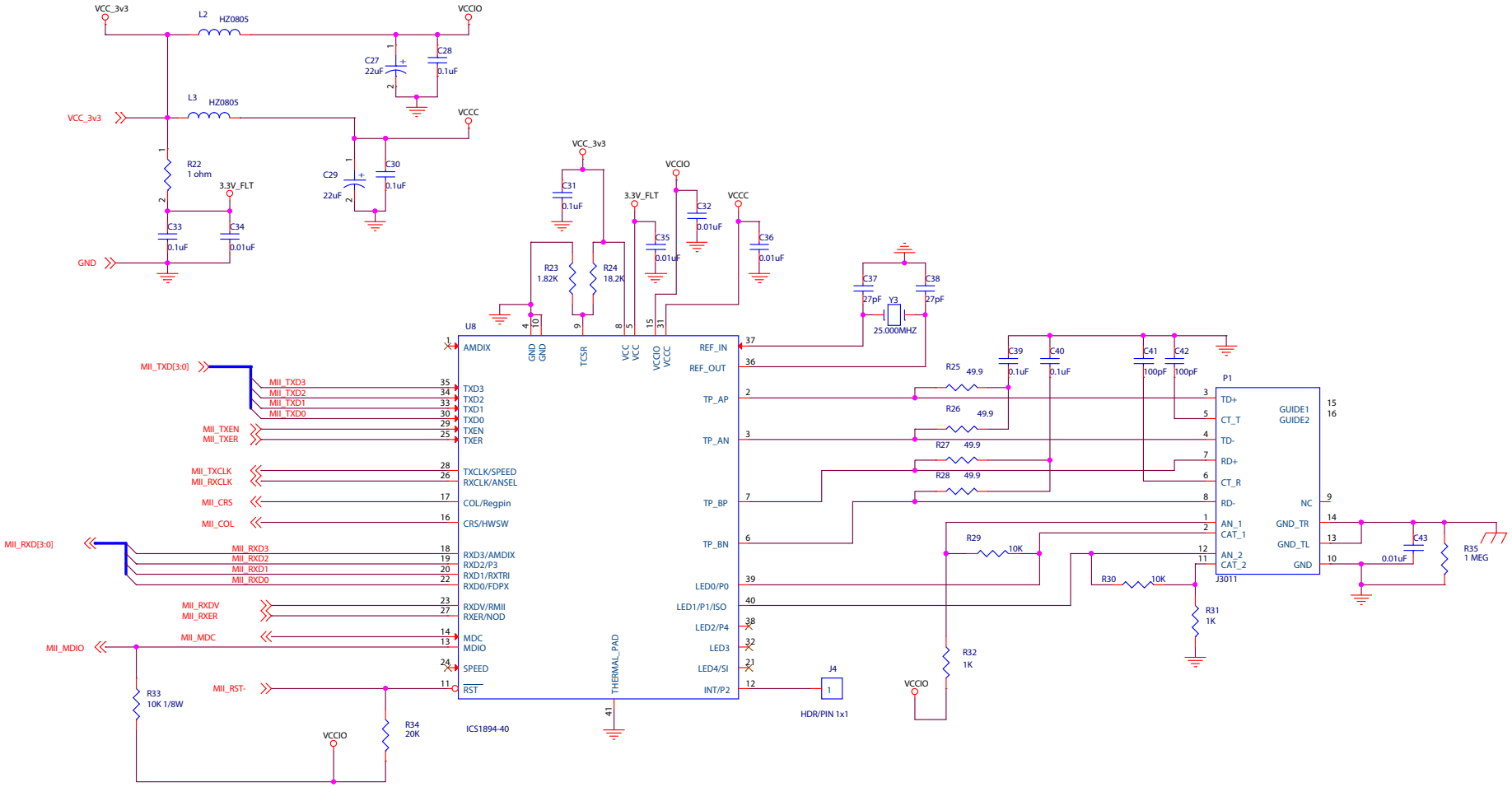

Figure 6. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet ModuleSchematic Diagram: Ethernet

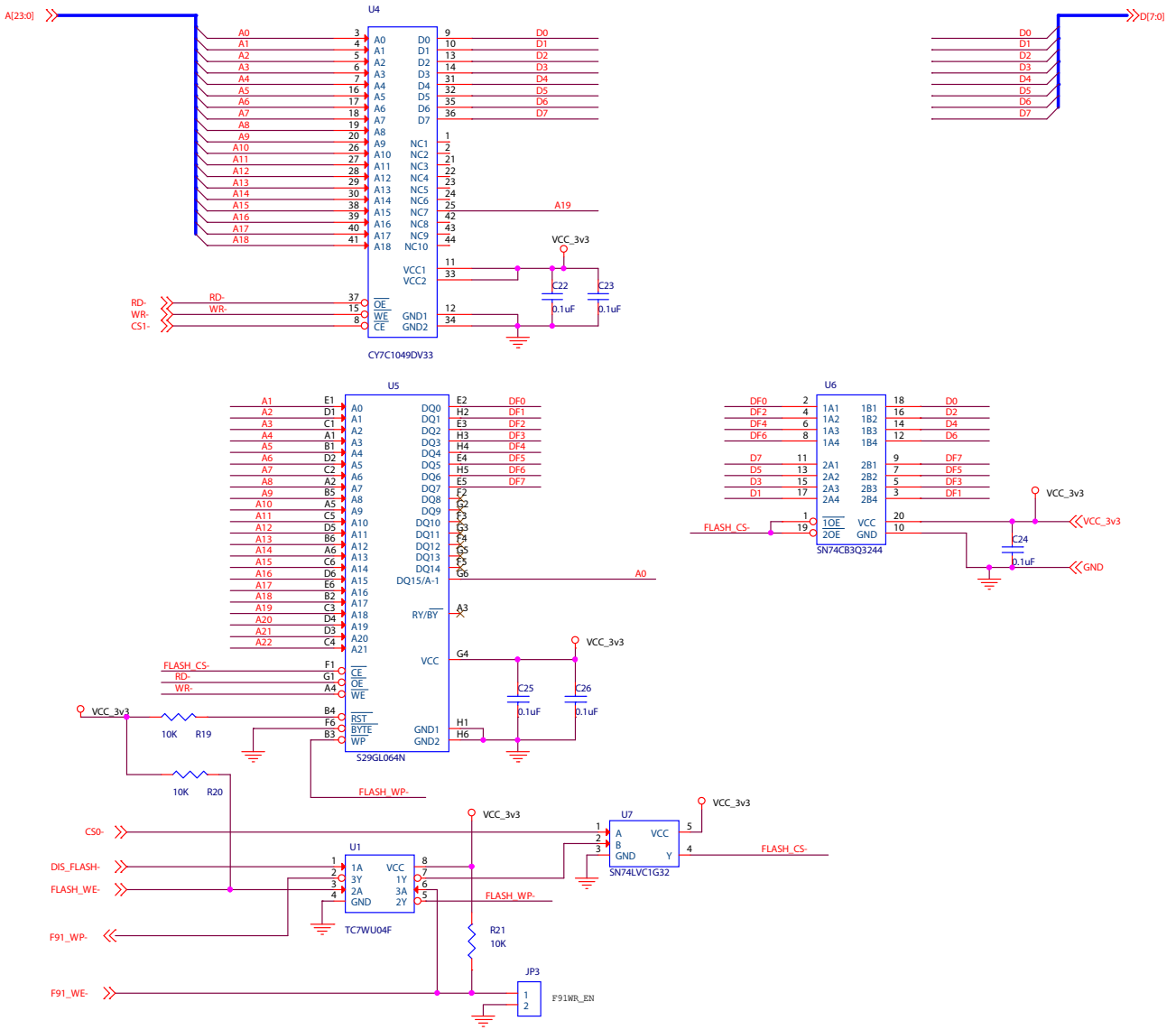

Figure 7. eZ80Acclaim!™/eZ80AcclaimPlus!™ Ethernet ModuleSchematic Diagram: SRAM and Flash Memories