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zilog

An IXYS Company

eZ80Acclaim!® Flash Microcontrollers

eZ80F91 MCU

Product Specification

PS019215-0910

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Revision History

Each instance in the Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages or appropriate links given in the table below.

Date	Revision Level	Section	Description	Page Number
September 2010	15	All	Updated logos and copyright date.	All
August 2008	14	Ordering Information	Updated Part Number Description section.	360
May 2008	13	Introduction, Figure 48, ZDI-Supported Protocol, and Figure 49	Replaced ZPAK II with USB Smart Cable	231, 232, and 233
September 2007	12	General-Purpose Input/ Output, Flash Memory, Universal Asynchronous Receiver/Transmitter, Serial Peripheral Interface, Real-Time Clock Control Register, I^2C Serial I/O Interface, Pin Description, and Ordering Information.	Updated Table 1, Figure 6, Flash Program Control Register, UART Transmitter, Figure 40, Table 93, I2C Registers and Ordering Information.	4, 53, 112,174, 176, 201, 223, and 359
February 2007	11	Register Map, GPIO Mode 7—Alternate Functions, Register Map - Table 3. Low-Power Modes, Electrical Characteristics chapters. Updated Table 93.		27, 45, 54, 339

Date	Revision Level	Section	Description	Page Number
June 2006	10	Global modifications	Updated for new release.	All
		Pin Identification on the eZ80F91 Device	Table 3: The description of the following pins modified: pins 55, 61, 63 and 69	6
		General-Purpose Input/ Output	GPIO chapter totally rewritten	49
		Chip Selects and Wait States	Input/Output chip select operation modified	65
		Flash Memory	The following sections are modified in Flash memory chapter: Erasing Flash memory, Information page characteristics, Flash Write/Erase protection register, Flash program control registers, and Table 43.	97
		Real-Time Clock Overview	Added a note in real time clock overview section	159
		Universal Asynchronous Receiver/Transmitter	Table 102 and 109 modified	175
		Infrared Encoder/Decoder Control Registers	The field [7:4] modified in Table 111	199
		Zilog Debug Interface	Updated the Introduction section, Added two paragraphs to ZDI Read Memory Registers	231
		On-Chip Oscillators	On page 349, Figure 63: Recommended Crystal Oscillator Configuration, the value of inductance L is changed to 3.3 µH. On page 351, Table 232, changed serial resistance value from 40 kΩ to 50 kΩ	336
		POR and VBO Electrical Characteristics	In Table 235: Min, Typ, and Max values of VBO voltage threshold modified and added IS_{por_vbo} parameter	341
		Ordering Information	Ordering information modified	359

Table of Contents

Architectural Overview

Zilog's eZ80F91 device is a member of Zilog's family of eZ80Acclaim!® Flash microcontrollers. The eZ80F91 is a high-speed microcontroller with a maximum clock speed of 50 MHz and single-cycle instruction fetch. It operates in Z80®-compatible addressing mode (64 KB) or full 24-bit addressing mode (16 MB). The rich peripheral set of the eZ80F91 makes it suitable for a variety of applications, including industrial control, embedded communication, and point-of-sale terminals.

Features

Key features of eZ80F91 device include:

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core (referred as *The CPU* in this document)
- 10/100 BaseT ethernet media access controller with Media-Independent Interface (MII)
- 256 KB Flash memory
- 16 KB SRAM (8 KB user and 8 KB Ethernet)
- Low-power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two Universal Asynchronous Receiver/Transmitter (UART) with independent Baud Rate Generators (BRG)
- Serial Peripheral Interface (SPI) with independent clock rate generator
- I^2C with independent clock rate generator
- IrDA-compliant infrared encoder/decoder
- Glueless external peripheral interface with 4 Chip Selects, individual Wait State generators, an external $\overline{WAIT}$ input pin—supports Z80-, Intel-, and Motorola-style buses
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with separate V_{DD} pin for battery backup and selectable on-chip 32 kHz oscillator or external 50/60 Hz input
- Four 16-bit Counter/Timers with prescalers and direct input/output drive
- Watchdog Timer with internal oscillator clocking option
- 32 bits of General-Purpose Input/Output (GPIO)
- On-Chip Instrumentation (OCI™) and Zilog Debug Interfaces (ZDI)

- IEEE 1149.1-compatible JTAG
- 144-pin LQFP and BGA packages
- 3.0 V to 3.6 V supply voltage with 5 V tolerant inputs
- Operating Temperature Range:
  - Standard: 0 ºC to +70 ºC
  - Extended: –40 ºC to +105 ºC

Note: *All signals with an overline are active Low. For example, the signal* $\overline{\text{DCD1}}$ *is active when it is a logical 0 (Low) state.*

The power connections conventions are provided in the table below.

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Block Diagram

Figure 1 on page 3 displays a block diagram of the eZ80F91 microcontroller.

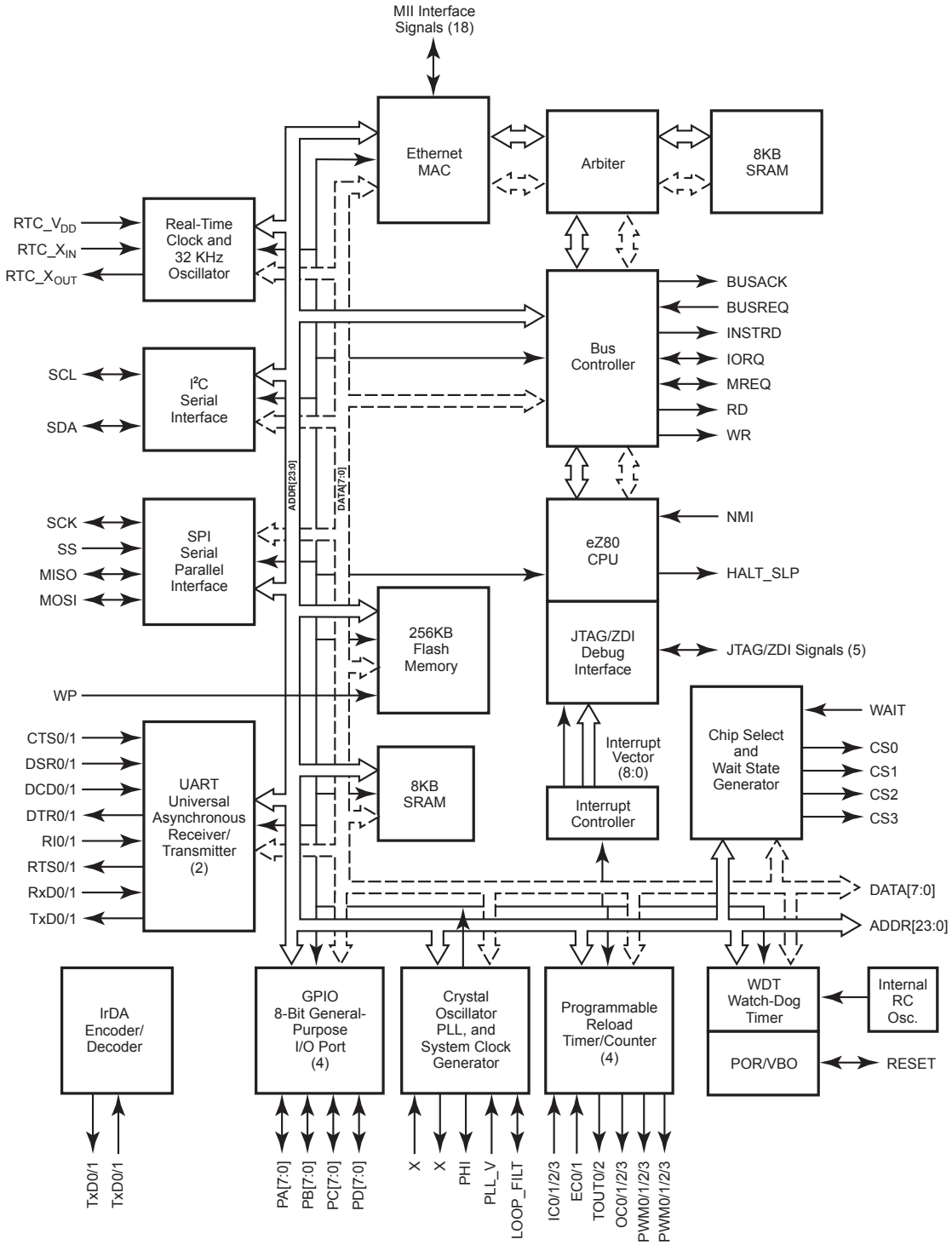

Figure 1. eZ80F91 Block Diagram

Pin Description

Table 1 lists the pin configuration of the eZ80F91 device in the 144-BGA package.

Table 1. eZ80F91 144-BGA Pin Configuration

	12	11	10	9	8	7	6	5	4	3	2	1
A	SDA	SCL	PA0	PA4	PA7	COL	TxD0	V_{DD}	Rx_DV	MDC	WPn	A0
B	V_{SS}	PHI	PA1	PA3	V_{DD}	TxD3	Tx_EN	V_{SS}	RxD1	MDIO	A2	A1
C	PB6	PB7	V_{DD}	PA5	V_{SS}	TxD2	Tx_CLK	Rx_ CLK	RxD3	A3	V_{SS}	V_{DD}
D	PB1	PB3	PB5	V_{SS}	CRS	TxD1	Rx_ER	RxD2	A4	A8	A6	A7
E	PC7	V_{DD}	PB0	PB4	PA2	Tx_ER	RxD0	A5	A11	V_{SS}	V_{DD}	A10
F	PC3	PC4	PC5	V_{SS}	PB2	PA6	A9	A17	A15	A14	A13	A12
G	V_{SS}	PC0	PC1	PC2	PC6	PLL_ V_{SS}	V_{SS}	A23	A20	V_{SS}	V_{DD}	A16
H	X_{OUT}	X_{IN}	PLL_ V_{DD}	V_{DD}	PD7	TMS	V_{SS}	D5	V_{SS}	A21	A19	A18
J	V_{SS}	V_{DD}	LOOP FILT_ OUT	PD4	TRIGOUT	RTC_ V_{DD}	NMIn	WRn	D2	CS0n	V_{DD}	A22
K	PD5	PD6	PD3	TDI	V_{SS}	V_{DD}	RESETn	RDn	V_{DD}	D1	CS2n	CS1n
L	PD1	PD2	TRSTn	TCK	RTC_ XOUT	BUSACKn	WAITn	MREQn	D6	D4	D0	CS3n
M	PD0	V_{SS}	TDO	HALT _ SLPn	RTC_ XIN	BUSREQn	INSTRDn	IORQn	D7	D3	V_{SS}	V_{DD}

Note: Lowercase n suffix indicates an active-low signal in this table only

Figure 2 displays the pin layout of the eZ80F91 device in the 144-pin LQFP package.

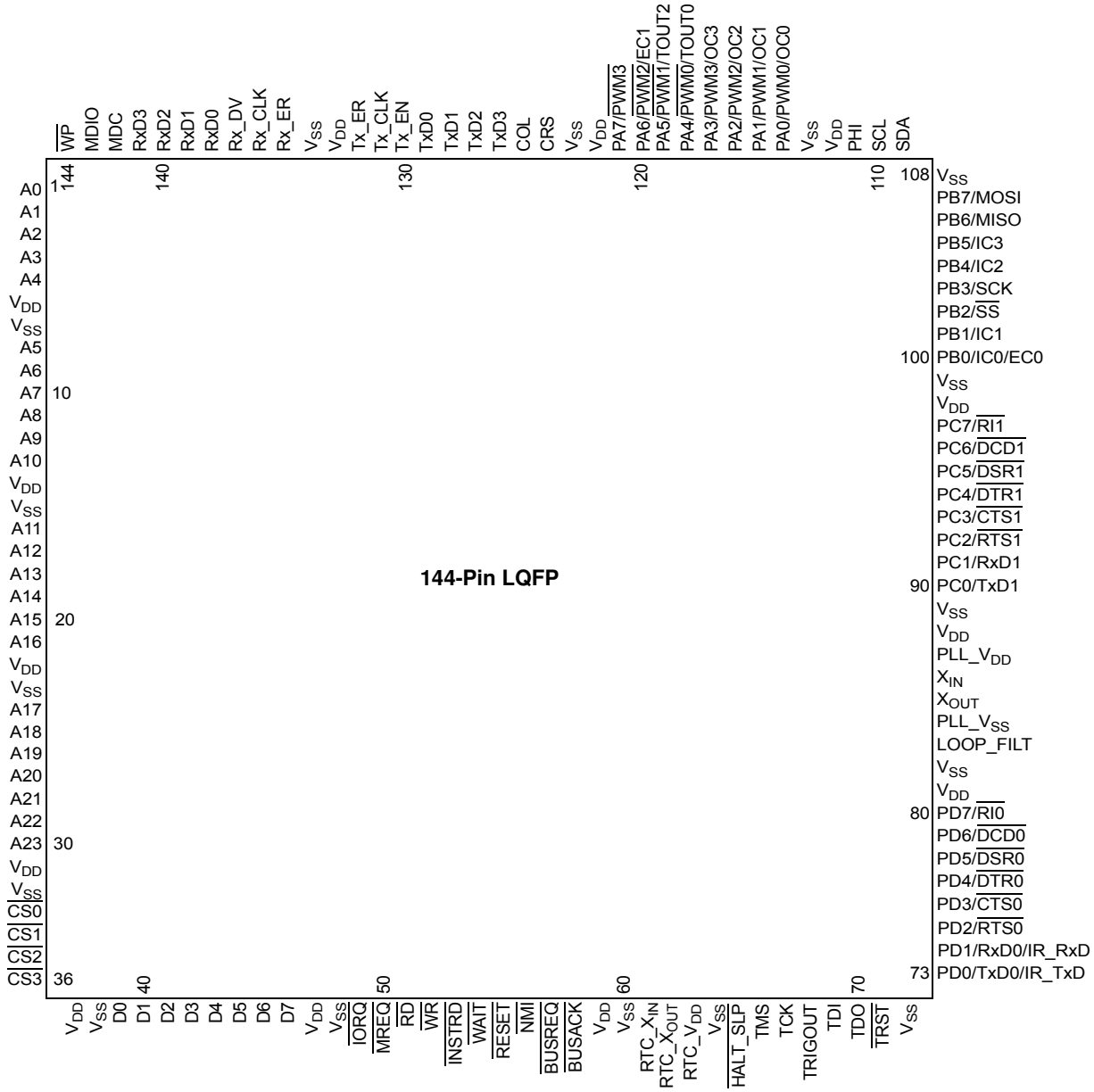

Figure 2. 144-Pin LQFP Configuration of the eZ80F91

Pin Characteristics

Table 2 lists the pins and functions of the eZ80F91 MCU's 144-pin LQFP package and 144-BGA package.

Table 2. Pin Identification on the eZ80F91 Device

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
1	A1	ADDR0	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
2	B1	ADDR1	Address Bus	Bidirectional	
3	B2	ADDR2	Address Bus	Bidirectional	
4	C3	ADDR3	Address Bus	Bidirectional	
5	D4	ADDR4	Address Bus	Bidirectional	
6	C1	V_{DD}	Power Supply		Power Supply.
7	C2	V_{SS}	Ground		Ground.
8	E5	ADDR5	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
9	D2	ADDR6	Address Bus	Bidirectional	
10	D1	ADDR7	Address Bus	Bidirectional	
11	D3	ADDR8	Address Bus	Bidirectional	
12	F6	ADDR9	Address Bus	Bidirectional	
13	E1	ADDR10	Address Bus	Bidirectional	
14	E2	V_{DD}	Power Supply		Power Supply.
15	E3	V_{SS}	Ground		Ground.
16	E4	ADDR11	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
17	F1	ADDR12	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
18	F2	ADDR13	Address Bus	Bidirectional	
19	F3	ADDR14	Address Bus	Bidirectional	
20	F4	ADDR15	Address Bus	Bidirectional	
21	G1	ADDR16	Address Bus	Bidirectional	
22	G2	V_{DD}	Power Supply		Power Supply.
23	G3	V_{SS}	Ground		Ground.
24	F5	ADDR17	Address Bus	Bidirectional	Configured as an output in normal operation. The address bus selects a location in memory or I/O space to be read or written. Configured as an input during bus acknowledge cycles. Drives the Chip Select/Wait State Generator block to generate Chip Selects.
25	H1	ADDR18	Address Bus	Bidirectional	
26	H2	ADDR19	Address Bus	Bidirectional	
27	G4	ADDR20	Address Bus	Bidirectional	
28	H3	ADDR21	Address Bus	Bidirectional	
29	J1	ADDR22	Address Bus	Bidirectional	
30	G5	ADDR23	Address Bus	Bidirectional	
31	J2	V_{DD}	Power Supply		Power Supply.
32	H4	V_{SS}	Ground		Ground.
33	J3	CS0	Chip Select 0	Output, Active Low	$\overline{CS0}$ Low indicates that an access is occurring in the defined $\overline{CS0}$ memory or I/O address space.
34	K1	CS1	Chip Select 1	Output, Active Low	$\overline{CS1}$ Low indicates that an access is occurring in the defined $\overline{CS1}$ memory or I/O address space.
35	K2	CS2	Chip Select 2	Output, Active Low	$\overline{CS2}$ Low indicates that an access is occurring in the defined $\overline{CS2}$ memory or I/O address space.
36	L1	CS3	Chip Select 3	Output, Active Low	$\overline{CS3}$ Low indicates that an access is occurring in the defined $\overline{CS3}$ memory or I/O address space.
37	M1	V_{DD}	Power Supply		Power Supply.
38	M2	V_{SS}	Ground		Ground.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
39	L2	DATA0	Data Bus	Bidirectional	The data bus transfers data to and from I/O and memory devices. The eZ80F91 drives these lines only during Write cycles when the eZ80F91 is the bus master.
40	K3	DATA1	Data Bus	Bidirectional	
41	J4	DATA2	Data Bus	Bidirectional	
42	M3	DATA3	Data Bus	Bidirectional	
43	L3	DATA4	Data Bus	Bidirectional	
44	H5	DATA5	Data Bus	Bidirectional	
45	L4	DATA6	Data Bus	Bidirectional	
46	M4	DATA7	Data Bus	Bidirectional	
47	K4	V_{DD}	Power Supply		Power Supply.
48	G6	V_{SS}	Ground		Ground.
49	M5	$\overline{IORQ}$	Input/Output Request	Bidirectional, Active Low	$\overline{IORQ}$ indicates that the CPU is accessing a location in I/O space. $\overline{RD}$ and $\overline{WR}$ indicate the type of access. The eZ80F91 device does not drive this line during RESET. It is an input during bus acknowledge cycles.
50	L5	$\overline{MREQ}$	Memory Request	Bidirectional, Active Low	$\overline{MREQ}$ Low indicates that the CPU is accessing a location in memory. The $\overline{RD}$, $\overline{WR}$, and $\overline{INSTRD}$ signals indicate the type of access. The eZ80F91 device does not drive this line during RESET. It is an input during bus acknowledge cycles.
51	K5	$\overline{RD}$	Read	Output, Active Low	$\overline{RD}$ Low indicates that the eZ80F91 device is reading from the current address location. This pin is in a high-impedance state during bus acknowledge cycles.
52	J5	$\overline{WR}$	Write	Output, Active Low	$\overline{WR}$ indicates that the CPU is writing to the current address location. This pin is in a high-impedance state during bus acknowledge cycles.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
53	M6	$\overline{\text{INSTRD}}$	Instruction Read Indicator	Output, Active Low	$\overline{\text{INSTRD}}$ (with $\overline{\text{MREQ}}$ and $\overline{\text{RD}}$) indicates the eZ80F91 device is fetching an instruction from memory. This pin is in a high-impedance state during bus acknowledge cycles.
54	L6	$\overline{\text{WAIT}}$	WAIT Request	Schmitt-trigger input, Active Low	Driving the $\overline{\text{WAIT}}$ pin Low forces the CPU to wait additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.
55	K6	RESET	Reset	Bidirectional, Active Low Schmitt-trigger input or open drain output	This signal is used to initialize the eZ80F91, and/or allow the ez80F91 to signal when it resets. See reset section for the timing details. This Schmitt-trigger input allows for RC rise times.
56	J6	$\overline{\text{NMI}}$	Nonmaskable Interrupt	Schmitt-trigger input, Active Low, edge-triggered interrupt	The $\overline{\text{NMI}}$ input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt- trigger to allow for RC rise times.
57	M7	BUSREQ	Bus Request	Schmitt-trigger input, Active Low	External devices request the eZ80F91 device to release the memory interface bus for their use by driving this pin Low.
58	L7	$\overline{\text{BUSACK}}$	Bus Acknowledge	Output, Active Low	The eZ80F91 device responds to a Low on $\overline{\text{BUSREQ}}$ making the address, data, and control signals high impedance, and by driving the $\overline{\text{BUSACK}}$ line Low. During bus acknowledge cycles ADDR[23:0], $\overline{\text{IORQ}}$, and $\overline{\text{MREQ}}$ are inputs.
59	K7	V_{DD}	Power Supply		Power Supply.
60	H6	V_{SS}	Ground		Ground.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
61	M8	RTC_X_{IN}	Real-Time Clock Crystal Input	Input	This pin is the input to the low-power 32 kHz crystal oscillator for the Real-time clock. If the Real-time clock is disabled or not used, this input must be left floating or tied to VSS to minimize any input current leakage.
62	L8	RTC_X_{OUT}	Real-Time Clock Crystal Output	Bidirectional	This pin is the output from the low-power 32 kHz crystal oscillator for the Real-Time Clock. This pin is an input when the RTC is configured to operate from 50/60 Hz input clock signals and the 32 kHz crystal oscillator is disabled.
63	J7	RTC_V_{DD}	Real-Time Clock Power Supply		Power supply for the Real-Time Clock and associated 32 kHz oscillator. Isolated from the power supply to the remainder of the chip. A battery is connected to this pin to supply constant power to the Real-Time Clock and 32 kHz oscillator. If the Real-time clock is disabled or not used this output must be tied to Vdd.
64	K8	V_{SS}	Ground		Ground.
65	M9	HALT_SLP	HALT and SLEEP Indicator	Output, Active Low	A Low on this pin indicates that the CPU has entered either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
66	H7	TMS	JTAG Test Mode Select	Input	JTAG Mode Select Input.
67	L9	TCK	JTAG Test Clock	Input	JTAG and ZDI clock input.
68	J8	TRIGOUT	JTAG Test Trigger Output	Output	Active High trigger event indicator.
69	K9	TDI	JTAG Test Data In	Bidirectional	JTAG data input pin. Functions as ZDI data I/O pin when JTAG is disabled. This pin has an internal pull-up resistor in the pad.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
70	M10	TDO	JTAG Test Data Out	Output	JTAG data output pin.
71	L10	TRST	JTAG Reset	Schmitt-trigger input, Active Low	JTAG reset input pin.
72	M11	V_{SS}	Ground		Ground.
73	M12	PD0	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		TxD0	UART Transmit Data	Output	This pin is used by the UART to transmit asynchronous serial data. This signal is multiplexed with PD0.
		IR_TxD	IrDA Transmit Data	Output	This pin is used by the IrDA encoder/ decoder to transmit serial data. This signal is multiplexed with PD0.
74	L12	PD1	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		RxD0	Receive Data	Input	This pin is used by the UART to receive asynchronous serial data. This signal is multiplexed with PD1.
		IR_RxD	IrDA Receive Data	Input	This pin is used by the IrDA encoder/ decoder to receive serial data. This signal is multiplexed with PD1.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
75	L11	PD2	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		RTS0	Request to Send	Output, Active Low	Modem control signal from UART. This signal is multiplexed with PD2.
76	K10	PD3	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		CTS0	Clear to Send	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD3.
77	J9	PD4	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		DTR0	Data Terminal Ready	Output, Active Low	Modem control signal to the UART. This signal is multiplexed with PD4.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
78	K12	PD5	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		DSR0	Data Set Ready	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD5.
79	K11	PD6	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		DCD0	Data Carrier Detect	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD6.
80	H8	PD7	GPIO Port D	Bidirectional	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port D pin, when programmed as output is selected to be an open-drain or open-source output. Port D is multiplexed with one UART.
		RI0	Ring Indicator	Input, Active Low	Modem status signal to the UART. This signal is multiplexed with PD7.
81	J11	V_{DD}	Power Supply		Power Supply.
82	J12	V_{SS}	Ground		Ground.
83	J10	LOOP_FILT	PLL Loop Filter	Analog	Loop Filter pin for the Analog PLL.
84	G7	PLL_V_{SS}	Ground		Ground for Analog PLL.
85	H12	X_{OUT}	System Clock Oscillator Output	Output	This pin is the output of the onboard crystal oscillator. When used, a crystal must be connected between X_{IN} and X_{OUT}.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
86	H11	X_{IN}	System Clock Oscillator Input	Input	This pin is the input to the onboard crystal oscillator for the primary system clock. If an external oscillator is used, its clock output must be connected to this pin. When a crystal is used, it must be connected between X_{IN} and X_{OUT}.
87	H10	PLL_V_{DD}	Power Supply		Power Supply for Analog PLL.
88	H9	V_{DD}	Power Supply		Power Supply.
89	G12	V_{SS}	Ground		Ground.
90	G11	PC0	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		TxD1	Transmit Data	Output	This pin is used by the UART to transmit asynchronous serial data. This signal is multiplexed with PC0.
91	G10	PC1	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		RxD1	Receive Data	Schmitt-trigger input	This pin is used by the UART to receive asynchronous serial data. This signal is multiplexed with PC1.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
92	G9	PC2	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		RTS1	Request to Send	Output, Active Low	Modem control signal from UART. This signal is multiplexed with PC2.
93	F12	PC3	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		CTS1	Clear to Send	Schmitt-trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC3.
94	F11	PC4	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DTR1	Data Terminal Ready	Output, Active Low	Modem control signal to the UART. This signal is multiplexed with PC4.

Table 2. Pin Identification on the eZ80F91 Device (Continued)

LQFP Pin No	BGA Pin No	Symbol	Function	Signal Direction	Description
95	F10	PC5	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DSR1	Data Set Ready	Schmitt-trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC5.
96	G8	PC6	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		DCD1	Data Carrier Detect	Schmitt-trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC6.
97	E12	PC7	GPIO Port C	Bidirectional with Schmitt-trigger input	This pin is used for GPIO. It is individually programmed as input or output and is also used individually as an interrupt input. Each Port C pin, when programmed as output is selected to be an open-drain or open-source output. Port C is multiplexed with one UART.
		RI1	Ring Indicator	Schmitt-trigger input, Active Low	Modem status signal to the UART. This signal is multiplexed with PC7.
98	E11	V_{DD}	Power Supply		Power Supply.
99	F9	V_{SS}	Ground		Ground.