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eZ80F91WF01SBCG

eZ80Acclaim*Plus!*™ Wireless Zdots® Single Board Computer

Product Specification

PS028002-1108

www.zilog.com

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

Date	Revision Level	Description	Page Number
November 2008	02	Changed WiFi to Wireless. Updated ZTP features, Figure 1, Table 4, Table 6.	1, 4, 8, 14
October 2008	01	Original issue.	All

Table of Contents

eZ80Acclaim*Plus!*™ Wireless Zdots® SBC

Zilog's eZ80Acclaim*Plus!* Wireless Zdots Single Board Computer (SBC) is a compact, high-performance board specially designed for the rapid development and deployment of embedded systems requiring control and Wireless internet/intranet connectivity.

This expandable Zdots SBC is powered by Zilog's latest power-efficient, high-speed, optimized pipeline architecture eZ80F91 connectivity ASSP, a member of eZ80Acclaim*Plus!* family.

eZ80F91 is a high-speed single-cycle instruction-fetch microcontroller, which operates with a clock speed of up to 50 MHz.

The rich-peripheral Wireless Zdots SBC makes it suitable for a variety of applications such as Health Care, CE Devices, Energy Management, Smart Appliances, Home Control, and Fitness.

A complete software library is also provided that will include a TCP/IP stack (ZTP), including an integrated, preemptive multitasking OS optimized for embedded systems. ZTP software suite is optimized to allow development of the low-cost systems. ZTP offers full-feature operating system services in addition to network services while occupying minimal Program Memory. The applications can be integrated with ZTP via application programming interface (API). ZTP is based on Zilog Real-Time Kernel (RZK), which includes an embedded file system and support for a wide range of eZ80® peripherals such as I^2C, SPI, UART, EMAC and RTC.

The key features of ZTP include:

- Compact, preemptive, multitasking, real-time kernel with inter-process communications (IPC) support and soft real-time attributes
- Complete TCP/IP stack
- Compatible with all members of the eZ80 family
- Wireless Station Device Mode-Configurable SSID, No Encryption, 64-bit WEP or 128-bit WEP Encryption Key support
- PPoE Client-PPoE Discovery and PPoE Session
- Implementation of the following standard network protocols: ARP, DHCP, DNS, FTP, HTTP, SSL, ICMP, IGMP, IP, PPP, RARP, SMTP, TCP, SNMP, UDP, SNTP, Telnet, TFTP, and TimeP
- Interoperable with all RFC-compliant TCP/IP and Network Protocol implementations to provide seamless connectivity
- A board support package (BSP) containing an Ethernet Media Access Controller (EMAC) driver using the eZ80F91 integrated EMAC

- A serial driver
- Final stack size is link/time configurable and determined by the protocols included in the build
- Application demonstrations

For more information on ZTP and RZK, see Related Documentation on page 15.

eZ80Acclaim*Plus!*™ Wireless Zdots® SBC Features

The features of the eZ80Acclaim*Plus!* Wireless Zdots SBC include:

- 5 MHz main clock; operating clock frequency up to 50 MHz using PLL
- RTL8711, 802.11 b/g Wireless transceiver with SPI interface
- 1 MB off-chip SRAM 10 ns
- 256 KB on-chip Flash memory
- Support for optional serial Flash
- 4 MB off-chip NOR Flash memory 70 ns
- Support for optional Battery-backed Real-Time Clock
- Two optional low-cost 2x15 expansion connectors that provide GPIO/I^2C/SPI/UARTs and MII interfaces and 5 V tolerant I/O pins
- Option for external antenna—Manufacturer Inpaq Corporation, part number DAMAOBM11500200
- Embedded Antenna
- Programmable power switch for Wireless transceiver and user input/output
- Small footprint: 2.2 inches by 3.5 inches
- 3.3 V operation
- Standard operating temperature range: 0 ºC to +70 ºC

eZ80AcclaimPlus!™ Connectivity ASSP Features

The features of the eZ80AcclaimPlus! Connectivity ASSP include:

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- 256 KB of Flash memory and 8 KB of SRAM
- 10/100 Mbps Ethernet MAC with 8 KB frame buffer
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators and support for 9-bit operation
- SPI with independent clock generator
- I^2C with independent clock generator
- New DMA-like eZ80® instructions for efficient block data transfer
- External interface with four chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses
- Flexible-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32 kHz oscillator, selectable 50/60 Hz input, and separate V_{DD} pin for battery backup
- Four 16-bit counter/timers with prescalers and direct input/output drive
- Watchdog Timer (WDT)
- 32 bits of General-Purpose Input/Output (GPIO)
- Zilog Debug Interface (ZDI)
- Supply voltage of 3.0 V to 3.6 V with 5 V tolerant inputs
- Standard operating temperature range: 0 ºC to +70 ºC

Block Diagram

Figure 1 displays the block diagram of the eZ80AcclaimPlus!™ Wireless Zdots® SBC.

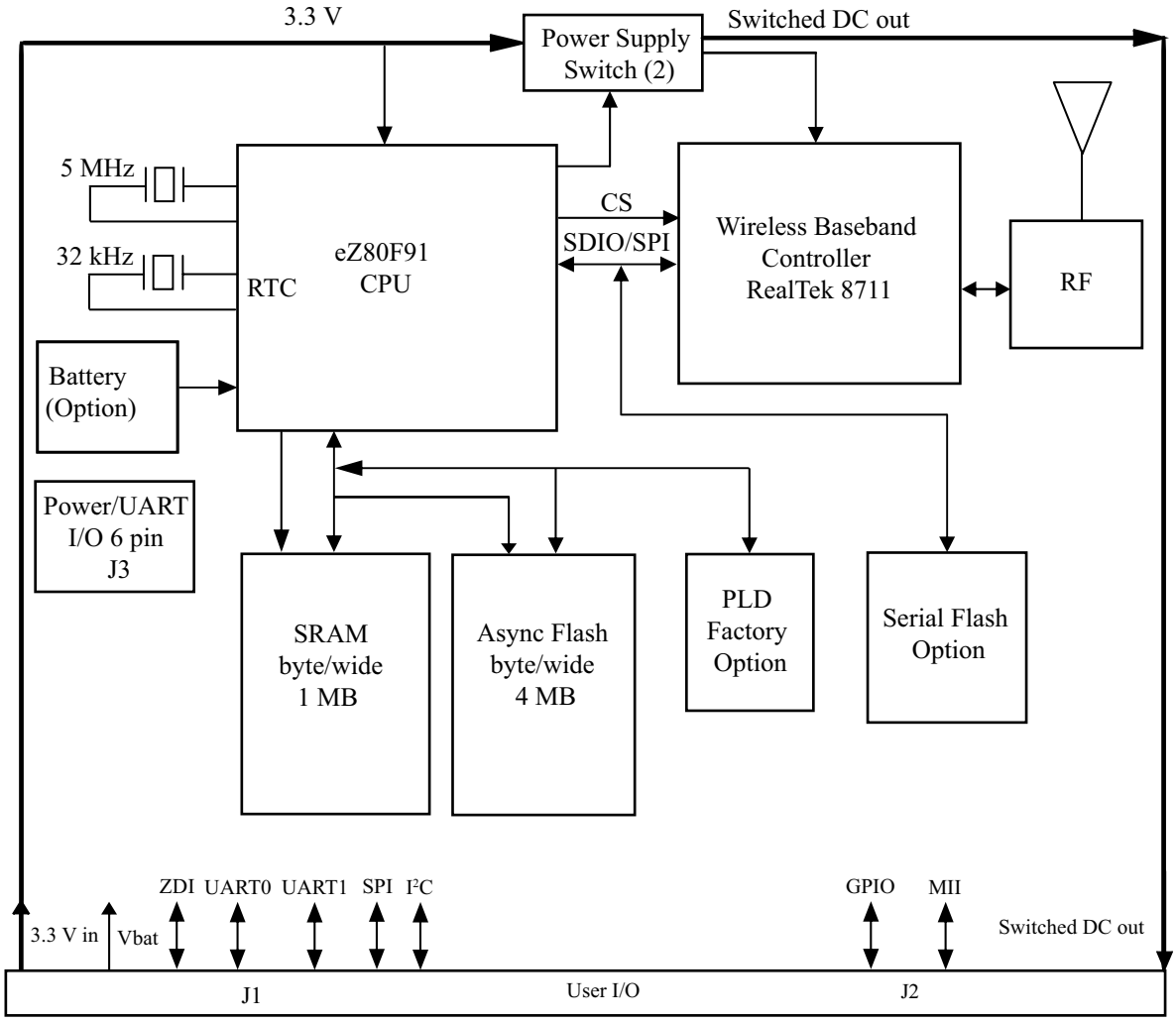

Figure 1. eZ80AcclaimPlus!™ Wireless Zdots® SBC Functional Block Diagram

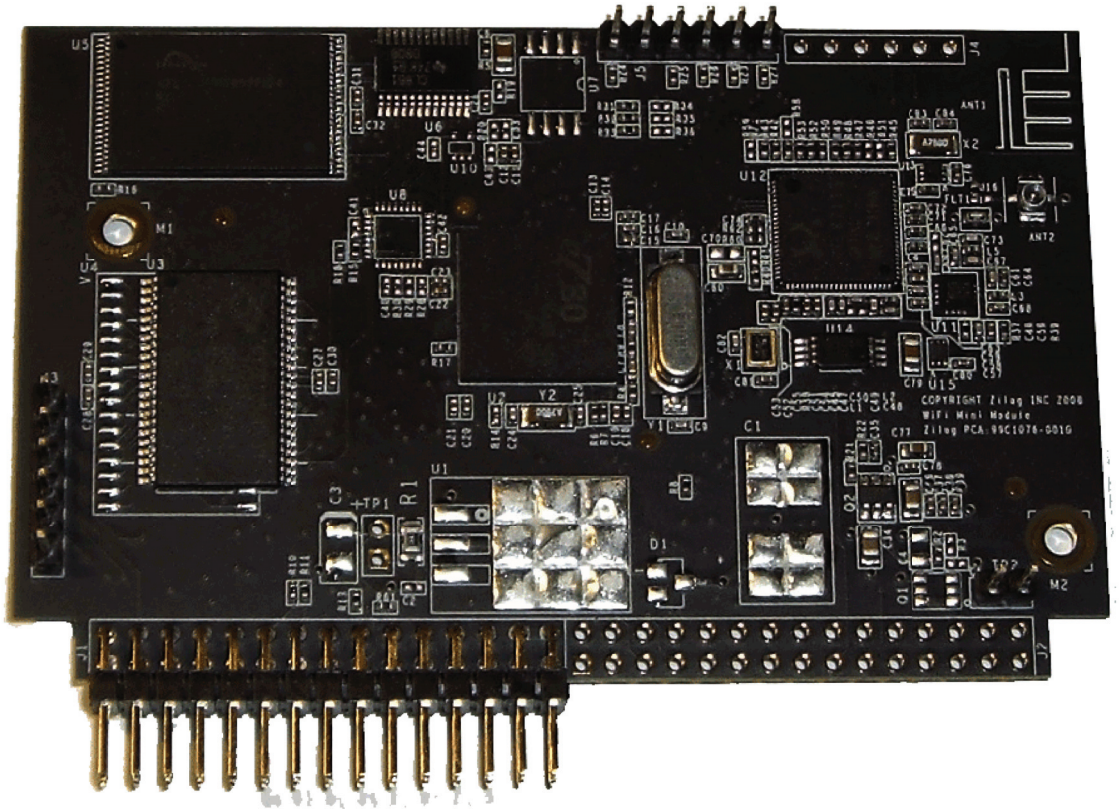

Figure 2. eZ80AcclaimPlus!™ Wireless Zdots® SBC

Note: *Pin 1 for J1, J2, J3, and J4 is indicated by a square on the bottom side of the board.*

Dedicated UART0 (Input/Output) Connector

See Table 4 on page 8 for a list of pins, symbols, and descriptions for the Zdots® SBC peripheral bus connector (J1). See Table 5 on page 10 for a list of pins, symbols, and descriptions for the Zdots SBC input/output connector (J2).

Note: *UART pins are 3.3 V input/output levels.*

Table 1. J3—Power/UART0 I/O

Pin Number	Description
1	VCC (3.3 V)
2	UART0 CTS (PD3)
3	UART0 RTS (PD2)
4	UART0 RXD (PD1)
5	UART0 TXD (PD0)
6	Ground

Table 2. Test Points and Shunts

Name	Description	
TP2	Test Points	
	1	Ground
	2	Ground

Table 3. Internal Controls

Pin Name	Description
Chip Select 0 CS0	Byte-wide Flash U5 (up to 4 MB 3FFFFFH)
Chip Select 1 CS1	Byte-wide SRAM U3 or U4 (up to 1 MB FFFFFH)
Chip Select 2 CS2	PLD U8 (factory option)
Chip Select 3 CS3	NC
PA7/PWM3	U8 PLD_TDI (PLD programming)
PA6/PWM2	U8 PLD_TMS (PLD programming)
PA5/PWM1	U8 PLD_TCK (PLD programming)
PA4/PWM0	U8 PLD_TDO (PLD programming)
PA3//PWM3_OC3	U8 PLD_Spare (optional use)
PA2/PWM2_OC2	U12 INT (input to eZ80)
PA1/PWM1_OC1	DC_OUT enable (Low enables output power on J2 pin 26)
PA0/PWM0_OC0	Wireless power enable (Low enables power to Wireless)
PB5	Prom_SS SPI Chip Select for U7 serial Flash

Table 3. Internal Controls (Continued)

Pin Name	Description
PB4	U12 SS SPI Chip Select
PB1	U8 PLD_Done (PLD programming)
PB0	U8 PLD_EN (PLD control)

Expansion Connectors Pin Description

Expansion Connector J1

Figure 3 displays the pin layout of the 30-pin Zdots® SBC expansion connector J1. Table 4 describes the pins and their functions.

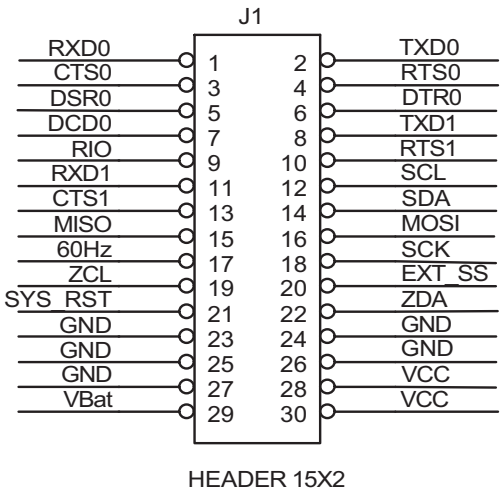

Figure 3. Zdots® SBC Expansion Connector J1 Pin Configuration

Table 4. Zdots® SBC Expansion Connector J1 Pin Functions*

Pin Number	Symbol	Signal Direction (with Respect to the Zdots SBC)	Comments
1	RXD0	Input (bidirectional)	UART0 RXD (PD1)
2	TXD0	Output (bidirectional)	UART0 TXD(PD0)
3	CTS0	Input (bidirectional)	UART0 CTS (PD3)
4	RTS0	Output (bidirectional)	UART0 RTS (PD2)
5	DSR0	Input (bidirectional)	UART0 DSR (PD5)
6	DTR0	Output (bidirectional)	UART0 DTR (PD4)
7	DCD0	Input (bidirectional)	UART0 DCD (PD6)
8	TXD1	Output (bidirectional)	UART1 TXD (PC0)
9	RIO	Input (bidirectional)	UART0 RI (PD7)
10	RTS1	Output (bidirectional)	UART1 RTS (PC2)

Table 4. Zdots® SBC Expansion Connector J1 Pin Functions* (Continued)

Pin Number	Symbol	Signal Direction (with Respect to the Zdots SBC)	Comments
11	RXD1	Input (bidirectional)	UART1 RXD (PC1)
12	SCL	Bidirectional	I^2C clock
13	CTS1	Input (bidirectional)	UART1 CTS (PC3)
14	SDA	Bidirectional	I^2C data
15	MISO	Input (bidirectional)	SPI MISO (PB6)
16	MOSI	Output (bidirectional)	SPI MOSI (PB7)
17	60 Hz	Input	NC (60 HZ RTC Clock IN)
18	SCK	Output (bidirectional)	SPI clock (PB3)
19	ZCL	Input	ZDI clock, debugging interface
20	EXT_SS	Output (bidirectional)	SPI slave select (PB2)
21	–SYS_RST	Bidirectional	System reset, active Low
22	ZDA	Bidirectional	ZDS data, debugging interface
23	GND	Power	Ground
24	GND	Power	Ground
25	GND	Power	Ground
26	GND	Power	Ground
27	GND	Power	Ground
28	V_{CC}	Power	VCC input 3.3
29	VBat	Power, battery	VBat input
30	V_{CC}	Power	VCC input 3.3

*All inputs are CMOS level 3.3 V (5 V tolerant), except where otherwise noted.

Expansion Connector J2

Figure 4 displays the pin layout of the 30-pin Zdots® SBC expansion connector J2. Table 5 describes the pins and their functions.

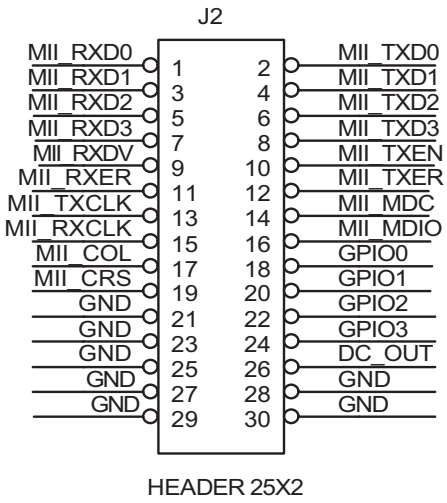

Figure 4. Zdots® SBC Expansion Connector J2 Pin Configuration

Table 5. Zdots® SBC Expansion Connector J2 Pin Functions*

Pin Number	Symbol	Signal Direction	Comments
1	MII_RXD0	Input	
2	MII_TXD0	Output	
3	MII_RXD1	Input	
4	MII_TXD1	Output	
5	MII_RXD2	Input	
6	MII_TXD2	Output	
7	MII_RXD3	Input	
8	MII_TXD3	Output	
9	MII_RXDV	Input	
10	MII_TXEN	Output	
11	MII_RXER	Input	
12	MII_TXER	Output	

Table 5. Zdots® SBC Expansion Connector J2 Pin Functions* (Continued)

Pin Number	Symbol	Signal Direction	Comments
13	MII_TXCLK	Input	
14	MII_MDC	Output	
15	MII_RXCLK	Input	
16	MII_MDIO	Bidirectional	
17	MII_COL	Input	
18	GPIO0	Bidirectional	PC4 (UART1 DTR)
19	MII_CRS	Input	
20	GPIO1	Bidirectional	PC5 (UART1 DSR)
21	GND	Power	Ground
22	GPIO2	Bidirectional	PC6 (UART1 DCD)
23	GND		Ground
24	GPIO3	Bidirectional	PC7 (UART1 RI)
25	GND	Power	Ground
26	DC_OUT	Output	Power Output (100 mA maximum)
27	GND	Power	Ground
28	GND	Power	Ground
29	GND	Power	Ground
30	GND	Power	Ground

*All inputs are CMOS level 3.3 V (5 V tolerant), except where otherwise noted.

On-Board Component Description

Power Options for the Real-Time Clock

An on-board SuperCap C1 (capacitance 0.2 F, Panasonic, part number EEC-EN0F204J1) powers the 32 kHz real-time clock when the external power is removed. It is charged through diode D1 (ON Semiconductor, part number MMBD101LT1G) when external power is applied to the board. The SuperCap C1 is not soldered on the board. You can add as an option.

Memory

The Wireless Zdots® SBC contains off-chip Flash, SRAM, and on-chip Flash memory and SRAM. The off-chip Flash of Zdots SBC has an access time of 70 ns. This access time requires four wait states to be added to the cycle when accessing external Flash at 50 MHz clock speed. There is up to 1 MB of fast SRAM on the Zdots SBC. Access time is 10 ns, which requires an additional one wait-state when accessing it.

Serial Interface Ports

The eZ80F91 contains two UARTs with programmable baud rate generators. UART0 is connected to J1 and J3. UART1 is connected to J1.

Note: *Do not connect an RS-232 interface without level shifters. There are no RS-232 level shifters on the Zdots SBC.*

Physical Dimensions

The dimensions of the Wireless Zdots® SBC (see Figure 5) are 2.20 inches x3.50 inches (55.88 mm x 88.90 mm).

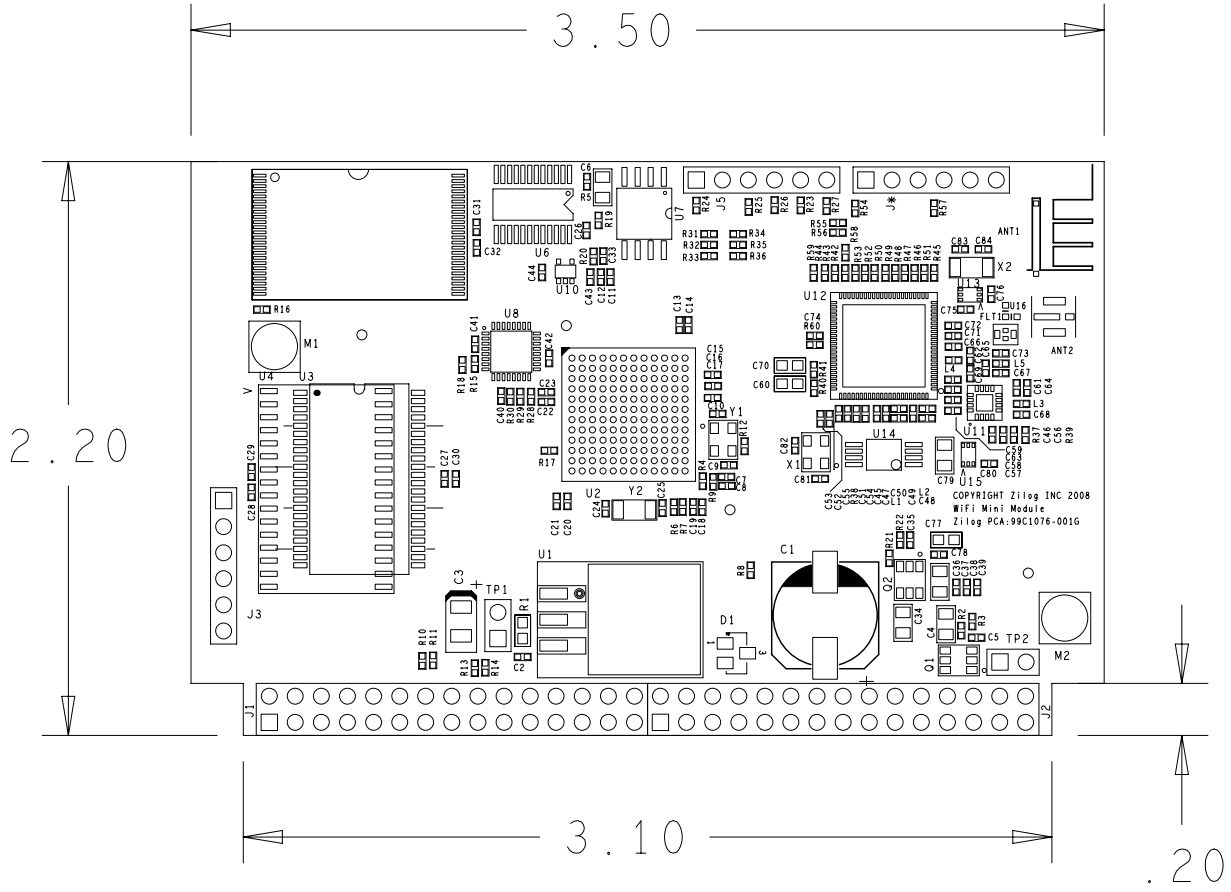

Figure 5. Physical Dimensions of the eZ80AcclaimPlus!™ Wireless Zdots® SBC

Absolute Maximum Ratings

Stresses greater than those listed in Table 6 on page 14 causes permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 6. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating humidity (RH @ 50 ºC)	25%	90%	
Operating voltage	3.0	3.6	V

Zdots® SBC Preliminary Engineering Parts List

Table 7 lists the installed components of the Wireless Zdots SBC.

Table 7. Preliminary Engineering Parts List for the Wireless Zdots® SBC

Part Name	Quantity	Location
IC, VLTG REG, 3.3 V, 0.8 A, TO-263	1	U1
IC, CPU, eZ80F91, BGA-144	1	U2
IC, SRAM, 1Mx8, 3 V, 10 ns, TSOP-44	1	U3
IC, SRAM, 128Kx8, 3 V, 10 ns, TSOP-32	1	U4 Install either U3 or U4, not both
IC, FLASH, 4Mx8, BOT, 3 V, 70 ns, TSOP-48	1	U5
IC, FET BUS SWITCH, 10 BIT, 3 V, TSSOP-24	1	U6
IC, SERIAL FLASH, 2 MB, SPI, 3 V, SOIC-8 (Optional)	1	U7
IC, CPLD, 32-CELL, 6 ns, QFN-32	1	U8
RTL8711	1	U9
IC, VLTG REG, 1.8 V, 50 mA, SOT-323	1	U10
DIODE, SCHOTTKY, 7 V, 0.25 µA LEAK, SOT-23	1	D1
MOSFET, P-CHAN, 20 V, 5.8 A, 2.5 V Vgs, 43 mΩ Rds, SOT-6	2	Q1, Q2
CONN, HDR/PIN, 2x15, 0.025SQ, DUAL ROW	2	J1, J2
CRYSTAL, 5.0 MHz, 18 pF, HC49US	1	Y1
CRYSTAL, 32.768 kHz, 12.5 pF, 4.9x1.8 SMD	1	Y2
SUPERCAP, 0.2 F, 3.3 V, COIN (Optional)	1	C1

Related Documentation

The documents associated with ZTP and RZK available for download on www.zilog.com are provided below:

- Zilog Full-Feature TCP/IP Software Suite Product Brief (PB0154)
- Zilog TCP/IP Software Suite Quick Start Guide (QS0049)
- Zilog TCP/IP Software Suite Programmer's Guide (RM0041)
- Zilog TCP/IP Stack API Reference Manual (RM0040)
- Zilog Real-Time Kernel Product Brief (PB0155)
- Zilog Real-Time Kernel Quick Start Guide (QS0048)
- Zilog Real-Time Kernel Reference Manual (RM0006)

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