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eZ80F92 Development Kit

User Manual

UM013911-0607

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Safeguards

The following precautions must be observed when working with the devices described in this document.

Caution: Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

Table of Contents

Introduction

The eZ80F92 Development Kit provides a general-purpose platform for evaluating the capabilities and operation of ZiLOG's eZ80F92 microcontroller. The eZ80F92 is a member of ZiLOG's eZ80Acclaim!® product line, which offers on-chip Flash capability. The eZ80F92 Development Kit features two primary boards: the eZ80Acclaim!® Development Platform and the eZ80F92 Flash Module. This arrangement provides a full development platform when using both boards. It can also provide a smaller-sized reference platform with the eZ80F92 Flash Module as a stand-alone development tool.[1]

Kit Features

The key features of the eZ80F92 Development Kit are:

- eZ80Acclaim!® Development Platform:
  - Up to 2MB fast SRAM (12ns access time; 1MB factory-installed, with 512KB on module, 512KB on platform)
  - Embedded modem socket with a U.S. telephone line interface
  - I^2C EEPROM
  - I^2C configuration register
  - GPIO, logic circuit, and memory headers
  - Supported by ZiLOG Developer Studio II and the eZ80Acclaim!® C-Compiler
  - LEDs, including a 7x5 LED matrix
  - Platform configuration jumpers

1. Other members of the eZ80Acclaim!® product line include the eZ80F91 and eZ80F93 microcontrollers. A scaled-down eZ80F92 Ethernet Module is also available. Contact your local ZiLOG Sales Office for more information.

  - Two RS232 connectors—console, modem
  - RS485 connector with cable assembly
  - ZiLOG Debug Interface (ZDI)
  - JTAG Debug Interface
  - 9 VDC power connector
  - Telephone jack
- eZ80F92 Flash Module:
  - eZ80F92 microcontroller[2] operating at 20 MHz, with 128 KB + 256 bytes internal Flash and 8 KB internal SRAM
  - 512 KB off-chip SRAM
  - Real-Time Clock with Battery Back-Up
- ZPAK II Debug Interface
- eZ80F92 Development Kit Software and Documentation CD-ROM

Hardware Specifications

Table 1 lists the specifications of the eZ80Acclaim!® Development Platform.

Table 1. eZ80Acclaim!® Development Platform Hardware Specifications

Operating Temperature:	20ºC ±5ºC
Operating Voltage:	9 VDC

2. Also available is the eZ80F93 microcontroller, which features 64 KB of internal Flash memory and 4 KB of internal SRAM. Please contact your local ZiLOG Sales Office for details.

eZ80F92 Development Board Revision History

99C0858-001 Rev C or later:

10/20/03 - Updated layout and added reset fix.

05/30/06 - The following components are not populated on the board:

- U11: Triac, SCR Phone Line D0-214
- U26 and U27: IC RS485, XCVR, Low PWR, 8-SOIC
- C3 and C4: CAP 1000pF Ceramic Disc 1KV
- D1 and D3: Diode LED Amber 0805 SMT
- T1: Inductor Ferrite Bead, 2x15 Turns
- J1: Conn HDR/Pin 1x32 2mm socket
- J5: Conn HDR/Pin 1x2 2mm socket
- J9: Conn HDR/Pin 1x9 2mm socket
- P4: Conn RJ14 Jack 6-Pos 4-CKT
- P5: Conn 9-CKT Cir rt-angl PC Mount

eZ80Acclaim!® Development Platform Overview

The purpose of the eZ80Acclaim!® Development Platform is to provide the developer with a set of tools for evaluating the features of the eZ80Acclaim!® family of devices, and to be able to develop a new application before building application hardware.

The eZ80F92 Development Kit features two primary boards: the eZ80Acclaim!® Development Platform and the eZ80F92 Flash Module. This arrangement provides a full development platform when using both boards. It can also provide a smaller-sized reference platform with the eZ80F92 Flash Module as a stand-alone development tool.

The eZ80Acclaim!® Development Platform is designed to accept a number of application-specific modules and Z8- and eZ80Acclaim!®-based add-on modules, including the eZ80F92 Flash Module, which features a real-time clock, an IrDA transceiver, and the eZ80F92 microcontroller.

The eZ80Acclaim!® Development Platform, together with its plugged-in eZ80F92 Flash Module, can operate in stand-alone mode with Flash memory, or interface via the ZPAK II emulator to a host PC running ZiLOG Developer Studio II Integrated Development Environment (ZDS IDE) software.

The address bus, data bus, and all eZ80F92 Flash Module control signals are buffered on the eZ80Acclaim!® Development Platform to provide sufficient drive capability.

A block diagram of the eZ80Acclaim!® Development Platform and the eZ80F92 Flash Module is shown in Figure 1.

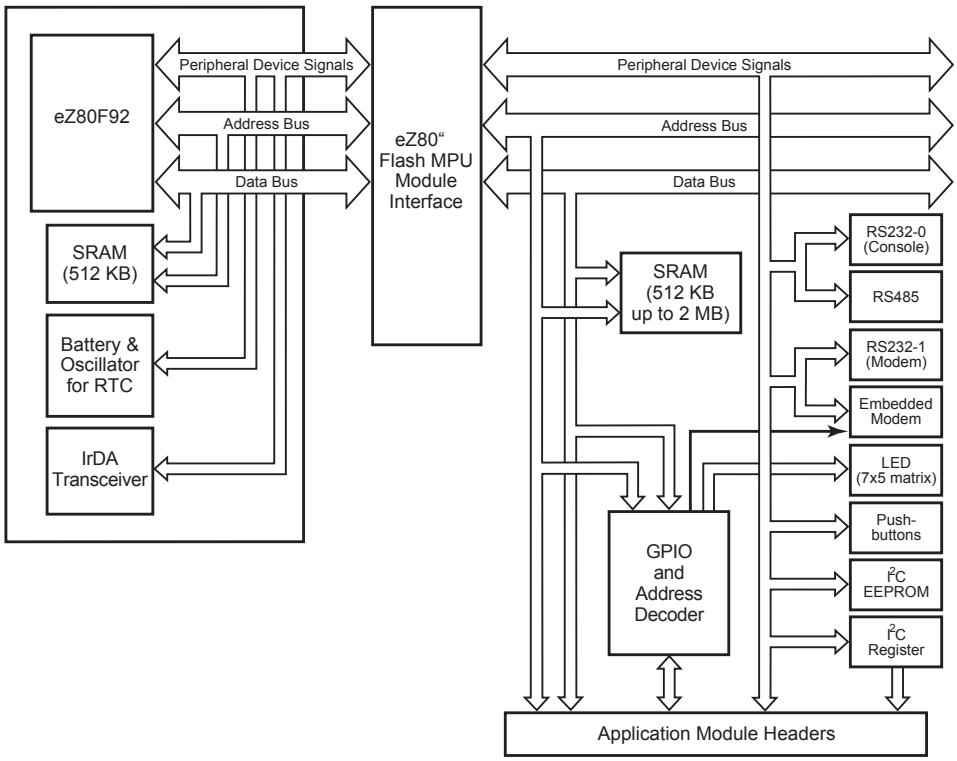
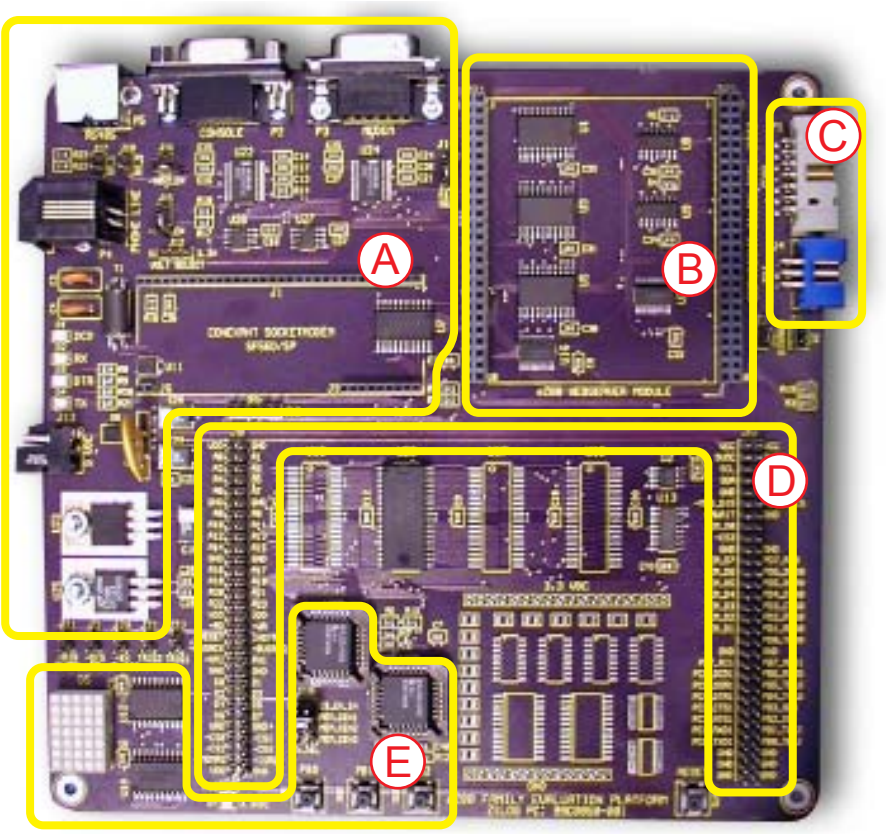


Figure 1. eZ80Acclaim!® Development Platform Block Diagram with eZ80F92 Flash Module

Figure 2 is a photographic representation of the eZ80Acclaim!® Development Platform segmented into its key blocks, as shown in the legend for the figure.

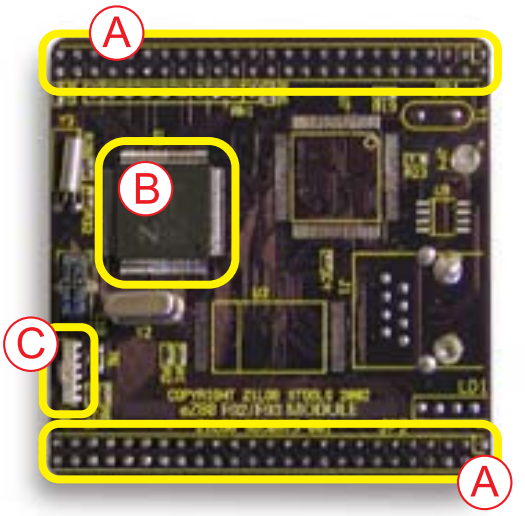


Note: Key to blocks A–E.

A. Power and serial communications.
B. eZ80F92 Flash Module interface.
C. Debug interface.
D. Application module interfaces.
E. GPIO and LED with Address Decoder.

Figure 2. The eZ80Acclaim!® Development Platform

Figure 3 is a photographic representation of the eZ80F92 Flash Module segmented into its key blocks, as shown in the legend for the figure.



Note: Key to blocks A–C.
A. eZ80F92 Flash Module interfaces.
B. CPU.
C. IrDA transceiver.

Figure 3. The eZ80F92 Flash Module

The structures of the eZ80Acclaim!® Development Platform and the eZ80F92 Flash Module are illustrated in the Schematic Diagrams starting on page 61.

eZ80Acclaim!® Development Platform

This section describes the eZ80Acclaim!® Development Platform hardware, its key components and its interfaces, including detailed programmer interface information such as memory maps, register definitions, and interrupt usage.

Functional Description

The eZ80Acclaim!® Development Platform consists of seven major hardware blocks. These blocks, listed below, are diagrammed in Figure 4.

- eZ80F92 Flash Module interface (2 female headers)
- Power supply for the eZ80Acclaim!® Development Platform, the eZ80F92 Flash Module, and application modules
- Application Module interface (2 male headers)
- GPIO and LED matrix
- RS232 serial communications ports
- Embedded modem interface
- I^2C devices

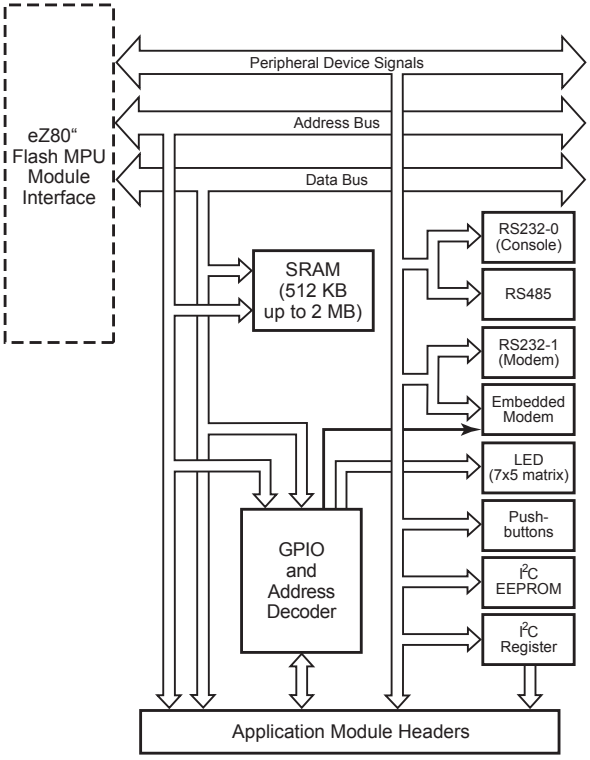


Figure 4. Basic eZ80Acclaim!® Development Platform Block Diagram

Physical Dimensions

The dimensions of the eZ80Acclaim!® Development Platform PCB is 177.8mm x 182.9mm. The overall height is 38.1mm. See Figure 5.

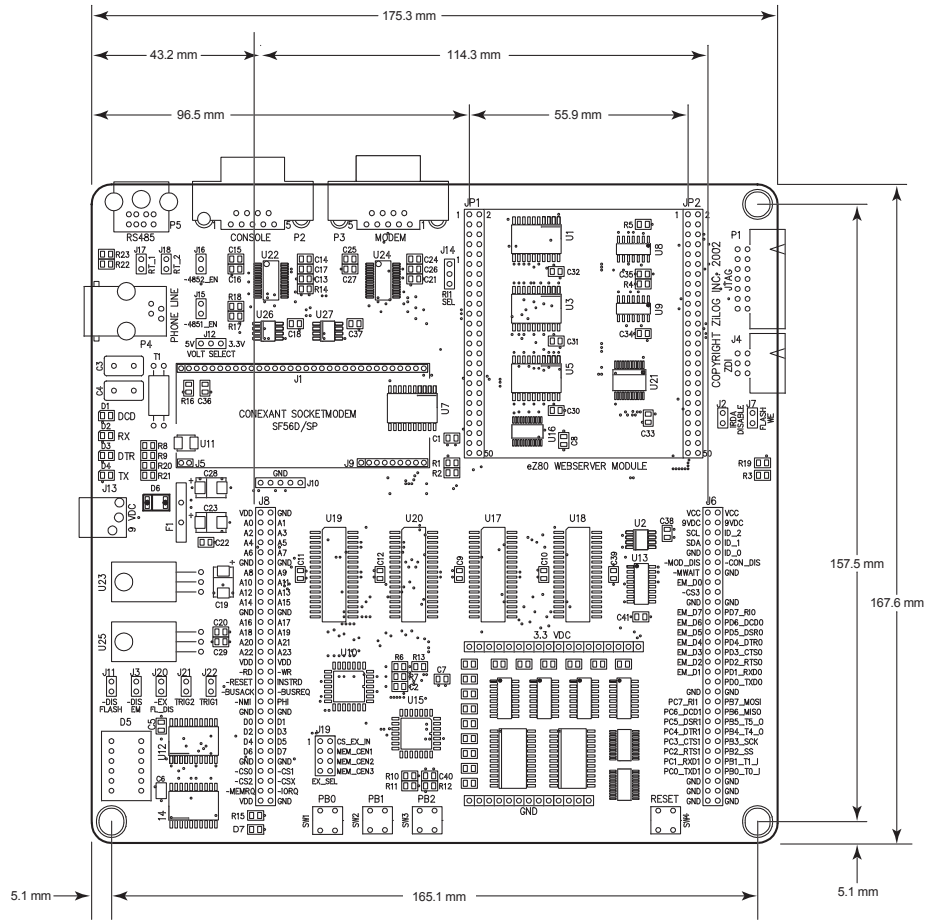


Figure 5. Physical Dimensions of the eZ80Acclaim!® Development Platform

Operational Description

The eZ80Acclaim!® Development Platform can accept any eZ80Acclaim!®-core-based modules, provided that the module interfaces correctly to the eZ80Acclaim!® Development Platform. The purpose of the eZ80Acclaim!® Development Platform is to provide the application developer with a tool to evaluate the features of the eZ80F92 Flash MCU, and to develop an application without building additional hardware.

eZ80F92 Flash Module Interface

The eZ80F92 Flash Module interface provides easy connection of the eZ80F92 Flash Module. It also provides easy connection for any eZ80Acclaim!®-based module designed to this interface. This includes modules using future eZ80Acclaim!® devices, and user-developed modules using current eZ80Acclaim!® devices.

The eZ80F92 Flash Module interface consists of two 50-pin receptacles, JP1 and JP2.

Peripheral Bus Connector

Figure 6 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header, located at position JP1 on the eZ80Acclaim!® Development Platform. Table 2 describes the pins and their functions.

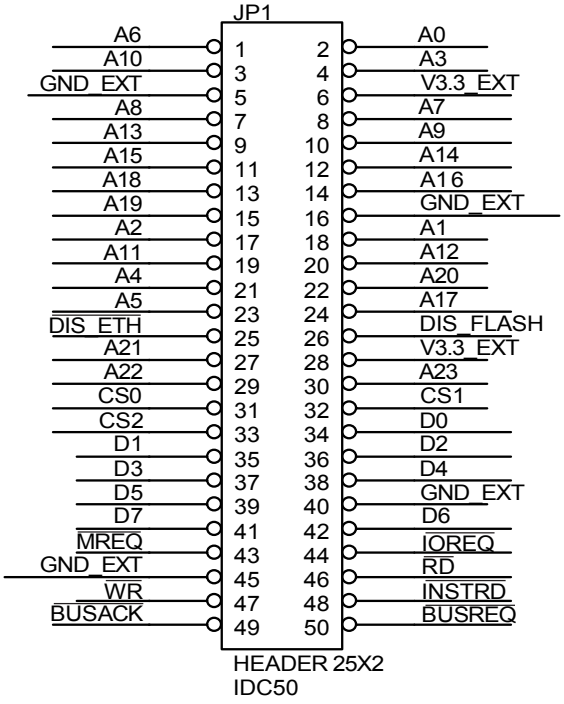


Figure 6. eZ80Acclaim!® Development Platform Peripheral Bus Connector Pin Configuration—JP1

Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1*

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
1	A6	Bidirectional		Yes
2	A0	Bidirectional		Yes
3	A10	Bidirectional		Yes
4	A3	Bidirectional		Yes
5	GND			
6	V_{DD}			
7	A8	Bidirectional		Yes
8	A7	Bidirectional		Yes
9	A13	Bidirectional		Yes
10	A9	Bidirectional		Yes
11	A15	Bidirectional		Yes
12	A14	Bidirectional		Yes
13	A18	Bidirectional		Yes
14	A16	Bidirectional		Yes
15	A19	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.
3. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform
Peripheral Bus Connector Identification—JP1* (Continued)**

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
16	GND			
17	A2	Bidirectional		Yes
18	A1	Bidirectional		Yes
19	A11	Bidirectional		Yes
20	A12	Bidirectional		Yes
21	A4	Bidirectional		Yes
22	A20	Bidirectional		Yes
23	A5	Bidirectional		Yes
24	A17	Bidirectional		Yes
25	$\overline{\text{DIS\_ETH}}$	Output	Low	No
26	$\overline{\text{EN\_FLASH}}$	Output	Low	No
27	A21	Bidirectional		Yes
28	V_{DD}			
29	A22	Bidirectional		Yes
30	A23	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.
3. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92's Peripheral Power-Down Register.

Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1* (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
31	CS0	Input	Low	Yes
32	CS1	Input	Low	Yes
33	CS2	Input	Low	Yes
34	D0	Bidirectional		Yes
35	D1	Bidirectional		Yes
36	D2	Bidirectional		No
37	D3	Bidirectional		Yes
38	D4	Bidirectional		Yes
39	D5	Bidirectional		Yes
40	GND			
41	D7	Bidirectional		Yes
42	D6	Bidirectional		Yes
43	$\overline{\text{MREQ}}$	Bidirectional	Low	Yes
44	$\overline{\text{IORQ}}$	Bidirectional	Low	Yes
45	GND			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.
3. External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92's Peripheral Power-Down Register.

Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1* (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
46	$\overline{RD}$	Bidirectional	Low	Yes
47	$\overline{WR}$	Bidirectional	Low	Yes
48	$\overline{INSTRD}$	Input	Low	Yes
49	$\overline{BUSACK}$	Input	Pull-Up 10KΩ; Low	Yes
50	$\overline{BUSREQ}$	Output	Pull-Up 10KΩ; Low	Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.
3. External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F92's Peripheral Power-Down Register.

I/O Connector

Figure 7 illustrates the pin layout of the I/O Connector in the 50-pin header, located at position JP2 on the eZ80Acclaim!® Development Platform. Table 3 describes the pins and their functions.

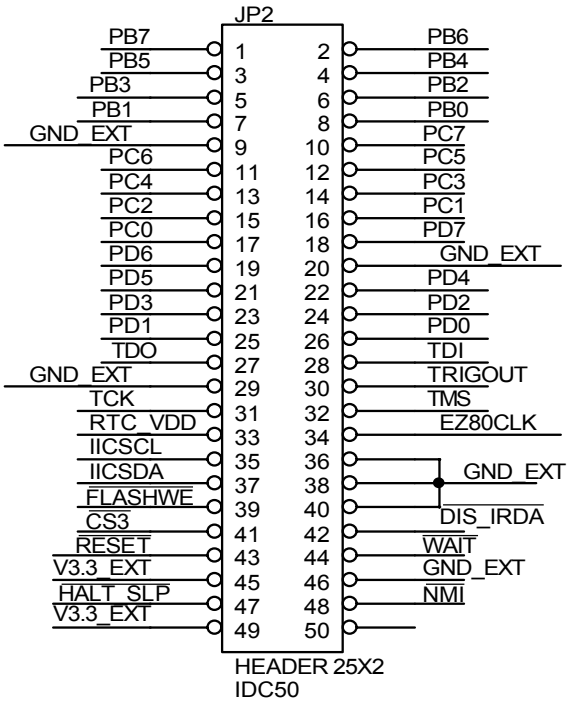


Figure 7. eZ80Acclaim!® Development Platform I/O Connector Pin Configuration—JP2

Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2*

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
1	PB7	Bidirectional		Yes
2	PB6	Bidirectional		Yes
3	PB5	Bidirectional		Yes
4	PB4	Bidirectional		Yes
5	PB3	Bidirectional		Yes
6	PB2	Bidirectional		Yes
7	PB1	Bidirectional		Yes
8	PB0	Bidirectional		Yes
9	GND			
10	PC7	Bidirectional		Yes
11	PC6	Bidirectional		Yes
12	PC5	Bidirectional		Yes
13	PC4	Bidirectional		Yes
14	PC3	Bidirectional		Yes
15	PC2	Bidirectional		Yes
16	PC1	Bidirectional		Yes
17	PC0	Bidirectional		Yes
18	PD7	Bidirectional		Yes

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.

Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2* (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
19	PD6	Bidirectional		
20	GND			
21	PD5	Bidirectional		Yes
22	PD4	Bidirectional		Yes
23	PD3	Bidirectional		Yes
24	PD2	Bidirectional		Yes
25	PD1	Bidirectional		Yes
26	PD0	Bidirectional		Yes
27	TDO	Input		Yes
28	TDI/ZDA	Output		Yes
29	GND			
30	TRIGOUT	Input	High	
31	TCK/ZCL	Output		Yes
32	TMS	Output	High	Yes
33	RTC_V_{DD}			
34	EZ80CLK	Input		Yes
35	SCL	Bidirectional		Yes
36	GND			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.

Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2* (Continued)

Pin #	Symbol	Signal Direction	Active Level	eZ80F92 Signal[2]
37	SDA	Bidirectional		Yes
38	GND			
39	$\overline{\text{FlashWE}}$	Output	Low	No
40	GND			
41	$\overline{\text{CS3}}$	Input	Low	Yes
42	$\overline{\text{DIS\_IrDA}}$	Output	Low	No
43	$\overline{\text{RESET}}$	Bidirectional	Low	Yes
44	$\overline{\text{WAIT}}$	Output	Pull-Up 10KΩ; Low	Yes
45	V_{DD}			
46	GND			
47	$\overline{\text{HALT\_SLP}}$	Input	Low	Yes
48	$\overline{\text{NMI}}$	Output	Low	Yes
49	V_{DD}			
50	Reserved			

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80F92 Module Schematics on pages 65 through 67.
2. The Power and Ground nets are connected directly to the eZ80F92 device.

Almost all of the connectors' signals are received directly from the CPU. Three input signals, in particular, offer options to the application developer by disabling certain functions of the eZ80F92 Flash Module.

These three inputs are:

- Enable Flash ($\overline{\text{EN\_FLASH}}$)*
- Flash Write Enable ($\overline{\text{FlashWE}}$)*
- Disable IrDA ($\overline{\text{DIS\_IrDA}}$)

These three signals are described below.

Enable Flash*

When active Low, the $\overline{\text{EN\_FLASH}}$ input signal enables the Flash chip on the eZ80F92 Flash Module.

Flash Write Enable*

When active Low, the $\overline{\text{FlashWE}}$ input signal enables Write operations on the Flash boot block of the eZ80F92 Flash Module.

Disable IrDA

When the $\overline{\text{DIS\_IrDA}}$ input signal is pulled Low, the IrDA transceiver, located on the eZ80F92 Flash Module, is disabled. As a result, UART0 can be used with the RS232 or the RS485 interfaces on the eZ80Acclaim!® Development Platform.

Note: *These inputs are only used if external Flash is present on the eZ80F92 Flash Module (as shipped from the factory, external Flash is not installed).

Application Module Interface

An Application Module Interface is provided to allow the user to add an application-specific module to the eZ80Acclaim!® Development Platform. ZiLOG's Thermostat Application Module (not provided in the kit) is an example application-specific module that demonstrates an HVAC control system. Implementing an application module with the Application Module Interface requires that the eZ80F92 Flash Module also be