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# *eZ80L92 Development Kit*

## User Manual

UM012913-0407


www.zilog.com

# *Safeguards*

The following precaution must be taken care while working with the devices mentioned in this document.

**Caution:** Always use a grounding strap to prevent damage resulting from electrostatic discharge (ESD).

# *Table of Contents*

# *Introduction*

The eZ80L92 Development Kit, PSI #eZ80L920210ZCO, provides a general-purpose platform for evaluating the capabilities and operation of ZiLOG's eZ80L92 microprocessor. The eZ80L92 Development Kit features two primary boards: the eZ80Acclaim!® Development Platform and the eZ80L92 Module. This arrangement provides a complete development platform while using both the boards. It also provides a smaller-sized reference platform with the eZ80L92 Module as a stand-alone development tool.

## Key Features of the Development Kit

The key features of the eZ80L92 Development Kit are:

- eZ80Acclaim!® Development Platform:
  - Up to 2 MB fast SRAM (12 ns access time).
  - Embedded Modem Socket with a U.S. Telephone Line Interface.
  - $I^2C$ EEPROM.
  - $I^2C$ Configuration Register.
  - General-Purpose Port and Memory Headers.
  - Supported by ZiLOG Developer Studio II and the eZ80® C-Compiler.
  - LEDs, including a 7x5 LED matrix..
  - Jumpers.
  - Two RS232 connectors—Console, Modem.
  - RS485 connector.
  - ZiLOG Debug Interface (ZDI).
  - JTAG Debug Interface.
  - 9 V DC Power Connector.
  - Telephone Jack.

- eZ80L92 Module:
  - eZ80L92 microprocessor operating at 48 MHz
  - 1 MB Flash Memory
  - 512 KB SRAM
  - 10BaseT Ethernet Interface
  - Real time clock with battery back-up
- ZPAK II Debug Interface.
- 4-port 10BaseT Ethernet hub.
- eZ80L92 Development Kit Software and Documentation CD-ROM.

## Hardware Specifications

Table 1 lists the specifications of the eZ80Acclaim!® Development Platform.

**Table 1. eZ80® Development Platform Hardware Specifications**

| | |
|---|---|
| Operating Temperature | 20 ºC ±5 ºC |
| Operating Voltage | 9 V DC |

## eZ80L92 Development Board Revision History

### 99C0858-001 Rev C or later:

**10/20/03** - Updated layout and added reset fix.

**05/30/06** - The following components are not populated on the board:

- U11: Triac, SCR Phone Line D0-214
- U26 and U27: IC RS485, XCVR, Low PWR, 8-SOIC
- C3 and C4: CAP 1000pF Ceramic Disc 1KV
- D1 and D3: Diode LED Amber 0805 SMT
- T1: Inductor Ferrite Bead, 2x15 Turns

- J1: Conn HDR/Pin 1x32 2mm socket
- J5: Conn HDR/Pin 1x2 2mm socket
- J9: Conn HDR/Pin 1x9 2mm socket
- P4: Conn RJ14 Jack 6-Pos 4-CKT
- P5: Conn 9-CKT Cir rt-angl PC Mount

## eZ80Acclaim!® Development Platform Overview

The purpose of the eZ80L92 Development Kit is to provide the developer with a set of tools for evaluating the features of the eZ80® family of devices and to develop a new application before building application hardware. The eZ80Acclaim!® Development Platform is designed to accept a number of application-specific modules and Z8® and eZ80® based add-on modules, including the eZ80L92 Module, which features an EMAC, an IrDA transceiver, and the eZ80L92 microprocessor.

The eZ80L92 Development Kit features two primary boards: the eZ80Acclaim!® Development Platform and the eZ80L92 Module. This arrangement provides a complete development platform while using both boards. It can also provide a smaller-sized reference platform with the eZ80L92 Module as a stand-alone development tool.

The eZ80Acclaim!® Development Platform can operate in stand-alone mode with Flash memory, or interface via the ZPAK II emulator to a host PC running ZiLOG Developer Studio II Integrated Development Environment (ZDS II IDE) software. If the eZ80Acclaim!® application demands Internet connectivity or a network connection, the eZ80® can serve web pages over a TCP/IP network allowing easy system monitoring and control, and effortless processor code updates.

The address bus, data bus, and all eZ80L92 Module control signals are buffered on the eZ80Acclaim!® Development Platform to provide sufficient drive capability. A block diagram of the eZ80Acclaim!® Development Platform and the eZ80L92 Module is shown in Figure 1.

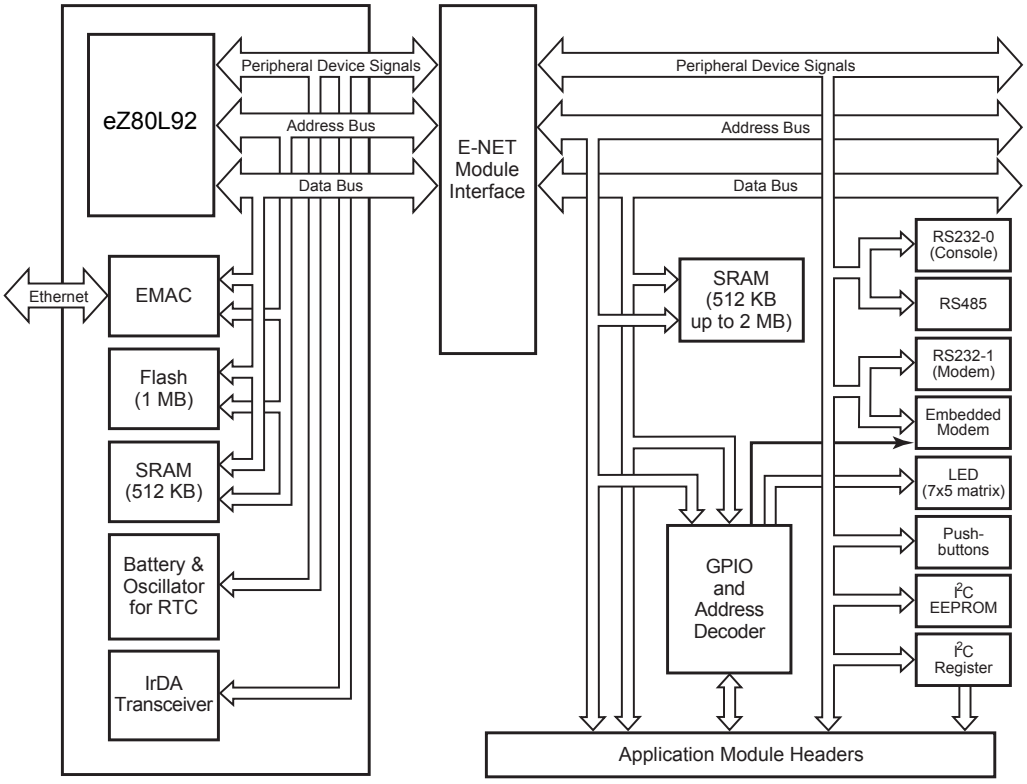
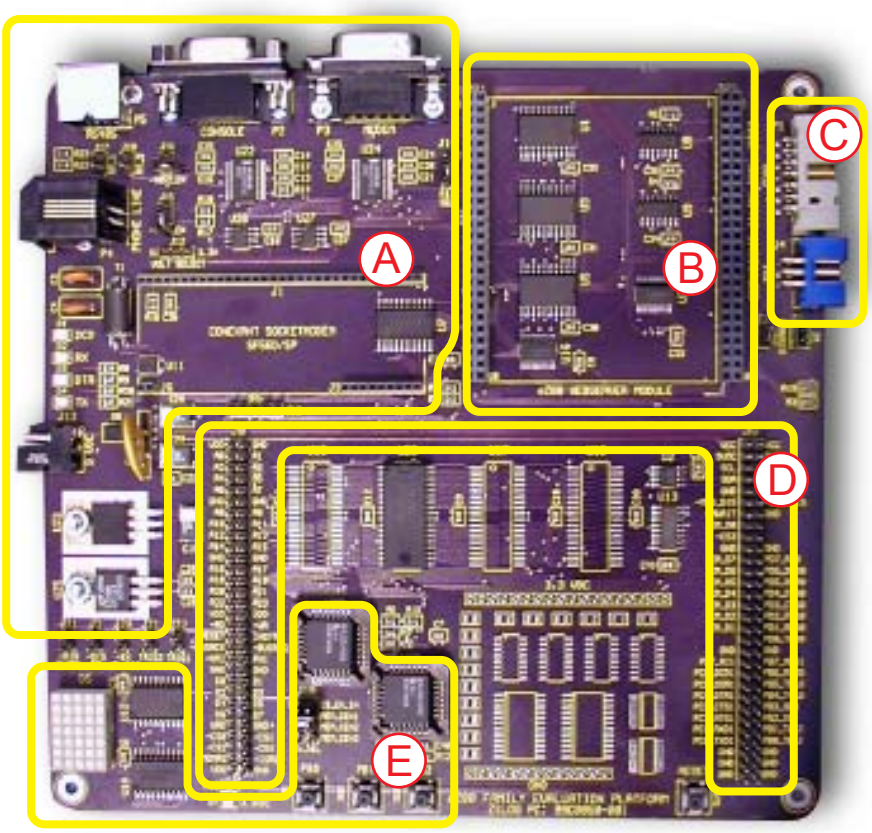



**Figure 1. eZ80Acclaim!® Development Platform Block Diagram with eZ80L92 Module**

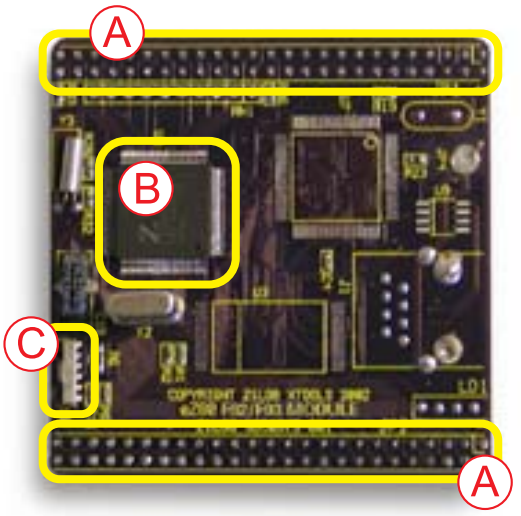
Figure 2 is a photographic representation of the eZ80Acclaim!® Development Platform segmented into its key blocks.




Note: Key blocks A–E
A. Power and serial communications.
B. eZ80L92 Module interface.
C. Debug interface.
D. Application Module Interfaces.
E. General-Purpose Port and LED with Address Decoder.

**Figure 2. The eZ80Acclaim!® Development Platform**

Figure 3 is a photographic representation of the eZ80L92 Module segmented into its key blocks.




Note: Key blocks A–C.

A. eZ80L92 Module interfaces.
B. CPU and memory.
C. Ethernet connection.
D. IrDA transceiver.

**Figure 3. The eZ80L92 Module**

The structures of the eZ80Acclaim!® Development Platform and the eZ80L92 Module are illustrated in the Schematic Diagrams from page 61.

# *eZ80® Development Platform*

This chapter describes the eZ80Acclaim!® Development Platform hardware, its key components and the interfaces, including detailed programmer interface information like memory maps, register definitions, and interrupt usage.

## Functional Description

The eZ80Acclaim!® Development Platform consists of seven major hardware blocks. These blocks, listed below, are illustrated in Figure 4.

- eZ80L92 Module interface (2 female headers).
- Power supply for the eZ80Acclaim!® Development Platform, the eZ80L92 Module, and application modules.
- Application module interface (2 male headers).
- General-Purpose Port and LED matrix.
- RS232 serial communications ports.
- Embedded modem interface.
- $I^2C$ devices.

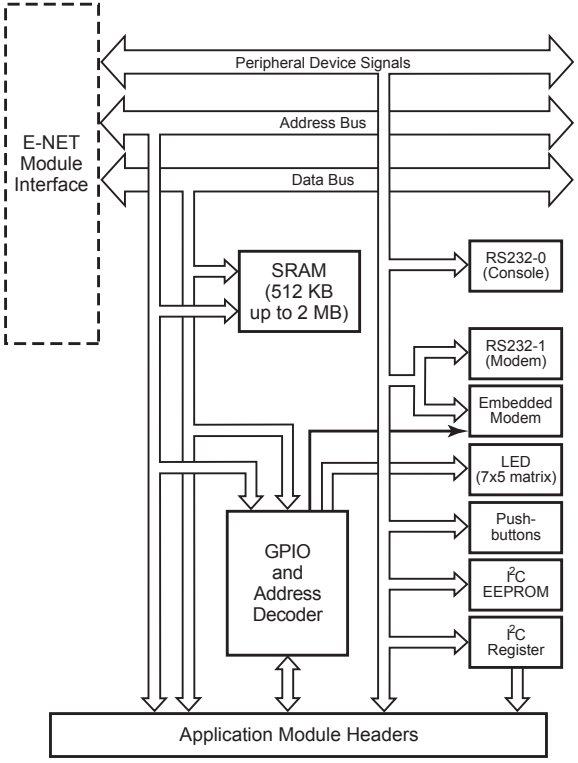



**Figure 4. Basic eZ80Acclaim!® Development Platform Block Diagram**

## Physical Dimensions

The dimension of the eZ80Acclaim!® Development Platform PCB is 177.8 mm x 182.9 mm. The overall height is 38.1 mm. See Figure 5.

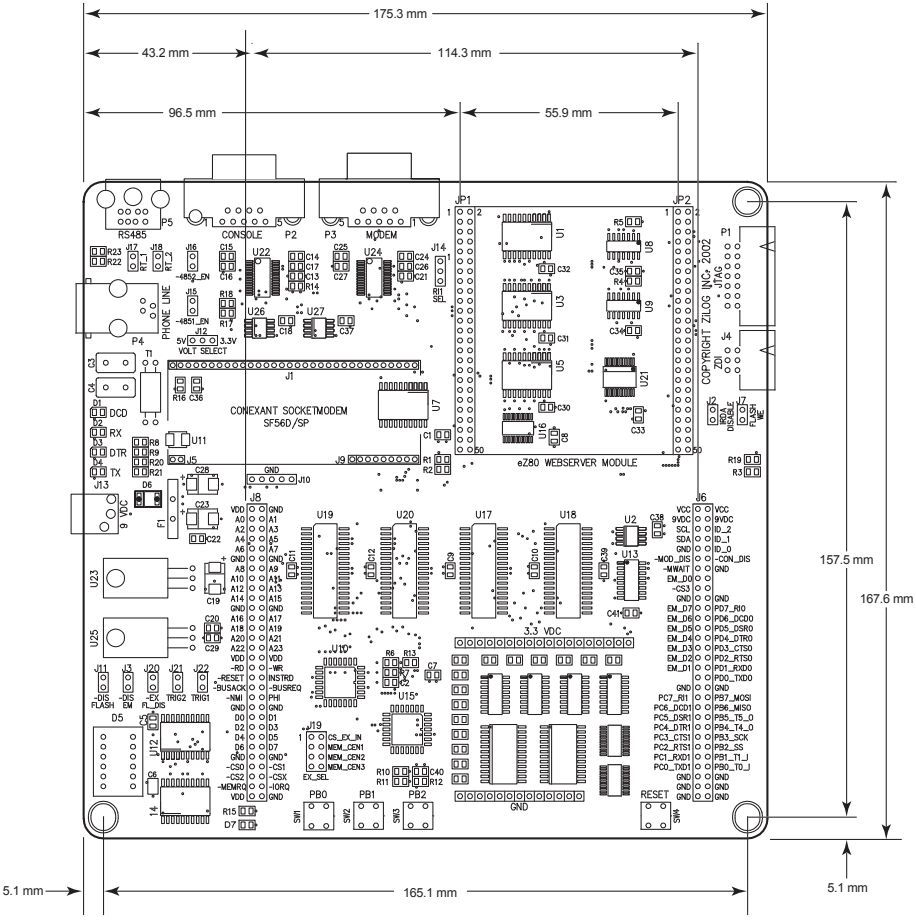



**Figure 5. Physical Dimensions of eZ80Acclaim!® Development Platform**

# Operational Description

The eZ80Acclaim!® Development Platform can accept any eZ80® core-based modules, provided that the module interfaces correctly to the eZ80Acclaim!® Development Platform. The purpose of the eZ80Acclaim!® Development Platform is to provide the application developer with a tool to evaluate the features of the eZ80L92 device and to develop an application without building additional hardware.

## eZ80L92 Module Interface

The eZ80L92 Module interface provides easy connection of the eZ80L92 Module. It also provides easy connection for any eZ80® based module designed to this interface. This includes modules using future eZ80® devices and user-developed modules using current eZ80® devices.

The eZ80L92 Module interface consists of two 50-pin receptacles, JP1 and JP2.

### Peripheral Bus Connector

Figure 6 illustrates the pin layout of the Peripheral Bus Connector in the 50-pin header located at position JP1 on the eZ80Acclaim!® Development Platform. Table 2 describes the pins and their functions.

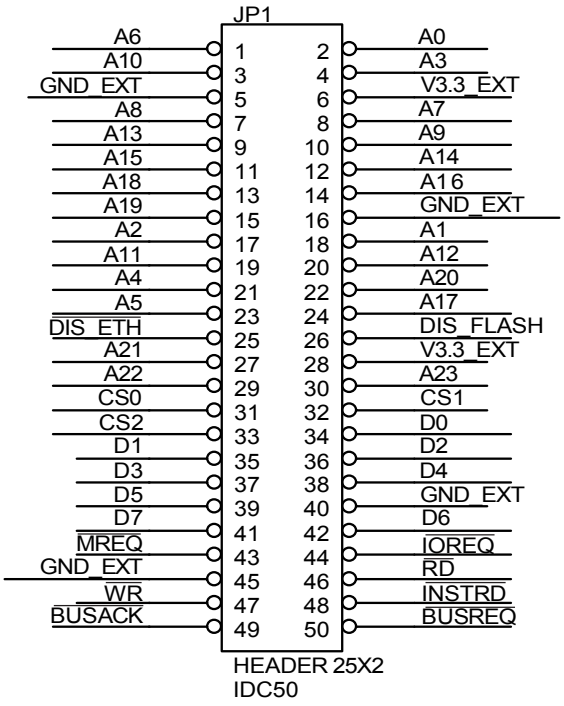



**Figure 6. eZ80Acclaim!® Development Platform Peripheral Bus Connector Pin Configuration—JP1**

**Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1[1]**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 1 | A6 | Bidirectional | | Yes |
| 2 | A0 | Bidirectional | | Yes |
| 3 | A10 | Bidirectional | | Yes |
| 4 | A3 | Bidirectional | | Yes |
| 5 | GND | | | |
| 6 | $V_{DD}$ | | | |
| 7 | A8 | Bidirectional | | Yes |
| 8 | A7 | Bidirectional | | Yes |
| 9 | A13 | Bidirectional | | Yes |
| 10 | A9 | Bidirectional | | Yes |
| 11 | A15 | Bidirectional | | Yes |
| 12 | A14 | Bidirectional | | Yes |
| 13 | A18 | Bidirectional | | Yes |
| 14 | A16 | Bidirectional | | Yes |
| 15 | A19 | Bidirectional | | Yes |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80L92 Module Schematics. see eZ80L92 Module.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either $V_{DD}$ or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1[1] (Continued)**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 16 | GND | | | |
| 17 | A2 | Bidirectional | | Yes |
| 18 | A1 | Bidirectional | | Yes |
| 19 | A11 | Bidirectional | | Yes |
| 20 | A12 | Bidirectional | | Yes |
| 21 | A4 | Bidirectional | | Yes |
| 22 | A20 | Bidirectional | | Yes |
| 23 | A5 | Bidirectional | | Yes |
| 24 | A17 | Bidirectional | | Yes |
| 25 | $\overline{\text{DIS\_ETH}}$ | Output | Low | No |
| 26 | $\overline{\text{EN\_FLASH}}$ | Output | Low | No |
| 27 | A21 | Bidirectional | | Yes |
| 28 | $V_{DD}$ | | | |
| 29 | A22 | Bidirectional | | Yes |
| 30 | A23 | Bidirectional | | Yes |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80L92 Module Schematics. see eZ80L92 Module.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

Additional note: external capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either $V_{DD}$ or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1[1] (Continued)**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 31 | CS0 | Input | Low | Yes |
| 32 | CS1 | Input | Low | Yes |
| 33 | CS2 | Input | Low | Yes |
| 34 | D0 | Bidirectional | | Yes |
| 35 | D1 | Bidirectional | | Yes |
| 36 | D2 | Bidirectional | | No |
| 37 | D3 | Bidirectional | | Yes |
| 38 | D4 | Bidirectional | | Yes |
| 39 | D5 | Bidirectional | | Yes |
| 40 | GND | | | |
| 41 | D7 | Bidirectional | | Yes |
| 42 | D6 | Bidirectional | | Yes |
| 43 | $\overline{\text{MREQ}}$ | Bidirectional | Low | Yes |
| 44 | $\overline{\text{IORQ}}$ | Bidirectional | Low | Yes |
| 45 | GND | | | |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80L92 Module Schematics. see eZ80L92 Module.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

Additional note: external capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either $V_{DD}$ or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92's Peripheral Power-Down Register.

**Table 2. eZ80Acclaim!® Development Platform Peripheral Bus Connector Identification—JP1[1] (Continued)**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 46 | $\overline{RD}$ | Bidirectional | Low | Yes |
| 47 | $\overline{WR}$ | Bidirectional | Low | Yes |
| 48 | $\overline{INSTRD}$ | Input | Low | Yes |
| 49 | $\overline{BUSACK}$ | Input | Pull-Up 10KΩ; Low | Yes |
| 50 | $\overline{BUSREQ}$ | Output | Pull-Up 10KΩ; Low | Yes |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The entire interface is represented in the eZ80L92 Module Schematics. see eZ80L92 Module.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

Additional note: external capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy the timing requirements for the eZ80® CPU. All unused inputs should be pulled to either $V_{DD}$ or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity. To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92's Peripheral Power-Down Register.

## I/O Connector

Figure 7 illustrates the pin layout of the I/O Connector in the 50-pin header located at position JP2 of the eZ80Acclaim!® Development Platform. Table 3 describes the pins and their functions.

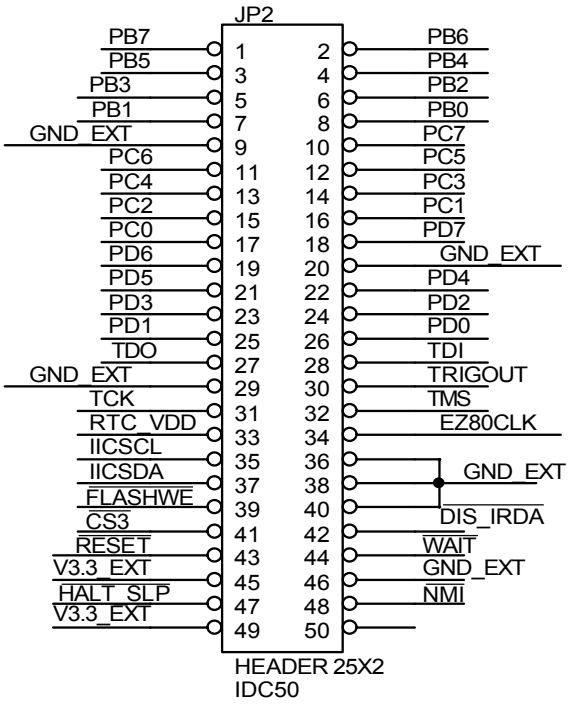



**Figure 7. eZ80Acclaim!® Development Platform I/O Connector Pin Configuration—JP2**

**Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2[1]**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 1 | PB7 | Bidirectional | | Yes |
| 2 | PB6 | Bidirectional | | Yes |
| 3 | PB5 | Bidirectional | | Yes |
| 4 | PB4 | Bidirectional | | Yes |
| 5 | PB3 | Bidirectional | | Yes |
| 6 | PB2 | Bidirectional | | Yes |
| 7 | PB1 | Bidirectional | | Yes |
| 8 | PB0 | Bidirectional | | Yes |
| 9 | GND | | | |
| 10 | PC7 | Bidirectional | | Yes |
| 11 | PC6 | Bidirectional | | Yes |
| 12 | PC5 | Bidirectional | | Yes |
| 13 | PC4 | Bidirectional | | Yes |
| 14 | PC3 | Bidirectional | | Yes |
| 15 | PC2 | Bidirectional | | Yes |
| 16 | PC1 | Bidirectional | | Yes |
| 17 | PC0 | Bidirectional | | Yes |
| 18 | PD7 | Bidirectional | | Yes |
| 19 | PD6 | Bidirectional | | |
| 20 | GND | | | |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The interface is represented in the eZ80L92 Module Schematics.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

**Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2[1]**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 21 | PD5 | Bidirectional | | Yes |
| 22 | PD4 | Bidirectional | | Yes |
| 23 | PD3 | Bidirectional | | Yes |
| 24 | PD2 | Bidirectional | | Yes |
| 25 | PD1 | Bidirectional | | Yes |
| 26 | PD0 | Bidirectional | | Yes |
| 27 | TDO | Input | | Yes |
| 28 | TDI/ZDA | Output | | Yes |
| 29 | GND | | | |
| 30 | TRIGOUT | Input | High | |
| 31 | TCK/ZCL | Output | | Yes |
| 32 | TMS | Output | High | Yes |
| 33 | RTC_$V_{DD}$ | | | |
| 34 | EZ80CLK | Input | | Yes |
| 35 | SCL | Bidirectional | | Yes |
| 36 | GND | | | |
| 37 | SDA | Bidirectional | | Yes |
| 38 | GND | | | |
| 39 | $\overline{\text{FlashWE}}$ | Output | Low | No |
| 40 | GND | | | |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The interface is represented in the eZ80L92 Module Schematics.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

**Table 3. eZ80Acclaim!® Development Platform I/O Connector Identification—JP2[1]**

| Pin No. | Symbol | Signal Direction | Active Level | eZ80L92 Signal[2] |
|---|---|---|---|---|
| 41 | $\overline{CS3}$ | Input | Low | Yes |
| 42 | $\overline{DIS\_IrDA}$ | Output | Low | No |
| 43 | $\overline{RESET}$ | Bidirectional | Low | Yes |
| 44 | $\overline{WAIT}$ | Output | Pull-Up 10 KΩ; Low | Yes |
| 45 | $V_{DD}$ | | | |
| 46 | GND | | | |
| 47 | $\overline{HALT\_SLP}$ | Input | Low | Yes |
| 48 | $\overline{NMI}$ | Output | Low | Yes |
| 49 | $V_{DD}$ | | | |
| 50 | Reserved | | | |

Notes:
1. For the sake of simplicity in describing the interface, Power and Ground nets are omitted from this table. The interface is represented in the eZ80L92 Module Schematics.
2. The Power and Ground nets are connected directly to the eZ80L92 device.

Almost all the connectors' signals are received directly from the CPU. Four input signals, in particular, offer options to the application developer by disabling certain functions of the eZ80L92 Module.

These four inputs signals are:

- Disable Ethernet ($\overline{DIS\_ETH}$)
- Enable Flash ($\overline{EN\_FLASH}$)
- Flash Write Enable ($\overline{FlashWE}$)
- Disable IrDA ($\overline{DIS\_IrDA}$)

These four inputs are described below.

### Disable Ethernet

When active Low, the $\overline{\text{DIS\_ETH}}$ output signal disables the EMAC from responding to CPU requests. As a result, additional inputs, outputs, or memory devices can be used in the CS3 address space. The logic that disables the Ethernet signal is listed in Appendix A on page 75.

### Enable Flash

When active Low, the $\overline{\text{EN\_FLASH}}$ input signal disables the Flash chip on the eZ80L92 Module.

### Flash Write Enable

When active Low, the $\overline{\text{FlashWE}}$ input signal enables Write operations on the Flash boot block of the eZ80L92 Module.

### Disable IrDA

When the $\overline{\text{DIS\_IrDA}}$ input signal is pulled Low, the IrDA transceiver, located on the eZ80L92 Module is disabled. As a result, UART0 can be used with the RS232 or the RS485 interfaces on the eZ80Acclaim!® Development Platform.

## Application Module Interface

An application module interface is provided to allow you to add an application-specific module to the eZ80Acclaim!® Development Platform. ZiLOG's Thermostat Application Module (not provided in the kit) is an example application-specific module that demonstrates an HVAC control system. Implementing an application module with the application module interface requires that the eZ80L92 Module also be mounted on the eZ80Acclaim!® Development Platform, as the eZ80L92 Module contains the eZ80L92 microprocessor. To mount an application module, use the two male headers J6 and J8.

Jumper J6 carries the general-purpose port and jumper J8 carries memory and control signals. To design an application module, you must be familiar with the architecture and features of the installed eZ80L92 Module. Table 4 and Table 5 list the signals and functions related to each of these jumpers by pin. Power and ground signals are omitted for the sake of simplicity.

**Table 4. General-Purpose Port Connector J6***

| Signal | Pin No. | Function | Direction | Notes |
|---|---|---|---|---|
| SCL | 5 | $I^2C$ Clock | Bidirectional | |
| SDA | 7 | $I^2C$ Data | Bidirectional | |
| $\overline{\text{MOD\_DIS}}$ | 9 | Modem Disable | Input | If a shunt is installed between pins 6 and 9, the modem function on the eZ80Acclaim!® Development Platform is disabled. |
| $\overline{\text{MWAIT}}$ | 13 | WAIT signal for the CPU | Input | |
| EM_D0 | 15 | GPIO, Bit 0 | Bidirectional | |
| $\overline{\text{CS3}}$ | 17 | Chip Select 3 of the CPU | Output | This signal is also present on the J8. |
| EM_D[7:1] | 21,23,25, 27,29,31, 33 | GPIO, Bit [7:1] | Bidirectional | |
| Reserved | 35 | | | |
| PC[7:0] | 39,41,43, 45,47,49, 51,53 | Port C, Bit [7:0] | Bidirectional | |

Note: All signals are driven directly by the CPU.