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eZ80L925048MOD

eZ80L92 Module

Product Specification

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Document Disclaimer

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The eZ80L92 Module

The eZ80L92 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity.

This low-cost, expandable module is powered by ZiLOG's latest power-efficient, high-speed, optimized pipeline architecture eZ80L92 device (eZ80L925048MOD), a member of ZILOG's new eZ80® microprocessor family.

The eZ80L92 microprocessor is a high-speed single-cycle instruction-fetch microprocessor, which can operate with a clock speed of 48MHz. It can operate in Z80-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of the eZ80L92 Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Module Features

- eZ80L92 MPU default factory operating clock frequency at 48MHz

- 10Base-T Ethernet Media Access Controller+ PHI with Onboard RJ45 connector

- 512KB zero-wait-state onboard SRAM

- 1MB onboard NOR Flash ROM (90–100ns)

- GoldCap backup for Real-Time Clock

- I/O connector provides 24 general-purpose 5V-tolerant I/O pinouts

- ZiLOG's industry-leading IrDA transceiver—ZiLOG ZHX1810

- In-circuit Flash programming circuitry

- Onboard connector provides I^{2}C 2-wire SDA/SCL interface

- Onboard connector provides I/O bus for external peripheral connections (IRQ, CS, 24 address, 8 data)

- Low-cost adaptation to carrier board   via two 2x25pin (2.54mm) headers

- Horizontal or vertical mounting onto the eZ80® Development Platform

- Small footprint 64x64mm; height is 24mm

- 3.3V power supply

- Standard operating temperature range: 0ºC to +70ºC

eZ80L92 Processor Features

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators
- SPI with independent clock rate generator
- I^2C with independent clock rate generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- New DMA-like eZ80® instructions for efficient block data transfer
- Glueless external memory interface with 4 chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate V_{DD} pin for battery backup
- Six 16-bit Counter/Timers with prescalers and direct input/output drive
- Watch-Dog Timer
- 24 bits of general-purpose I/O
- JTAG and ZDI debug interfaces
- 100-pin LQFP package
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Standard operating temperature range: 0ºC to +70ºC

> **Note:** All signals with an overline are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and $\overline{B}$/W, for which BYTE is active Low.

Block Diagram

Figure 1 illustrates a block diagram of the eZ80L92 Module.
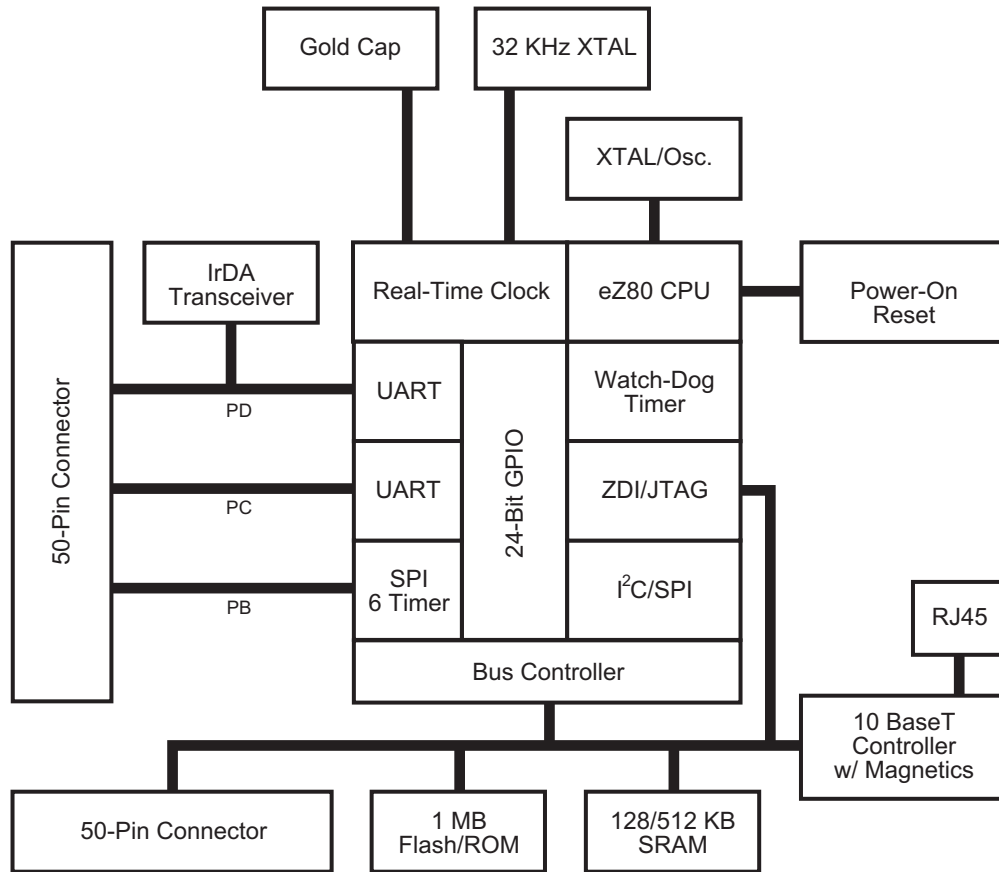
Figure 1. eZ80L92 Module Functional Block Diagram

Pin Description

Peripheral Bus Connector

Figure 2 illustrates the pin layout of the 50-pin I/O Connector, located at position JP1 on the eZ80L92 Module. Table 1 describes the pins and their functions.
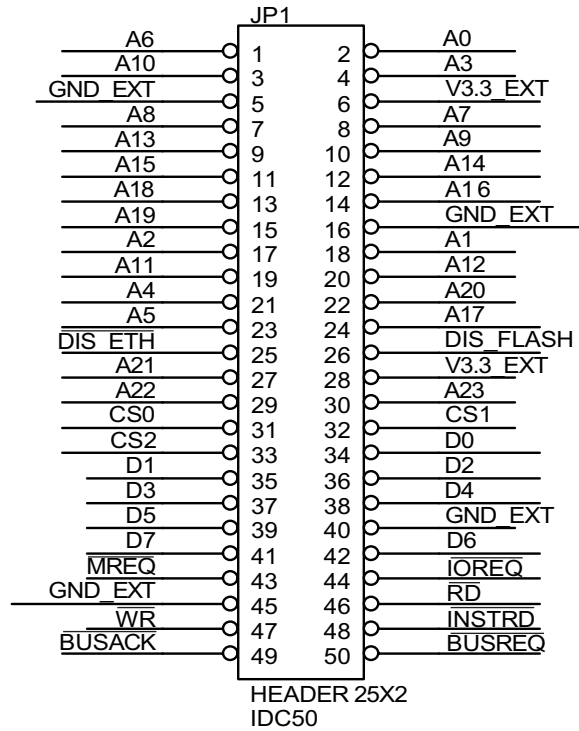
Figure 2. eZ80L92 Module Peripheral Bus Connector Pin Configuration

Table 1. eZ80L92 Module Peripheral Bus Connector Pin Identification*

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
1	A6		Bidirectional	
2	A0		Bidirectional	
3	A10		Bidirectional	
4	A3		Bidirectional	
5	GND			V_{SS}/Ground (0V).
6	V_{DD}			3.3V Supply Input Pin.
7	A8		Bidirectional	
8	A7		Bidirectional	
9	A13		Bidirectional	
10	A9		Bidirectional	
11	A15		Bidirectional	
12	A14		Bidirectional	
13	A18		Bidirectional	
14	A16		Bidirectional	
15	A19		Bidirectional	
16	GND			V_{SS}/Ground (0V).
17	A2		Bidirectional	
18	A1		Bidirectional	
19	A11		Bidirectional	
20	A12		Bidirectional	
21	A4		Bidirectional	
22	A20		Bidirectional	
23	A5		Bidirectional	
24	A17		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the eZ80® CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 1. eZ80L92 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
25	$\overline{\text{DIS\_Eth}}$	PU 10KΩ	Input	A Low disables on-module EMAC from responding to CS3 on a per-cycle basis. CS3 can be used on the eZ80® Development Platform; CMOS Input 3.3V (5V tolerant)
26	$\overline{\text{DIS\_Flash}}$	PU 10KΩ	Input	A Low disables on-module Flash memory from responding to CS0 on a per-cycle basis. CS0 can be used on the eZ80® Development Platform for external memory purposes; CMOS Input 3.3V (5V tolerant).
27	A21		Bidirectional	
28	V_{DD}			3.3V supply input pin.
29	A22		Bidirectional	
30	A23		Bidirectional	
31	$\overline{\text{CS0}}$		Output	
32	$\overline{\text{CS1}}$		Output	
33	$\overline{\text{CS2}}$		Output	
34	D0	PU 4k7Ω	Bidirectional	
35	D1	PU 4k7Ω	Bidirectional	
36	D2	PU 4k7Ω	Bidirectional	
37	D3	PU 4k7Ω	Bidirectional	
38	D4	PU 4k7Ω	Bidirectional	
39	D5	PU 4k7Ω	Bidirectional	
40	GND			V_{SS}/Ground (0V).
41	D7	PU 4k7Ω	Bidirectional	
42	D6		Bidirectional	
43	$\overline{\text{MREQ}}$		Bidirectional	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the eZ80® CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 1. eZ80L92 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
44	$\overline{\text{IORQ}}$		Bidirectional	
45	GND			V_{SS}/Ground (0V).
46	$\overline{\text{RD}}$		Bidirectional	
47	$\overline{\text{WR}}$		Bidirectional	
48	$\overline{\text{INSTRD}}$		Output	
49	$\overline{\text{BUSACK}}$	PU 10KΩ	Output	
50	$\overline{\text{BUSREQ}}$	PU 10KΩ	Input	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the eZ80® CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

I/O Connector

Figure 3 illustrates the pin layout of the 50-pin I/O Connector, located at position JP2 of the eZ80L92 Module. Table 2 describes the pins and their functions.
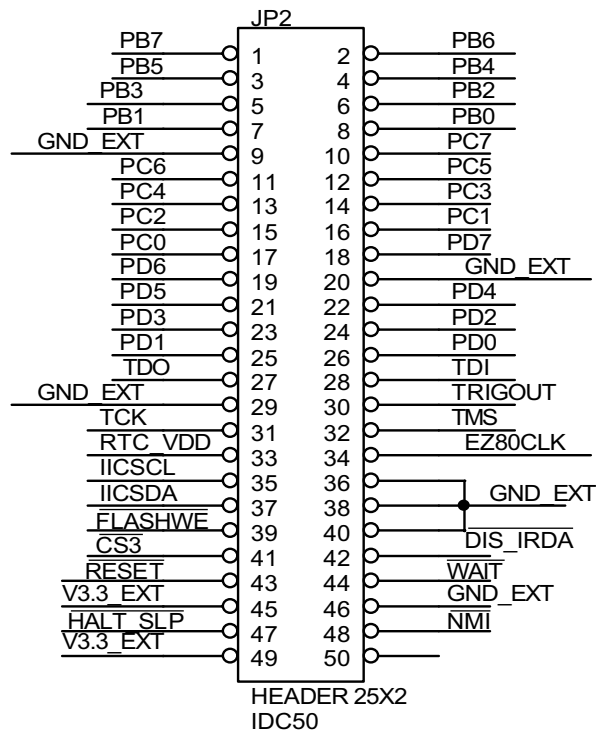
Figure 3. eZ80L92 Module I/O Connector Pin Configuration

Table 2. eZ80L92 Module I/O Connector Pin Identification*

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
1	PB7		Bidirectional	
2	PB6		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10 pF to satisfy timing requirements for the CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80L92 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
3	PB5		Bidirectional	
4	PB4		Bidirectional	
5	PB3		Bidirectional	
6	PB2		Bidirectional	
7	PB1		Bidirectional	
8	PB0		Bidirectional	
9	GND			V_{SS}/Ground (0V).
10	PC7		Bidirectional	
11	PC6		Bidirectional	
12	PC5		Bidirectional	
13	PC4		Bidirectional	
14	PC3		Bidirectional	
15	PC2		Bidirectional	
16	PC1		Bidirectional	
17	PC0		Bidirectional	
18	PD7		Bidirectional	
19	PD6		Bidirectional	
20	GND			V_{SS}/Ground (0V).
21	PD5		Bidirectional	
22	PD4	PD 4k7	Bidirectional	
23	PD3		Bidirectional	
24	PD2		Bidirectional	
25	PD1		Bidirectional	
26	PD0		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80L92 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
27	TDO		Output	JTAG data output pin.
28	TDI/ZDA	PU 10KΩ	Input	JTAG data input pin.
29	GND			V_{SS}/Ground (0V).
30	TRIGOUT		Output	Active High trigger event indicator.
31	TCK/ZCL	PU 10KΩ	Input	JTAG clock. High on reset enables ZDI mode; Low on reset enables OCI debug.
32	TMS	PU 10KΩ	Input	JTAG Test Mode Select.
33	RTC_V_{DD}			RTC supply from GoldCap (or external battery).
34	EZ80CLK		Output	48MHz synchronous CPU clock.
35	SCL	PU 4k7	Bidirectional	I^{2}C Bus Clock.
36	GND			V_{SS}/Ground (0V).
37	SDA	PU 4k7	Bidirectional	I^{2}C Bus Data.
38	GND			V_{SS}/Ground (0V).
39	$\overline{\text{FlashWE}}$	PU 10KΩ	Input	Low enables Write to onboard Flash memory. If this pin is unconnected, the Flash memory is write-protected.
40	GND			V_{SS}/Ground (0V).
41	$\overline{\text{CS3}}$		Output	Used on module for CS8900 EMAC.
42	$\overline{\text{DIS\_IRDA}}$	PU 10KΩ	Input	Low disables onboard IRDA transceiver to use PD0/PD1 UART pins externally.
43	$\overline{\text{RESET}}$	PU 2k2	Bidirectional	Reset output from Module or push-button reset.
44	$\overline{\text{WAIT}}$	PU 2k2	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the eZ80® CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.
45	V_{DD}			3.3V supply input pin.

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80L92 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
46	GND			V_{SS}/Ground (0V).
47	$\overline{\text{HALT\_SLP}}$		Output, Active Low	A Low on this pin indicates that the eZ80® CPU enters either HALT or SLEEP mode because of execution of either a HALT or SLP instruction.
48	$\overline{\text{NMI}}$	PU 10KΩ	Schmitt Trigger Input, Active Low	The NMI input is a higher priority input than the maskable interrupts. It is always recognized at the end of an instruction, regardless of the state of the interrupt enable control bits. This input includes a Schmitt trigger to allow RC rise times. This external NMI signal is combined with an internal NMI signal generated from the WDT block before being connected to the NMI input of the eZ80® CPU.
49	V_{DD}			3.3V supply input pin.
50	Reserved		NC	Reserved—No Connection.

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.

All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.

To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.

All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 24 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V tolerant. Some of the General-Purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80L92 dual modes, please refer to the eZ80L92 Product Specification (PS0130).

Onboard Battery Backup

An onboard 0.1F capacitor (GoldCap) is used to bridge power outages of 2–4 hours if the power supply to the module is disconnected. The capacitor is charged to 3.1V during normal operation and is discharged through the on-chip Real Time Clock. The V_{RTC} pin is available on the I/O connector of the module to connect external components to a power supply or to a larger GoldCap.

⚠️ **Caution:** Do not connect a Lithium Battery to the GoldCap capacitor, because onboard charging circuitry for the capacitor can destroy the lithium battery.

Ethernet Media Access Controller

The eZ80L92 Module contains a CS8900A EMAC (MAC, PHI, and RAM) which is attached to the data/address bus of the processor. This chip is connected to the processor's CS3 Chip Select, A0–A3, D0–D7, RD, WR, and PD4 pins for interrupt purposes. Connection of pins PD6 and PD7 for LANACT (wake-up from sleep) and SLEEP is optional and resistor-selectable onboard (see below).

Ethernet LEDs

There are two green LEDs, a Link LED and a LAN LED, that are located adjacent to each other on the eZ80L92 Module. A flashing LAN LED (top) indicates received link pulses from the 10Base-T Ethernet. This LAN LED should be ON if RX+ is connected to TX+ and RX– is connected to TX–. A steady Link LED (bottom) indicates Traffic (RX or TX) on the LAN.

An RJ45 loopback connector can be used to verify the correct operation of the Receiver and the Transmitter. The green LED should be on if RX+ is connected with TX+ and RX– is connected with TX–.

Ethernet Connectors

The eZ80L92 Module is equipped with an RJ45 connector that features integrated magnetics (transformer, common mode chokes). The remaining pins on the onboard RJ45 connector are not connected.

Node assignments for the RJ45 Ethernet connector are shown in Table 3.

Table 3. Ethernet Connector Pin Assignments

Pin	Function
1	TX+
2	TX–
3	RX+
6	RX–

Node assignment, in contrast to hub assignment, means that a straight-through cable (equivalent pin numbers on both sides of the cable are connected to each other) is used to attach the board to an Ethernet hub or switch. To connect the eZ80L92 Module directly to another node (e.g., a personal computer), a crossover cable must be used.

The EMAC can be additionally protected by placing a U9 ESD protection array on the module. This array can be either of the LCDA15C-6 (Semtech) or ESDA25B1 (ST Microelectronics) devices.

GPIO Pins for Enabling LAN Activity, Sleep, Interrupt

GPIO input bit PD4 serves as an active High interrupt input for the EMAC's INTRQ0 output.

GPIO output bit PD7 can be used to enter the EMAC into SLEEP mode. When pulling SLEEP (PD7) Low after enabling HWStandbyE and HWSleepE modes, the chip draws lower current, because only the receiver is operating. A zero-Ohm resistor at position R14 on the eZ80L92 Module is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

If LAN activity is detected, the LANACT signal is pulled Low. The LANACT is connected to GPIO input PD6 and can be used in interrupt edge-detection mode to wake up and reinitialize the Ethernet chip. A zero-Ohm resistor at position R15 on

the module is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

EMAC Ports

Chip Select CS3 is used for selecting the EMAC via I/O decoding. The I/O base address is user-selectable. The EMAC is connected as an 8- or 16-bit device with 8-word-wide I/O registers:

EMAC Wait States

The CS8900A EMAC should be operated in Intel bus mode so that the setup and hold times for the I/O access are met. For 48 MHz operation, first set CS3_BMC (I/O address `0xF3h`) to 84h (Intel bus mode with four system clock cycles per bus cycle) and then CS3_CTL (I/O Address `0xB3`) to `18h` (0 wait states for I/O). For a 20.8 ns CPU Clock cycle time, the Read and Write access time is:

2 x 4 x 20.8 ns–16 ns (for capacitive and chip delays) = 150 ns

Memory

The eZ80L92 Module offers SRAM and Flash memories and the wait states that support memory operations, as described in this section.

Wait States

To ensure that valid data is read from or written to slower memories, a number of wait states must be inserted into the memory or I/O access operations by the processor. The number of wait states that are required should be added by programming the chip select control registers. To calculate the minimum number of wait states required, refer to Table 4.

Table 4. Chip Frequency to Wait State Cycle Time Calculation

MHz	Cycle Time
12	83.3 ns
20	50.0 ns
24	41.7 ns
36	27.8 ns
40	25.0 ns
48	20.8 ns

Static RAM

The eZ80L92 Module features 512KB of fast SRAM. Access speed is typically 12ns or faster, allowing zero-wait-state operation at 48MHz. With the CPU at 48MHz, onboard SRAM can be accessed with zero wait states in eZ80 mode. CS1_CTL (chip select CS1) can be set to `08h` (no wait states).

Flash Memory

The Flash Boot Loader, application code, and user configuration data are held permanently in NOR Flash memory. A typical application requires eight times more ROM for code than RAM. As an example, for 128KB onboard SRAM, 1MB of ROM is required. The eZ80L92 Module allows NOR Flash memories between 4 megabits (512KB) and 32 megabits (4MB) to be used. The chips are housed in wide TSOP40 cases. Flash ROM access times are 55–150ns; typically 90ns.

NOR Flash should be operated in Intel bus mode to satisfy setup and hold times and to prevent bus contention with a Write cycle that could possibly follow. For proper CPU operation at 48MHz, first set the bus mode control register CS0_BMC (I/O address `0xF0h`) to `82h`, then set the Chip Select Control register CS0_CTL (I/O address `0xAAh`) to `08h`. These settings select Intel Bus Mode with two system clocks per bus cycle and zero wait states.

IrDA Transceiver

An onboard IrDA transceiver (ZiLOG ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The receiver supply current is 90–150μA and the transmitter supply current is 260mA when the LED is active.The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80L92 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the DIS_IRDA pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, DIS_IRDA is left floating and PD2 is set to Low.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset. The chip generates a reset pulse with a duration of 200ms if the power supply drops below

2.93V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80L92 Module with a low-impedance output (e.g. a 100-Ohm pushbutton).

Serial Interface Ports

The processor contains two 16550-style UARTs with programmable baud rate generators. UART0 is typically used for console I/O and initial boot code upload or to connect remote peripherals that can be controlled and monitored via Ethernet. UART0 is connected to GPIO PD[0:3] on the I/O connector. There are no RS232-level shifters on the eZ80L92 Module.

▶ **Note:** Do not connect an RS-232 interface without level shifters.

UART1 can be used for modem attachment or as a communications port to a host computer, where the embedded Ethernet module emulates an AT-style modem for internet access. UART1 does not offer onboard RS232-level shifters.

Physical Dimensions

The size of the eZ80L92 Module PCB is 64x64mm. With an RJ45 Ethernet connector, the overall height is 25mm, as shown in Figure 4.
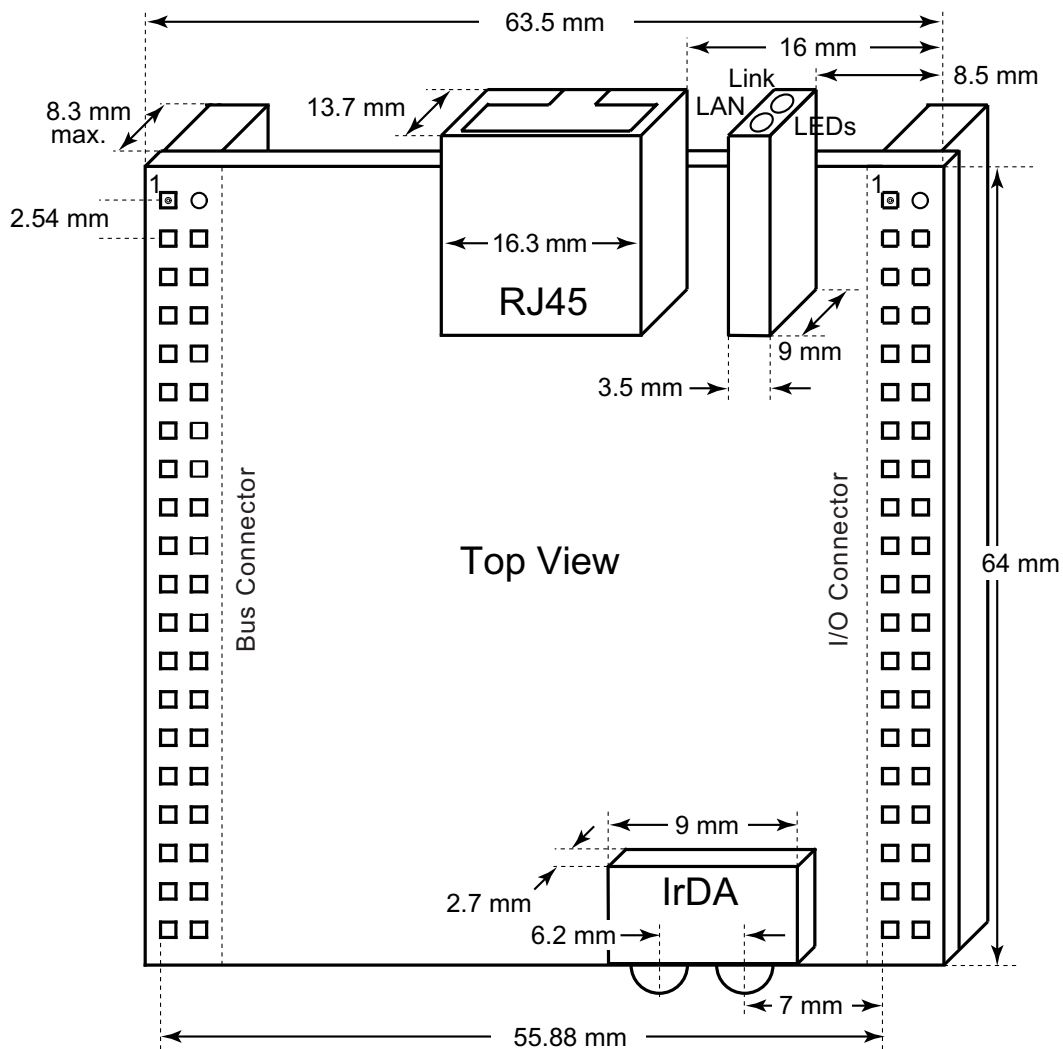

Figure 4. Dimension Drawing

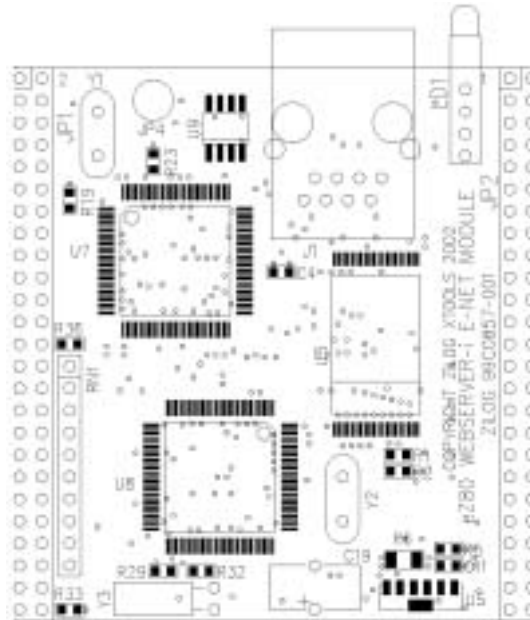Figure 5 illustrates a top view of the eZ80L92 Module.

Figure 5. Top Layer

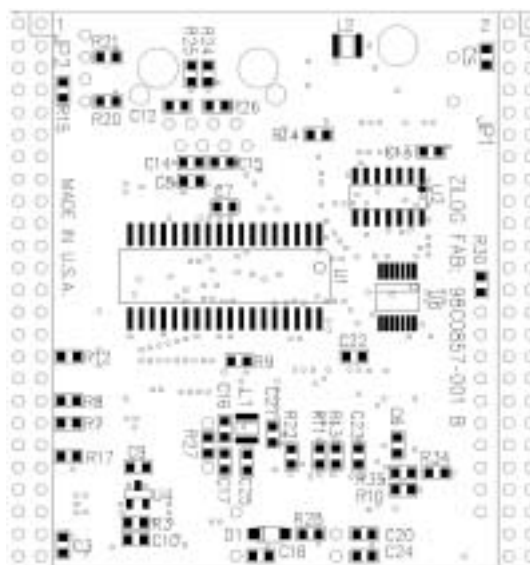Figure 6 illustrates a bottom view of the eZ80L92 Module.

Figure 6. Bottom Layer

Mounting the Module onto the eZ80® Development Platform

The eZ80L92 Module can be mounted in several positions. Depending on volume and area restrictions, it can be mounted horizontally or vertically with or without components between the connectors on the eZ80® Development Platform. See Figure 8 for examples.
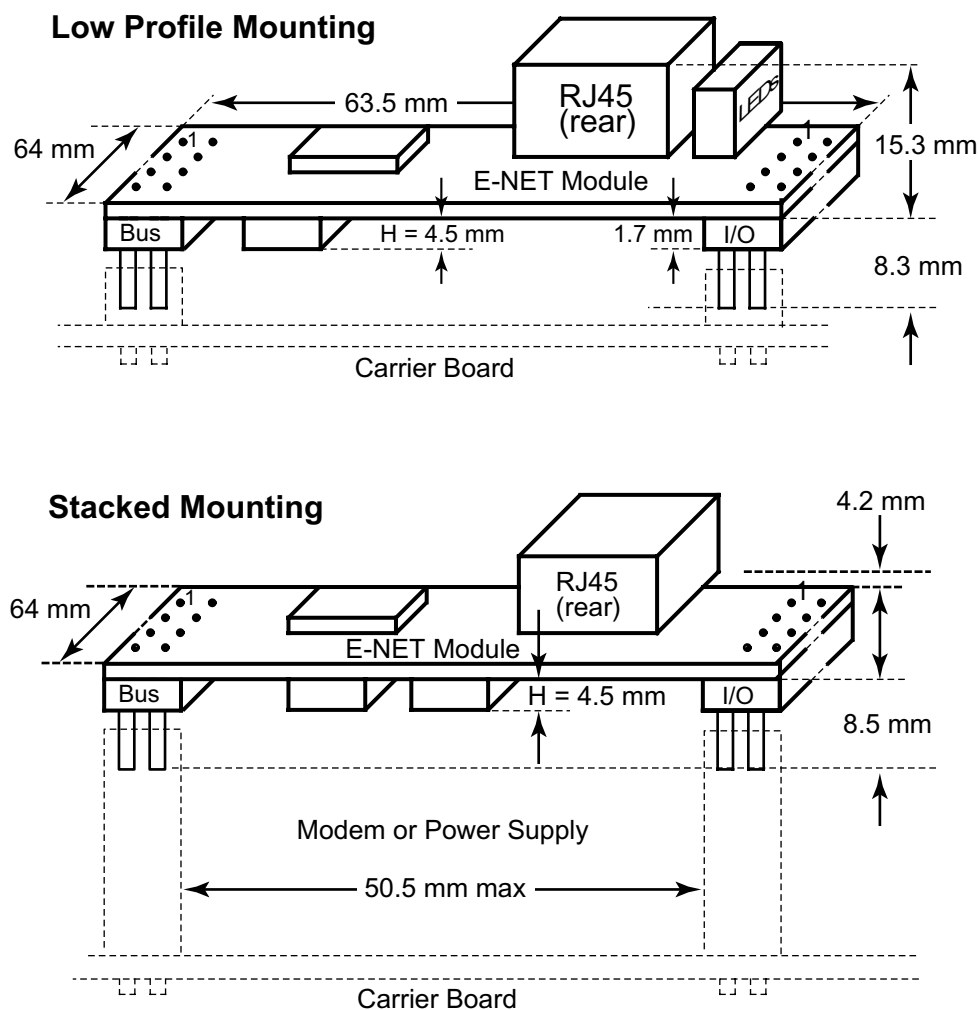

Figure 7. Mounting Examples